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Design, Analysis and Implementation of a Versatile Low Level Radio Frequency System for Accelerating Cavities

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Abstract:

This thesis describes analog and digital Low-Level Radio Frequency (LLRF) solutions applied to RF cavities of particle accelerators. For cavity analysis, a generic electrical model is developed to represent the cavity dynamic response under a beam. This model is then used as the basis for the design and analysis of two LLRF systems being the analog LLRF of the ALBA booster and the digital LLRF of the future Bilbao Proton and Neutron Source (ESS-Bilbao) linac. Details of the design and implementation of both LLRF systems are given followed by the experimental results obtained with different types of cavities verifying the validity of both LLRF systems. Also, the basic design of the ESS-Bilbao Beam Position Monitoring (BPM) RF electronics is described and the preliminary results obtained with a BPM test bench are presented.

There are two important considerations in the development of an electrical model analogy for RF cavities to be used for system analysis or LLRF loop design, being: transient response and cavity impedance mismatches. In the literature, however, either one or both of these issues are often neglected depending on whether the RF cavity is being looked at from a high-power or a LLRF perspective. In this thesis, in the first place, a transient model for RF cavities under beam loading is developed so that it represents the important RF aspects of the cavity such as impedance mismatches and reflected voltage as well as its transient response, for example at start-up or upon beam arrival. As a special case, the model is applied to the RF cavity of the ALBA storage ring to study the effects arising from beam loading, system start-up and delays on the performance of the LLRF regulation loops. For the simulation of the regulation loops in time domain a mathematical technique is introduced to map the cavity resonant frequency to baseband, leading to a baseband-equivalent model for the cavity with almost the same results as the conventional RF model but with significantly higher simulation speed.

In the continuation, the design and implementation of the IQ-based analog LLRF system for the ALBA booster is presented. The important LLRF parameters have been measured with the cavity running under low and high RF power and compared to the specifications verifying that all the requirements can be met with the proposed LLRF design.

Finally, the design and some performance results of the pulsed digital LLRF for the RFQ (Radio Frequency Quadrupole) systems of Rutherford Appleton Laboratory - Front End Test Stand and the future ESS-Bilbao linac are presented. Contrary to the standard digital LLRF front-end in which the cavity probe voltage is first down converted to an Intermediate Frequency (IF) and then subsampled, in this design, an analog IQ demodulator has been used to directly convert the probe voltage to I (In-phase) and Q (Quadrature-phase) components in baseband. The main advantage of this method is that the need for a precise synchronization and timing system for down-conversion and ADC sampling is eliminated leading to a simple and versatile design which can be used for a large variety of RF frequencies and virtually any LLRF application including CW, ramping and pulsed. The errors associated with the use of ana-

log IQ demodulators have been identified and corrected by FPGA algorithms and proper setting of the control loop parameters. Furthermore, a baseband-equivalent model for the RF plant is developed in MATLAB-Simulink to study the RFQ transient response under beam loading in the presence of phase and delay errors. The practical results obtained with a mock-up cavity and an RFQ cold model verify that amplitude and phase stabilities in the acceleration fields down to a fraction of one percent and one degree, and phase margins larger than $\pm 50^{\circ}$ can be achieved with this method preserving the linearity and bandwidth of the regulation loops and fulfilling the required specifications for the accelerator.

Resumen:

En esta tesis se describen diversas soluciones analógicas y digitales para realizar sistemas de control LLRF (Radio Frecuencia de Bajo Nivel) para cavidades resonantes de radiofrecuencia de aceleradores de partículas. Para analizar dichas cavidades, se desarrolla un modelo genérico que representa la respuesta dinámica de la cavidad bajo la influencia del haz de partículas. Después, se usa este modelo para desarrollar y analizar un sistema analógico de LLRF para el 'booster' del sincrotrón ALBA, así como un sistema LLRF digital para el linac de la futura Fuente Europea de Protones y Neutrones de Bilbao (ESS-Bilbao). A continuación, se presentan los detalles del diseño e implementación de los dos sistemas LLRF aludidos, así como los resultados experimentales obtenidos en distintas cavidades de radiofrecuencia, así verificando la validez de los dos diseños propuestos. También, se presenta el diseño básico de la electrónica de RF de un sistema de Monitorización de la Posición del Haz de Partículas (BPM) y los resultados preliminares obtenidos con un haz simulado en un banco de ensayos desarrollado al efecto.

Hay dos consideraciones importantes a la hora de desarrollar un modelo eléctrico de cavidades radiofrecuencia útil para analizar el sistema o diseñar un lazo de LLRF: la respuesta transitoria y los desajustes de impedancia. Sin embargo, en la literatura raramente se consideran estas cuestiones de manera conjunta, y una suele prevalecer sobre la otra, dependiendo de si la cavidad de radiofrecuencia se mira desde una perspectiva de alta potencia o de LLRF. En esta tesis, en primer lugar, se desarrolla un modelo para representar los aspectos más importantes de la cavidad, incluyendo desajustes de impedancia, potencia reflejada y la respuesta transitoria, por ejemplo en el arranque del sistema o en los instantes de llegada del haz de partículas que carga la cavidad. Como un caso especial, se aplica el modelo a las cavidades RF del anillo de almacenamiento (storage ring) de ALBA, estudiando así los efectos de carga del haz (beam loading), el arranque del sistema y los retardos en la respuesta de los lazos de regulación. Para simular estos lazos, se emplea una técnica matemática para hacer corresponder la frecuencia resonante de la cavidad a banda base, obteniendo de esta manera un modelo equivalente en banda base de la cavidad, con una respuesta aproximadamente igual al modelo convencional RF, pero con una velocidad de simulación mucho mayor.

A continuación, se presenta el diseño y la implementación del sistema de LLRF analógico del 'booster' de ALBA, basado en lazos de realimentación de las señales IQ del sistema. Se miden los parámetros importantes del LLRF operando la cavidad tanto a baja como a alta potencia de RF, verificando así el diseño propuesto.

Finalmente, se presenta el diseño, implementación y diversos resultados experimentales del sistema LLRF digital pulsado que hemos desarrollado para el Cuadrupolo de Radio Frecuencia (RFQ) del Rutherford Appleton Laboratory - Front End Test Stand (Oxfordshire, Inglaterra) y para el futuro linac de ESS-Bilbao. En lugar de emplear un 'front-end' analógico estándar que convierta las señales medidas en la cavidad a una Frecuencia Intermedia (IF) para a con-

tinuación submuestrear este señal, en este diseño usamos un demodulador IQ analógico, que transforma directamente las señales RF medidas en sus componentes En-fase (I) y Cuadratura (Q) en banda base. La ventaja principal de usar este método es eliminar la necesidad para un sistema preciso y complejo de sincronización y 'timing', lo cual da lugar a un sistema LLRF simple y versátil que puede servir para un rango grande de frecuencias y virtualmente para cualquier aplicación LLRF, sean pulsadas, en rampa o de onda continua (CW). Los errores asociados al uso de demoduladores de IQ analógicos han sido identificados y corregidos mediante algoritmos implementados en la FPGA y por medio del ajuste apropiado de los parámetros del lazo de control. Además, se ha desarrollado un modelo equivalente en banda base del RFQ en MATLAB-Simulink para estudiar su respuesta transitoria en condiciones de carga del haz y en presencia de errores de fase y retardos. Los resultados experimentales obtenidos con una cavidad de prueba y un modelo en cobre del RFQ verifican que en lazo cerrado pueden obtenerse campos acelerantes con niveles de estabilidad de amplitud y fase superiores al 1 por ciento y 1 grado respectivamente, además de un margen de fase mayor de $\pm 50^{\circ}$ que confiere robustez al sistema, conservando al mismo tiempo la linealidad y el ancho de banda de los lazos de regulación, y cumpliendo por tanto sobradamente las especificaciones requeridas para el acelerador.

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بنی آدم اعضای یک پیکرند که در آفرینش زیک گوهرند

چو عضوی به درد آورد روزگار دگر عضوها را نماند قرار

تو کز محنت دیگران بی غمی نشاید که نامت نهند آدمی

"سعدی"

Human being are members of a whole,
In creation of one essence and soul.

If one member is afflicted with pain,
Other members uneasy will remain.

If you've no sympathy for human pain,
The name of human you cannot retain!

Sa'di (1184 - 1283)

to my wife Atefeh

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Chapter 1

Introduction to accelerators and LLRF systems

1.1 Particle Accelerators

A particle accelerator is a machine in which electric fields are used to accelerate well-defined beams of electrically-charged particles to high energies. The particle accelerator beam can then be used for both fundamental and applied science as well as in many technical and industrial fields. For example, in Colliders [1, 2, 65], the accelerated particles are smashed into each other to study the structure and properties of matter or the interaction between high energy particles. The well-known LHC[1] built at the Swiss-French border falls into this category of particle accelerators. In this case, two hadron[2] beams of either protons or lead ions will travel in opposite directions inside a circular accelerator gaining energy in each turn. By colliding the two beams head-to-head at very high energies physicists recreate the conditions just after the Big Bang. The particles created as the result of this collision will then be analyzed by teams of physicists using some special detectors dedicated to the LHC experiments.

Synchrotron Light Sources [12, 13, 53] form another category of particle accelerators in which the emitted radiation from the particle beam (know as Synchrotron Radiation) is used in science research such as the study of atomic structure, medicine, biology, chemistry, crystallography, etc. In a synchrotron facility a beam of light particles, typically electrons, is accelerated in several stages to reach an energy level normally in the giga-electron-volt range. The beam path is then bent by some special magnets to generate bright X-rays or ultra violet photons dedicated to different experiments.

[1] Large Hadron Collider

[2] In particle physics, a hadron is a composite particle made of quarks held together by the strong force (as atoms and molecules are held together by the electromagnetic force). Hadrons are categorized into two families: baryons (made of three quarks) and mesons (made of one quark and one antiquark), source: Wikipedia.

Spallation sources can be mentioned as another category of particle accelerators in which a high energy beam hits a heavy metal target thus generating a beam of high energy neutrons. The ESS-Bilbao (European Neutron Source - Bilbao) Linac which is currently being built in Leioa-Spain, for example, hosts an H+ ion source based on the ECR[3] principle generating a low energy beam of protons with a nominal current of 100 mA. This beam is then accelerated and focused along the Linac length to higher energies. At the other end of the Linac a rotating solid target will be installed where neutron production takes place as the result of direct reactions with light nuclei, as well as several proton extraction lines devoted to experiments on materials processing, radiobiology or nuclear astrophysics.

Particle accelerators are generally classified into linear accelerators [1, 93, 108] (Linacs) and circular accelerators including Synchrotrons, Cyclotrons, Betatrons, etc. In Linacs, particles are generated at one end of the accelerator and then they are accelerated to higher energies and focused along the straight beam path while the target is located at the other end. In circular accelerators, the beam path is bent by dipolar magnets so that the particles can circulate around the ring for unlimited time with an energy gain in each revolution. The generated photon beam (in case of synchrotron light sources) will then follow a path tangential to the movement of the particles.

A conventional modern synchrotron light facility normally consists of three main parts: The Linac, where particles are generated and accelerated up to a primary energy level; The Booster Synchrotron, in which the energy is further increased until it reaches the desired level; The main ring also known as the Storage Ring, where the particles circulate for several hours while decaying exponentially due to the interaction with the residual air molecules on their path and machine imperfections. As the particles circulate around the storage ring, they emit synchrotron radiation because of the curvature of their path due to Bending Magnets[4] and Insertion Devices[5]. The emitted light will then enter some Beam Lines where it is filtered and manipulated by special optical devices according to the foreseen application. At the end of each beam line exists a small laboratory known as Experimental Hatch where the photon beam hits a sample and the data is collected and analyzed by the users of the Synchrotron facility as it is shown in Fig. 1.1.

[3] Electron Cyclotron Resonance

[4] Bending magnets are dipolar electrical magnets placed around the accelerator ring each bending the path of the particle beam by a certain angle due to the Lorentz Force imposed on the charged particles. The total deflection caused by bending magnets around the ring is 360° providing a closed path for the circulating beam. Bending magnets are also sources of synchrotron radiation.

[5] Although Insertion Devices (Undulators and Wigglers) are not essential to a synchrotron facility, their function is to produce highly brilliant synchrotron radiation. Undulators and Wigglers are arrays of dipolar magnets making the particle bunch oscillate constructively or unconstructively along its path, hence generate intense X-rays and ultraviolet radiation.

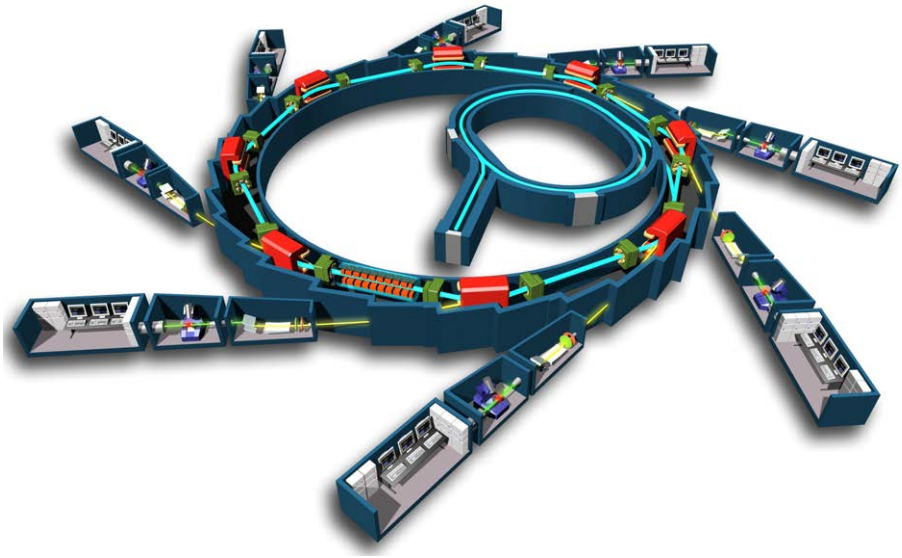

Figure 1.1: Simplified schematics of a synchrotron light facility including the Linac, booster, storage ring and the beam lines; source: SOLEIL synchrotron

1.2 RF systems

The RF[6] system is an essential part of any kind of particle accelerators. The main task of the RF system is giving energy to the beam. Besides, the RF system has a key role in the stability of the particle beam [106, 107, 108]. In a synchrotron light source, usually, one RF plant is used in the booster synchrotron to ramp the energy of the injected beam until the extraction level where it is injected into the storage ring and one or several RF plants are used in the storage ring to compensate for the energy losses due to synchrotron radiation. Similarly, in a linear accelerator, the RF system is used to increase the energy of the beam up to higher values as the beam travels from one Linac end to the other.

A typical RF plant consists of an RF amplifier (for example: Klystron or IOT[7]) supplied by a HVPS[8], a waveguide system, an RF cavity and the corresponding LLRF[9] electronics for field regulation as shown in FIG. 1.2.

[6]Radio Frequency
[7]Inductive Output Tube
[8]High Voltage Power Supply
[9]Low Level Radio Frequency

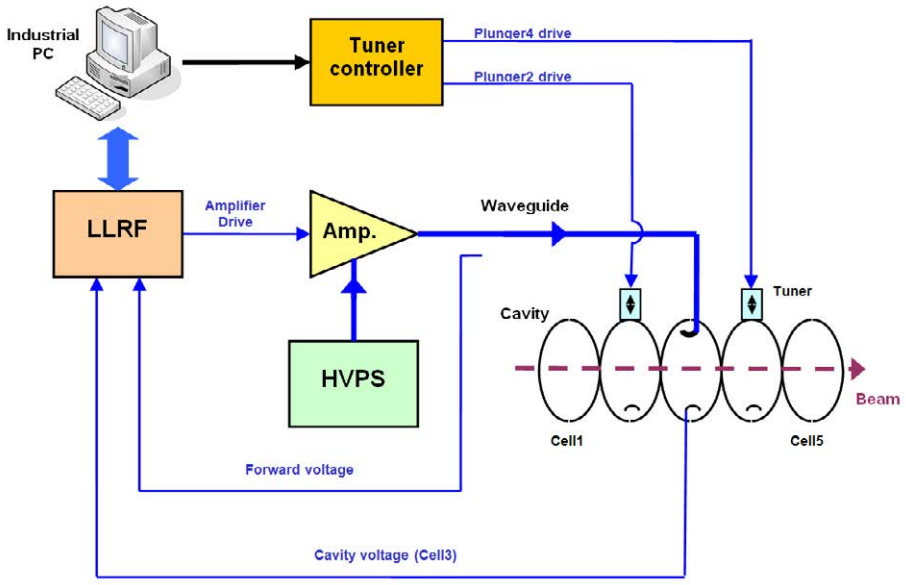

Figure 1.2: Simplified schematics of an RF plant and the regulation loops

1.2.1 RF cavities

An RF cavity is a metallic structure under vacuum, consisting of one or several cells, in which an electromagnetic field interacting with the particle beam is confined. RF cavities can be generally classified as normal-conducting [4, 53, 94] and Super-conducting [46, 107] depending on the material they are made of. While normal-conducting cavities operate at room temperature, super-conducting cavities have to be cooled down in a Helium bath to few degrees Kelvin so that their superconducting behavior can be achieved. Advantages of superconducting cavities in comparison to normal-conducting cavities include their extremely high quality factor and negligible power losses. Nevertheless, their maintenance is more difficult due to the need of the cryogenic system. Fig. 1.3 shows a picture of the normal-conducting 5-cell cavity (PETRA type) of the ALBA booster.

When particles arrive to the cavity, they see an electromagnetic field oscillating with a frequency of a few hundred MHz. The fundamental mode (TM 010) is shown in Fig. 1.4. The electric component of this field gives particles a 'kick' thus increasing their energy as they pass through the cavity.

Particles must see a certain phase of the electric field in order to get accelerated properly. Particles, which arrive in the cavity sooner than they are supposed, will get less energy kick and will be slowed down compared to a synchronized particle. The opposite happens to particles arriving late in the cavity. Particles with a phase too far from optimum cannot be properly accelerated and will be lost. The result is that the RF field divides the particle beam into bunches with a separation defined by the RF frequency.

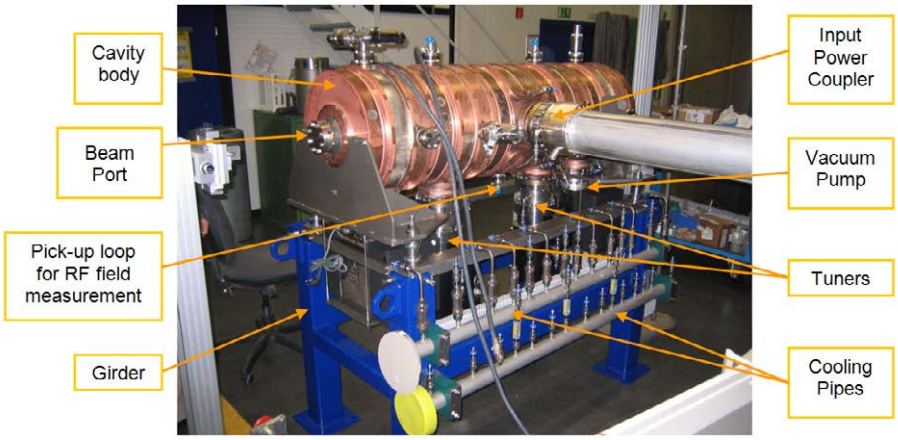

Figure 1.3: Picture of the 5-cell cavity for the future ALBA booster

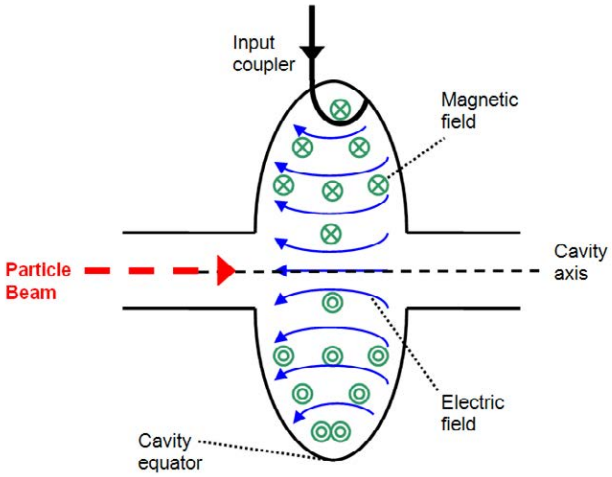

Figure 1.4: Electric and magnetic fields in a cavity cell

1.2.2 RF transmitters

In RF terminology, a transmitter is the combination of all the equipments for generating high power RF energy and transferring it to the cavity. An RF transmitter typically consists of the RF amplifier and the associated high-voltage power supply in addition to a waveguide system for power transmission to the cavity. Three types of RF amplifiers are often used in particle accelerators for medium and high power levels being Klystrons, IOTs and solid-state amplifiers. Although detailed discussion about the characteristics of these amplifiers is out of the scope of this thesis, it can be generally mentioned that Klystrons are best suited for high power applications (200 kW and above) while IOTs and solid-state amplifiers are better choices for lower power levels. IOTs, in general, have a higher efficiency and a more linear response compared to Klystrons. Nevertheless, with the current technology, their maximum power is limited to 100 kW approximately. Solid-state amplifiers, on the other hand, comprise many small units connected in series and parallel each generating a fraction of the output power. Solid-state amplifiers are becoming more and more popular due to their modular design, high efficiency and high reliability.

The output power of the RF amplifier is fed into the cavity through a waveguide system. When the output power of one amplifier is not sufficient, the power of two or more amplifiers can be combined through Magic Tees[10] or Cavity Combiners[11] to reach the desired power level. A Circulator is placed on the way of the forward power, before it is fed into the cavity, to protect the amplifier against any reflections due to impedance mismatches. The reflected power from the cavity will therefore be guided by the circulator to a Dummy Load where it will be dissipated into heat. Fig. 1.5 shows the layout of the ALBA storage ring RF plant.

As the figure shows, for each cavity, the required power is generated by two IOTs and combined by a Cavity Combiner (CaCo). The output power of the CaCo passes through the circulator and then it is fed into the cavity by a waveguide system while any reflected power will be redirected by the circulator to the dummy load.

1.2.3 LLRF systems

The LLRF system of an RF plant usually consists of an Amplitude Loop, a Phase Loop and a Tuning Loop to regulate the amplitude and the phase of the cavity voltage and the resonant frequency of the cavity, respectively [26, 27]. The amplitude and phase loops should have a wide bandwidth [27, 82], in the order of a few hundred kHz, to be able to compensate HVPS ripples and to have a good time response (for example: when a pulsed or a ramping RF field is needed). The tuning loop, which has a bandwidth of a few hundred Hz, controls the

[10] Magic Tee is a T-shaped passive RF device with isolated splitting/combing waveguide ports used to split or combine RF power.

[11] Cavity Combiner also splits or combines RF power through isolated ports, but unlike the Magic Tee, it is done by a cavity.

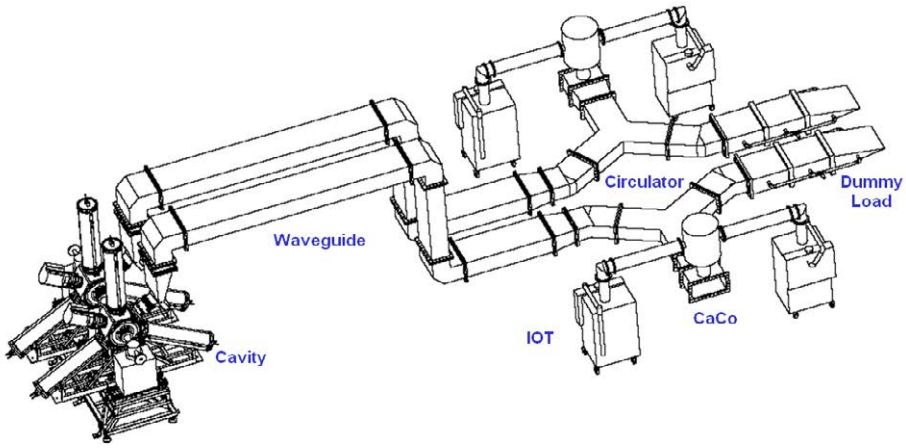

Figure 1.5: Layout of the ALBA storage ring RF plant

Cavity Tuners[12] to minimize the cavity reflected power due to cavity warming and Beam Loading [44, 45, 46]. In multi-cell cavities a Field-flatness Loop may also be used to ensure a uniform field distribution among the cells.

The figure of merit of an amplitude/phase loop in time domain is the short and long term stabilities[13] it provides for the RF field while in the frequency domain it is the bandwidth and stability margins of the loops themselves. The goal in the design of an amplitude/phase loop is that:

- it gives as much stability as possible to the RF field (typical values are $\pm 1\%$ and $\pm 1^\circ$ of amplitude and phase stability[14] respectively).
- to provide a large-enough bandwidth to suppress the highest frequency disturbance that may affect the RF field in the cavity.
- to have a good stability margin (phase margins of 45° or more).
- to have a large dynamic range (23 dB or more) if it is intended for energy ramps.

[12] Cavity Tuner is a mechanical device mounted on the cavity to control the internal geometry, thus the resonant frequency of the cavity.

[13] The time-domain stability of a LLRF system which can be expressed as short and long term stabilities should not be confused with what is known in control theory as system stability (i.e. poles of the transfer function having negative real components). Short term stability is defined as the unwanted variations of a signal due to fast disturbances (for example: noise or ripple) measured during short time periods (for example: 1 sec or less) while long term stability is the slow variations of the signals due to temperature changes, offsets, aging, etc. during a long period (8 hours or longer).

[14] In the LLRF field, amplitude and phase stabilities of a RF system are defined as the overall unwanted variations of the amplitude and phase of the cavity voltage about their set values expressed in % and ° respectively.

In case of the tuning and field-flatness loops the goal is to provide enough accuracy in cavity tuning to have the least amount of reflected power and to have a uniform field distribution in all the cells although the cavity may suffer from a number of disturbances including Beam Loading[15] [9, 10, 37, 44, 45, 46], field ramping and temperature variations.

The low-level electronics of a RF plant can be analog [8, 9, 27, 42] or digital [31, 33, 73, 85]. While the short-term stability of an ALLRF[16] depends mainly on ripple and noise (which can be internal or external), its long-term stability depends on voltage drifts caused by temperature variations. The overall stability depends on many factors including, PCB[17] design, bandwidth, components quality, filtering, shielding etc. and sometimes the ALLRF designer has to make a compromise when two or more factors are opposing each other (for example: putting less filtering increases the bandwidth but can have a negative effect on noise). Although in a DLLRF[18] system the digital processing part is not supposed to be affected by noise -unless the noise level is too high- its stability can still be degraded by the noise on the analog front ends. The inherent noise on the analog signals goes through all the electronics just like the desired signals without being filtered out if its frequency content falls within the LLRF bandwidth. Therefore, the trend in the design of DLLRF systems is to simplify the analog front-ends as much as possible to provide higher stabilities. The ultimate case would be sampling directly on RF frequency because this would minimize the number of components in the analog front ends [87]. Although this does not yet give very good results due the current speed of digital processors and precision of ADCs[19], it is believed to be more widely used in the near future as technology improves.

1.3 State of the art in LLRF

The on-going progress in LLRF systems can be viewed from different perspectives. Here we focus on three aspects of the LLRF systems as follows:

1.3.1 Control method / topology

In the design of low-level RF controllers the main objective is to achieve higher amplitude and phase stabilities. Besides, the control system must be able to satisfy other requirements including large bandwidth and dynamic range and little susceptibility to noise. Although these requirements usually can be met

[15] Beam Loading is the influence of the particle beam on the cavity impedance. Beam can cause a significant change in the amplitude and phase of the cavity voltage resulting in large amounts of reflected power if not compensated. Beam loading will be discussed in details in the subsequent chapters.

[16] Analog Low-level Radio Frequency

[17] Printed Circuit Board

[18] Digital Low-level Radio Frequency

[19] Analog to Digital Converters

using traditional PID[20] controllers, some research work is going on aiming at achieving higher stabilities and improved response using other types of controllers. One example is the application of Pole-placement Feedbacks for higher stabilities and improved time response in RF cavities [32]. Another example is the use of Kalman filters for reducing noise thus improving the stability of the regulation loops at DESY-Hamburg [33]. Additionally, in the design of the controllers for an RF system the requirements of that particular case must be taken into account. For example a superconducting RF cavity might suffer from Lorentz Force Detuning and Microphonics[21] [34, 43, 46, 47] while these errors are negligible in the case of a normal-conducting cavity.

For the ESS-B Linac, in order to improve the formation of the beam, avoid an additional beam chopper and reduce operational costs, it is planned to pulse the ion source and the high power RF system. As the beam pulse will be narrower than the RF pulse, the cavity field should have settled before the beam pulse enters the cavity so that the beam sees the right voltage and phase. That puts new requirements on the dynamic range, bandwidth and transient response of the LLRF. The LLRF system should also provide a large phase margin to avoid loop instabilities in addition to being compact, modular and easy-to-operate.

LLRF systems for Linacs similar to ESS-B have been built in the past at SNS and J-PARC. In the implementation of the SNS LLRF, large effort has been made to keep the latency below 150 ns so that the required bandwidth can be achieved by an all-digital LLRF system. Also, mechanical modes of the superconducting cavities have been successfully damped out using AFF[22] compensation resulting in a significant decrease of the amplitude and phase errors [82]. In case of J-PARC, a digital LLRF system utilizing feedback and feed-forward control has been made and tested with amplitude and phase stabilities of 0.3% and 0.2° under beam loading [83].

1.3.2 RF modeling and simulation

An RF cavity and its input power coupler, in their general form, are modeled by a shunt RLC circuit and a step-up transformer respectively. The RF amplifier is modeled as a current source, supplying the cavity through a transmission line, and the beam is modeled as another current source connected directly across the RLC circuit. Although this is a lumped model, one can still use it to explain the important aspects of the RF cavity under beam, including: cavity detuning, impedance mismatch between the cavity and the amplifier, effect of the beam on the cavity impedance, etc. There are, however, two important considerations in the development of this model so that it leads to correct and informative results when actual parameters are plugged into the model equations. These

[20] Proportional Integral Derivative

[21] Lorentz Force Detuning and Microphonics are two sources of error in super-conducting RF cavities having very high quality factor thus very narrow bandwidth. Lorentz force detuning is the predictable error in the cavity resonant frequency caused by small changes in dimension due to high-gradient RF fields while Microphonics is the unpredictable modulation of the cavity resonant frequency due to mechanical vibrations.

[22] Adaptive Feed Forward

are: 1) reflected voltage from the cavity due to impedance mismatches and 2) cavity transient response. The importance of the reflected voltage is linked to the fact that the total cavity voltage is the sum of the forward and reflected voltages as it is well known in transmission line theory. Furthermore, the effect of the reflected voltage must be taken into account in the calculation of optimum values for the cavity coupling factor and detuning for a certain beam magnitude and phase. Transient analysis of the cavity, on the other hand, not only gives good insight into the system behavior (for example, at start-up or upon beam arrival) but also can be very important for the design of the LLRF regulation loops. In the conventional RF models, however, either one or both of these considerations are often overlooked. This is because the RF aspects of cavities are usually addressed in steady-state conditions using the Fourier notation [10, 106, 107, 108]. On the other hand, in LLRF loop design, some RF aspects of the cavity such as the reflected voltage and the effect of the coupler on the cavity impedance are often ignored even though these models might very well represent the transient cavity behavior [11, 32, 109]. Therefore, an RF/LLRF model both representing the transient response and the cavity impedance mismatch is beneficial for LLRF design and analysis.

As an RF cavity has a very large quality factor, a complete RF simulation in time domain usually takes a long time resulting in excessive output data which might not be easy to handle. On the other hand, for transient time simulations the aim is to let the simulations run until the output settles so that one can examine the transient response of the system. In addition to that, it is generally preferred to have as much details as possible in the RF model to have reliable simulation results. These opposing requirements (i.e. reliable simulations with large *simulated time* but short *simulation time*) normally can not be met through conventional simulation methods. One way to overcome this problem is to eliminate the RF carrier in the simulations so that one can see the envelope of the RF waveforms without having to simulate each RF period throughout the whole simulation time [81, 109]. This new method which is called Envelope Simulation can be utilized in the ADS[23] software from Agilent. In this way, RF simulations in time domain can be performed with a very short simulation time compared to the conventional methods. Moreover, as a complete RF model can be simulated conveniently, one can also expect reliable simulation results.

1.3.3 Design and implementation

The amplitude and phase of the cavity voltage can be regulated using traditional amplitude and phase loops [42] or the I/Q loops [26, 27]. The second approach, however, is the preferred one because it allows using two similar loops for I and Q thus simplifying their implementation. Furthermore, with the IQ method, the phase of the cavity voltage can be controlled from 0° to 360° while with phase loops the maximum phase control range is only from 0° to 180° [20].

[23] Advanced Design System

Recent advances in IQ modulator / demodulator ICs [24] have made it possible to implement the I and Q loops with a very good performance yet with low cost and compact design [14, 17].

The I/Q loops can be implemented using analog or digital electronics [31, 85]. The analog solution is cheap and provides a short group delay and a large bandwidth which can easily meet usual RF regulation demands. Nevertheless, an ALLRF can suffer from a number of inherent errors including DC offsets, drifts and high noise level. As a result of these, its application is typically limited to $\pm 0.5\%$ and $\pm 0.5^{\circ}$ of amplitude and phase stability. A DLLRF has the advantage of giving much more flexibility. Substantial changes in the design are possible by changing the program code without affecting the hardware. With DLLRF, the amplitude and phase stability can be improved significantly. The main drawbacks of a DLLRF system are its lower speed, higher cost and higher complexity. Generally it is used when complex control methods have to be implemented and/or high RF stabilities are required [31, 33].

A combined solution which benefits from the advantages of both analog and digital electronics is based on an analog front-end for direct RF conversion to baseband IQ (and vice versa) and an FPGA unit running error compensation and control algorithms. This design scheme has been adopted for the implementation of the ESS-Bilbao LLRF due to its advantages including simplicity, versatility and large bandwidth. LLRF systems based on the same or a similar design principle have been developed for PEP-II B Factory [99], S-DALINAC-Darmstadt [100], SCSS [101] and successfully put into operation, even for very high RF stability requirements of XFELs [102]. With this solution, however, the accuracy of the probe voltage conversion to digital I and Q plays the main role in the resultant RF stability. For that reason, errors inherent to analog IQ demodulators need to be identified and corrected in the FPGA to improve the RF stability.

1.4 Objectives and overview of the thesis

The objectives of the current thesis are classified as the following together with an overview of the thesis work:

1.4.1 Detailed analysis of RF cavities

In order to design a proper controller for RF cavities it is important to study their behavior in detail. In that respect the impedance of the cavity should be calculated taking into account the cavity coupling factor and detuning. In order to match the cavity to the RF transmitter, the cavity impedance must be the same as the characteristic impedance of the transmission line feeding power into the cavity. The cavity parameters should therefore be chosen to have a good impedance match resulting in minimum reflected power, hence avoid unnecessary power losses and saturations. The cavity impedance can be

[24] Integrated Circuits

calculated in steady state or transient. The second approach, however, is more interesting from a control point of view as it gives information about the cavity transient response.

In Chapter 2 Section 2.1, we will develop a transient model for the cavity using Laplace notation. In this model the reflected current from the cavity due to the coupler mismatchs will also be taken into account while in the literature, usually, the cavity is modeled by a lumped RLC circuit supplied directly by a current source, therefore it does not take the effect of these reflections into account [11, 109]. The developed model can be used to simulate the cavity response in time and frequency domains in *MATLAB / Simulink* or similar software. This model, when converted to its equivalent transfer function, can also be used for closed-loop cavity simulations.

1.4.2 Detailed analysis of the interaction between the cavity, the RF transmitter and the particle beam

Cavity analysis becomes a complex problem when the beam loading effect is considered. The beam changes the impedance of the cavity as seen by the RF transmitter [10]. Therefore, the previous cavity model should be modified so that it also takes the influence of the beam into account. With a beam-loaded cavity, new values for the cavity coupling factor and detuning must be found to match the cavity to the transmitter for a certain value of the beam magnitude and phase.

Chapter 2 Section 2.2 discusses the effect of the beam on the cavity impedance [81]. As the aim is to develop a model for transient analysis, Laplace transformation will be used again. Nevertheless, when it is needed, one can switch to a steady state model by replacing 's' with 'jω' in the cavity impedance. The transient model is advantageous because it explains how the cavity quantities such as current, voltage and power change with time when there is a transient condition (ex. upon startup or when the beam arrives). With the conventional RF models, the cavity impedance is calculated using Fourier notation and the transient response is usually not addressed as its analysis becomes too complex [10, 106, 107, 108].

1.4.3 Design and simulation of a LLRF system for closed-loop RF field regulation and control in the presence of the particle beam

In Chapter 3 Section 3.1, the design of the ALBA feedback loops for cavity field regulation (amplitude and phase) and tuning/field-flatness will be presented. The design of all these loops is based on the IQ demodulation method which has advantages compared to the traditional amplitude and phase loops. The validity of the design is verified by computer simulations in Chapter 3 Section 3.1.7 and also by practical tests in Chapter 3 Section 3.3. For the simulations, though, a typical problem is the long simulation time which is due to the relatively slow

cavity response compared to the RF period. In order to remove this problem, a mathematical technique will be introduced to map the cavity resonant frequency from RF to baseband, resulting in a baseband-equivalent model for the cavity [81]. As this model does not deal with the RF frequency, it can be simulated much faster than the conventional RF-baseband model. Moreover, one can use it to see the time evolution of the amplitude and phase of the RF signals. The validity of the baseband−equivalent model is ensured by comparing it to the conventional RF model and verifying that the results from both models are the same. The baseband-equivalent model is then used for closed loop simulations of the RF system under beam with a very short simulation time.

1.4.4 Implementation of the amplitude, phase and tuning loops for the ALBA LLRF system

The implementation of the ALBA LLRF electronics will be presented in Chapter 3 Section 3.2. The design of the in-house developed units for the regulation loops will be presented, followed by the design of the Graphical User Interface. We will also discuss some practical issues such as noise protection, grounding, DC offset compensation, dynamic-range improvement etc. in the design and implementation of the boards. Although these issues usually are not addressed when LLRF systems are looked at from a purely theoretical perspective, they can become very important in practice when high signal accuracies are needed.

1.4.5 Practical verification of the LLRF system

The validity of the loop design is verified in Chapter 3 Section 3.3 by practical tests in the CELLS RF laboratory and at ELETTRA-Italy. The important characteristics of the loops such as bandwidth, noise level, dynamic range, and amplitude/phase ripple reduction factors, etc. are measured and compared to the specifications. The ability of the LLRF system to work reliably for ALBA is ensured by verifying that the actual parameters are in agreement with the specifications.

1.4.6 Design and implementation of the ESS-Bilbao LLRF system

Chapter 4 Sections 4.1 to 4.5 are devoted to the design and implementation of the ESS-Bilbao DLLRF system[25]. Although, conceptually, the design is very similar to the one of ALBA[26], when it comes to implementation, there are sig-

[25]This system was originally developed for the RFQ system of RAL-FETS (Rutherford Appleton Laboratory - Front End Test Stand) in UK [75] but a duplicate of the system is planned to be built in the future to be used for the ESS-Bilbao RFQ [73, 80].

[26]For amplitude and phase regulation, both designs are based on decomposing the cavity probe signal into I and Q components regulated by two PI controllers while a baseband phase shifter is used to ensure loop stability. In case of the tuning loop, the phase difference between the forward and cavity voltages is measured by two IQ demodulators and the tuner is moved so that this phase difference always stays as close as possible to its reference.

nificant differences between the two as the analog one was implemented by some in-house developed boards while in case of the digital one all the signal processing is done by a commercial FPGA unit controlled by the MATLAB-Simulink program. The digital LLRF therefore gives significant flexibility for future modifications of the control algorithms in addition to improving the system accuracy due to the minimization of signal drifts and noise. In order to make sure that the LLRF system will be able to meet the RF stability requirements, errors of analog IQ demodulators have been identified and corrected by FPGA algorithms and proper setting of the control loop parameters as explained in Chapter 4 Sections 4.1.

The block diagrams of the amplitude/phase and tuning loops of the ESS-Bilbao LLRF are presented in Chapter 4 Section 4.1 along with an explanation of the function of each block. These block diagrams are then used as the basis of the FPGA program which is explained in details in Section 4.5. This chapter also presents the implementation of the ESS-Bilbao LLRF consisting of several units each having a certain task and a short description of the MATLAB-Simulink GUI[27] which is based on the HIL[28] Co-simulation method. In the continuation, a description of the full LLRF parameters to be controlled by the operator is given together with some guidelines on how these parameters should be correctly adjusted for a successful operation of the regulation loops.

1.4.7 Experimental results verifying the DLLRF design

Finally, Section 4.6 presents the experimental results obtained from the LLRF system tested with an Aluminum prototype cavity at the Electricity and Electronics Department of the University of the Basque Country (UPV/EHU) and an RFQ cold model at the Imperial College London. Several tests were carried out to check the behavior of the LLRF system such as short-term and long-term stabilities, linearity, transient response and loop stability. Validity of the LLRF design is ensured by comparing the actual parameters obtained from these tests to the specifications.

1.5 Summary

A particle accelerator is a machine in which a beam of charged particles is accelerated to high speeds (energies) by the electric component of an electromagnetic field. Particle accelerators can be of different types and characteristics depending on their foreseen application.

An essential part of any particle accelerator is the RF system whose task is to give energy to the particle beam and provide the required conditions for its stability. A conventional RF plant can be divided into three main parts being the RF cavity where the electromagnetic field interacting with the beam is stored, an RF transmitter for generating high power RF energy and transferring it

[27] Graphical User Interface
[28] Hardware In the Loop

to the cavity and finally a so-called LLRF system regulating the RF field and the cavity resonant frequency. The feedback loops incorporated in the LLRF system on one hand regulate the amplitude and the phase of the cavity field to the values needed for beam acceleration and on the other hand compensate for several types of disturbances such as the beam loading effect, temperature variations and the ripples of the high voltage power supply of the RF amplifier.

The current Ph.D. thesis mainly focuses on two aspects of LLRF systems being 1) their simulation and analysis and 2) their design and implementation. Considering the first aspect, a detailed transient model for the RF cavity under beam loading is developed which serves as the basis for the subsequent LLRF simulations. With respect to the implementation, details of the design and implementation of two LLRF systems are given being the ALLRF system of the ALBA booster and the DLLRF of the ESS-B accelerating structures. Although these two designs are conceptually quite similar (both are based on direct RF-baseband conversion, baseband signal processing and finally up-conversion to RF), there are significant differences in their implementation as the first one is intended for ramping RF applications using a normal-conducting 5-cell cavity while the second one is optimized for high-power pulsed RF applications with the normal-conducting and superconducting accelerating structures of the ESS-B Linac. Validity of both designs is ensured by extensive series of experimental tests and verifying that the LLRF performance meets the specifications.

Chapter 2

Cavity Modeling and Simulation

2.1 Cavity Modeling and Simulation without Beam

The conventional electrical model of an RF cavity is a shunt RLC circuit supplied by a current source. Although this is a lumped model, one can still use it to explain some RF aspects such as impedance mismatch to the RF transmitter, and reflected power from the cavity. In the literature, usually cavity impedance is calculated using Fourier notation; the result is that it only gives final values of the RF signals without giving any information about transients. From the control point of view, however, it is essential to know the response of the RF cavity to transients, because only then one can see the time evolution of these signals. Transient model of the RF system can be generated using Laplace transformation instead of Fourier in the calculation of the cavity impedance. Therefore, for transient analysis it would be more convenient to model the RF system using Transfer Functions. RF signals will be then represented by their corresponding Laplace transforms in the frequency domain and their inverse Laplace in the time domain.

In this chapter we start with the classical RLC model for RF cavities [10] and we develop a transient model for the cavity without beam. This model can be used to calculate the time response of the cavity voltage (amplitude and phase), forward and reflected power etc. as well as the cavity frequency response. For the calculation of some cavity parameters such as time constant and bandwidth, however, it would be easier to use the steady state model. This is simply done by replacing 's' with 'jω' in the cavity impedance. In the following section we modify the cavity model so that it also represents the effects of the particle beam on the cavity impedance.

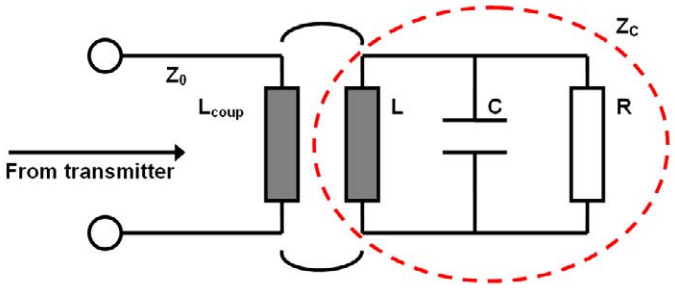

Figure 2.1: Electrical model of an RF cavity

2.1.1 Cavity without coupler

The cavity is modeled by a shunt RLC circuit supplied by a step-up transformer as shown in FIG. 2.1 [10]. In this model the RLC circuit represents the cavity itself and the transformer represents the input coupler which feeds power into the cavity.

The impedance of the cavity (for the moment we don't consider the transformer) will be as the following:

$$Z_c = \frac{RL.s}{RLC.s^2 + L.s + R} = \frac{\frac{R\omega_0}{Q_0}}{s^2 + \frac{\omega_0}{Q_0}.s + \omega_0^2} \tag{2.1}$$

The unloaded quality factor Q_0[1] and the resonant frequency of the cavity ω_0 are linked to the electrical-model parameters by the following equations:

$$Q_0 = \frac{R}{\omega_0 L} = R\omega_0 C \tag{2.2}$$

FIG. 2.2 shows the Bode diagram of the ALBA booster cavity without coupler assuming $Q_0 = 29000$, $R = 3.5e6$ and $\omega_0 = 2\pi.500e6\ rad/s^2$.

As one can see in the figure, the cavity impedance has a magnitude peak at its resonant frequency. The phase of the cavity changes from $+90°$ to $-90°$ in the vicinity of the resonant frequency.

The cavity impedance (generally complex) has a real and an imaginary part depending on the frequency as shown in FIG. 2.3.

With $\omega < \omega_0$ the imaginary part of the cavity impedance is positive while with $\omega > \omega_0$ it is negative. Therefore, when $\omega < \omega_0$ the cavity behavior is inductive and when $\omega > \omega_0$ it is capacitive. At resonance, the imaginary part of the cavity impedance becomes zero and the cavity behaves like a pure resistive load.

[1] By definition, unloaded quality factor is the cavity quality factor without coupler.

[2] In all this chapter, without loss of generality, we will assume these parameters in the numerical examples.

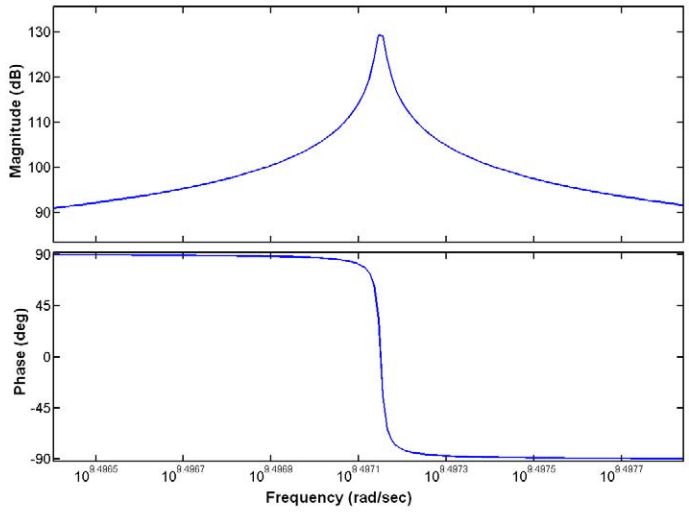

Figure 2.2: Bode plot of the cavity model without coupler

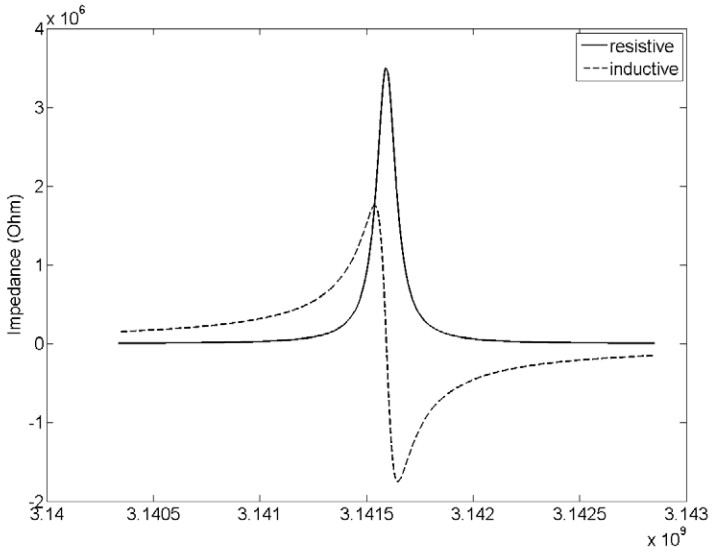

Figure 2.3: Resistive and inductive parts of the cavity impedance vs. frequency

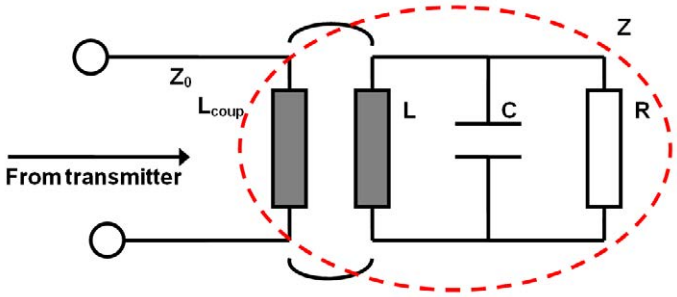

Figure 2.4: Electrical model of a RF cavity including the coupler

2.1.2 Cavity with coupler

Now, we study the influence of the coupler.

As the coupling is inductive[3], the transformed cavity impedance (i.e. the cavity impedance looking into the transformer primary side) will be:

$$Z = \frac{L_{coup}}{L} Z_C = \frac{L_{coup}}{L} \frac{RL.s}{RLC.s^2 + L.s + R} \tag{2.3}$$

We define coupling factor β as:

$$\beta = \frac{L_{coup}}{L} \frac{R}{Z_0} \tag{2.4}$$

where Z_0 is the characteristic impedance of the transfer line into the cavity. In practice β depends on the size and angular position of the input coupling loop. The cavity impedance in terms of the transmission line impedance Z_0 and the coupling factor β will be:

$$Z = \frac{\beta Z_0 L.s}{RLC.s^2 + L.s + R} \tag{2.5}$$

2.1.3 Reflection of electromagnetic waves

FIG. 2.5 shows a transmission line with characteristic impedance Z_0 terminated by load Z.

We will have [10]:

$$\begin{aligned} V(x) &= V_{fwd}(x) + V_{refl}(x) \\ I(x) &= I_{fwd}(x) - I_{refl}(x) \end{aligned} \tag{2.6}$$

[3]Power coupling can also be capacitive, but the most common type of coupling for RF cavities is inductive coupling where a loop is used to feed power into the cavity.

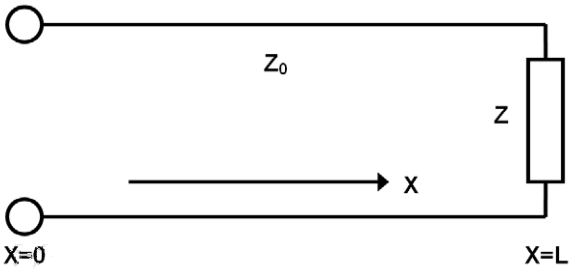

Figure 2.5: Reflection of electromagnetic waves

$$\begin{aligned} V_{fwd}(x) &= Z_0.I_{fwd}(x) \\ V_{refl}(x) &= Z_0.I_{refl}(x) \end{aligned} \tag{2.7}$$

$$\frac{V(x=L)}{I(x=L)} = Z \tag{2.8}$$

$$V_{refl} = r.V_{fwd} \tag{2.9}$$

Where the subscripts $_{fwd}$ and $_{refl}$ denote the cavity forward and reflected current/voltage, x is the distance along the transmission line and r is the reflection coefficient at $x = L$. From these equations r can be calculated as the following:

$$r = \frac{V_{refl}}{V_{fwd}} = \frac{Z - Z_0}{Z + Z_0} \tag{2.10}$$

The last equation shows that the reflected voltage from the load is zero (i.e. $r = 0$) when $Z = Z_0$ (Z_0 is real).

After substituting Z in EQ. 2.10, we'll have:

$$r = \frac{\beta L.s - RLC.s^2 - L.s - R}{\beta L.s + RLC.s^2 + L.s + R} \tag{2.11}$$

The total cavity voltage (i.e. sum of the forward and reflected voltages) can be calculated as the following[4]:

$$\acute{V}_{cav-amp} = \acute{V}_{fwd} + \acute{V}_{refl} = \acute{V}_{fwd}(1 + r) = \acute{I}_{fwd}Z_0(1 + r) \tag{2.12}$$

Where the primes (i.e. ´) are used for the primary side of the transformer (the quantities on the secondary side are without primes). From EQ. 2.11

[4]By $V_{cav-amp}$ we mean the cavity voltage which is generated by the amplifier. We use this naming convention to avoid confusions in the following section where we calculate the total cavity voltage (i.e. the sum of the amplifier-generated and beam-generated voltages in the cavity).

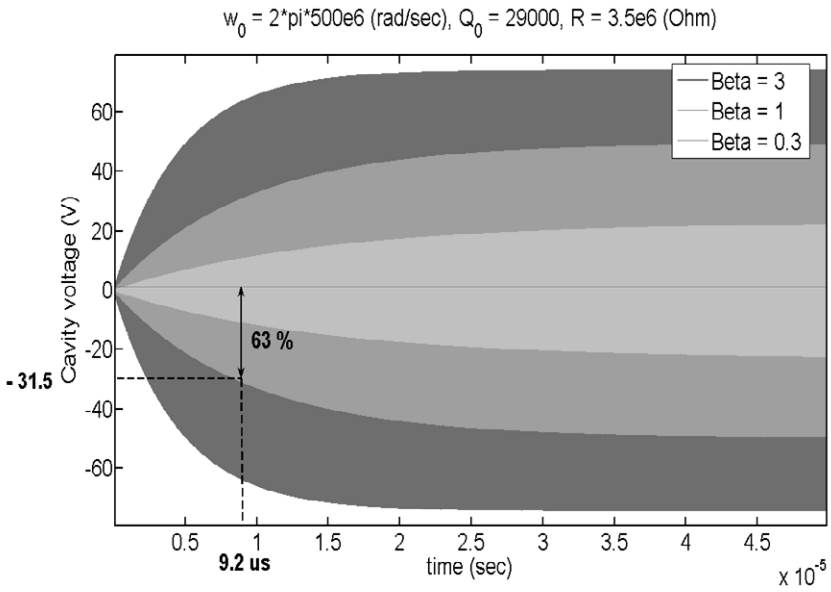

Figure 2.6: Transient response of the cavity with different coupling factors

and EQ. 2.12 the cavity impedance for the amplifier can be calculated as the following:

$$\acute{Z}_{cav-amp} = \frac{\acute{V}_{cav-amp}}{I_{amp}} = \frac{2\beta Z_0 L.s}{RLC.s^2 + \beta(L+1).s + R} \tag{2.13}$$

The last equation can be also written as the following:

$$\acute{Z}_{cav-amp} = \frac{\acute{V}_{cav-amp}}{\acute{I}_{fwd}} = \frac{2\beta Z_0}{\beta + 1 + Q_0\left(\frac{s}{\omega_0} + \frac{\omega_0}{s}\right)} \tag{2.14}$$

FIG. 2.6 shows the transient cavity response to a sinusoidal forward current with $\omega = \omega_0$ and different coupling factors.

2.1.4 Band-width and quality factor of the loaded cavity

Now, we derive a formula for the bandwidth and quality factor of the loaded cavity (i.e. cavity with coupler). As this analysis is valid in steady-state, we replace s by $j\omega$ in EQ. 2.1 and EQ. 2.12. This will give us:

$$Z(j\omega) = \frac{\beta.Z_0}{1 + jQ_0\zeta} \qquad (steady\ state) \tag{2.15}$$

$$\acute{V}_{cav-amp}(j\omega) = \acute{V}_{fwd}(j\omega)\frac{2\beta}{\beta + 1 + jQ_0\zeta} \qquad (steady\ state) \tag{2.16}$$

Where ζ is the normalized cavity detuning defined as:

$$\zeta = \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \tag{2.17}$$

The cavity power will be:

$$P_{cav} = P_{loss} = P_{fwd} \frac{4\beta^2}{(\beta+1)^2 + {Q_0}^2 \zeta^2} \tag{2.18}$$

The peak power occurs when $\zeta = 0$ ($\omega = \omega_0$). This will give:

$$\zeta = 0 \quad \Rightarrow \quad P_{loss} = P_{fwd} \frac{4\beta^2}{(\beta+1)^2} \tag{2.19}$$

Now, we calculate ω_{3dB} where by definition the cavity power is half of its peak value:

$$P_{loss}(\omega = \omega_{3dB}) = 0.5 P_{loss}(\omega = \omega_0) \tag{2.20}$$

Therefore we'll have:

$$P_{fwd} \frac{4\beta^2}{(\beta+1)^2 + {Q_0}^2 \zeta_{3dB}^2} = 0.5 \frac{4\beta^2}{(\beta+1)^2} \tag{2.21}$$

This will result in:

$$Q_0 \zeta_{3dB} = \beta + 1 \tag{2.22}$$

On the other hand, for small detuning (i.e. when $\omega \approx \omega_0$) we have:

$$\zeta = \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} = \frac{\omega^2 - {\omega_0}^2}{\omega\omega_0} \cong \frac{(\omega_0 + \Delta\omega)^2 - {\omega_0}^2}{\omega_0^2} \approx \frac{2\Delta\omega}{\omega_0} \tag{2.23}$$

Therefore, at ζ_{3dB} we'll have:

$$\zeta_{3dB} \approx \frac{2\Delta\omega_{3dB}}{\omega_0} = \frac{1}{Q} \tag{2.24}$$

where, by definition we have:

$$Q = \frac{\omega_0}{B.W.} = \frac{\omega_0}{2\Delta\omega_{3dB}}$$

By comparing EQ. 2.22 to EQ. 2.24 we'll get:

$$Q = \frac{\omega_0}{2\Delta\omega_{3dB}} = \frac{1}{\zeta_{3dB}} = \frac{Q_0}{\beta+1} \tag{2.25}$$

EQ. 2.25 gives loaded quality factor Q[5] in terms of the unloaded quality factor Q_0 and the coupling factor β.

FIG. 2.7 shows $\frac{P_{cav}}{P_{fwd}}$ versus detuning frequency for different coupling factors. As it can be seen, the response of the cavity depends on the coupling factor.

[5] By definition, loaded quality factor is the cavity quality factor with the coupler.

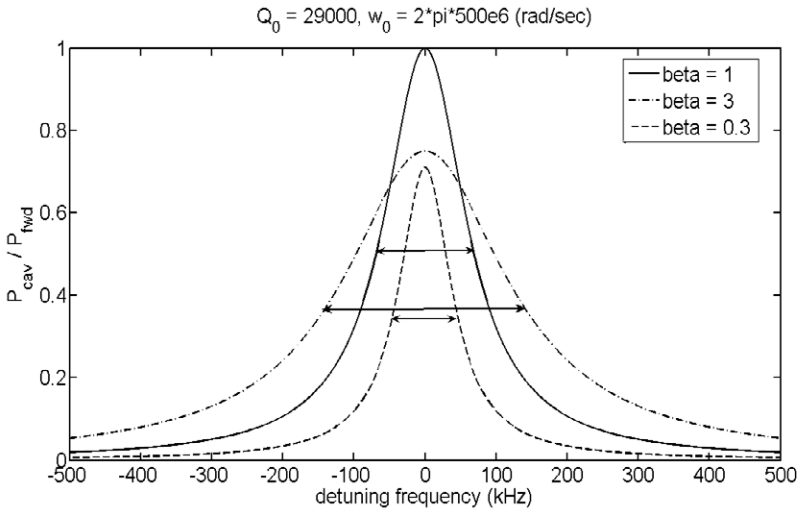

Figure 2.7: Frequency response of the cavity for different coupling factors

2.1.5 Cavity filling time and time-constant

The time-constant of the cavity τ can be calculated as the following:

$$\tau = \frac{1}{B.W.} = \frac{1}{2\Delta\omega_{3dB}} = \frac{Q}{\omega_0} \tag{2.26}$$

The cavity power then scales as:

$$P_{cav} \propto e^{-\frac{t}{\tau}} \tag{2.27}$$

The cavity voltage scales with τ_V which is twice the power time-constant τ.

$$\tau_V = 2\tau = \frac{2Q}{\omega_0} \tag{2.28}$$

$$V_{cav} \propto \sqrt{P_{cav}} \propto e^{-\frac{t}{\tau_V}}$$

For example with $\beta = 1$ we read a time constant $\tau = 9.2\ \mu s$ in FIG. 2.6 which can also be calculated as the following:

$$\tau_V = \frac{2Q}{\omega_0} = \frac{2 \times 14900}{2\pi \times 499.654e6} = 9.2\ \mu s$$

Using the instantaneous values of the forward and reflected voltages (i.e. $V_{fwd}(t)$, $V_{refl}(t)$), we calculate the forward, reflected and cavity power in time domain as follows:

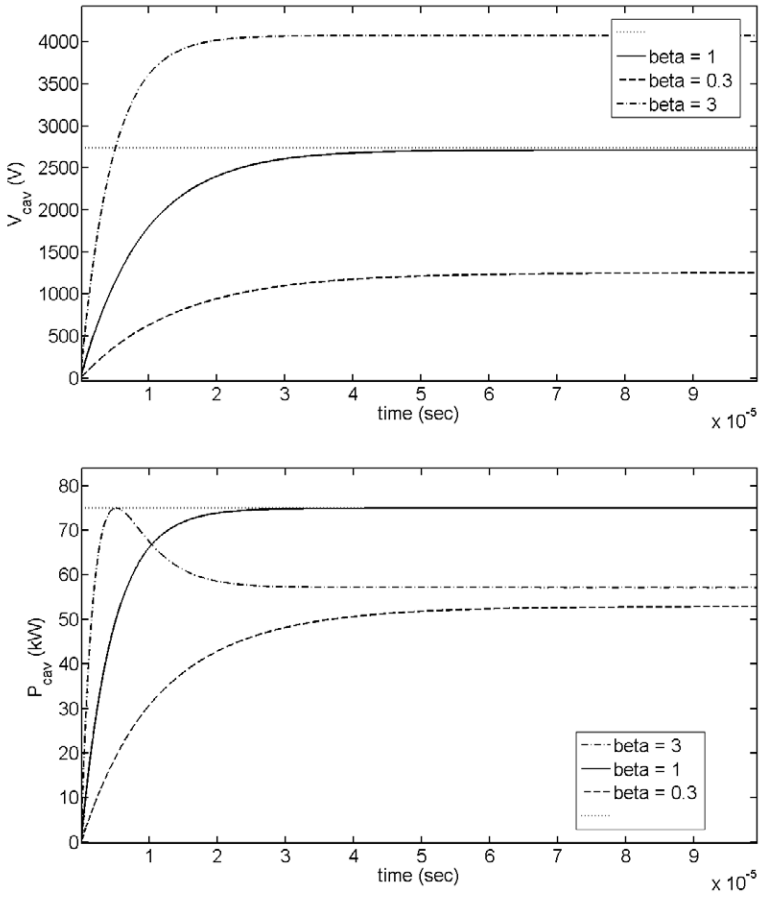

Figure 2.8: Transient cavity voltage (top) and power (bottom) with different coupling factors

$$\begin{aligned} P_{fwd}(t) &= \frac{\acute{V}^2_{fwd}(t)}{Z_0} \\ P_{refl}(t) &= \frac{\acute{V}^2_{refl}(t)}{Z_0} \\ P_{cav}(t) &= P_{fwd}(t) - P_{refl}(t) \end{aligned} \tag{2.29}$$

The magnitudes of $V_{cav}(t)$ and $V_{refl}(t)$ are plotted in FIG. 2.8 and FIG. 2.9 together with their corresponding power waveforms for different β values[6].

[6]The power values are averaged over each RF period.

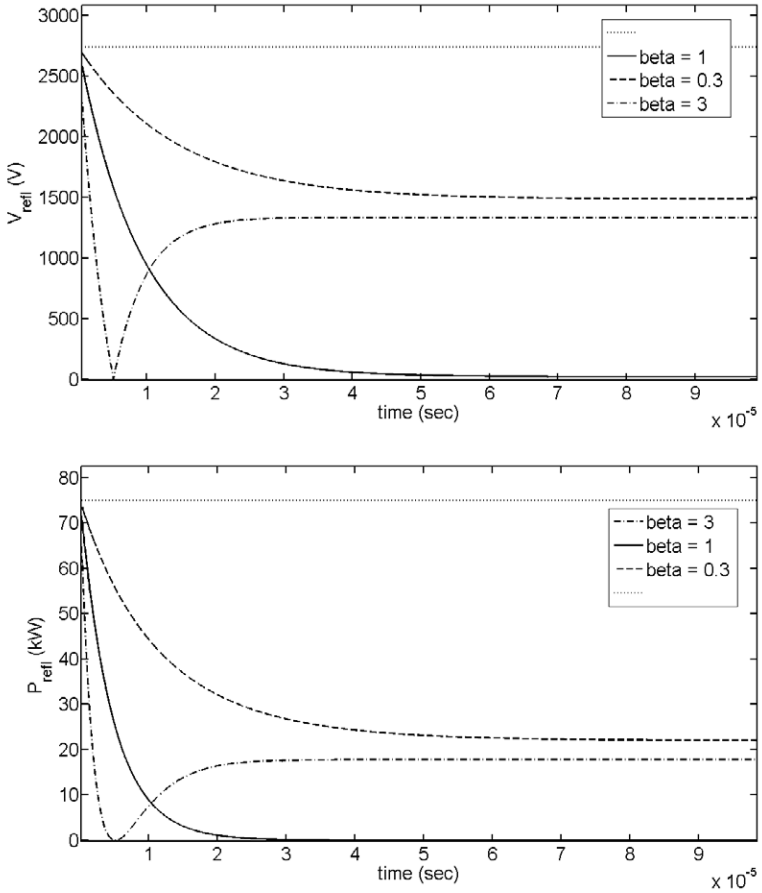

Figure 2.9: Transient reflected voltage (top) and power (bottom) with different coupling factors

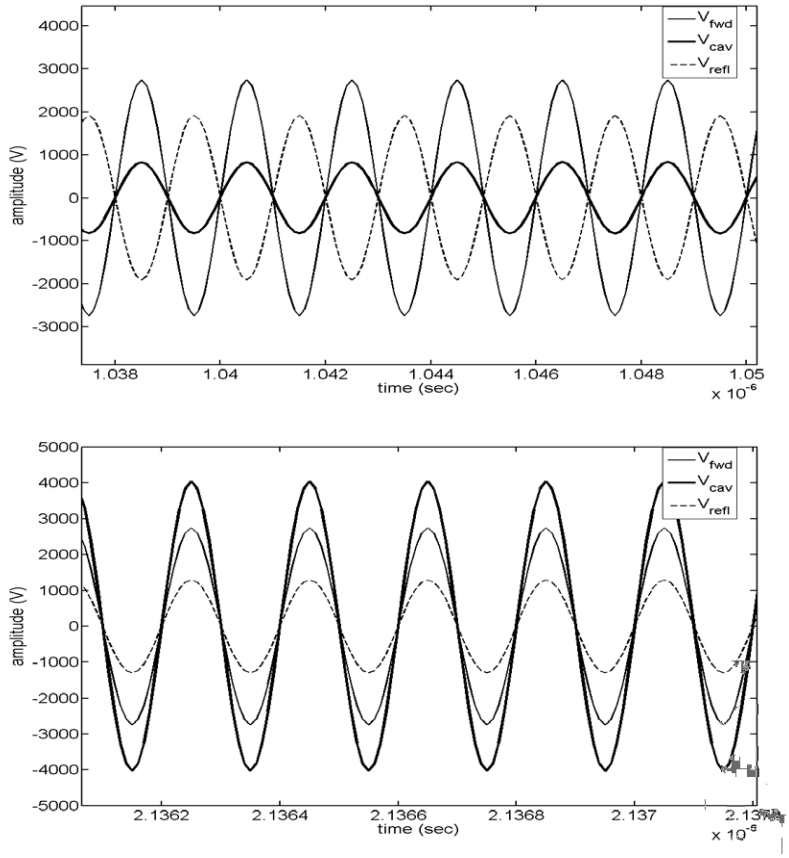

Figure 2.10: Top - Forward, cavity and reflected voltages before $t = 5\ \mu s$ ($\beta = 3$); Bottom - Forward, cavity and reflected voltages after $t = 5\ \mu s$ ($\beta = 3$)

As one can see in FIG. 2.8 when $\beta = 3$, the cavity voltage becomes even larger than the forward voltage. This is due to the fact that $V_{refl}(t)$ changes its phase by 180 °at $t \approx 5\ \mu s$ for the cavity under study. Therefore for $t > 5\ \mu s$ the magnitude of the reflected voltage adds to the forward voltage instead of being subtracted from it as can also be seen in FIG. 2.10.

The higher cavity voltage, however, does not mean more power transfer into the cavity as in this case the cavity impedance is three times higher than when $\beta = 1$.

2.1.6 Cavity detuning

The waveforms that we have plotted so far are for $\zeta = 0$ (i.e. $\omega = \omega_0$). In this condition regardless of the β value, the cavity presents a pure resistive load (in

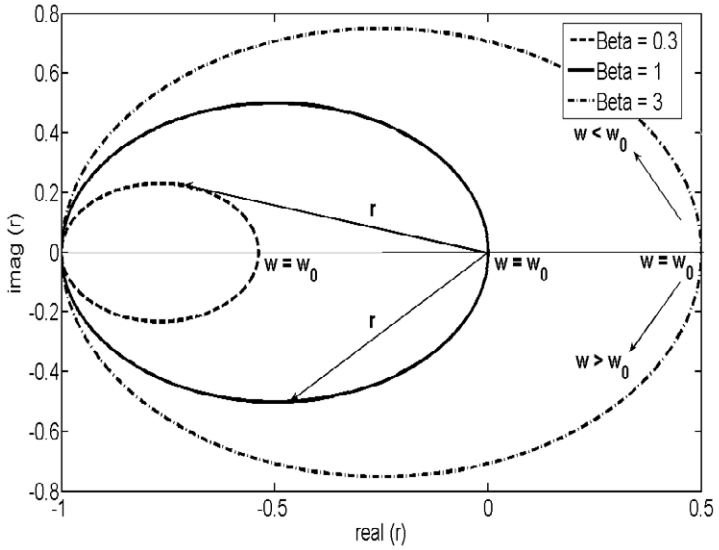

Figure 2.11: Reflection coefficient versus frequency

steady state) to the amplifier, resulting in zero reactive power while there might exist reflected power. In general, depending on the detuning factor ζ the cavity impedance can have an imaginary component as well as its real component (although it is not desirable when there is no beam).

Here, we calculate the real and imaginary parts of the reflection coefficient of the cavity. Using the following equations:

$$r = \frac{Z - Z_0}{Z + Z_0} \qquad Z = \frac{\beta . Z_0}{1 + jQ_0\zeta}$$

$Re(r)$ and $Im(r)$ are calculated as:

$$r = Re(r) + Im(r) = \frac{\beta - 1 - jQ_0\zeta}{\beta + 1 + jQ_0\zeta}$$

$$\begin{aligned} Re(r) &= \frac{(\beta+1)(\beta-1) - {Q_0}^2\zeta^2}{(\beta+1)^2 + {Q_0}^2\zeta^2} \\ Im(r) &= -\frac{2\beta Q_0\zeta}{(\beta+1)^2 + {Q_0}^2\zeta^2} \end{aligned} \tag{2.30}$$

The complex reflection coefficients are plotted in FIG. 2.11 for $Q_0 = 29000$ and different β values.

As one can see in FIG. 2.11, the plots of the reflection coefficient in the complex plane are circles all passing through the $(-1, 0)$ point with their radius

depending on the coupling factor. For a perfect impedance match, r must be zero. This only happens with $\omega = \omega_0$ and $\beta = 1$. Note that for a given cavity with fixed β and Q_0 the reflection coefficient only depends on the cavity detuning ζ.

FIG. 2.12 shows the cavity voltage for different values of cavity detuning and different coupling factors.

As an illustrative example, we use the previous equations to calculate the steady state cavity voltage when there is detuning. With $\beta = 0.3$ and detuning = 50 kHz we will have:

$$\zeta = \frac{499.654e6}{499.654e6 + 50e3} = \frac{499.654e6 + 50e3}{499.654e6} = -2.0e-4$$

This will result in (EQ. 2.16):

$$\acute{Z}_{cav-amp} = \frac{\acute{V}_{cav-amp}}{\acute{I}_{fwd}} = \frac{2\beta Z_0}{\beta + 1 + j.Q_0\zeta}$$

$$= \frac{2 \times 0.3 \times 50}{0.3 + 1 - j29000 \times 2e-4} = 11 + 4.9j[\Omega] = 5\angle 77.4^\circ[\Omega]$$

The simulated $\acute{V}_{cav-amp}$ versus $\acute{I}_{fwd}$ in steady state verifies this result (see FIG. 2.13).

2.1.7 Reflected power vs. reactive power

As we have seen so far, when $\zeta = 0$, there is no reactive power flowing in the transmitter-cavity system. This is due to the fact that the cavity impedance has no imaginary component; therefore the forward current and the cavity voltage are in phase resulting in zero reactive power although reflected power might be zero or not depending on β. With $\zeta \neq 0$, the cavity impedance has an imaginary component as well as its real component. The real part of the impedance results in power losses in the cavity (i.e. P_{loss}) while the imaginary part results in reactive power. We investigate this in more details giving one example. We consider again the case $\beta = 0.3$ and $\zeta = -2.0e-4$. We'll have:

$$\begin{aligned}
\acute{I}_{fwd} &= \acute{I}_{amp} = 54.77\angle 0^\circ = 54.77 + 0j\ [A] \qquad (by\ assumption) \\
\acute{V}_{fwd} &= Z_0.\acute{I}_{fwd} = 2788.5\angle 0^\circ = 2788.5 + 0j\ [V] \\
\acute{V}_{cav-amp} &= 54.77\angle 0^\circ \times 5\angle 77.4^\circ = 273.85\angle 77.4^\circ = 59.74 + 267.25j\ [V] \qquad (EQ.\ 2.16) \\
\acute{V}_{refl} &= \acute{V}_{cav-amp} - \acute{V}_{fwd} = 2741.82\angle 174.4^\circ = -2728.86 + 267.25j\ [V] \\
\acute{I}_{refl} &= \acute{V}_{refl}/Z_0 = 54.84\angle 174.4^\circ = -54.58 + 5.35j\ [A] \\
\acute{I}_{cav-amp} &= \acute{I}_{fwd} - \acute{I}_{refl} = 109.48\angle -2.8^\circ = 109.35 - 5.35j\ [V] \\
P_{fwd} &= 0.5\left|\acute{V}_{fwd}\right|.\left|\acute{I}_{fwd}\right| = 75\ [kW]
\end{aligned}$$

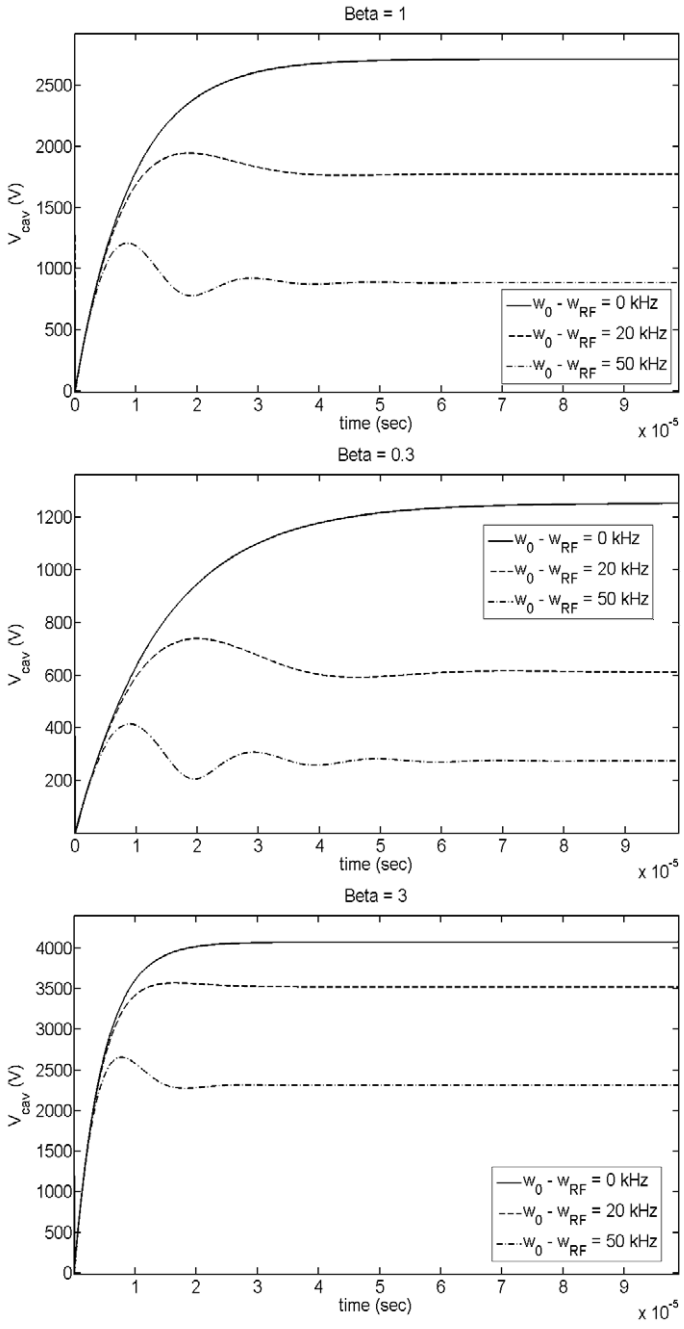

Figure 2.12: Transient cavity voltage with detuning = 0, 20 kHz and 50 kHz (Top: $\beta = 1$; Middle: $\beta = 0.3$; Bottom: $\beta = 3$)

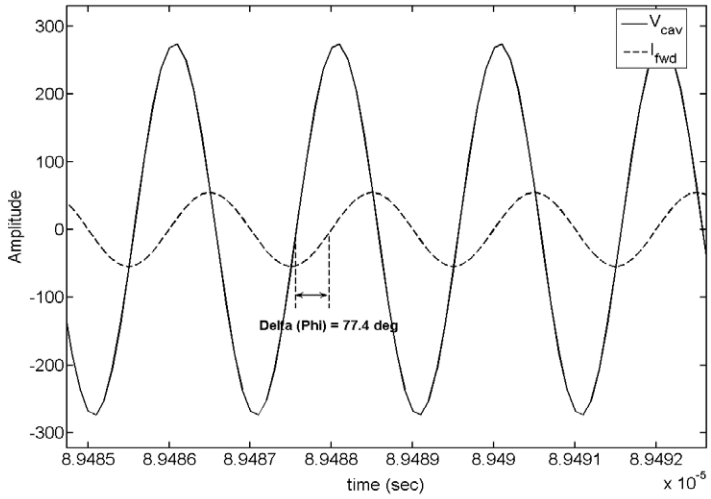

Figure 2.13: Cavity voltage and forward current in steady state (detuning=50 kHz, $\beta = 0.3$)

$$
\begin{aligned}
P_{active} &= P_{loss} = 0.5 \left|\acute{V}_{cav-amp}\right| . \left|\acute{I}_{cav-amp}\right| . \cos(\angle \acute{V}_{cav-amp} - \angle \acute{I}_{cav-amp}) = 2.5\ [kW] \\
P_{reactive} &= 0.5 \left|\acute{V}_{cav-amp}\right| . \left|\acute{I}_{cav-amp}\right| . \sin(\angle \acute{V}_{cav-amp} - \angle \acute{I}_{cav-amp}) = 14.8\ [kVAR] \\
P_{refl} &= P_{fwd} - P_{loss} = 75 - 2.5 = 72.5\ [kW]
\end{aligned}
$$

In this case, the amplifier generates a total forward power of 75 kW flowing in the transmission line. From this amount, only 2.5 kW enters the cavity (due to the bad impedance matching of the cavity to the transmission line) while the rest (i.e. 72.5 kW) reflects back towards the amplifier. Also, due to the imaginary component of the cavity impedance, there exists a phase difference of 80.2° between the cavity current and voltage resulting in a reactive power of 14.8 kVAR in the cavity.

In optimum conditions when the cavity is perfectly matched to the amplifier, all the amplifier power enters the cavity and the reflected power goes down to zero.

2.2 Cavity Modeling and Simulation with Beam

In Section 2.1 a transient model for the RF cavity without beam was presented. Although this simple model can explain the most important time-domain and frequency-domain aspects of the RF cavity, it will not be valid anymore when there is beam. Presence of the beam causes a significant change in the amplitude and phase of the cavity voltage. Assuming that the RF amplifier feeds the cavity

with the same forward current, it will see a different cavity voltage upon the beam arrival. As this will be equivalent to a different cavity impedance, the previous conditions for impedance matching will not be valid anymore. Here, the objective is to minimize the reflected power to avoid amplifier saturation and unnecessary power losses. This implies finding new values for the cavity detuning and coupling factor to keep the cavity matched to the amplifier for a certain beam current and phase. Once matching conditions are fulfilled, any changes in the beam current or phase will cause an impedance mismatch, hence another values for the coupling factor and detuning must be found to eliminate the reflected power again. It should also be noted that although the detuning frequency can be controlled during the operation of the RF system, it would not be convenient to change the coupling factor because it implies changing the orientation of the coupling loop in the cavity. Therefore, the coupling factor is normally set for the maximum beam current, which is considered the worst-case, and it is kept at that position unless the cavity should be optimized for another beam current[7].

This section starts with the definition of the beam. We will also briefly explain conditions which are needed for beam stability with an impact on the beam-generated cavity voltage. Then, we will expand the cavity model, which was developed in Section 2.1, so that it also takes the influence of the beam into account. Finally, we will present an analytical solution for the coupling factor and detuning in order to match the cavity to the RF transmitter when there is beam.

2.2.1 The beam

The beam is the flow of particles in the accelerator. The beam consists of many particle bunches[8] distributed around the accelerator according to a pre-defined Filling Pattern[9]. The minimum possible separation between two bunches in time domain is equal to one RF period. In ALBA, for instance, this is about 2 ns corresponding to 60 cm in air while the bunch length is in the order of few millimeters.

As an example, the nominal ALBA beam current is 400 mA and the circumference of the storage ring is 268.8 m. Taking the RF frequency (i.e. 500 MHz) into account, the harmonic number[10] will be 448. Considering a uniform

[7] In some accelerator facilities, there have been proposals for movable cavity couplers even though mechanically, it might be a complex device. In that case, the coupling factor can be changed during RF operation by turning the coupling loop to keep the reflected power minimized even if the beam current changes.

[8] Bunch is the ensemble of many particles filling one bucket. Bucket is an imaginary space on the beam path (defined by optical parameters) in which the particles can survive. Particles which are outside the buckets will be lost.

[9] Filling Pattern defines how empty buckets are filled with particles. The most straightforward filling pattern is the uniform one which means all the buckets are filled with particles. Other types of filling patterns such as one-third are also common due to different reasons such as improvement of the beam stability and ion clearing. In this case, one-third of the buckets around the accelerator are filled consecutively and the rest are left empty.

[10] Harmonic number is the total number of buckets around the ring which is calculated as:

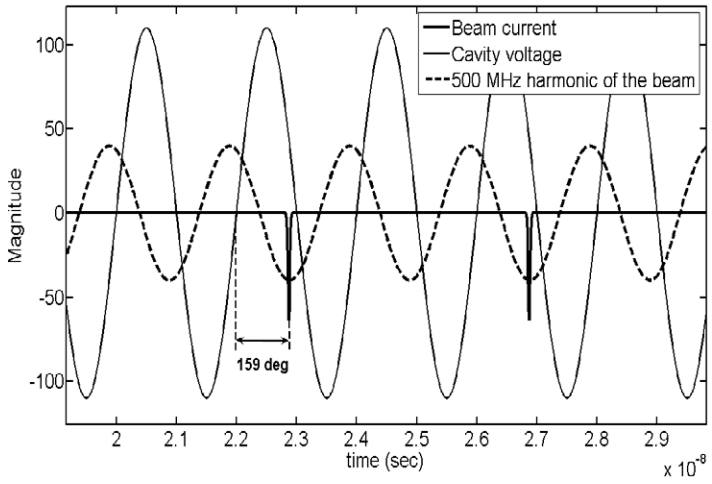

Figure 2.14: Demonstration of the Synchronous Phase (waveforms are not in scale)

filling pattern, the charge in each bunch will be 8e-10 C which is equivalent to 5 billion electrons.

The charge of each bunch has a Gaussian distribution in space. For stability reasons, the beam should have a certain phase difference with respect to the cavity voltage. This is called Synchronous Phase[11] and its value is 159° for ALBA as demonstrated in FIG. 2.14.

It should be noted that in reality, unlike what is shown in FIG. 2.14, the beam pulse does not see a single value of the cavity voltage. This is because it takes half an RF period until the bunch traverses the cavity cell[12]. The bunch will therefore see all the cavity voltages from the time instant it enters the cavity from one beam port until it leaves the cavity from the other port. Although our lumped RLC model can not represent this transit time, its effect can be compensated by multiplying the nominal shunt impedance[13] of the cavity by the Transit Time Correction Factor.

Taking the cavity transit time into account, the Synchronous Phase is defined as the phase difference between the cavity voltage and the crest of the bunch when the bunch is in the center of the cavity.

Contrary to synchrotrons, in Linacs, the synchronous phase might not have a

$h = \frac{Circ. \times f_0}{C}$ where $Circ.$ is the circumference of the ring in meters, f_0 is the RF frequency in $Hertz$ and C is the speed of light in m/s.

[11] Synchronous Phase is the phase difference between the zero crossing of the cavity voltage and the crest of the beam pulse. In some texts it might be alternatively defined as the phase difference between the peak of the cavity voltage and the crest of the beam pulse.

[12] Here, we assume that the cavity length is half of the RF wavelength.

[13] The nominal shunt impedance is the one which is used for beam optics calculations.

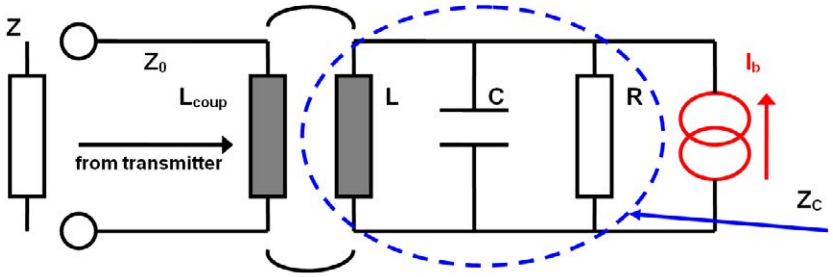

Figure 2.15: Cavity impedance as seen by the beam

single value. For instance, in the ESS-B RFQ[14], the synchronous phase changes by tens of degrees as the bunch travels from one end of the RFQ to the other end.

2.2.2 Influence of the beam on the RF cavity

So far, we have only considered the RF cavity without beam. Although this assumption is valid in an RF laboratory (because there, beam can not be generated) and -to some degree- in a booster synchrotron (because the beam has a negligible effect on the cavity voltage due to its low current), it is not valid anymore in a storage ring or a typical Linac where the beam-generated cavity voltage is comparable to the amplifier-generated voltage. Presence of the beam causes a dramatic change in the cavity impedance seen by the RF amplifier thus resulting in a significant change in the amplitude and phase of the cavity voltage if not compensated. Furthermore, the impedance change results in reflected power from the cavity traveling back towards the RF amplifier. These unwanted effects, which we refer to as Beam Loading, are compensated by the so-called amplitude, phase and tuning loops[15] which are parts of the LLRF system of an RF plant.

FIG. 2.15 shows the cavity model supplied by an additional current source representing the beam.

The cavity voltage due to the beam can be calculated by multiplying the cavity impedance by the beam current.

As we have calculated in Section 2.1.1, the cavity impedance (without coupler) is:

$$Z_c = \frac{RL.s}{RLC.s^2 + L.s + R}$$

Now, we consider the coupler which is modeled by the transformer. As the primary side of this transformer is terminated in Z_0, the coupler effect on

[14]Radio Frequency Quadrupole
[15]The function of these loops is explained in details in the following chapters.

the cavity impedance can be taken into account by putting a resistor equal to $Z_0 \frac{L}{L_{coupl}} = \frac{R}{\beta}$ in parallel to R. Therefore in the RLC model, R should be replaced by: $R_{eq} = R \| \frac{R}{\beta} = \frac{R}{1+\beta}$. This will result in:

$$Z_{cav-beam} = \frac{RL.s}{RLC.s^2 + L(\beta+1).s + R} \tag{2.31}$$

where $Z_{cav-beam}$ is the cavity impedance seen by the beam.

In order to be compatible with the cavity impedance calculated in Section 2.1.2, we move $Z_{cav-beam}$ to the primary side of the transformer. This is done by multiplying $Z_{cav-beam}$ with $\frac{L_{coupl}}{L} = \frac{\beta Z_0}{R}$. Then, we will have:

$$\acute{Z}_{cav-beam} = \frac{\beta Z_0 L.s}{RLC.s^2 + L(\beta+1).s + R} \tag{2.32}$$

Note that apart from a factor of two[16], the cavity impedance for the beam is the same as the one for the amplifier (see EQ. 2.13).

FIG. 2.16 shows the simulated cavity voltage due to a pulsed beam (here, we assume one bucket out of each three is filled) and compares the result to a sinusoidal beam with a peak value twice larger than the DC beam current.

As one can see in the figure, the response of the cavity is not much different in both cases. The difference becomes smaller and smaller as the cavity voltage grows until it finally reaches its steady-state value. For simulations though, it would be much easier to consider a sinusoidal source rather than a pulsed one. Therefore, in the following simulations we approximate the beam by a sinusoidal current source unless it is stated otherwise.

The beam-generated voltage on the primary side will be:

$$\acute{V}_{cav-beam} = \acute{I}_{beam}.\acute{Z}_{cav-beam} \tag{2.33}$$

Where $\acute{I}_{beam}$ and $\acute{Z}_{cav-beam}$ are the transferred beam current and cavity impedance respectively.

Considering a sinusoidal beam with the same frequency as the RF amplifier, the magnitude of $\acute{I}_{beam}$ can be calculated as the following:

$$\left|\acute{I}_{beam}\right| = 2I_{DC}\sqrt{\frac{L}{L_{coupl}}} = 2I_{DC}\sqrt{\frac{R}{\beta Z_0}} \tag{2.34}$$

where I_{DC} is the nominal average beam current.

It should also be noted that contrary to what is shown in FIG. 2.16, the beam current does not contribute to building up voltage in the cavity. In reality, the phase difference between the beam and the cavity voltage is so that the beam absorbs power from the cavity; therefore it tends to reduce the cavity voltage. The absorbed power accelerates the particles, hence compensates for the losses

[16] A rough explanation of this missing factor of two is given here: The beam sees the parallel combination of the shunt impedance and the transformed characteristic impedance; therefore, only half of the beam current contributes to the cavity voltage while by assumption all the forward current contributes to building up voltage in the cavity.

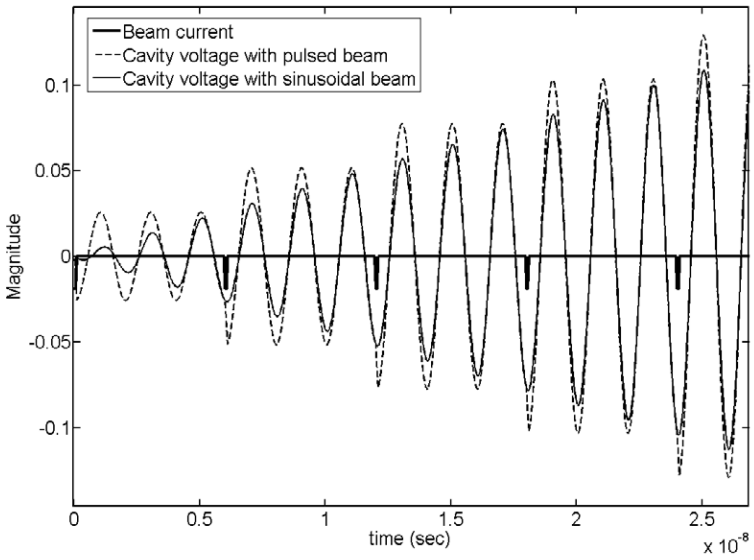

Figure 2.16: Comparison between the simulated cavity voltages due to pulsed and sinusoidal beams upon beam arrival (the beam current is not in scale).

due to synchrotron radiation (in synchrotrons) or increases the beam energy (in Linacs).

2.2.3 Transient cavity response due to the amplifier and beam

Now, we simulate the cavity voltage with the presence of the RF amplifier and the beam. In this case we have to supply our cavity model with two current sources (one to represent the RF amplifier and the other to represent the beam). We use the *Superposition Theorem* to calculate the total cavity voltage due to both sources:

$$\begin{aligned} \acute{V}_{total}(s) &= \acute{V}_{cav-amp}(s) + \acute{V}_{cav-beam}(s) \\ &= \acute{I}_{amp}(s).\acute{Z}_{cav-amp}(s) - \acute{I}_{beam}(s).\acute{Z}_{cav-beam}(s) \end{aligned} \quad (2.35)$$

Where $\acute{V}(s)_{total}(s)$ is the total cavity voltage on the primary side and $\acute{I}_{amp}(s)$ and $\acute{I}_{beam}(s)$ are the Laplace transforms of the amplifier and beam currents respectively (their phase difference must be taken into account). The negative sign before $\acute{I}_{beam}(s)$ accounts for the negative beam current (the magnitude of $\acute{I}_{beam}(s)$ in the equations is assumed to be positive).

Using EQ. 2.13 and EQ. 2.32, we will have:

$$\acute{V}_{total}(s) = \left(2\acute{I}_{amp}(s) - \acute{I}_{beam}(s)\right) \frac{\beta Z_0 L.s}{RLC.s^2 + L(\beta+1).s + R} \qquad (2.36)$$

Example 2-1: Here we assume that we have a cavity with $\omega_0 = 2\pi.500e6\ rad/sec$, $Q_0 = 29000$ and $R = 3.5\ M\Omega$ and we want to keep the cavity voltage at 600 kV_{peak} with phase angle=69° with respect to the beam (i.e. $\varphi_S = 69° + 90° = 159°$) with the beam current being $I_{DC} = 400$ mA. First, we assume that we want to achieve this cavity voltage with coupling factor $\beta = 1$ and detuning $\zeta = 0$.

Recalling EQ. 2.36 in steady state conditions and considering the beam we will have:

$$\acute{V}_{total} = (2\acute{I}_{amp} - \acute{I}_{beam}) \frac{\beta Z_0}{\beta + 1 + jQ_0\zeta} \qquad (steady\ state) \qquad (2.37)$$

Substituting $\acute{V}_{total}$ and $\acute{I}_{beam}$ by their values (they are referred to the primary side) we will have:

$$600e3\angle 69°.\sqrt{\frac{\beta Z_0}{R}} = (2\acute{I}_{amp} - 0.4\times 2\angle 0°.\sqrt{\frac{R}{\beta Z_0}}).\frac{\beta Z_0}{\beta + 1 + jQ_0\zeta} \qquad (steady\ state)$$

After solving this equation for $\acute{I}_{amp}$ we will have: $\acute{I}_{amp} = 129.1\angle 19.1°\ A$ (the reference phase is assumed to be the phase of the beam). FIG. 2.17 shows the simulations results with this value of the forward current.

As one can see in FIG. 2.17 (middle), before the arrival of the beam, the steady state reflected voltage is zero due to the values of the coupling factor and detuning. After the beam arrival, however, there is a significant amount of reflected voltage. The total forward power is 416.7 kW from which 86 kW goes to the beam, 51.4 kW dissipates in the cavity walls and the rest (i.e. 279.3 kW) reflects from the cavity due to improper matching with the beam.

2.2.4 Compensation of steady state beam loading

As it was verified by the example 4-1, with $\beta = 1$ and $\zeta = 0$, the steady state reflected power is only zero if there is no beam. Here, we present an analytical solution for β and ζ aiming at eliminating the reflected power for a certain beam current and phase. As this analysis in valid in steady state, we use EQ. 2.37 again. After rearranging this equation we will have:

$$\acute{V}_{total} = \acute{I}_{amp}(2 - A.e^{j\omega T}).\frac{\beta Z_0}{\beta + 1 + jQ_0\zeta} \qquad (steady\ state) \qquad (2.38)$$

Where A is the normalized magnitude of the transferred beam current by the forward current and T is the delay of the beam current with respect to the cavity voltage calculated as the followings:

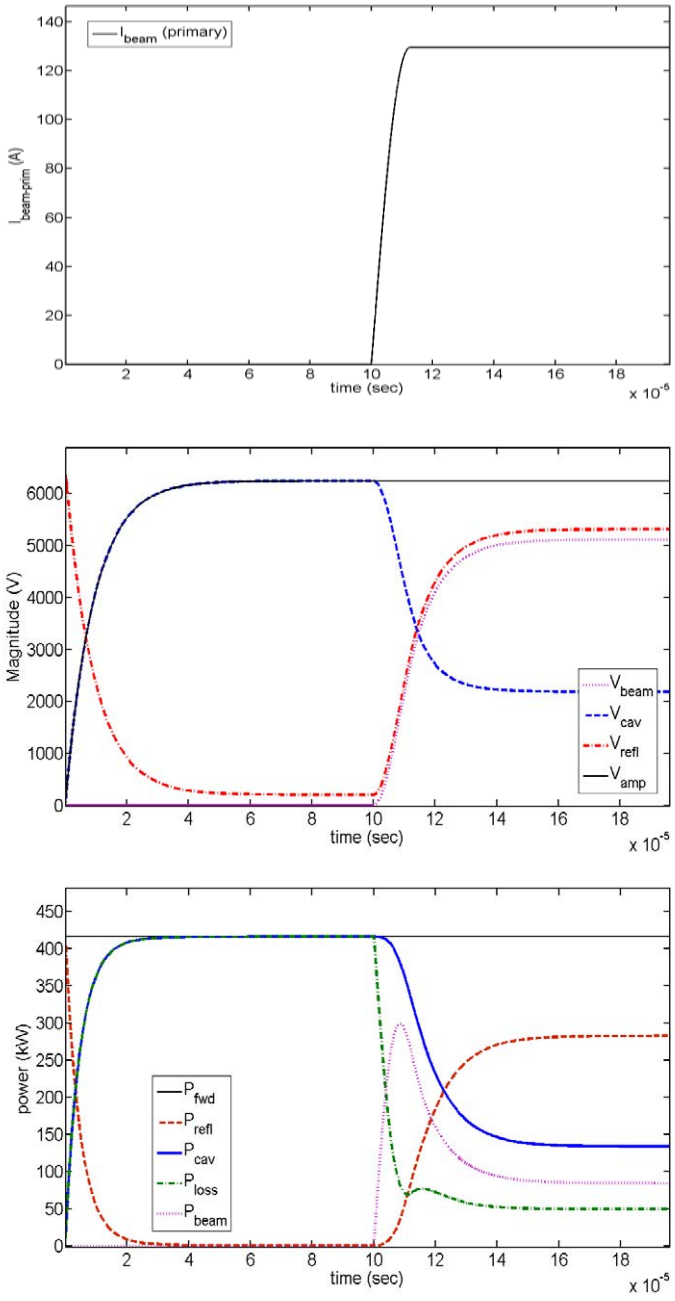

Figure 2.17: Simulation results for the unmatched cavity with beam ($\beta = 1$,$\zeta = 0$); Top - beam current referred to the primary side; Middle - cavity, beam, reflected and amplifier voltages (all referred to the primary side); Bottom - forward, reflected, cavity, loss and beam powers

$$A = \frac{2I_{DC}}{\left|\acute{I}_{amp}\right|}.\sqrt{\frac{R}{\beta Z_0}} \tag{2.39}$$

$$T = \frac{\varphi - 90^\circ}{\omega}.\frac{\pi}{180^\circ} \tag{2.40}$$

From equations EQ. 2.38 and EQ. 2.40 we will have:

$$\acute{Z}_{total} = \frac{\acute{V}_{total}}{\acute{I}_{amp}} = \frac{\beta(2 - A.sin\varphi_S - jA.cos\varphi_S)Z_0}{\beta + 1 + jQ_0\zeta} \tag{2.41}$$

In order to match the cavity to the RF transmitter, the right-hand side of EQ. 2.41 must be equal to Z_0. This will result in:

$$\frac{\beta(2 - A.sin\varphi_S - jA.cos\varphi_S)}{\beta + 1 + jQ_0\zeta} = 1$$

Solving for the real and imaginary parts we will have:

$$\begin{aligned} \beta &= \frac{1}{1 - A.sin\varphi_S} = \frac{1}{1 - \frac{2I_{DC}}{|I_{amp}|}\sqrt{\frac{R}{\beta Z_0}}sin\varphi_S} \\ \zeta &= \frac{-A\beta.cos\varphi_S}{Q_0} = -\frac{2I_{DC}}{|I_{amp}|}.\sqrt{\frac{R}{\beta Z_0}}.\frac{\beta.cos\varphi_S}{Q_0} \end{aligned} \tag{2.42}$$

With this choice of β and ζ the steady state reflected power from the cavity will be zero with the beam having a magnitude I_{DC} and a delay angle $\varphi_S - 90^\circ$ with respect to the total cavity voltage.

Example 2-2: Here, we repeat example 2-1 but this time we replace β and ζ by their optimum values obtained from EQ. 2.42. This will give us:

$$\begin{aligned} \beta &= 2.67 \\ \Delta f &= f - f_0 = 37.5\ kHz \end{aligned}$$

In this case, a forward power $P_{fwd} = 137.4\ kW$ and an amplifier current $I_{amp} = 74.1\angle 69^\circ\ A$ will be needed to maintain the cavity voltage as its desired magnitude and phase (i.e. 3705.6 V_P on the primary side with 69° phase difference with respect to the beam current). This shows a significant decrease in the required forward power which is the result of proper matching of the cavity to the RF transmitter. The results of these simulations are shown FIG. 2.18.

As one can see in the figures, with this choice of coupling factor and detuning, the reflected power goes down to zero in the presence of the beam (the little offset in the steady state reflected voltage is because of the simulation errors due to the choice of the time step). It can also be seen in FIG. 2.18 (bottom) that before the beam arrival (i.e. $t < 100\ \mu s$), there is a significant amount of

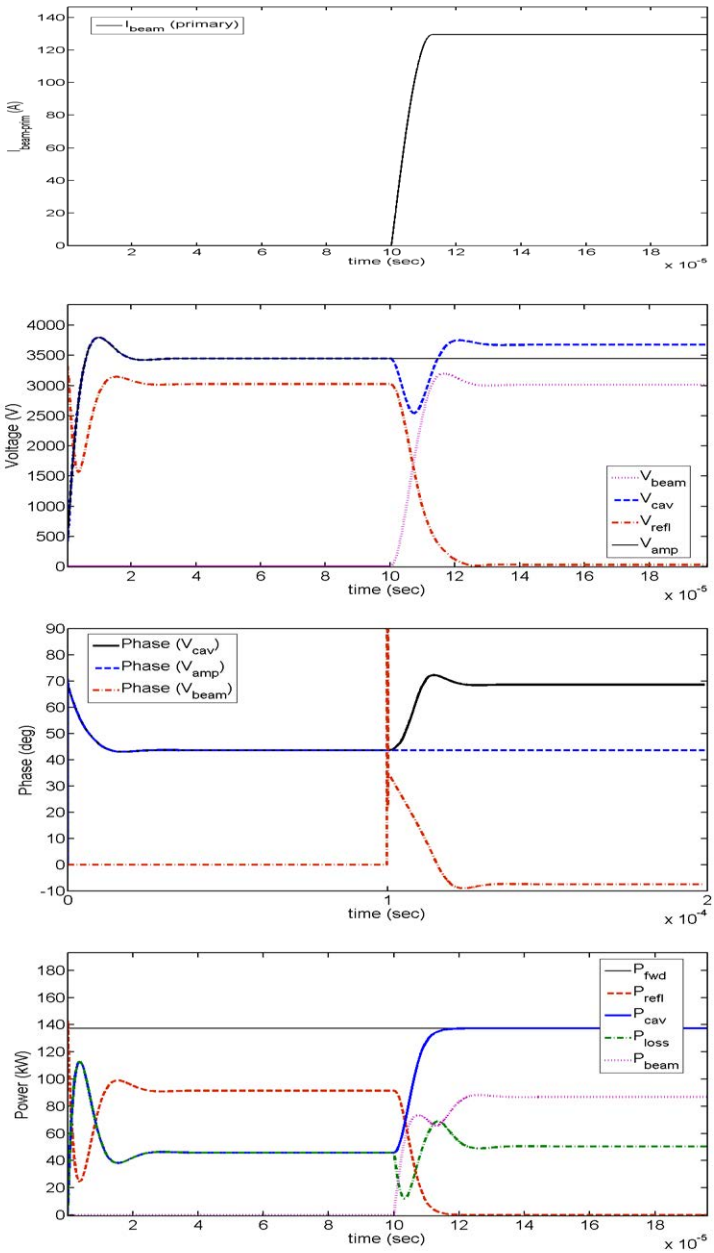

Figure 2.18: Simulation results for the matched cavity with beam; Top - beam current referred to the primary side; Second from top - cavity, beam, reflected and amplifier voltages (all referred to the primary side); Third from top - cavity, beam and amplifier phases; Bottom - forward, reflected, cavity, loss and beam powers

reflected power due to the impedance mismatch. In this condition, the beam power is zero and all the cavity power is transformed into heat. FIG. 2.18 (third from top) shows that after the beam arrival, the cavity phase with respect to the beam settles at its desired value (i.e. 69°). As the reflected power with the beam is zero, the phase of the cavity voltage is the same as the phase of the amplifier current. Therefore, the cavity presents a pure resistive load to the RF transmitter.

It is also worth mentioning that in practice, regardless of the matching situation, the amplitude and phase loops keep the amplitude and phase of the cavity voltage at their desired values unless there is an amplifier saturation. If this happens, the cavity voltage will be lower than its desired value and the RF amplifier will not be able to deliver more power because it would exceed its actual power rating. With the tuning loop working properly, the phase difference between the forward voltage and the cavity voltage will be a fixed value corresponding to the delay time between the measurement points for the forward and cavity voltages. This, together with the right coupling factor will create ideal matching conditions, resulting in zero reflected power. In this condition, all the amplifier power enters the cavity; part of this power will be given to the beam and the rest will be dissipated in the cavity walls. When the reflected power is zero, the conditions for the regulation of the cavity voltage become more relaxed because the amplifier is farther from its saturation threshold.

2.3 Summary and concluding remarks

This chapter has discussed RF cavity modeling and simulation. The cavity and its input power coupler, in their general form, are modeled as a shunt RLC circuit and a step-up transformer respectively. The RF amplifier is modeled as a current source supplying the cavity through a transmission line with the characteristic impedance Z_0. Although this generic model can explain some of the most important aspects of the cavity, two additional considerations are required so that the model leads to correct and informative results. These are 1) cavity impedance mismatches to the transmission line and 2) cavity transient response. In the existing articles on cavity modeling and simulation, however, one or both of these issues are often overlooked depending whether the cavity is being looked at from a high-power or a LLRF perspective. These drawbacks are resolved in this chapter by calculating the cavity transfer function using the Laplace notation and taking into account the effect of the input coupler on the cavity impedance.

Considering this model, the following two conditions will be required for making sure that all the forward power enters the cavity without beam: 1) the turn ratio of the transformer should be chosen so that it matches the cavity shunt impedance to Z_0 (i.e. coupling factor equal to one) and 2) the cavity resonant frequency should be equal to the RF frequency (i.e. detuning equal to zero). Any coupling factor and detuning other than these, will then cause part of the amplifier power to reflect from the cavity. Moreover, in the transient simulations

it can be seen that changing the coupling factor and detuning can degrade the cavity transient response due to voltage overshoots and oscillations. These issues have been discussed in detail in the current chapter both analytically and by computer simulations. In the continuation, the cavity model is modified so that it also represents the beam loading effect. This is done by adding another current source, representing the beam, to the cavity model and applying the superposition theorem to calculate the total cavity voltage due to the amplifier and the beam. As the previous values of the coupling factor and detuning only result in zero reflected power under no-beam conditions, new values for these parameters are calculated to suppress the reflected power for a certain beam current and phase. The results are then verified by computer simulations and a few examples using the ALBA RF parameters. The developed model will be used in the following chapters of the current thesis for closed-loop simulations of the ALBA RF cavity and the ESS-B RFQ.

Chapter 3

ALLRF System for the ALBA Booster

3.1 Design and Simulation of a LLRF System for Cavity Field Regulation

The task of the LLRF system of an RF plant is to regulate the voltage (amplitude and phase) and the resonant frequency of the cavity[1]. For this purpose three regulation loops are traditionally used being the so-called Amplitude Loop, Phase Loop and Tuning Loop. In multi-cell cavities a Field-flatness Loop may also be adopted to equalize the magnitude of the cavity voltage in all the cells. As it was mentioned earlier, cavity field regulation can be done by the amplitude and phase loops or alternatively, by I/Q loops. The second approach, however, is more appropriate for a modern LLRF system due to different reasons: With the IQ approach, the design of the I and Q loops will be the same making its implementation easier in comparison to the amplitude and phase loops which are different in design. Furthermore, the IQ approach provides a full control range of 0° to 360° while with the traditional phase loops the control range can not be larger than 180°. In addition to these, recent advances in RF/Microwave electronics has made it possible to make low-cost and compact IQ-based LLRF systems with much better performance compared to the traditional ones. For these reasons, it was decided to use an IQ-based LLRF system for ALBA. In this chapter, first, the design of the ALBA ALLRF system for amplitude/phase regulation will be presented. In the next sections, the function of the main building blocks comprising the regulation loops will be discussed in detail and

[1] Although this is usually defined as the task of a LLRF system, a complete LLRF is not only limited to these regulations loop. In practice, a LLRF system also includes RF diagnostics, fast and slow interlocks, hardware for data communication between the global control system and the low level electronics and also some measurement equipments. In this thesis, though, we only limit ourselves to the regulation/control aspect of LLRF systems as discussing the other parts will be out of the scope of this work.

Table 3.1: Specifications of the ALBA storage ring RF system

Parameter	Value	Unit
RF Frequency	499.654	MHz
No. of cavities	6	
Shunt impedance	3.5	MΩ
Unloaded quality factor	29000	
RF power (per cavity)	150	kW
RF voltage (per cavity)	600	kV
Beam current	400	mA
Over-voltage factor	2.8	
Synchroneous phase	159	°
Tuning range	2	MHz
Waveguide cutoff freq.	615	MHz

Table 3.2: Specifications of the ALBA booster RF system

Parameter	Value	Unit
RF Frequency	499.654	MHz
Repetition frequency	3	Hz
No. of cavities	1	
Shunt impedance	14	MΩ
RF power (at 3 GeV)	40	kW
RF voltage (at 3 GeV)	1	MV
Beam current	2	mA
Beam power (at 3 GeV)	1.3	kW
Over-voltage factor	2.8	
Synchroneous phase	159	°
Tuning range	2	MHz

simulations results verifying the design of the loops will be shown followed by the design of the ALBA tuning and field-flatness loops. Finally, the implementation of the ALLRF system and the experimental results obtained with it at CELLS and ELETTRA lab. will be discussed in detail.

3.1.1 The ALBA RF/LLRF specifications

The specifications of the RF systems for the ALBA storage-ring and booster are shown in TABLE 3.1[2] and TABLE 3.2 respectively [26, 27].

The ALBA storage ring RF system consists of 6 modified EU[3] type cavities manufactured by *ACCEL* with a peak power of 150 kW per cavity. The power for each cavity is generated by two TH793-1 IOTs from *Thales Electron Devices* and

[2]Over-voltage factor is defined as the ratio of the peak cavity voltage to the voltage seen by the particle bunch (i.e. the voltage corresponding to the Synchronous Phase).

[3]European Union

Table 3.3: Specifications of the phase loop

Stability	±1	°
Bandwidth	>200	kHz
No. of bits	16	bits
DAC throughput	100	kS/s
Loop delay	<1000	ns
Phase control range	0 to 360	°

Table 3.4: Specifications of the amplitude loop

Stability	±1	%
Bandwidth	>200	kHz
No. of bits	16	bits
DAC throughput	100	kS/s
Loop delay	<1000	ns
Dynamic range	>23	dB

Table 3.5: Specifications of the tuning loop

Bandwidth	100 app.	Hz
Tuning range	2	MHz
Tuning resolution	100 to 1000	Hz

a 38 kV, 4 A HVPS from *Thomson Broadcast and Multimedia*. The waveguide pieces are mainly purchased from *MEGA Industries*.

The ALBA booster consists of a 5-cell *PETRA* type cavity, also made by *ACCEL*, supplied by an IOT and a HVPS similar to those for the storage ring.

TABLE 3.3 to TABLE 3.5 presents the specifications of the ALBA LLRF system (the booster and storage ring LLRF specifications are the same).

3.1.2 IQ approach for cavity field regulation

FIG. 3.1 shows the simplified schematics of the ALBA booster ALLRF for amplitude and phase regulation.

For cavity field regulation, the probe voltage in the cavity central cell (3rd cell) is first decomposed into in-phase (I) and quadrature (Q) components and then converted from differential into single-ended by an IQ demodulator board. The cavity I and Q components are then compared to their set values and the resultant I and Q errors are fed into two PIDs regulating the I and Q, hence the amplitude and the phase of the cavity voltage. The outputs of the two PIDs are, in the next stage, multiplied by an adjustable gain and added to the feed-forward set values before being fed into the baseband phase shifter. The phase shifter makes a controlled rotation of the IQ vector so that it compensates for the fractional part of the loop delay, hence prevent the loops from becoming unstable. The I and Q outputs of the phase shifter are then converted from single-ended to differential and modulated by a quadrature modulator board. The output of the modulator, after being pre-amplified, serves as the input of

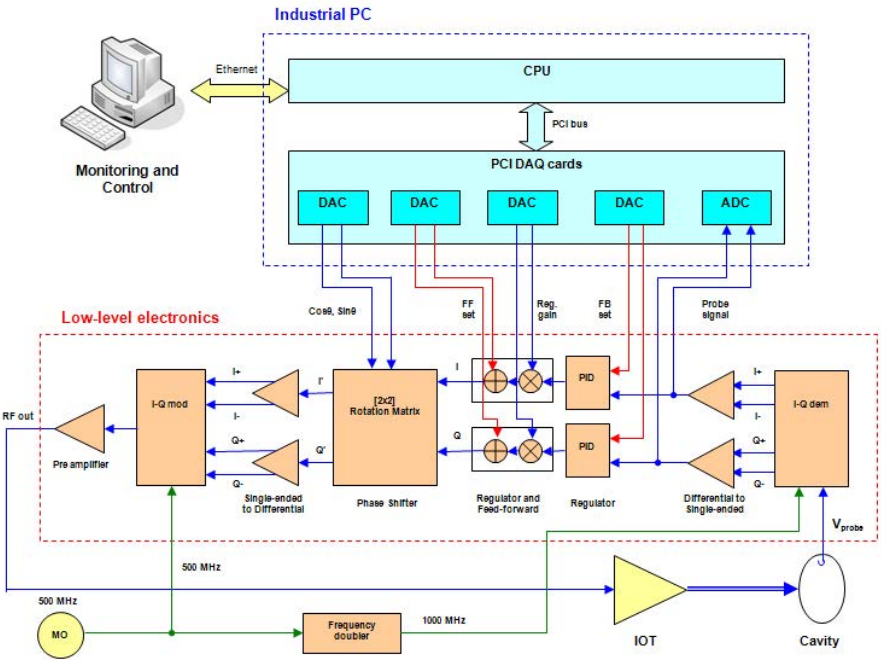

Figure 3.1: Layout of the IQ-based amplitude and phase loops (ALBA booster)

the solid-state amplifier driving the IOT.

By choosing proper reference values for the I/Q loops (i.e. *IFB* and *QFB*) the operator will be able to control the amplitude of the cavity voltage from nearly zero to a maximum defined by the IOT power rating and the phase from 0° to 360° thus providing full control over the amplitude and phase of the cavity voltage.

The reason for the *IFF* and *QFF* inputs is two-folded: first, it can be used as a function generator when the system is operated in open-loop; in this case, the *I/Q Reg. gains* are set to 0 V to open the loops, so that the IOT is driven only by the *IFF* and *QFF* inputs. Secondly, it can be used to compensate predictable errors such as the beam before these errors are sensed and compensated by the I/Q loops.

By setting proper values for the phase shifter inputs (which are marked as $Sin\theta$ and $Cos\theta$) the operator can provide an adjustable phase shift from 0° to 360° and an adjustable gain from 0 to 1.4[4]. Then, the operator should choose proper $Sin\theta$ and $Cos\theta$ values to have both loops stable with the largest possible phase margin. This is done by first finding upper and lower stability thresholds for the phase shift and then setting the phase shift to the middle point. This

[4]The phase shift of the phase shifter should not be confused with the one which is due to the setting of *IFB* and *QFB*. The purpose of the first phase shift is just to make the IQ loops stable while the second one is the controlled phase of the cavity voltage.

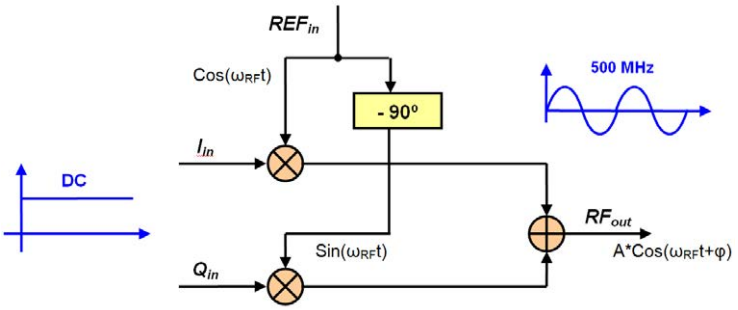

Figure 3.2: Simplified block diagram of an IQ modulator

ensures stable operation of the I/Q loops in addition to providing the largest loop stability margin. After finding the optimum phase shift value, the phase shifter adjustment should be kept the same unless there is a change in the loop delay (ex: a cable is changed) which implies finding a new set value for the phase shift. The scale factor of the phase shifter can also be used as an alternative way to control the loop gain in addition to the *Reg. gain* inputs.

In the following sections the function of each of these blocks will be explained in detail.

3.1.3 IQ modulator

An IQ modulator can be considered as a two-dimensional AM[5] modulator. While in AM the communication information is stored in the amplitude variations of the modulated signal, in IQ data transmission, information is stored in the amplitude variations of the inphase and quadrature components of the modulated signal. As the inphase and quadrature components are 90° out of phase with respect to one another, one can use them as two independent channels to transmit data on the same RF carrier. Therefore an IQ-modulated signal can carry more information compared to an AM-modulated signal, but the compromise is that for IQ modulation/demodulation a reference RF with the same frequency as the RF signal will be needed while this is not the case for AM modulation/demodulation.

FIG. 3.2 shows the block diagram of an IQ modulator:

The amplitude and phase of the modulated output (RF_{out}) is related to the I_{in} and Q_{in} inputs as the following:

$$|RF_{out}| = \sqrt{{I_{in}}^2 + {Q_{in}}^2}, \qquad \angle RF_{out} = arctan2(I_{in}, Q_{in}) \tag{3.1}$$

Where $arctan2$ means 4-quadrant tangent inverse (i.e. it can change between 0° and 360°).

[5] Amplitude Modulation

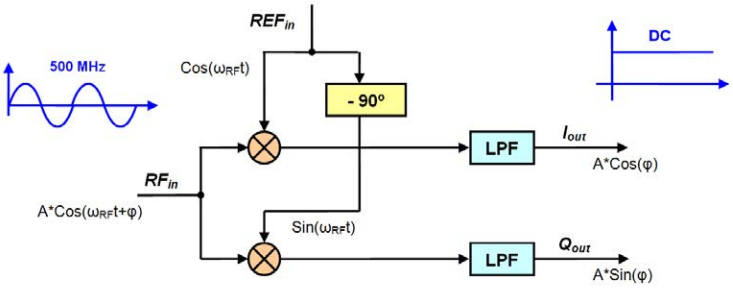

Figure 3.3: Simplified block diagram of an IQ demodulator

3.1.4 IQ demodulator

FIG. 3.3 shows the block diagram of an IQ demodulator.

RF_{in} in this figure is the RF input to be demodulated, REF_{in} is the reference input whose frequency is assumed to be the same as the RF_{in} and I_{out} / Q_{out} are the baseband outputs. As the figure shows, the RF_{in} is once mixed with REF_{in} and another time with 90° phase-shifted REF_{in}. The output of each mixer mainly has two frequency components: one at twice the RF frequency and the other at baseband. The outputs of the mixers, after being low-pass filtered to remove their unwanted frequency contents (i.e. the one with twice the RF frequency and its higher harmonics), give the inphase and quadrature components of the RF_{in}.

Note that if the frequency of RF_{in} is not exactly the same as REF_{in}, the I_{out} and Q_{out} signals will oscillate with the difference frequency between RF_{in} and REF_{in}.

3.1.5 PID regulator

As it is well-known in control theory, a PID consists of a gain, an integrator and a differentiator as shown schematically in FIG. 3.4.

Assuming that the gains of the proportional, integral and derivative parts are K_p, K_i and K_d respectively, the transfer function of the ideal PID will be as the following:

$$C(s) = K_p + \frac{K_i}{s} + K_d.s = \frac{K_d.s^2 + K_p.s + K_i}{s} \tag{3.2}$$

As it is shown in FIG. 3.1 two PIDs are used to regulate the inphase and quadrature components of the cavity voltage. The proportional and integral gains are adjusted so that the two loops give the desired response. The derivative part can also be used to slightly improve the response of the loops in case of ramping RF such as in the booster synchrotron.

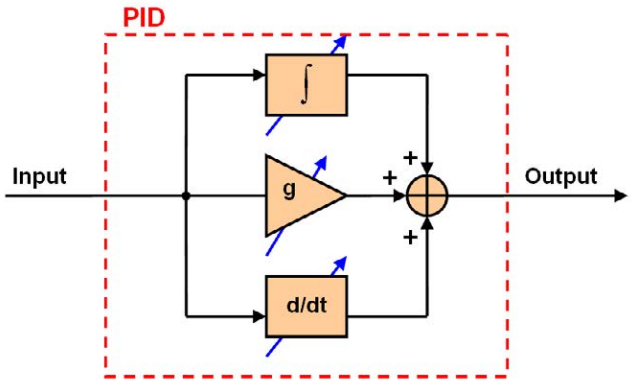

Figure 3.4: Block diagram of an ideal PID controller / regulator

3.1.6 Baseband phase-shifter

The base-band phase shifter makes a controlled rotation of the IQ vector before the I and Q signals are fed into the modulator. The additional phase shift, which is provided by the phase shifter, compensates for the fractional part of the loop delay, hence prevents the loops from becoming unstable. For example if the total I/Q loop delay is 346.3 times the RF period, the phase shifter should be set to provide a phase shift equivalent to -0.3 periods (i.e. $-108°$). The loop will then experience an effective delay of 346 periods and the two PIDs see the IQ vector with correct phase. Note that if the phase shifter is not properly adjusted, the transient I and Q signals will be disturbed due to the fractional part of the delay. This will prevent the PIDs from functioning properly. For example an uncompensated delay of 180° would be equivalent to a positive feedback making the loop unstable.

The phase shifter is basically a rotation matrix represented by EQ. 3.3:

$$\begin{bmatrix} I_{out} \\ Q_{out} \end{bmatrix} = \begin{bmatrix} Cos\theta & -Sin\theta \\ Sin\theta & Cos\theta \end{bmatrix} \times \begin{bmatrix} I_{in} \\ Q_{in} \end{bmatrix} \tag{3.3}$$

FIG. 3.5 shows the phasor representation of the phase shifter with A_{in} being the input IQ phasor, A_{out} the output phasor and θ the phase shift.

At ALBA the baseband phase shifter was implemented using four multipliers and two adders as it is shown schematically in FIG. 3.6.

It should be noted that $Sin\theta$ and $Cos\theta$ in FIG. 3.6 are just nicknames for these two inputs. Practically, these signals can have any value as long as they are within the dynamic range of the ICs. This means that in practice the phase shifter board not only provides a controlled phase shift, but also a controlled gain. For example with $Sin\theta = -1.2\ V$ and $Cos\theta = 0.4\ V$ the phase shifter board generates a phase shift of $-71.5°$ and an amplification factor of 1.26 (here, we assume that 1 V corresponds to an amplification factor of 1).

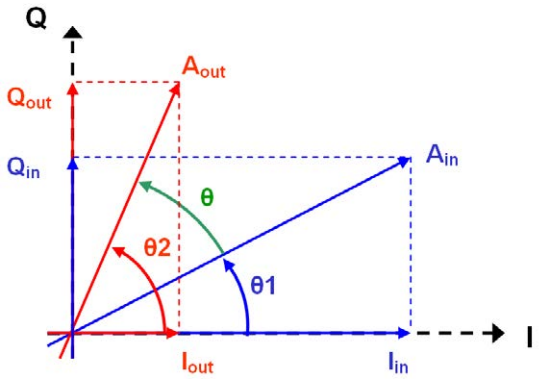

Figure 3.5: Phasor representation of the baseband phase-shifter

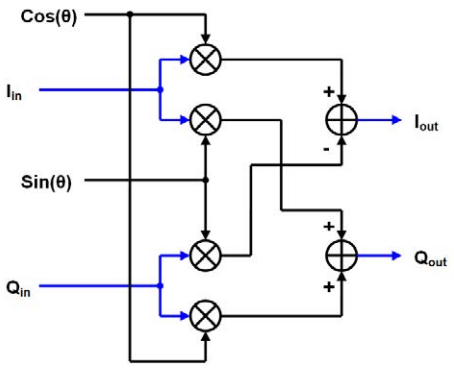

Figure 3.6: Block diagram of the baseband phase-shifter

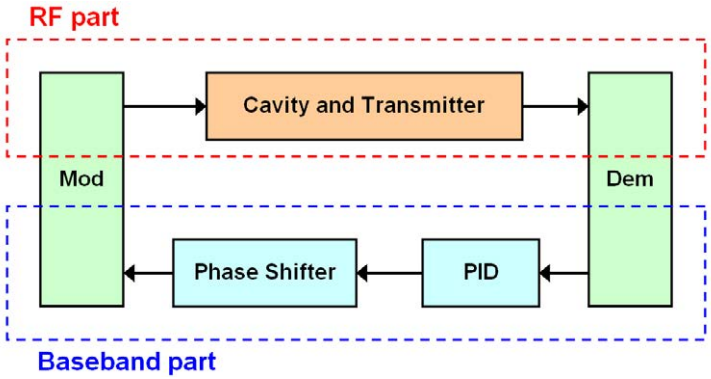

Figure 3.7: Block diagram of the IQ loops highlighting the RF and baseband parts

3.1.7 Simulation of the IQ loops in Simulink

In this subsection, we validate the control system which was presented in the previous sections by MATLAB/Simulink simulations. It should be noted, however, that as the complete loop consists of an RF part (i.e. the cavity and the transmitter) and a baseband part (i.e. the LLRF), a conventional simulation would be very slow. This is linked to the fact that the RF part has very fast variations with time due to the RF frequency, but the variations of the baseband signals is rather slow due to the high quality factor of the cavity. Therefore, for the RF part a very short sample time would be needed while this will be too conservative for the baseband signals which we are mainly interested in. Here, we introduce and use a mathematical method which significantly increases the simulation speed and at the same time provides almost the same precision as the one with the conventional model.

Baseband-equivalent model of the RF cavity

FIG. 3.7 shows the block diagram of the IQ loop highlighting the RF and baseband parts.

With a baseband-equivalent model, the frequency response of the cavity is mapped from RF to baseband. Therefore, the cavity model can be placed in cascade with the low-level part. As in this case, no RF component exists in the loop anymore, a much larger time step can be chosen for the simulations; hence the simulation time and the computational load will be significantly reduced. With the baseband-equivalent model of the cavity, the block diagram of the loop will be simplified as shown in FIG. 3.8.

In order to derive the mathematical model of the baseband equivalent cavity, we recall EQ. 2.36:

$$\acute{V}_{total}(s) = \left(2\acute{I}_{amp}(s) - \acute{I}_{beam}(s)\right) \frac{\beta Z_0 L.s}{RLC.s^2 + L(\beta+1).s + R}$$

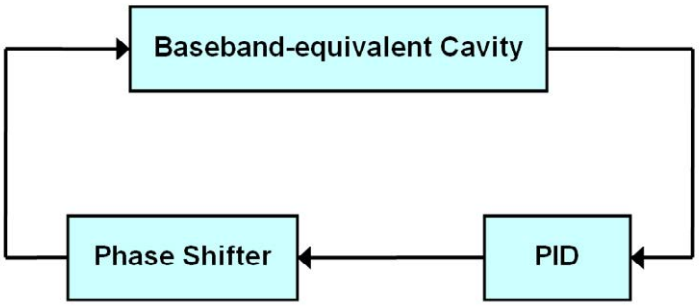

Figure 3.8: Block diagram of the baseband-equivalent loop

This equation can be rewritten as the following in terms of Q_0 and ω_0:

$$\acute{V}_{total}(s) = \left(2\acute{I}_{amp}(s) - \acute{I}_{beam}(s)\right) \frac{\frac{\beta Z_0 \omega_0}{Q_0}.s}{s^2 + \frac{(\beta+1)\omega_0}{Q_0}.s + {\omega_0}^2} \tag{3.4}$$

With total cavity current defined as:

$$\acute{I}_{total}(s) = 2\acute{I}_{amp}(s) - \acute{I}_{beam}(s) \tag{3.5}$$

and after replacing 's' with $\frac{d}{dt}$, EQ. 3.4 will be equivalent to the following differential equation:

$$\frac{d^2\acute{V}_{total}(t)}{dt^2} + \frac{(\beta+1)\omega_0}{Q_0}\frac{d\acute{V}_{total}(t)}{dt} + {\omega_0}^2\acute{V}_{total}(t) = \frac{\beta Z_0 \omega_0}{Q_0}\frac{d\acute{I}_{total}(t)}{dt} \tag{3.6}$$

We define the cavity voltage and current as [11]:

$$\begin{aligned} \acute{V}_{total}(t) &= \left[\acute{V}_r(t) + j\acute{V}_i(t)\right].e^{j\omega_{RF}t} \\ \acute{I}_{total}(t) &= \left[\acute{I}_r(t) + j\acute{I}_i(t)\right].e^{j\omega_{RF}t} \end{aligned} \tag{3.7}$$

Where $\acute{V}_r(t)$ and $\acute{V}_i(t)$ are the real (inphase) and imaginary (quadrature-phase) components of the relevant variable in baseband and ω_{RF} is the operating frequency.

From equations EQ. 3.6 and EQ. 3.7 we will have:

$$\begin{aligned} &\frac{d^2\left[(\acute{V}_r + j\acute{V}_i).e^{j\omega_{RF}t}\right]}{dt^2} + \frac{(\beta+1)\omega_0}{Q_0}\frac{d\left[(\acute{V}_r + j\acute{V}_i).e^{j\omega_{RF}t}\right]}{dt} \\ + \quad &{\omega_0}^2(\acute{V}_r + j\acute{V}_i).e^{j\omega_{RF}t} = \frac{\beta Z_0 \omega_0}{Q_0}\frac{d\left[(\acute{I}_r + j\acute{I}_i).e^{j\omega_{RF}t}\right]}{dt} \end{aligned} \tag{3.8}$$

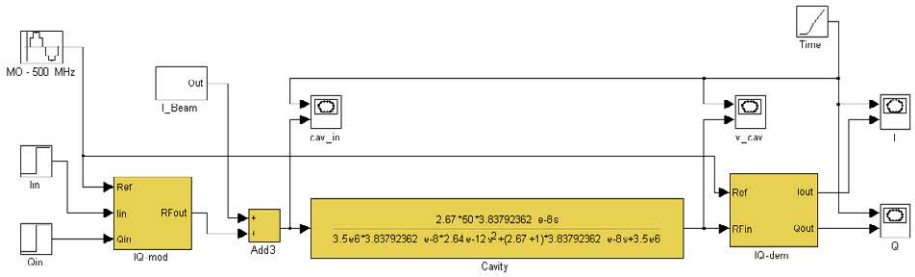

Figure 3.9: Conventional model of the cavity and the IQ modulator/demodulator

Taking into account that the variations of $\acute{V}_r(t)$ and $\acute{V}_i(t)$ is much slower that the RF frequency (i.e. $\frac{d\acute{V}_r}{dt} << \acute{V}_r\omega_{RF}$) and ignoring the negligible terms, the following two equations will result from equating the real and imaginary parts on both sides of EQ. 3.8:

$$\begin{aligned} 2Q_0\frac{d\acute{V}_r}{dt} + (\beta+1)\frac{d\acute{V}_i}{dt} + (\beta+1)\omega_{RF}\acute{V}_i + 2Q_0(\omega_0-\omega_{RF})\acute{V}_i = \beta Z_0\omega_{RF}\acute{I}_r \\ 2Q_0\frac{d\acute{V}_i}{dt} + (\beta+1)\frac{d\acute{V}_r}{dt} + (\beta+1)\omega_{RF}\acute{V}_r - 2Q_0(\omega_0-\omega_{RF})\acute{V}_r = \beta Z_0\omega_{RF}\acute{I}_i \end{aligned} \quad (3.9)$$

EQ. 3.9 can be rewritten in the frequency domain as the following:

$$\begin{aligned} \acute{V}_r(s) = \acute{I}_r(s)\frac{\beta Z_0\omega_{RF}}{2Q_0.s+(\beta+1)\omega_{RF}} - \acute{V}_i(s)\frac{(\beta+1).s+2Q_0(\omega_0-\omega_{RF})}{2Q_0.s+(\beta+1)\omega_{RF}} \\ \acute{V}_i(s) = \acute{I}_i(s)\frac{\beta Z_0\omega_{RF}}{2Q_0.s+(\beta+1)\omega_{RF}} + \acute{V}_r(s)\frac{(\beta+1).s+2Q_0(\omega_0-\omega_{RF})}{2Q_0.s+(\beta+1)\omega_{RF}} \end{aligned} \quad (3.10)$$

EQ. 3.10 define the baseband-equivalent cavity model.

In order to verify these results, the response of the conventional cavity model was compared to the baseband-equivalent model in Simulink. FIG. 3.9 to FIG. 3.13 show both Simulink models and the results of the simulations for $\beta = 2.67$ and $f - f_0 = -37.5\ kHz$.

As one can see in FIG. 3.13 the simulation results from the two models are almost identical. It should be noted, however, that the computational load for the baseband-equivalent model was much less than that of the conventional model in these simulations. The evidence for the reduction of simulation time can be given as the following: by comparing the RF model (EQ. 2.36) to the baseband-equivalent model (EQ. 3.10) one can understand that in terms of model complexity these two models are somewhat comparable as both represent a second-order system, but the simulation time of the baseband-equivalent model will be much shorter due to the choice of the time step. With $f = 500\ MHz$ and considering

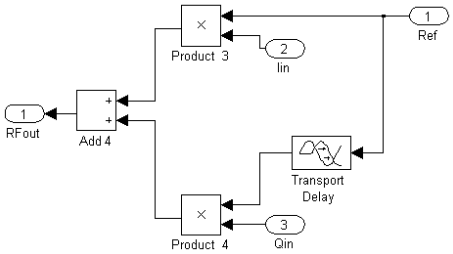

Figure 3.10: Detailed model of the IQ modulator

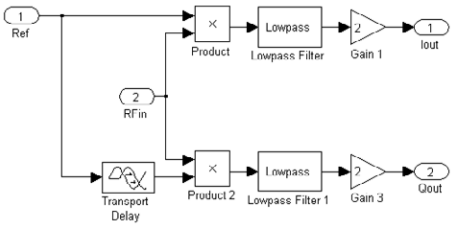

Figure 3.11: Detailed model of the IQ demodulator

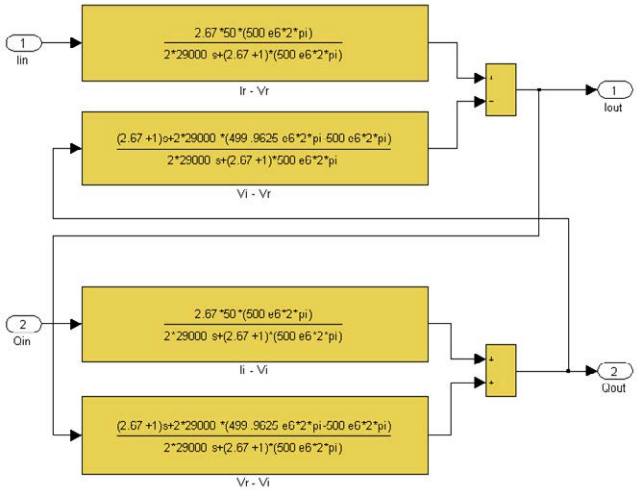

Figure 3.12: Baseband-equivalent model of the cavity

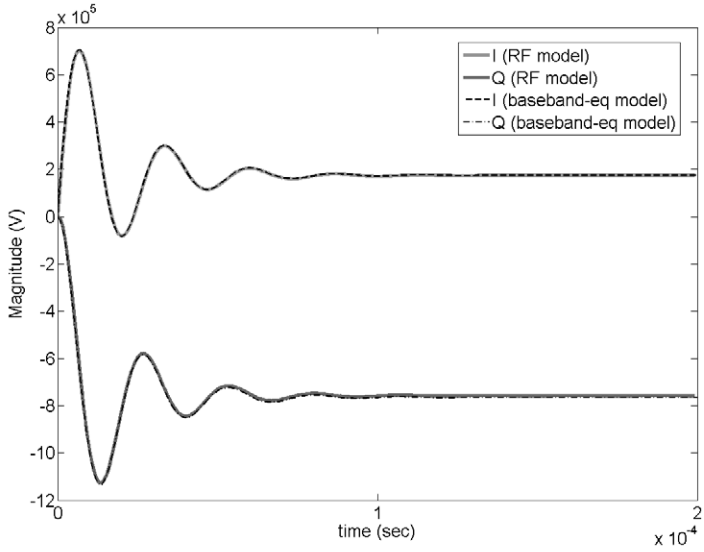

Figure 3.13: Comparison between the simulation results of the conventional cavity model and the baseband-equivalent model shown in FIG. 3.9 to FIG. 3.12

10 samples per period[6] one needs a time step equal to 200 ps for the RF model. For the baseband-equivalent model, on the other hand, one can choose a much larger time step. Taking into account that the settling time of the baseband signals is in the order of $20 - 50$ μs, a time step of 200 ns would be small enough to see the loop response. That already makes a difference of 1000.

Baseband-eq. simulation of the IQ loops

FIG. 3.14 shows the baseband-equivalent model of the IQ feedback loop.

Detailed model of the Baseband-eq. cavity is the one shown in FIG. 3.12. FIG. 3.15 shows the detailed model of the Phase Shifter.

In the simulations, the gain of the amplifier supplying the cavity (including the amplifier transconductance due to voltage-to-current inversion) was assumed to be 50, the attenuation factor of the pickup loop (for cavity voltage measurement) was set to 2e-4 and the loop delay was set to 500 times the RF period[7]. Then the phase shifter was set for 0° phase shift and the gains of the PI regulators were adjusted by trial and error to have a satisfactory response. With the parameters mentioned above and assuming a 50 Ω system, the inputs $I_{ref} = 0.266\ V$ and $Q_{ref} = 0.692\ V$ will result in the required cavity voltage

[6]With very few samples the amplitude and phase of the RF signals cannot be regenerated properly.

[7]These values are approximately the same as the real ones corresponding to the ALBA RF plant according to the RF experiments.

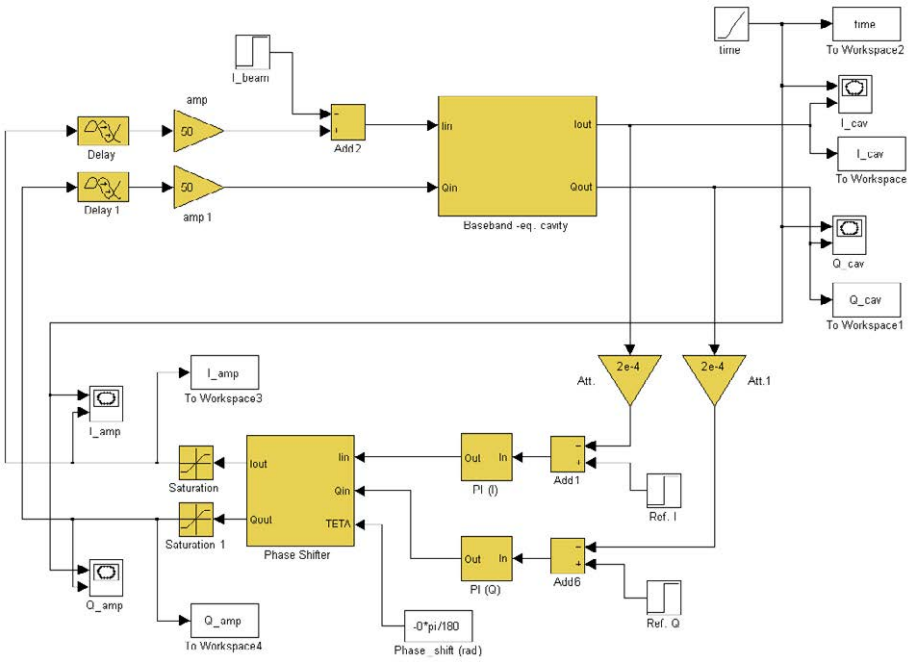

Figure 3.14: Simulink model of the complete IQ loop with baseband-equivalent cavity model

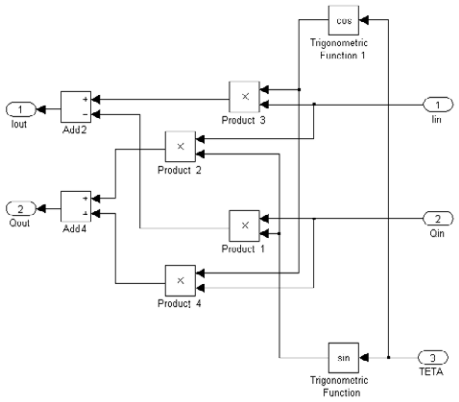

Figure 3.15: Detailed model of the baseband phase shifter

($\acute{V}_{total} = 3705\ \angle 69°$). The beam ($I_{DC} = 400\ mA$) was assumed to arrive at $t = 100\ \mu s$. FIG. 3.16 shows the results of the simulations with $\beta = 2.67$ and $f - f_0 = 37.5\ kHz$.

FIG. 3.16 (bottom) compares the phase of the total cavity voltage to the one of the amplifier current. As it can be seen, after the beam arrival, the phase of the amplifier current settles at the same value as the phase of the cavity voltage. This is due to the right choice of the cavity coupling factor and detuning corresponding to the magnitude and the phase of the beam. In this condition, the steady state reflected voltage from the cavity will be zero because the cavity behaves like a resistive load for the amplifier.

Simulation results with a DC error in the reference phase of the phase shifter are shown in FIG. 3.17.

Similarly, FIG. 3.18 shows the effect of the loop delay on the cavity voltage.

These two graphs show that increasing the loop delay changes the transient response in two different ways. If the delay is increased by integer multiples of the RF period, the loop response will degrade in the same way as in a conventional feedback loop. For example, when the loop delay is 500 RF periods, the transient response is slightly degraded compared to the ideal case with zero delay as shown in FIG. 3.18. By increasing the delay to 1000 RF periods, some oscillations appear on the transient response. If the delay is further increased, larger oscillations show up on the signals until the loop finally becomes unstable. In order to avoid such signal degradations, the delay of the ALLRF feedback loop should be less than 1000 ns[8]. This is done mainly by using short RF cables and fast electronics.

On the other hand, changing the fractional part of the loop delay has a much more severe effect on the loop response. In that respect it can be mentioned that increasing the loop delay from 500 RF periods to 501 RF periods will have a negligible effect on the transient response but changing it to 500.5 RF periods (without compensating it by the phase shifter) will change the negative feedback to positive, hence makes the loop unstable.

Assuming a fixed loop delay, by changing the amount of the phase shift from 0° to 360°, the feedback loop will only be stable in a certain phase range defined by two phase thresholds as demonstrated in FIG. 3.19. The position of this phase range in the 0° - 360° plane depends on the fractional part of the loop delay and its width on the phase margin of the feedback loop[9]. For optimum performance, the phase shifter should be adjusted to be in the middle of the two thresholds as shown in FIG. 3.19. This, on one hand, makes the I and Q loops decoupled[10] and on the other hand gives best results in terms of loop stability and transient response.

[8] In the ALLRF design, the goal was to keep the total delay around 500 ns.

[9] By increasing the integer delay the width of the stable region will shrink.

[10] When decoupled, the I and Q loops function like two independent loops.

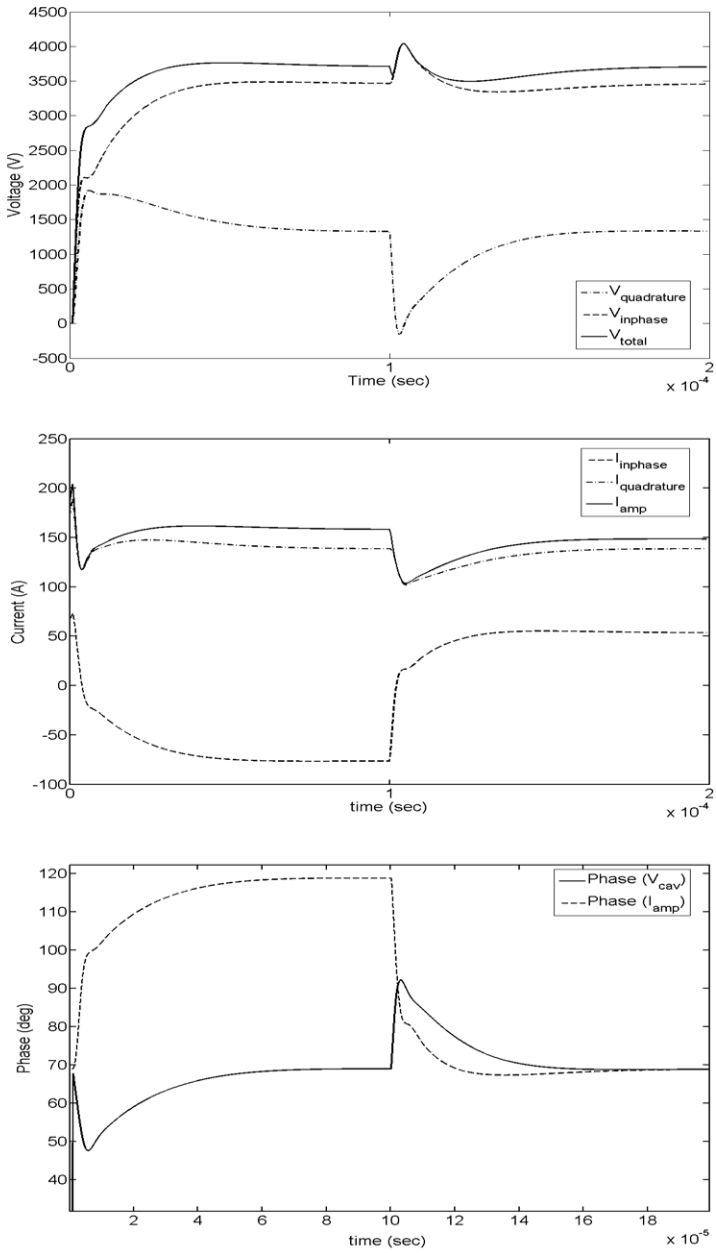

Figure 3.16: Closed-loop simulation of the baseband-equivalent cavity, RF amplifier and LLRF; Top - magnitude of the total cavity voltage together with its inphase and quadrature components; Middle - magnitude of the amplifier current together with its inphase and quadrature components; Bottom - Comparison between the phases of the cavity voltage and the amplifier current

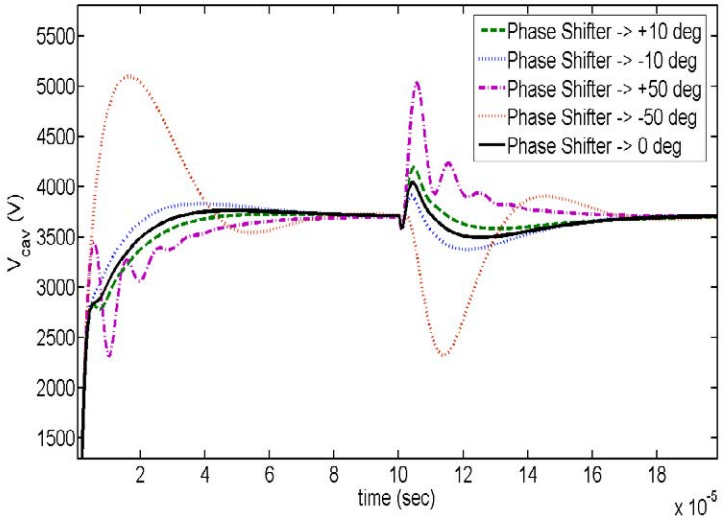

Figure 3.17: Influence of the phase shifter phase error on the transient cavity voltage. The phase error causes oscillations on the cavity voltage which can make the loop unstable if the error is too high.

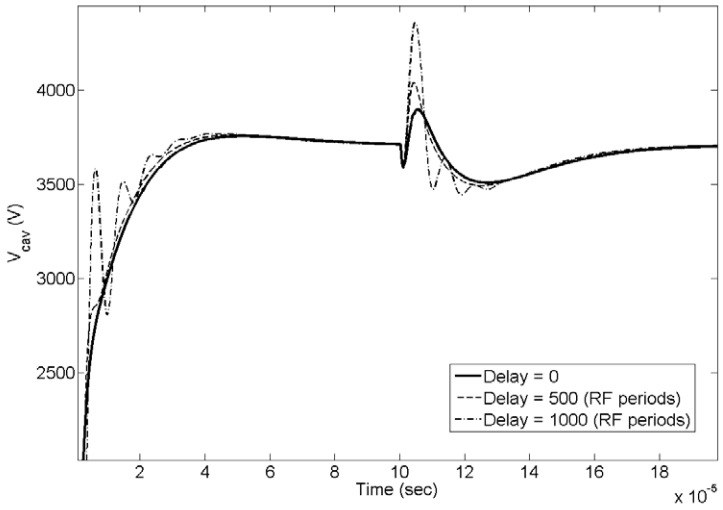

Figure 3.18: Influence of the loop delay on the transient cavity voltage. The figure shows that even with the phase shifter properly adjusted, large loop delays cause oscillations on the cavity voltage degrading the performance of the loops. In the extreme case the loop can even become unstable.

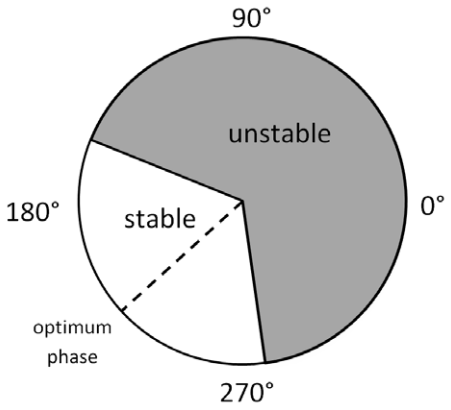

Figure 3.19: Demonstration of the stable phase range and the optimum phase

3.1.8 Design of IQ-based tuning and field-flatness loops

The tuning loop controls the resonant frequency of the cavity in order to have minimum reflected power with the presence of the beam and other disturbances such as temperature variations. For this purpose, the two tuners of the 5-cell ALBA cavity are driven in the same direction so that the phase difference between the forward voltage and the cavity probe voltage remains as close as possible to its reference value where the reference phase is the one which results in minimum reflected power from the cavity and provides stable Robinson operation[11].

A field-flatness loop can additionally be used to equalize the magnitude of the electric field in all the cells. In this case the two tuners are driven in opposite directions so that the difference of the voltage in the 2^{nd} and the 4^{th} cells remains as small as possible.

FIG. 3.20 shows the simplified schematics of the tuning and field-flatness loops of the ALBA booster.

As can be seen in the figure, the design of the ALBA tuning and field-flatness loops is also based on IQ demodulation. Four RF signals (i.e. V_{fwd}, V_{cell3}, V_{cell2} and V_{cell4}) are in this case demodulated by four IQ demodulator boards and sampled by some ADC cards hosted by an industrial PC[12]. The first two signals are used for tuning and the last two for field-flatness. The industrial PC calculates the phase difference between the forward and the 3^{rd} cell voltages as well as the normalized amplitude difference between the 2^{nd} and 4^{th} cells using EQ. 3.11.

[11] Robinson instability criterion puts two limits on the cavity detuning angle: the upper limit is zero and the lower limit is the one which results in an amplifier voltage inphase with the beam current. Detailed discussion of the Robinson instability is out of the scope of this work. Interested reader is referred to [109] or the original article by K.W. Robinson (1964)

[12] The V_{refl} is only demodulated for monitoring purposes.

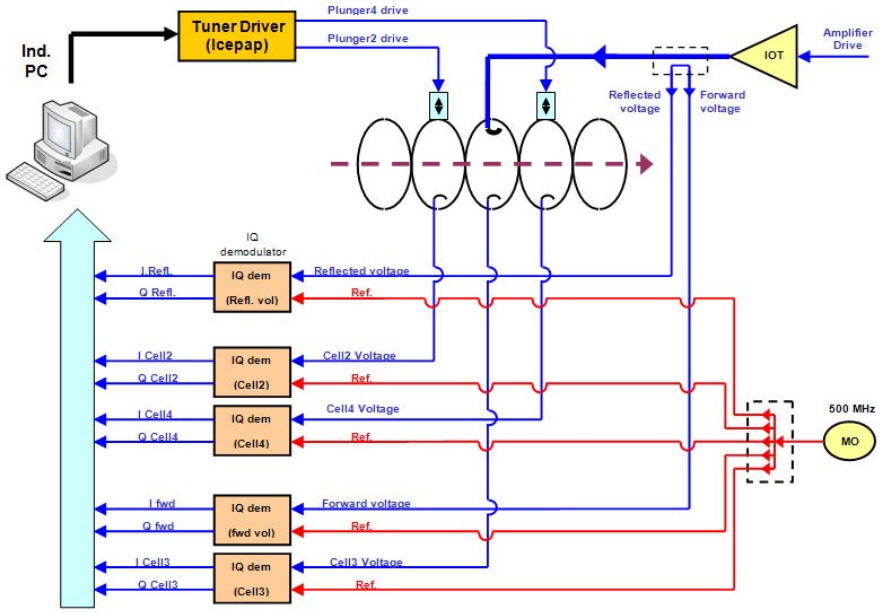

Figure 3.20: Layout of the IQ-based tuning and field-flatness loops (ALBA booster)

$$\begin{aligned} \Delta\theta(V_{fwd}, V_{cell3}) &= arctan2(I_{fwd}, Q_{fwd}) - arctan2(I_{cell3}, Q_{cell3}) \\ \Delta Amp(V_{cell2}, V_{cell4}) &= \frac{\sqrt{{I_{cell2}}^2 + {Q_{cell2}}^2} - \sqrt{{I_{cell4}}^2 + {Q_{cell4}}^2}}{\sqrt{{I_{cell2}}^2 + {Q_{cell2}}^2}} \end{aligned} \tag{3.11}$$

Depending on the $\Delta\theta(V_{fwd}, V_{cell3})$ and $\Delta Amp(V_{cell2}, V_{cell4})$ values, the industrial PC sends pulses to the Tuner Driver, moving the two tuners[13] in the right direction to have the $\Delta\theta$ as close as possible to its reference value and ΔAmp as close as possible to zero. This is done by defining two windows with $\pm$C1 and $\pm$C2 thresholds (C2 resides within C1) centred at the desired phase where the C1 window defines the acceptable range of the error and C2 the threshold that the error should be brought to when it exceeds the +C1/-C1 thresholds. This is illustrated in FIG. 3.21 for tuning.

If for example the phase error exceeds the tuning threshold $+C1$, the two tuners move in the right direction until the error becomes smaller than $-C2$ and

[13]The tuners used for the ALBA RF cavities are based on stepper motors moving a piston-like plunger in the cavity thus changing its resonant frequency. Each tuner is driven by a Tuner Driver. The Tuner Driver (Ice-PAP) on one hand provides the required current for the stepper-motor coils and on the other hand communicates the control and hand-shaking commands to the control computer.

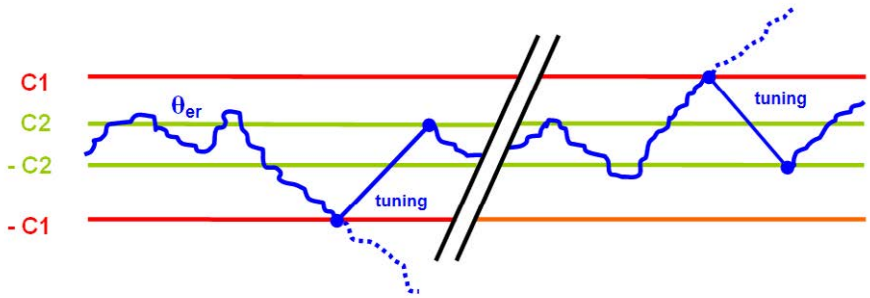

Figure 3.21: Tuning thresholds

then the tuners stay at that position until the next time that the error exceeds either $+C1$ or $-C1$ threshold.

The field-flatness is based on the same regulation principle. The only difference is that when one of the error thresholds ($+C1$ or $-C1$) is exceeded, the two tuners move in opposite directions until the amplitude error enters the acceptable range defined by $\pm$C2.

It should be noted that the error thresholds for the tuning and field-flatness are not necessarily equal. They should be chosen according to the requirements (typical values of C1 and C2 for ALBA are 2% and 1% respectively).

In the ALBA booster, tuning and field-flatness will be done one after another only at the peak of the ramping curve after the signals have settled as shown in FIG. 3.22[14].

After a change in the system status (ex. beam arrival), the two tuners will find their right positions in a few ramping cycles so that both tuning and field-flatness conditions are satisfied.

3.2 Implementation of the ALBA Booster LLRF

The implementation of the ALBA booster LLRF was done in-house. All the main building blocks of the IQ loops, the low-level hardware for RF diagnostics and some peripheral units were designed and built at CELLS[15]. The implementation of the booster ALLRF was a multistage procedure which started with the design and fabrication of the PCBs and continued with mounting components on the PCBs, mounting the PCBs inside metallic enclosures for noise protection, assembling the units, mounting the units into industrial racks and finally

[14]Enabling the loops during the whole ramping time would make the tuners move inward-outward continuously with a risk of equipment wear-out due to mechanical tensions. Having the tuning loop synchronized with the 3 Hz trigger of the booster, on the other hand, will only make the reflected power minimized when the RF power is at its peak level, but there will be some reflected power during the rest of the ramping period.

[15]The implementation of the fast and slow interlock system and the high-level controls is not explained here as it is out of the scope of this work.

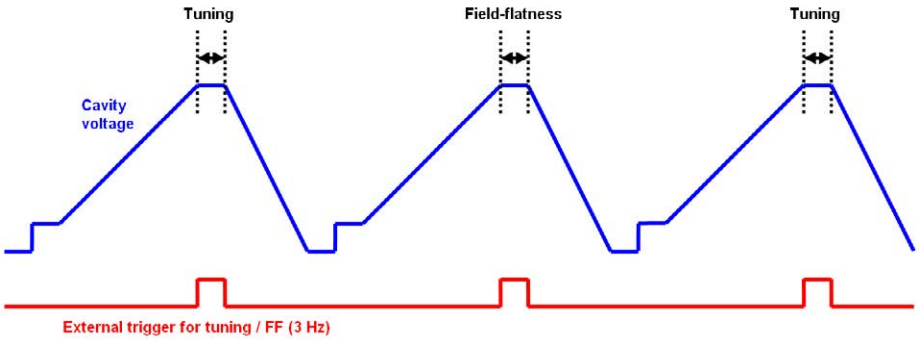

Figure 3.22: Synchronization of tuning and field flatness with the 3 Hz booster trigger

installing the electronics at the location of the RF transmitter. In this section we explain the design and implementation of the electronics for the feedback loops and RF diagnostics. We will also briefly discuss the peripheral units (ex. DC power supply and RF distribution) which were needed to complete the LLRF system. In the continuation, we discuss some practical issues such as grounding and noise protection. We will conclude the section by a short description of the Graphical User Interface (GUI).

3.2.1 The IQ demodulator

The IQ demodulator is the main building block of the ALBA ALLRF system. The total number of demodulators for one RF plant is 20 approximately, where 1 is used for the IQ loops, 4 for tuning and field-flatness, 10 for RF diagnostics and 5 as spares. As the IQ demodulator board includes both RF and baseband parts, several issues such as impedance matching, grounding, signal offset, group delay, bandwidth, dynamic range, noise, etc. had to be taken into account in the design and implementation of the boards.

FIG. 3.23 shows a picture of the IQ demodulator board.

The board is based on the AD8348 quadrature demodulator IC from Analog Devices [14]. The RF input signal is fed into the RF_{in} port (SMA connector). This port is matched to 50 Ω through a Micro-strip line. The level of the RF_{in} signal is typically 0 dBm and the absolute maximum is about 10 dBm. Close to the IC, the RF_{in} signal is converted to differential and its impedance is matched to 200 Ω (the input impedance of the RF_{in} pins) through a resistor network and then fed into the IC by a capacitive AC coupler. The reference RF, which must be at twice the RF frequency [14], is fed to the LO_{in} port which is also matched to 50 Ω by a Mirco-strip. This signal, after being converted from single-ended to differential by a Balun Transformer, is matched to the input impedance of the demodulator IC (50 Ω for this pin) and then fed into the IC through an AC coupler. The baseband I and Q outputs are available on the I_{out} and Q_{out}

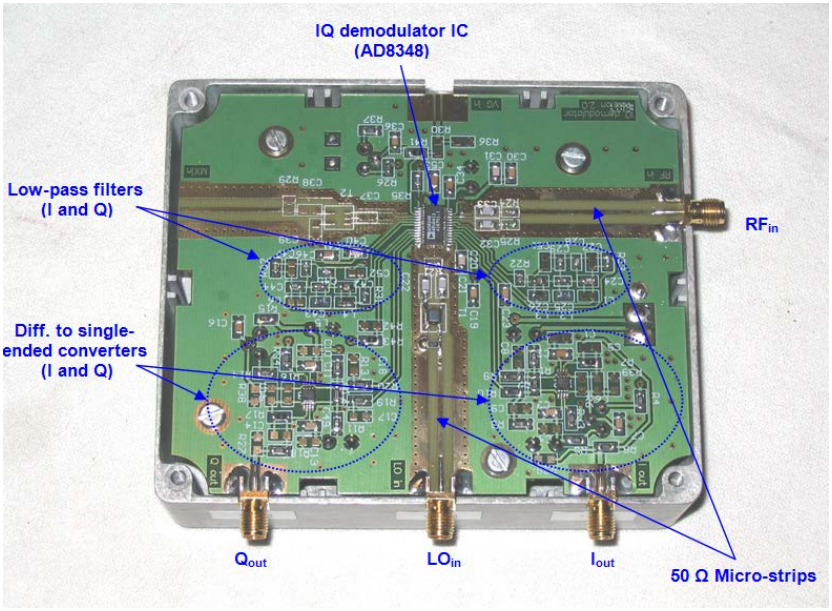

Figure 3.23: Picture of the IQ demodulator board

ports.

The PCB has been designed so that by some minor modifications it can also be used as a mixer. In this case, the missing components for the mixer input (top left of FIG. 3.23) must be mounted in their places. The board will then mix this signal with RF_{in} and the resultant inphase and quadrature components will be available on the I_{out} and Q_{out} ports.

It should be noted that although the Micro-strip lines were designed to provide a very good match to 50 Ω, practically, their impedance was slightly different due to manufacturing errors and board imperfections. The small error in these impedances was corrected later on by additional capacitors/resistors which were mounted on proper positions on the Micro-strip lines. The value and positions of these correcting elements were found by trial and error. FIG. 3.24 and FIG. 3.25 show the measured S_{11} and S_{22} parameters of the RF_{in} and LO_{in} ports before and after the impedance corrections (port 1 of the Network Analyzer was connected to the RF_{in} and port 2 to LO_{in}; therefore S_{11} and S_{22} show the reflection coefficient for these ports).

As it can be seen, the reflection coefficient went down from $-9.4\ dB$ to $-25.2\ dB$ (it was improved by $15.8\ dB$) for the RF_{in} port and from $-9.3\ dB$ to $-19.7\ dB$ ($10.4\ dB$ improvement) for the LO_{in} port. With the new S parameters, the reflected voltages at these RF ports are negligible.

The higher harmonics which are generated in the demodulation process are removed by two 4^{th} order elliptic low-pass filters with 20 MHz cutoff frequency and 20 ns of group delay approximately. These filters have been designed so

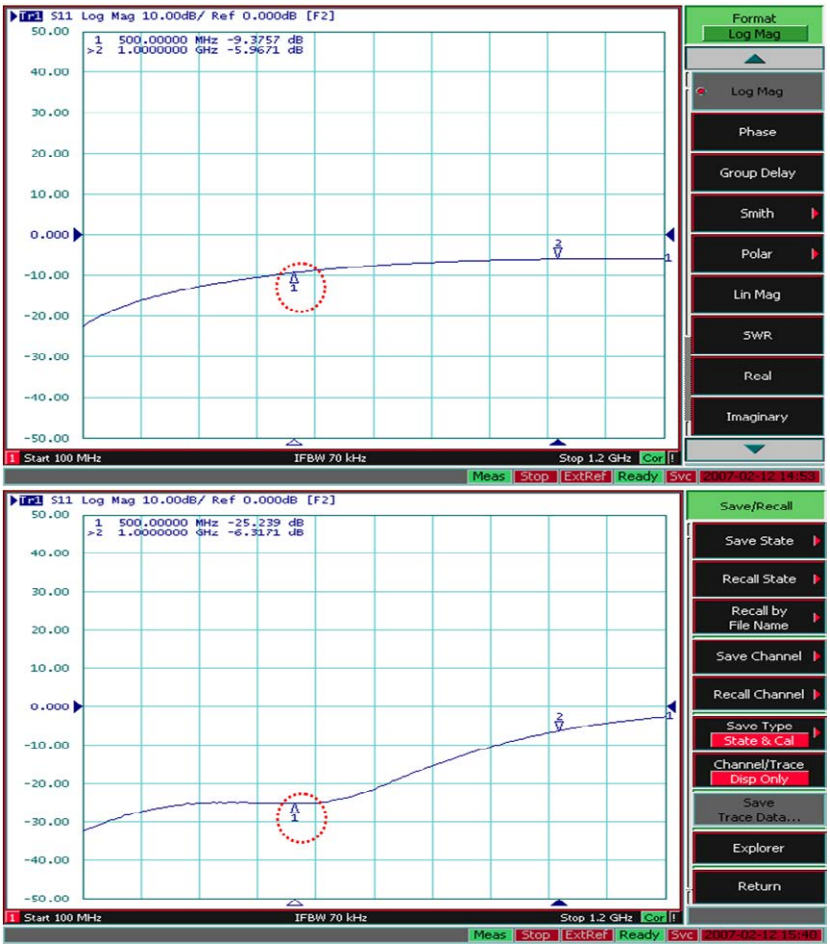

Figure 3.24: Measured S_{11} of the RF_{in} port (500 MHz); Top: before impedance matching; Bottom: 15 dB of S11 improvement after impedance matching

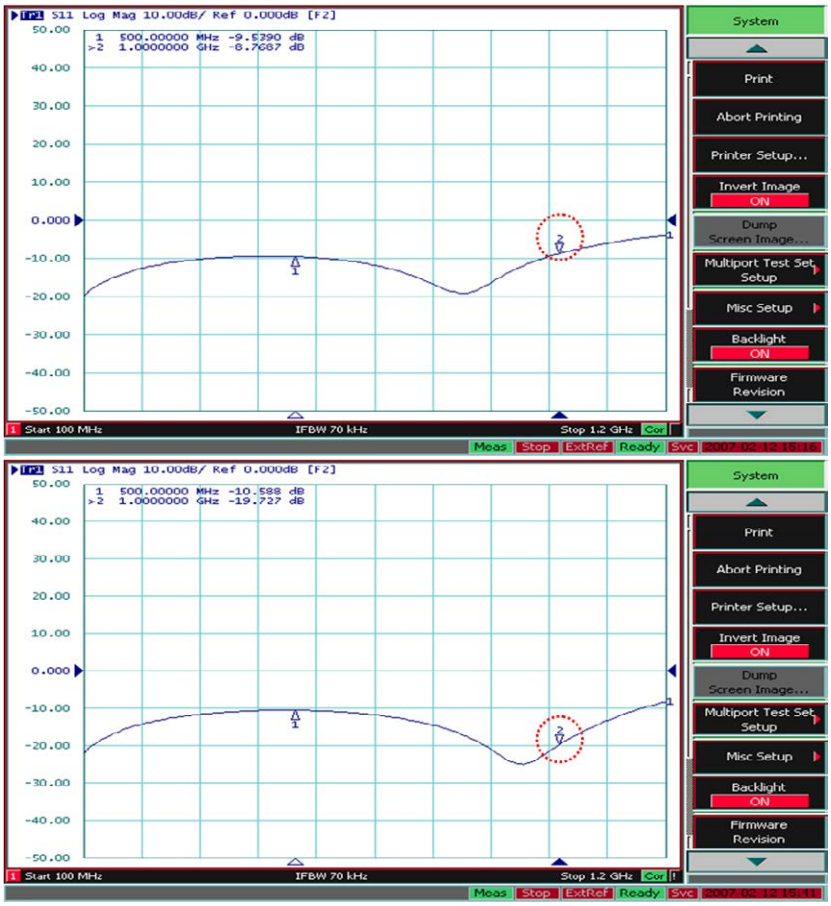

Figure 3.25: Measured S_{22} of the LO_{in} port (1000 MHz); Top: before impedance matching; Bottom: 11 dB of S22 improvement after impedance matching

that their input and output impedances are matched to the impedance of the corresponding pins of the IC. FIG. 3.26 shows the simulated response of these filters.

The I and Q outputs of the AD8348 are converted from differential to single-ended by two unity-gain Differential Receiver Amplifiers (AD8130 [15]) and then are sent to the I_{out} and Q_{out} ports. The voltage range for these outputs is $\pm 1.4\ V_{PP}$.

The gain of the IQ demodulator and the offsets of the baseband I/Q can be precisely adjusted by three potentiometers which are mounted on the other side of the metallic enclosure (not shown in the picture).

3.2.2 The IQ modulator

FIG. 3.27 shows a picture of the IQ modulator board.

On this board, two AD8132 ICs [16] convert the I_{in} and Q_{in} signals from single-ended to differential and an AD8345 [17] performs the IQ modulation. The AD8345 datasheet specifies a differential voltage range of 1.2 V_{PP} with a bias level of 0.7 V for the baseband inputs; this is also done by the two AD8132. The two RF ports (i.e. LO_{in} and RF_{out}) are matched to 50 Ω by Micro-strip lines. The LO_{in} input is converted from single-ended to differential by a Balun transformer and AC coupled to the modulator IC. Similar to the IQ demodulator board, the small errors in the impedances of the RF lines were removed by mounting capacitors/resistors on proper positions with one end soldered on the Micro-strip line and the other end on the nearest ground plane.

3.2.3 The PID

As the PID works in baseband, its requirements do not need to be very strict. Nevertheless, it is important to have very low offset on the comparator output (i.e. the error signal) as any DC error on this signal would shift the regulated I and Q signals by the same amount. This will be equivalent to a DC error in the amplitude and phase of the regulated cavity voltage. The comparator was implemented by an AD8130 and the PID itself by two dual op-amp AD8056 ICs [18] where the first AD8056 was used for the proportional and integral parts and the second one for the derivative part and sign inversion as can also be seen in FIG. 3.28.

The reference input is fed into the REF_{in} and the measured input to the $ACTUAL_{in}$ port. The board also sends these two signals to the Monitoring ports to be sampled by the DAQ cards for monitoring reasons. The output of the PID is accessible on the *Output* port. The $'P'$, $'I'$ and $'D'$ functions can be used individually or combined by putting jumpers in proper positions on the board. The $'P'$, $'I'$ and $'D'$ gains and the input offset are adjusted by the four potentiometers mounted on the board.

In order to test the performance of the PID, a simple loop was formed by directly connecting the PID output to its input. FIG. 3.29 and FIG. 3.30

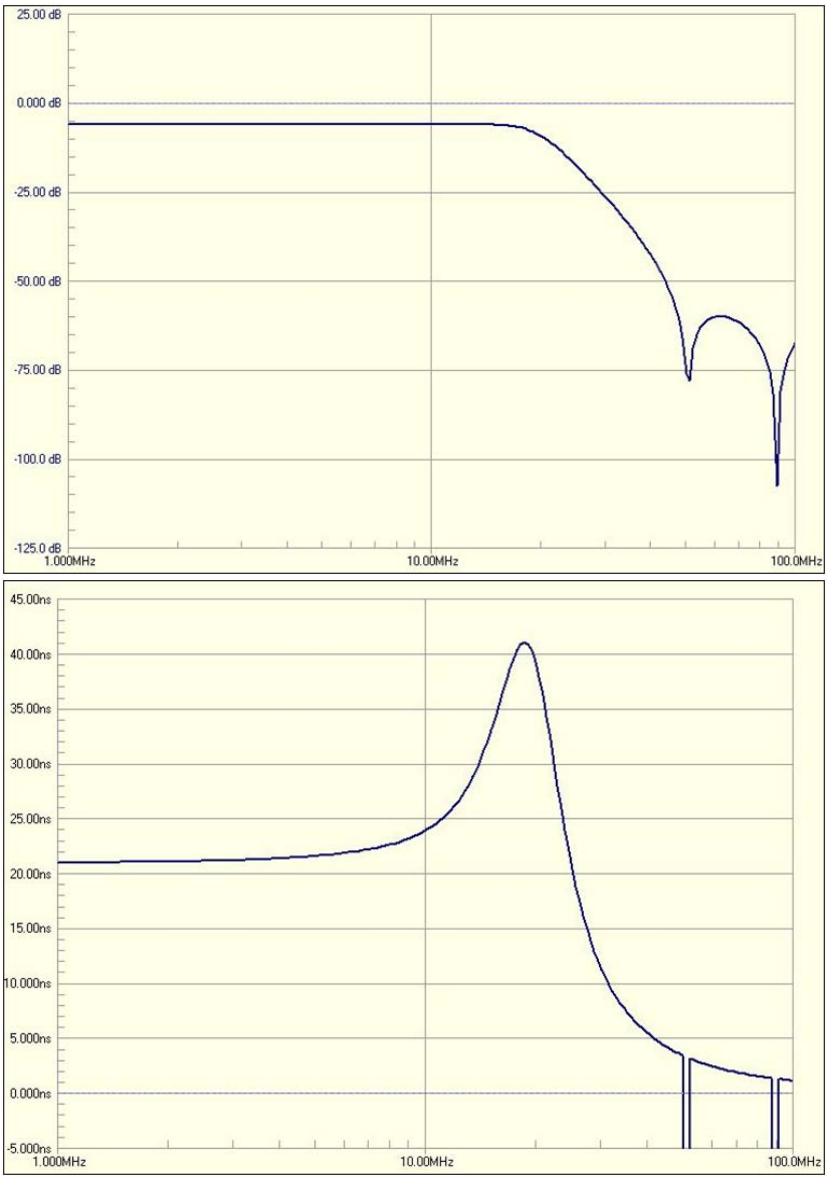

Figure 3.26: Simulated frequency response of the 4^{th} order elliptic low-pass filters for the IQ demodulator; Top - magnitude (f_{3dB}=20 MHz approximately); Bottom - group delay (21 ns in the passband)

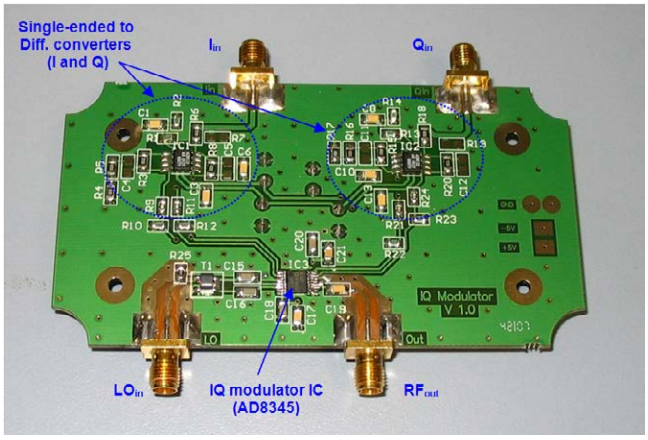

Figure 3.27: Picture of the IQ modulator board

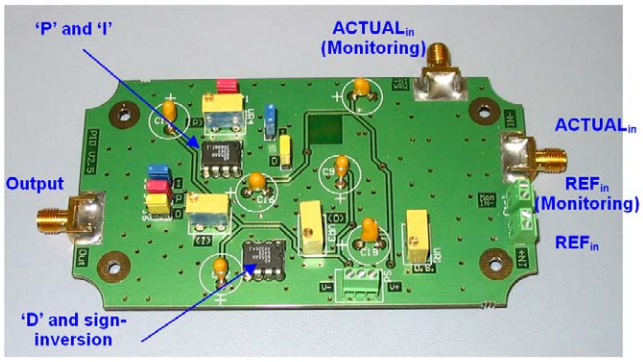

Figure 3.28: Picture of the PID board

compare the responses of P, PI and PID controllers for rectangular and ramp inputs.

As can be seen in the figures, the addition of the derivative part did not improve the response significantly (it slightly improved the response to the ramp input).

PID windup

The combination of integral action and actuator saturations can cause integrator wind-up in real operating conditions pushing the regulation loop out of its linear operating range. Wind-up can happen due to different reasons such as large changes in the reference input, large disturbances, equipment malfunctions, etc. When it happens, the control loop will be broken because the actuator has reached its saturation limit. The integrator will then continue to accumulate the error and this may result in a very large integral action. It will then take some time until the error changes its polarity and the integrator goes back to normal output values. When the integrator winds up, the actuator usually bounces back and forth between its limits and the output undergoes damped oscillations before the system finally goes back to its linear region and the output settles.

In order to avoid integrator windup for the ALBA ALLRF, the low-level boards were designed so that their dynamic ranges were very close to each other (this is typically $\pm 1\ V$ for all the low-level boards). This means that the integrator output saturates at almost the same level as the actuator (the IQ modulator in this case). In this way, the error will not be accumulated by the integrator to reach large values (i.e. it does not wind up). Nevertheless, it has been foreseen to add an anti-windup mechanism to the integrator as a future modification if needed.

The dV/dt limiter

The derivative part of the PID output can become very large at high frequencies. This not only can cause large peaks on the signals when sudden changes are imposed on the loop, but also significantly amplifies high frequency noise. In order to avoid this, a roll-off mechanism was foreseen for the derivative part of the ALLRF PIDs. This was simply done by adding a low-pass filter to the derivative controller to reduce its high-frequency gain[16].

3.2.4 The Phase Shifter

The baseband Phase Shifter was implemented by six AD835 ICs [19] each comprising one 4-quadrant multiplier and one adder. The combination of these ICs performs the amplification and phase rotation which was explained earlier in Subsection 3.1.6 as well as the addition of the feed-forward set values to the

[16] This roll-off mechanism is not considered in the generic PID transfer function represented by EQ. 3.2.

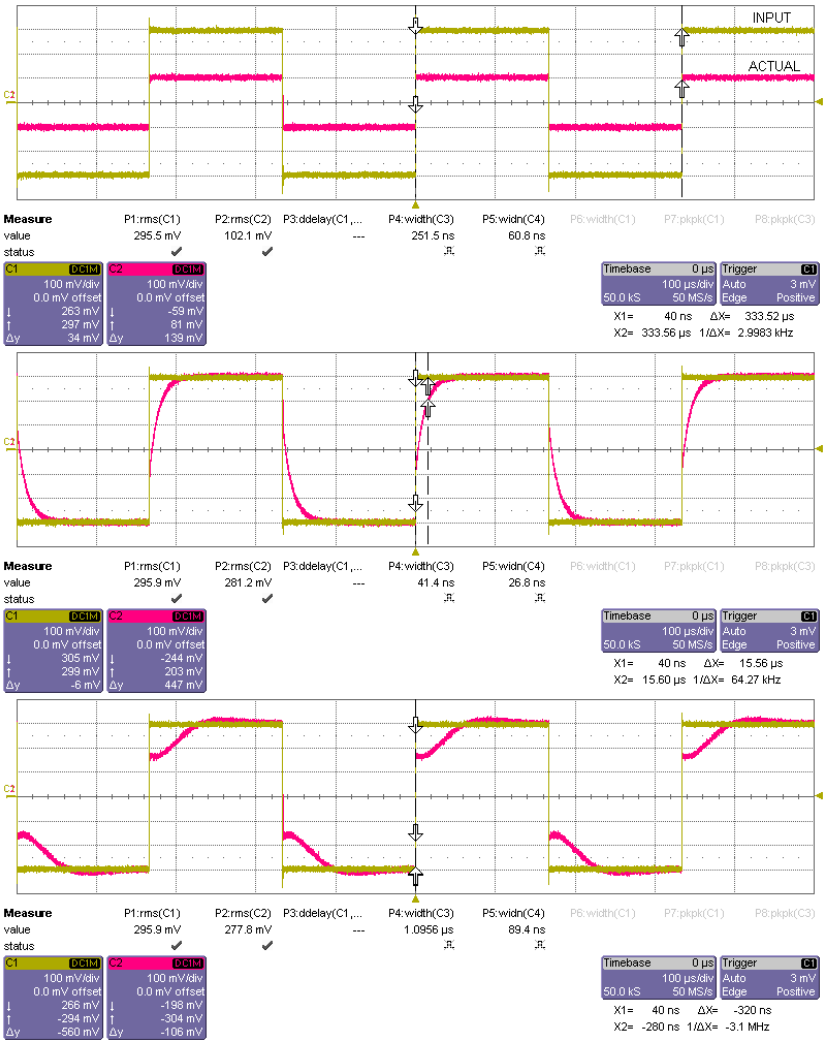

Figure 3.29: Measured response of the regulator to a step input; Top - P; Middle - PI; Bottom - PID

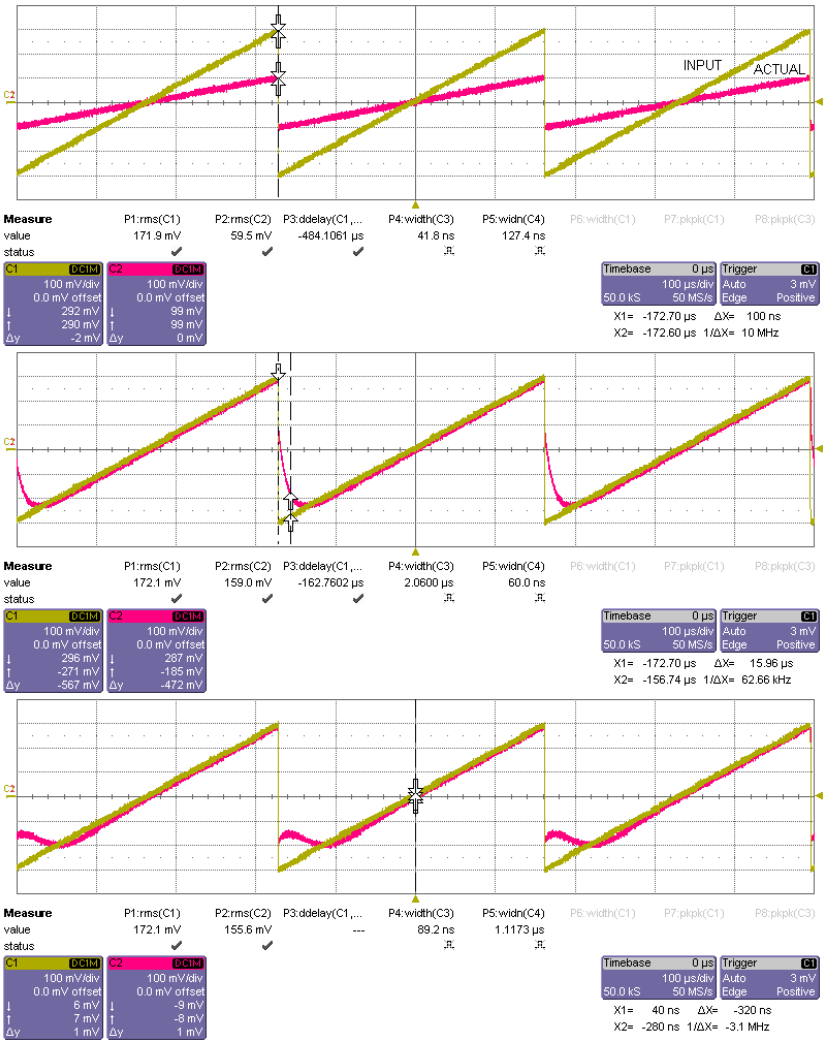

Figure 3.30: Measured response of the regulator to a ramp input; Top - P; Middle - PI; Bottom - PID

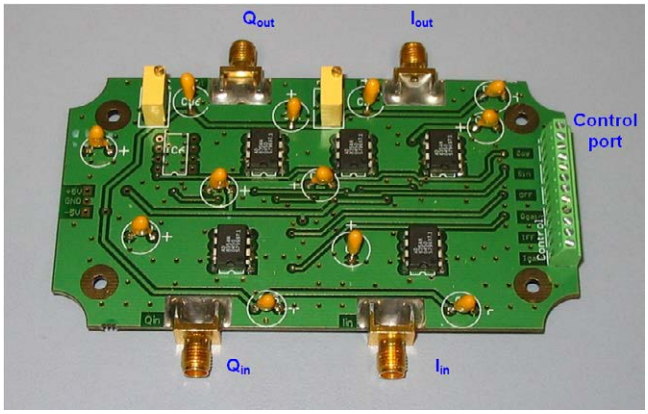

Figure 3.31: Picture of the Phase Shifter board

PID outputs. The input I and Q ($\pm 1\ V_{PP}$) are fed into the I_{in} and Q_{in} ports. These signals are then multiplied by their corresponding gains and added to the feed-forward set values in the lower two ICs shown in FIG. 3.31. The resultant signals are then sent to the 4 higher ICs in the figure to perform the amplification and rotation of the IQ vector. The output I and Q are available on the I_{out} and Q_{out} ports. The control inputs (i.e. $Sin(\theta)$, $Cos(\theta)$, IFF, QFF and the I/Q *gain* factors) are fed into the *Control port* as can be seen in FIG. 3.31.

It should be noted that although DC errors of the *Phase Shifter* signals (due to offsets) will be removed by the PIDs, these errors can still be disturbing at high signal levels because they will push the ICs towards saturation due to their limited voltage range. For this reason, two potentiometers were mounted on the phase shifter board to eliminate the output offsets. The input offsets, on the other hand, can be eliminated by adding appropriate DC values to the feed-forward signals in the Control Computer.

3.2.5 The Amp/Ph Regulation unit

FIG. 3.32 shows a picture of the prototype unit for amplitude and phase regulation.

The design of this unit is the same as the one presented in FIG. 3.1. The RF_{in} and LO_{in} signals are fed into the two ports on the left side of the front panel and the RF_{out}, after 15 dB additional amplification, is available on the port on the right side of the front panel. This signal (4 dBm peak) serves as the input of the Solid-state amplifier (600 W) which drives the IOT. The control and read-back signals of the unit are available on two multi-pin connectors which are mounted on the rear panel. The electronics of the *Amp/Ph Regulation Unit* were mounted on an Aluminum block with 1 cm thickness approximately to provide a good ground, hence protect them against environmental noise and floating. For this prototype, the $\pm 5\ V$ and $+12\ V$ DC power supplies and

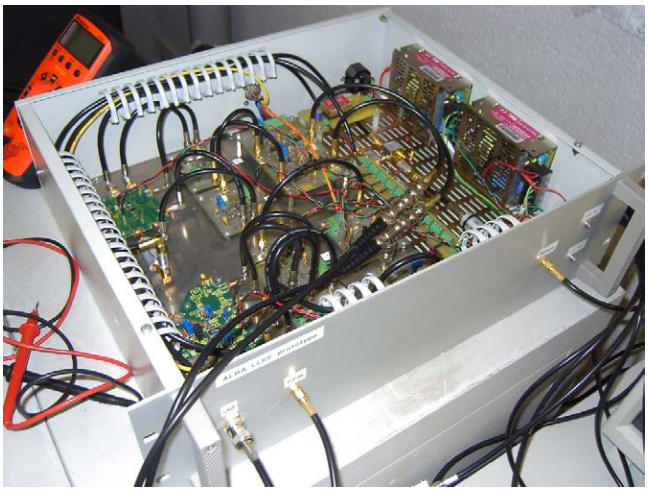

Figure 3.32: Picture of the prototype unit for amplitude and phase regulation

some RF components such as RF amplifiers, filters, frequency doublers, etc. were mounted in the same unit. For the final version of the unit, though, these components were mounted in separate units to preserve the ALLRF modularity.

3.2.6 The Tuning/FF unit

FIG. 3.33 shows picture of the prototype unit for cavity tuning and field-flatness.

As it was mentioned earlier, four IQ demodulators are needed for tuning and field-flatness (the four bigger boxes in the figure). The outputs of these demodulators are sent to an *Adapter/Filter board* (the top-most box on the right). There, they are lightly low-pass filtered to remove their high frequency noise and then are redirected to the front panel for local monitoring and also to the rear panel to be sampled by the data acquisition cards incorporated in the industrial PC which controls the cavity tuners.

3.2.7 The complete ALLRF prototype

In order to be able to test the ALLRF prototype at the ALBA RF laboratory, a few other units had to be made being the *Power Supply Unit*, the *RF Distribution Unit* and the *RF Diagnostics Units*.

The complete LLRF prototype was mounted in two industrial racks with a high of 2 m each. The first rack (FIG. 3.34) includes the low-level electronics for the regulation loops and RF diagnostics. The second rack (not part of the current work) was used for the interlocks and some measurement equipments.

A brief description of the LLRF units is given in the following:

The uppermost unit in FIG. 3.34 is the *Power Supply Unit* (linear type) which supplies $\pm 5\ V$ and $+12\ V$ to the rest of the units.

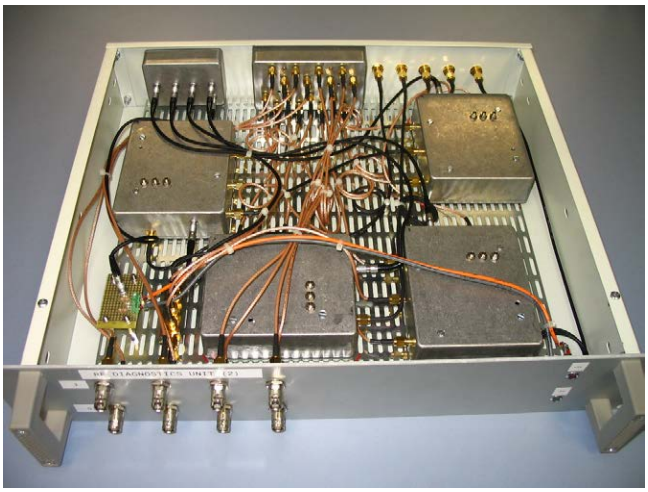

Figure 3.33: Picture of the prototype unit for tuning and field-flatness

The next unit is the *Industrial PC Unit* which also hosts the data-acquisition cards for A-D and D-A conversion. The input/output signals of this unit are accessible on the *Patch Panel* beneath the *Industrial PC*.

The *RF Distribution Unit* receives the 500 MHz reference from the *Master Oscillator*[17] (not shown here) and after frequency doubling and amplification, distributes both 500 MHz and 1000 MHz references among the other units.

The next two units (i.e. *Amp/Ph Regulation Unit* and *Tuning/FF Unit*) include all the low-level electronics which are needed for the amplitude, phase and tuning loops.

The two units marked at *RF diagnostics (1)* and *RF diagnostics (2)* have a design very similar to the *Tuning/FF Unit* but they are intended for RF diagnostics only. Each of these units is used to measure the amplitude and phase of up to four RF signals at different positions of the RF plant. These signals are used during RF operation for monitoring purposes or for post-mortem analysis of the data (ex. when a fault occurs).

The two lower-most patch panels receive RF signals from different locations of the RF plant, send them to the corresponding units and also make some of them accessible on the front panel for local measurements.

It should be note that although the designs of all the IQ demodulator boards of the ALLRF prototype are the same, the external filtering imposed on the I/Q outputs are slightly different due to different requirements. For example, as the tuning/field-flatness process is relatively slow, the filters of the *Tuning/FF Unit* are stronger to provide these signals with as less noise as possible. On the other hand in the *RF Diagnostic Unit* lighter filters have been used to provide these

[17] *Master Oscillator*, which works at the same frequency as the RF system, generates the reference clock for the entire accelerator. In this way, the beam and all the subsystems which work at RF frequency are synchronized with each other.

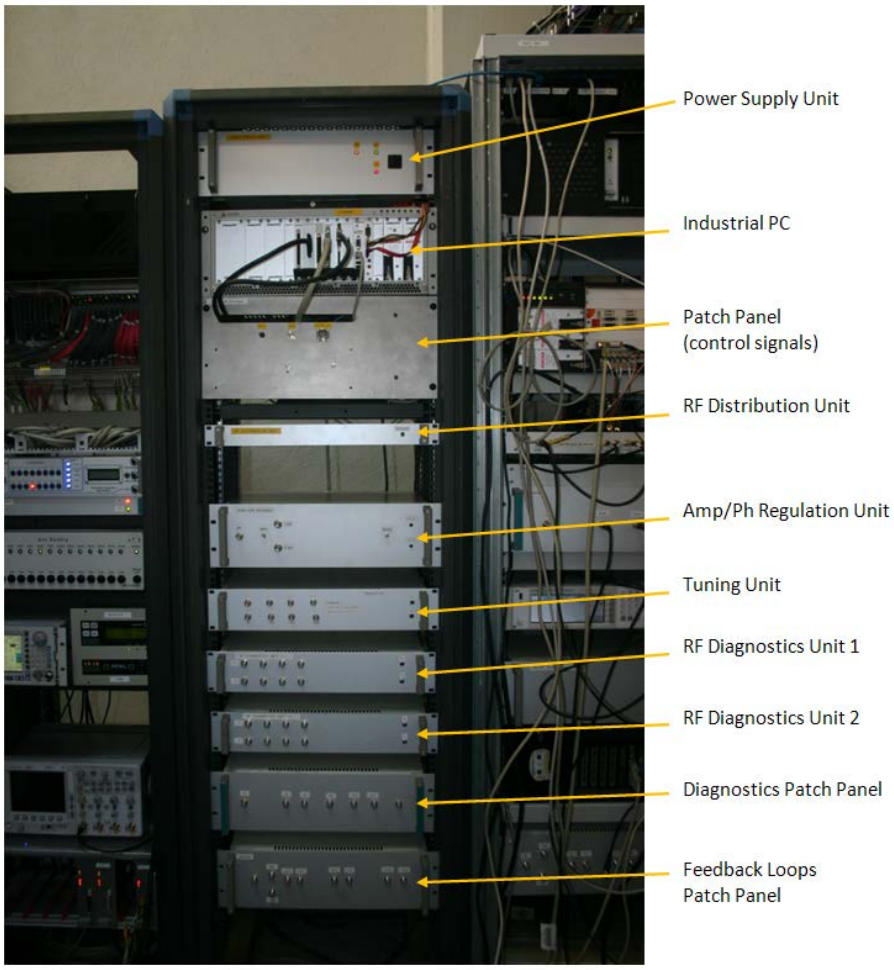

Figure 3.34: Picture of the complete ALLRF prototype installed at CELLS (Barcelona - Spain)

Figure 3.35: Final version of the Diagnostics Front-end Unit

signals with enough bandwidth for post-mortem data analysis. For the IQ loops, however, as both bandwidth and accuracy are important, the filters have been chosen so that the two requirements are satisfied simultaneously.

The design of the final ALLRF system for the ALBA booster is the same as the prototype, but the unit preparation and serigraphy were outsourced. FIG. 3.35 shows a picture of the Diagnostics Front-end Unit in its final form (the same unit design has been adopted for the rest of the ALLRF units).

3.2.8 Some practical considerations

Noise Protection

Noise protection becomes one of the most important issues when high signal-accuracies are needed. Noise can be internal or external depending where it originates from. The first tests with the ALBA LLRF system showed that three noise sources had the highest contribution to the performance degradation of the loops: The first one was the ripples from the SMPSs[18] which were used in the first prototype to supply the electronics. This problem was removed by using Linear Power Supplies instead of the SMPSs and in some cases by Ferrite beads. The second noise was a high frequency oscillation (88 MHz - 108 MHz) which was present on almost all the baseband signals. Later, it was discovered that this noise was due to an external FM[19] transmitter. The problem was removed by providing metallic enclosures for all the electronics and improving the grounding system. Finally, the third noise source was the RF signal generator which was used for IQ modulation/demodulation. As this signal generator was mainly

[18] Switched-Mode Power Supplies
[19] Frequency Modulation

intended for laboratory tests (i.e. it was relatively low-quality), there was a significant amount of phase noise on its output and that consequently affected the low-level signals. Later, the signal generator was replaced with another one with much better performance and this problem was also removed.

Grounding

Providing a good grounding system is essential in most circuit designs. A good ground not only prevents the signals from floating, but also can have a major effect on noise protection. For this reason, the ground plane on both sides of the PCBs was extended to cover as much area of the boards as possible. The ground was further reinforced by mounting the most critical electronics on Aluminum blocks and connecting the ground of all the electronics to the chassis of the units and also to the body of the racks.

Delays and phase shifts

In high frequency applications, a very small delay will be equivalent to a large phase shift in the RF signals. As an example with $f_{RF} = 500\ MHz$, the RF period will be 2 ns corresponding to 60 cm of wavelength in air and 45 cm approximately in Copper conductors. Therefore, a cable length of 45 cm (or equivalently a delay of 2 ns) will generate a phase shift of 360° in the RF signals. In order to get the best performance from the loops, the total loop delay must be made as small as possible. This implies making cables and PCB tracks short. When differential signals are used, the two tracks for the positive and negative signals should be placed very close to each other. This not only makes the lengths of the two lines almost equal (i.e. equal delays on both lines to avoid unwanted phase shifts) but also helps reducing magnetic couplings with adjacent tracks.

3.2.9 The Graphical User Interface (GUI)

ALBA is equipped with a control-room where all the machine parameters are monitored and controlled via several terminals each dedicated to some part of the accelerator. During machine operation, when access to the ring is prohibited by the interlock system, the operators know the actual status of the machine and send the required control commands via these terminals. In that respect, some terminals are dedicated to the RF system providing the operator with the RF and LLRF data.

FIG. 3.36 shows a preliminary design of the GUI for the ALBA ALLRF system. The design of the GUI was part of the current work, but its implementation in Python and integration into the TANGO[20] control system of ALBA was done by the ALBA Computing Division.

The light-blue boxes show the read-back values and the green boxes the set values. The upper half of the screen is used for amplitude and phase regulation.

[20] TAco Next Generation Objects

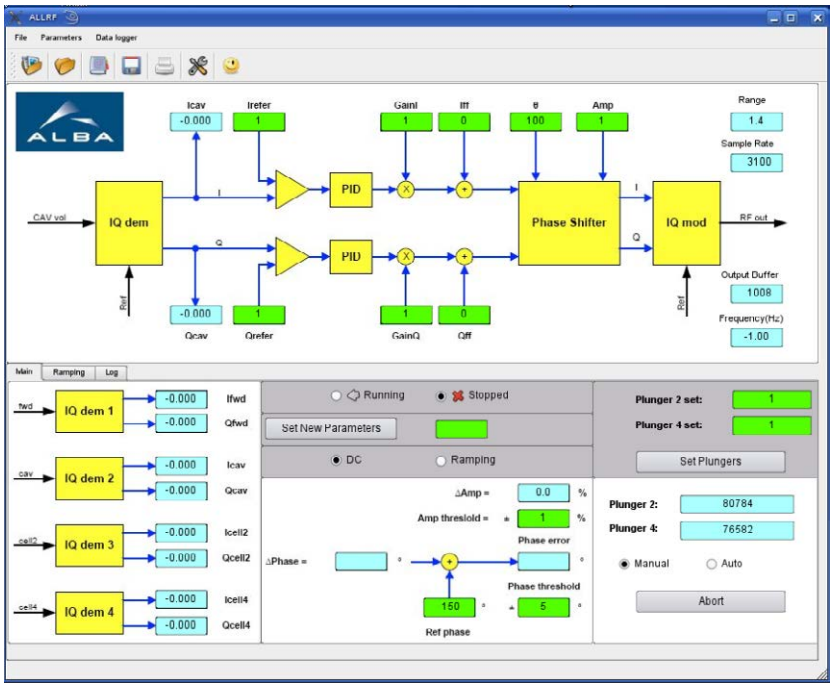

Figure 3.36: Preliminary design of the ALLRF GUI

There, the operator is able to read the actual I and Q of the measured cavity voltage, set the reference I and Q for the two PIDs, set the feed-forward values and the input parameters of the phase shifter plus some other parameters such as the voltage range and sampling rate for the DAQ cards. The lower half is used for tuning and field-flatness. There, the operator can read the I and Q outputs of the four demodulators which are used for this purpose, read the calculated amplitude and phase errors, set the tuning and field-flatness regulation thresholds and read the actual positions of the tuners. This part also provides the operator with some additional features such as enabling/disabling the loops, manual movement of the tuners (in this case, reference positions for the tuners are entered manually into the corresponding boxes) and switching between CW and ramping modes (the CW mode is intended for the storage ring and test purposes and the ramping mode for the booster). The other pages of the GUI (not shown in the figure) allows the operator to load the ramping data (I_{set}, Q_{set}, IFF and QFF), view and edit them before they are sent to the output and also provides the operator with the most-recently recorded data for post-mortem analysis in case of fault/interruption.

3.3 Experimental Results

The in-house developed ALBA ALLRF went through extensive tests to assert its ability to work continuously and reliably under the real conditions of the future ALBA machine. Several tests were performed on the ALLRF system at the ALBA RF lab and elsewhere being the tests during the development and trouble-shooting of the low-level electronics, low-power and high-power tests without beam and finally tests with a simulated beam. These tests not only ensured the ability of the ALLRF to work according to the specifications, but also helped remove some unforeseen errors in the design of the boards and the program of the control computer. In one occasion the ALLRF was shipped to the high-power RF lab at ELLETRA[21]-Italy and tested with an RF cavity and transmitter under high power (this was done before the establishment of the CELLS high-power RF lab when making such a test at CELLS was not possible). Later on, when the CELLS RF lab was established, similar tests were done in-house with almost the same results. In this section, we will present the results of the tests for CW/ramping operation, ripple reduction, bandwidth, dynamic range, phase control range, noise level, etc. at the CELLS RF laboratory. We will also report on the tests which were done at ELETTRA although in some cases the waveforms could not be recorded due to the lack of modern equipments at the high power RF lab.[22]. Finally, we will present the results of the ALLRF

[21] Elettra is an international multisciplinary laboratory specialized in synchrotron radiation and its use in the science of matter. It is located in Basovizza on the outskirts of Trieste and is operated by Sincrotrone Trieste S.C.p.A. as a user facility. The laboratory features a 2.4 GeV, third-generation synchrotron radiation source, also named Elettra, and a fourth-generation light source based on a free-electron laser. Source: ELETTRA website

[22] The measurement equipments available for these tests were mainly old ones without modern features such as save waveform. Because of this, in most cases, the measurement data was

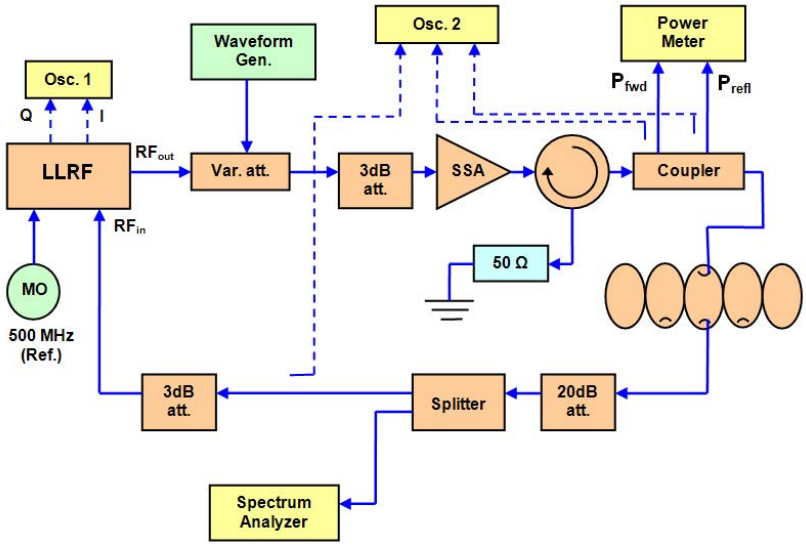

Figure 3.37: Schematics of the setup for amplitude regulation test

tests with a simulated beam.

3.3.1 ALLRF tests at the CELLS RF lab.

The following tests were done with a 5-cell cavity, similar to the one that will be used for the ALBA booster, and a 500 W Solid State Amplifier (SSA). Because the Tuning/Field-flatness Unit was not ready by the time the tests were carried out, the frequency of the RF generator was adjusted manually from time to time in order to keep the reflected power minimized.

Amplitude/phase regulation test with PI

The schematics of the setup for amplitude regulation test is shown in FIG. 3.37.

The drive of the SSA was AM-modulated by a voltage controlled attenuator and a waveform generator. The probe signal from the central cell was fed back into the LLRF to compensate for the artificially-induced ripples on the amplitude on the cavity voltage. In this test, the reference I and Q were set to 1 V. The forward power was measured at 47 dBm (51 W) and the reflected one at 32 dBm (1.6 W). The waveform generator was set to sinusoidal output with an amplitude of 2 V_{PP} and an offset of 9 V. The modulation frequency was then changed from a minimum of 3 kHz to a maximum of 20 kHz.

FIG. 3.38 shows the frequency-domain results of the amplitude test without regulation to the one with PI regulation.

manually recorded.

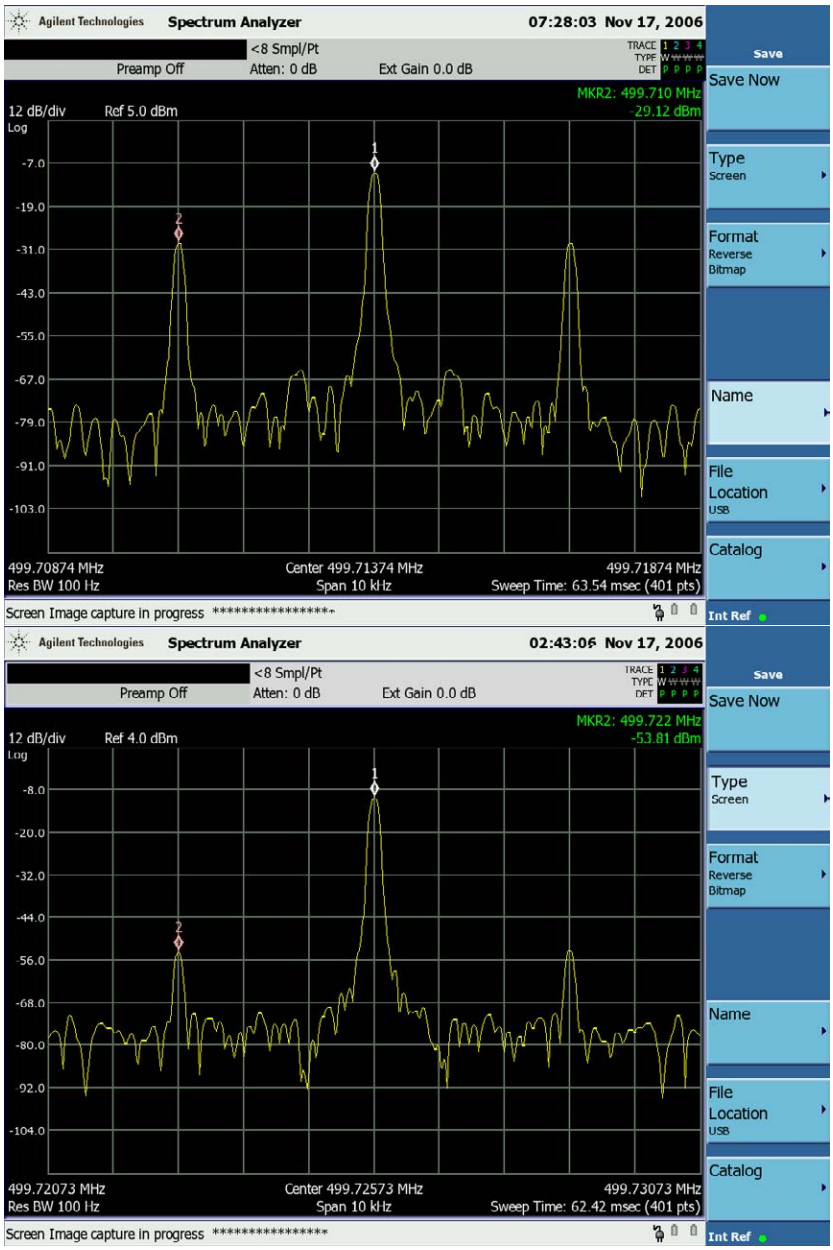

Figure 3.38: Measured spectrum of the cavity voltage with $f_{ripple} = 3\ kHz$; Top: open loop; Bottom: 25 dB ripple reduction in closed loop mode

The central peak in FIG. 3.38 is the RF frequency (500 MHz) and the two small ones on both sides are due to the ripples on the amplitude of the cavity voltage, therefore the frequency difference between the main peak and either of the smaller peaks shows the ripple frequency (in this case the ripple frequency was 3 kHz). As the figure shows, enabling the PI loop had not effect on the fundamental resonance but significantly reduced the ripple amplitude.

As the ripple frequency was increased, larger ripples became visible on the cavity voltage because of the limited bandwidth of the loop. For example at $f_{ripple} = 3\ kHz$ the ratio between the original ripple and the first harmonic of the cavity ripple was 17.77 indicating that the loop removed 94.4% of the ripple and the remaining 3.6% appeared on the cavity voltage. The ripple reduction factor was 85.2% for $f_{ripple} = 6\ kHz$ and 73.3% for $f_{ripple} = 10\ kHz$. For frequencies above 35 kHz, the loop had negligible effect on ripple reduction[23].

A similar test was done to evaluate the performance of the loops when ripples were imposed on the phase of the cavity voltage. The setup was similar to the one in FIG. 3.37 but a voltage-controlled phase-shifter was used instead of the voltage-controlled attenuator to generate a disturbance on the cavity phase. FIG. 3.39 shows the results of this test in time domain[24].

As the figures shows, the regulator removed the disturbance in 20 μs approximately. This is almost equal to the natural settling time of the cavity itself indicating that the rise-time of the loop was mainly due to the dynamics of the cavity and not the dynamics of the low-level electronics.

Amplitude/phase regulation test with PID

The ripple reduction performance of the loop can be slightly improved by adding a derivative term to the previously-used PI regulators. A PI regulator needs some time to reduce the I_{error} and Q_{error} down to zero. This is due to the cumulative nature of the integral part which is based on charging/discharging a capacitor. The derivative part additionally gives a *predictive* capability to the regulator by acting on the slope of the error rather than its value. This can be helpful for ripple reduction at high frequencies where a PI is not sufficient. Nevertheless, one has to be careful with derivative regulators because in general they have a tendency to amplify high frequency variations. Setting the derivative gain of the regulator to high values can result in too much noise on the output or even instabilities.

The previous tests with the cavity and the amplifier were repeated after enabling the derivative parts of the PID regulators. The results showed that the performance of the IQ loop did not change much up to 10 kHz, but for higher frequencies, smaller ripples showed up on the output thanks to the derivative component of the PID. At $f_{ripple} = 10\ kHz$, for example, the difference between the PI and the PID is 3 dB for the first harmonic of the ripple as shown in

[23]This bandwidth is enough in practice because the real ripple frequency of the ALBA HVPS will be in the order of 1 kHz approximately.

[24]In frequency domain, phase ripples also result in two sidebands above and below the carrier frequency with a frequency difference equal to the ripple frequency.

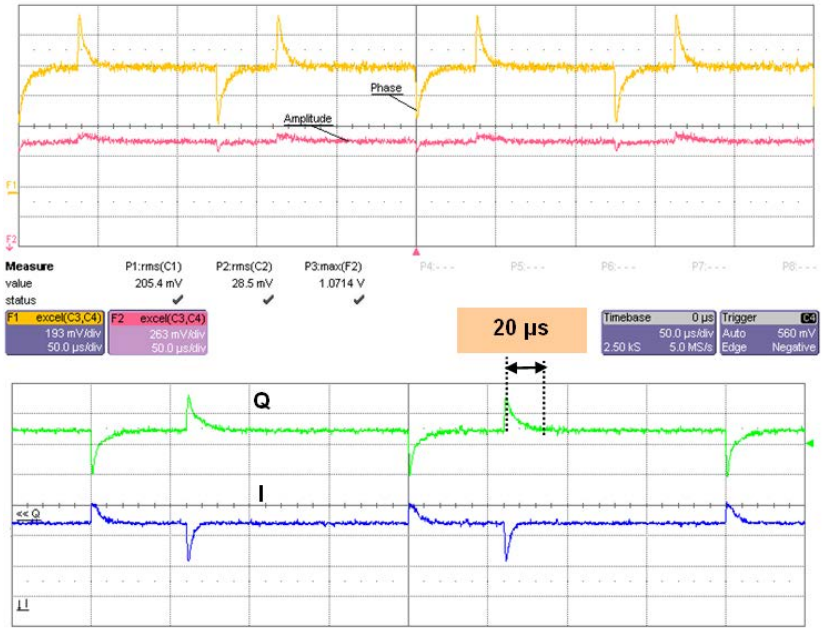

Figure 3.39: Result of the phase regulation test; Top - amplitude and phase of the cavity voltage; Bottom - corresponding I and Q of the cavity voltage

FIG. 3.40. At higher ripple frequencies, the difference became larger but as mentioned earlier, the derivative gain could not be increased much because then it amplified the high frequency noise.

Ramping test

For this test, the LLRF was operated in ramping mode. The I and Q set values followed equal waveforms with a minimum equal to 35 mV, a maximum equal to 1.4 V and a repetition rate of 35 Hz. With these reference waveforms, the amplitude of the cavity voltage changed by $\Delta amp = 20log(\frac{1400}{35}) = 32\ dB$ from minimum to maximum while the phase remained always at $\theta = tan^{-1}(\frac{Q}{I}) = 45°$. FIG. 3.41 and FIG. 3.42 show the results of this test measured by an oscilloscope.

As FIG. 3.42 shows, the measured dynamic range of the ALLRF system was 28 dB approximately. The difference between the set value (i.e. 32 dB) and the measured one was due to the uncorrected offsets and the noise on the baseband signals. The little dead-time before the flat-top was due to a bug in the control program (it was removed later by the control staff).

Phase control range

As it was mentioned earlier, one of the advantages of the IQ loops compared to the traditional amplitude/phase loops is that with the IQ method the cavity phase can be controlled to have any value between 0° and 360° while with phase loops the maximum phase control range is limited to 180°. This is due to the fact that a conventional phase detector does not distinguish $+\alpha°$ from $-\alpha°$ [20] while with an IQ demodulator these two phases are distinguished from each other because they generate different IQ values. The ability of the IQ loop to fully control the phase is verified by FIG. 3.43 which shows the IQ signals with the cavity phase covering the 4 quadrants in ramping mode.

Baseband noise

FIG. 3.44 shows the measured cavity I and Q in ramping mode just before the flat-top[25].

The figure shows a noise level of 10 mV_{PP} approximately on the I/Q signals. The noise, however, went down to 5 mV_{PP} approximately after the RF generator (R&S SM300) was replaced with a better one (Agilent 4421B) and shielding was provided for the electronics. Taking into account that the I/Q voltage range is $\pm 1.4\ V_{PP}$ a noise level of 5 mV_{PP} will result in a short-term amplitude/phase stability of $\pm 0.2\%$ and $\pm 0.4°$ approximately while in the specifications the amplitude/phase stabilities are $\pm 1\%$ and $\pm 1°$ respectively.

FIG. 3.45 shows the measured power spectrum of the baseband signals affected by another noise source being in this case an external radio FM transmitter (this noise was removed by the electronics shielding).

[25]This measurement was done before the LLRF shielding and grounding were improved and the RF generator was replaced with a better one for noise reduction purposes.

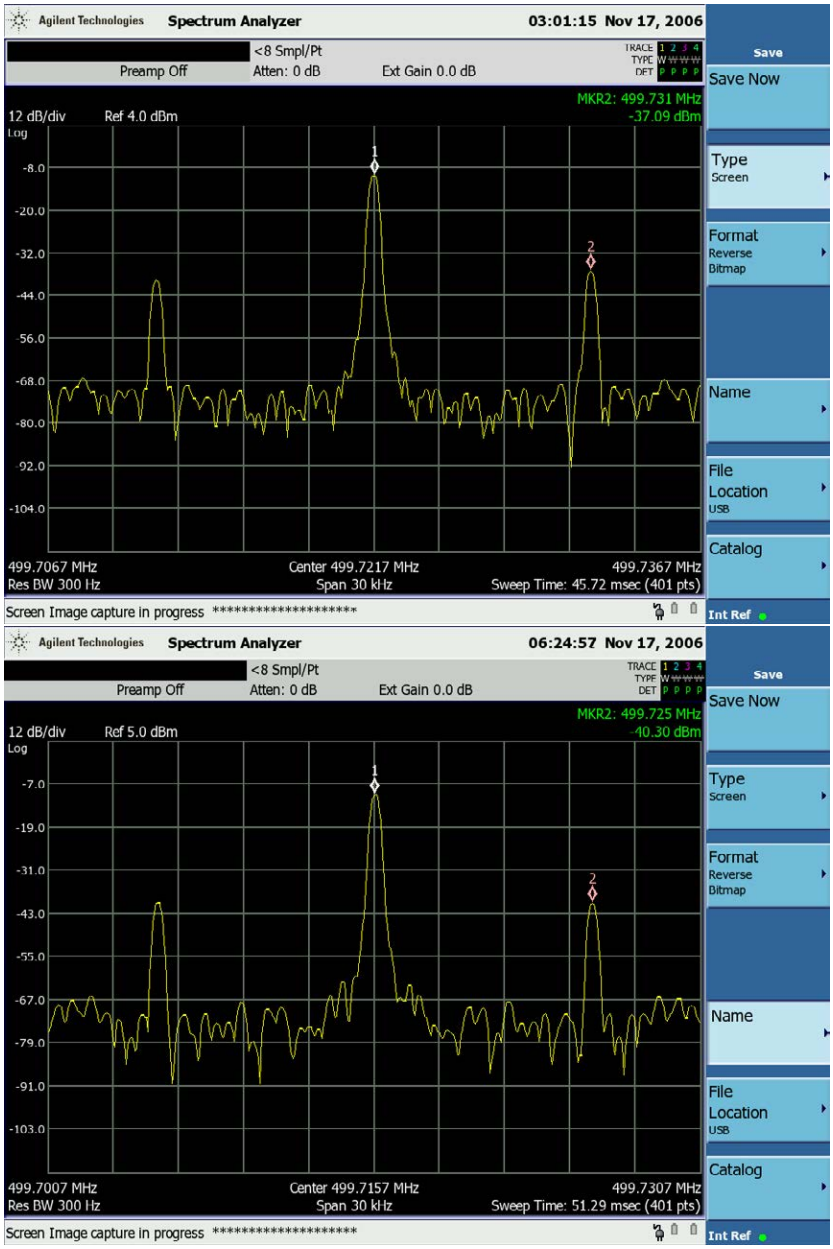

Figure 3.40: Comparison between the PI and PID responces at $f_{ripple} = 10\ kHz$; the ripple amplitude is 3 dB lower with PID (bottom) compared to PI (top).

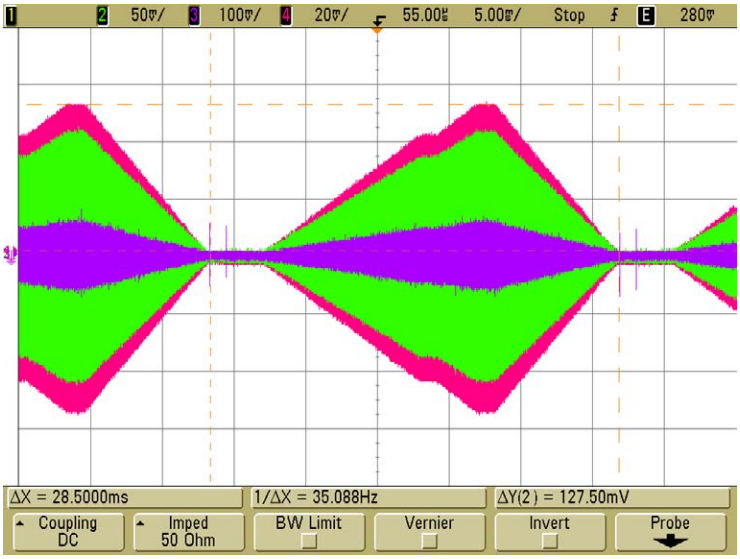

Figure 3.41: Outer: V_{cav}; Middle: V_{fwd}; Inner: V_{refl} (not in scale)

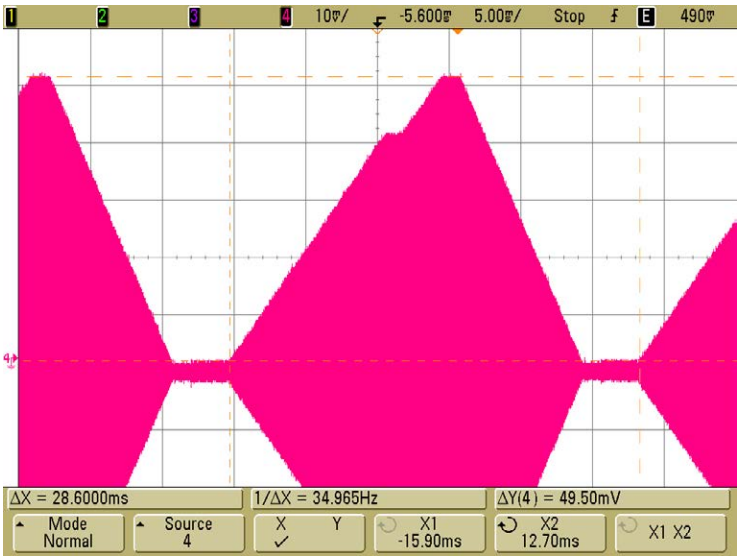

Figure 3.42: Cavity voltage in the ramping mode with a measured dynamic range of 28 dB approximately

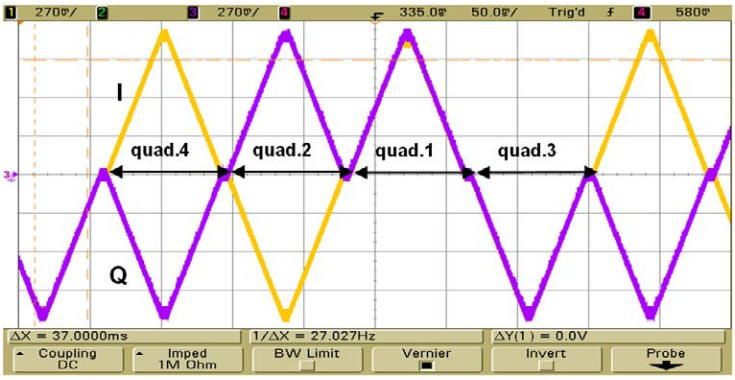

Figure 3.43: Measured I/Q of the cavity voltage in the ramping mode with 4-quadrant phase coverage

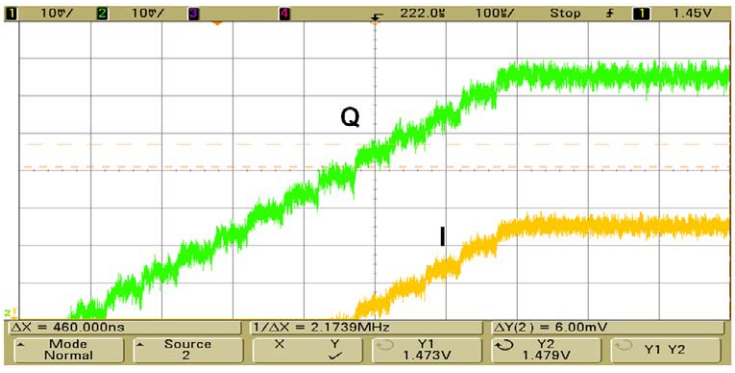

Figure 3.44: Measured I/Q of the cavity voltage in ramping mode; the two waveforms are given a relative offset in the oscilloscope to improve their visibility.

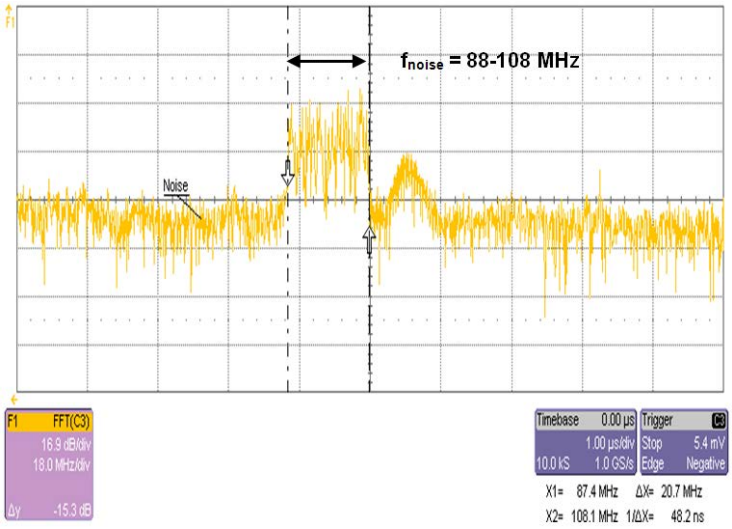

Figure 3.45: Spectrum of the FM noise on the baseband signals (without proper shielding)

3.3.2 LLRF tests at the ELETTRA RF lab

These tests were done with a 60 kW transmitter (Klystron) and a 5-cell cavity similar to the one of the ALBA booster. The LLRF prototype was used to regulate the amplitude and phase of the cavity voltage while the tuning loop was the one from ELETTRA. The 500 MHz reference clock for the LLRF was provided by an RF generator from ELETTRA. The measured gap voltage with maximum level of 0 dBm was fed to the LLRF input and the LLRF output drove the transmitter with 15 dBm at maximum. For a soft start-up[26], a controlled attenuator (0-35 dB) was put at the LLRF output and for the phase regulation test, a voltage-controlled phase shifter was placed in series with the controlled attenuator at the LLRF output.

FIG. 3.46 shows a picture of the ELETTRA high-power RF lab. and the RF transmitter (Klystron) used for the LLRF tests.

For the start-up, the control voltage of the attenuator was set to 5.6 V approximately (i.e. attenuation = 17 dB) to avoid the risk of driving the transmitter with a high input. The reference I and Q were set to 140 mV and 100 mV respectively. The cavity power was measured at 2.5 kW and the read-back I and Q were different from the set values. In the next step, the base-band phase shifter was adjusted to compensate for the loop delays. After the phase adjustment, the cavity power was measured at 250 W and the read-back I and Q were the same as the reference ones indicating that both I and Q loops were stable and the LLRF was regulating the RF voltage. After the stability of the

[26] A soft start-up mechanism is not needed for ALBA due to the choice of the voltages and power levels.

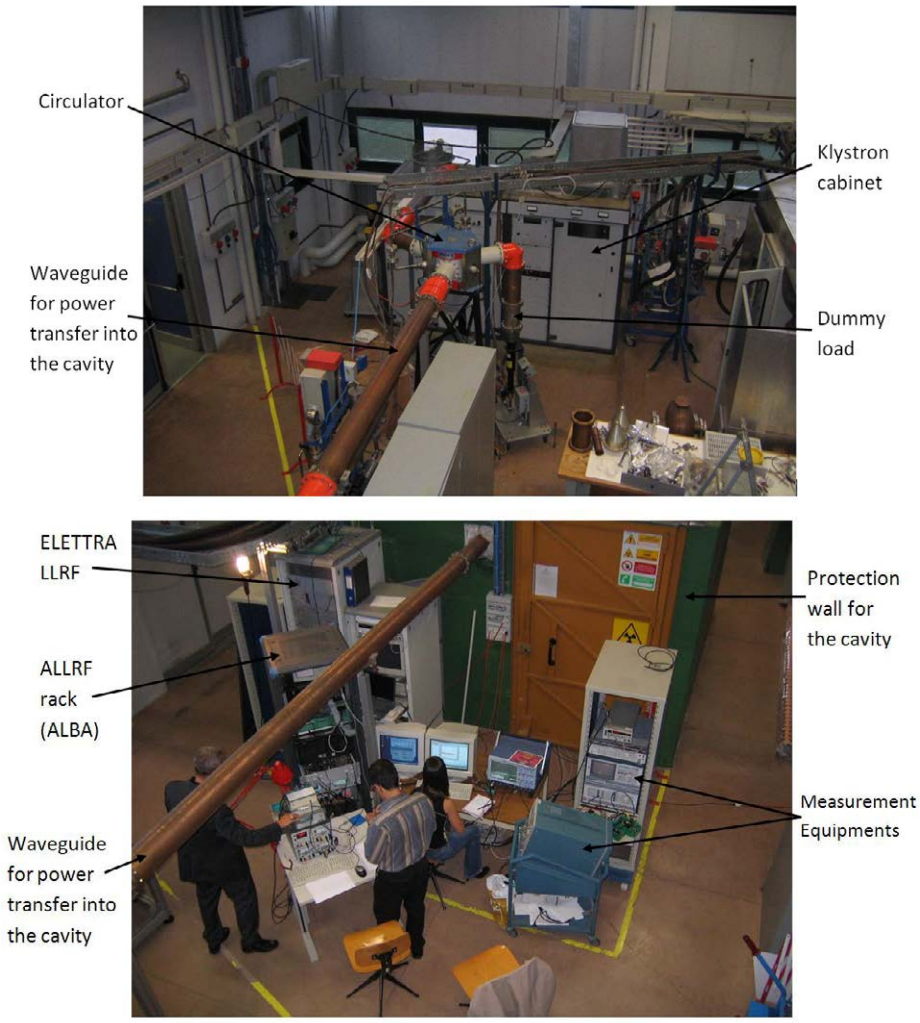

Figure 3.46: Picture of the ELETTRA high-power RF lab. showing the klystron, the waveguide system, the LLRF rack and the measurement equipments

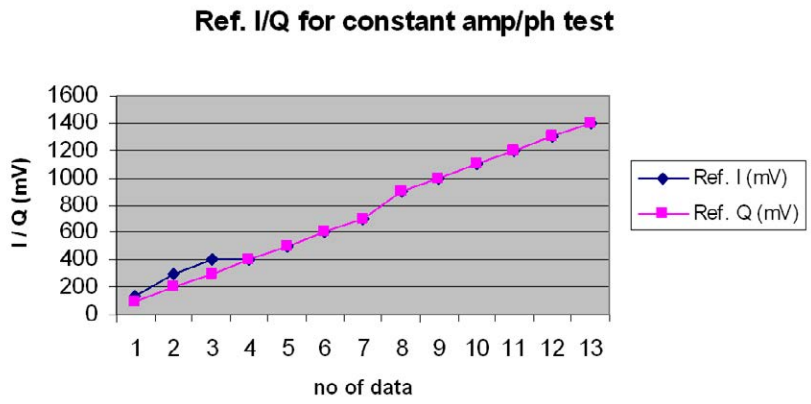

Figure 3.47: Reference I/Q values for the CW (constant amp/ph) test

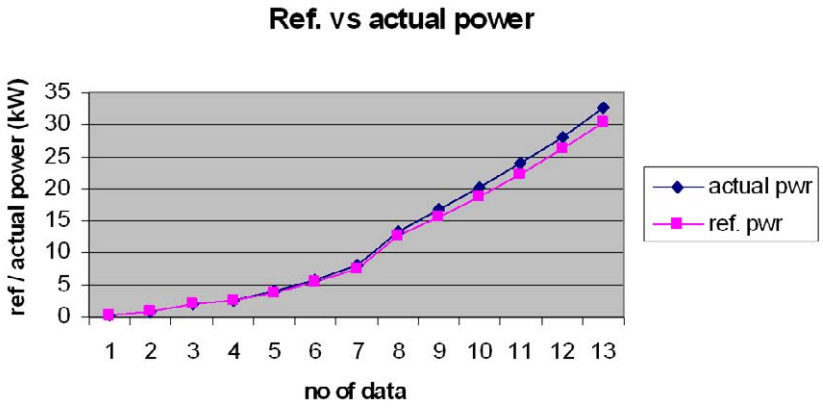

Figure 3.48: Reference vs. actual power with the IQ values shown in FIG. 3.47

I and Q loops was assured, the control voltage of the attenuator was reduced to 1.5 V approximately to minimize the attenuation thus avoid saturations at higher power levels.

CW tests

For this test, the I/Q set values were manually increased in steps of 60/40 mV up to the maximum levels (i.e. 1400 mV). The time interval between the steps was 2 min approximately to let the vacuum pressure settle after the stress caused by the reference change. At the maximum level the RF power was measured at 32.5 kW and no saturation was observed on the measured I/Q signals. FIG. 3.47 and FIG. 3.48 show the reference I/Q values and their corresponding power levels.

The difference between the reference power and the actual one at higher

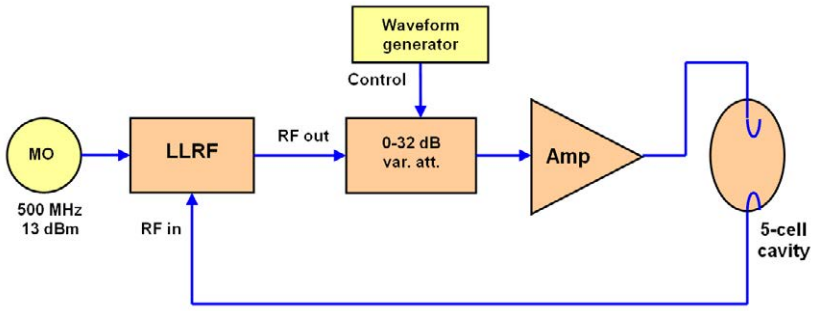

Figure 3.49: Simplified schematics of the setup for amplitude regulation test

power levels is believed to be due to the uncorrected DC offsets and the nonlinearity of the Klystron amplifier[27].

Amplitude regulation test

For the amplitude regulation test, the controlled attenuator was connected to a waveform generator to AM-modulate the drive signal of the transmitter. The RF power was increased step by step to 13.2 kW ($I = Q = 900\ mV$). The waveform generator was enabled with sinusoidal output and the ripples on the cavity voltage were measured with different modulation depths and frequencies to determine the response of the loop for amplitude regulation. A simplified schematic view of the loop and the results of this test are shown in figures FIG. 3.49 to FIG. 3.51.

FIG. 3.50 shows that the loop was able to remove amplitude ripples up to 10 kHz approximately. At higher frequencies the loop became less effective and at 35 kHz it almost had no effect on the ripple. This regulation bandwidth is sufficient for the ALBA ALLRF because the highest-frequency ripples that may affect the RF field are known to be due to the HVPS of the IOT. As these power supplies are based on full-wave inverters, their ripple frequency is mainly concentrated at multiples of 50 Hz (ex: 600 Hz in case of a full-wave 12-pulse inverter) but still less that the regulation bandwidth.

FIG. 3.51 shows that above 30 mV, the ripple amplitude increases linearly with the modulation depth (i.e. the induced ripple) as expected from a linear system.

Phase regulation test

For this test, a voltage controlled phase shifter was placed at the LLRF output in series with the controlled attenuator. The RF power was increased step by

[27]These nonlinearities are less in case of ALBA because IOTs are known to have a more linear response compared to klystrons. Also, the nonlinearities of the power part can be compensated by the LLRF regulation loop if well adjusted.

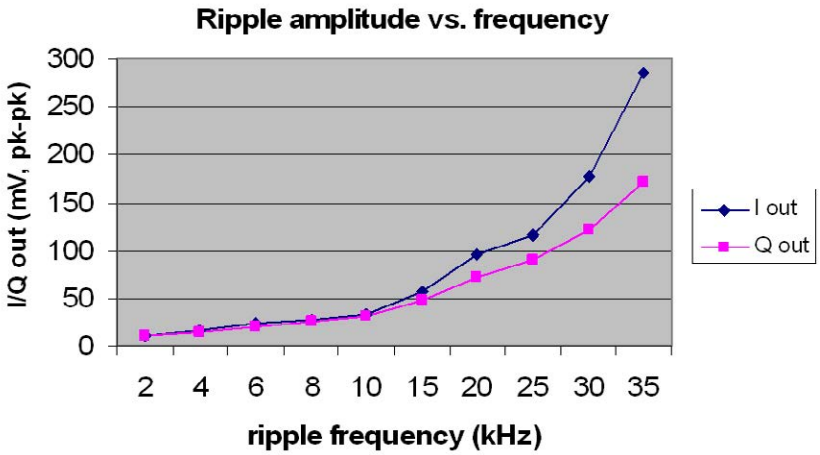

Figure 3.50: Amplitude ripple vs. frequency (modulation depth $= 1\ V\ \approx 3\ dB$)

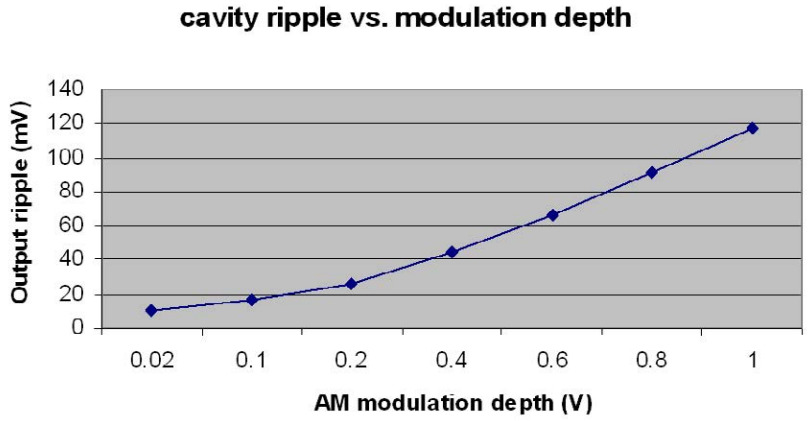

Figure 3.51: Amplitude ripple vs. modulation depth (ripple freq. $= 20\ kHz$)

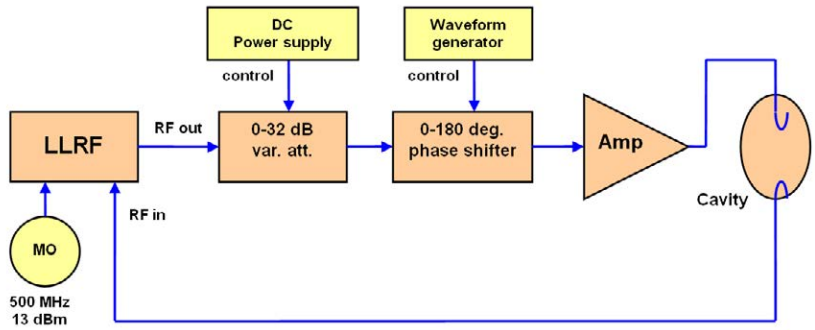

Figure 3.52: Simplified schematics of the setup for the phase regulation test

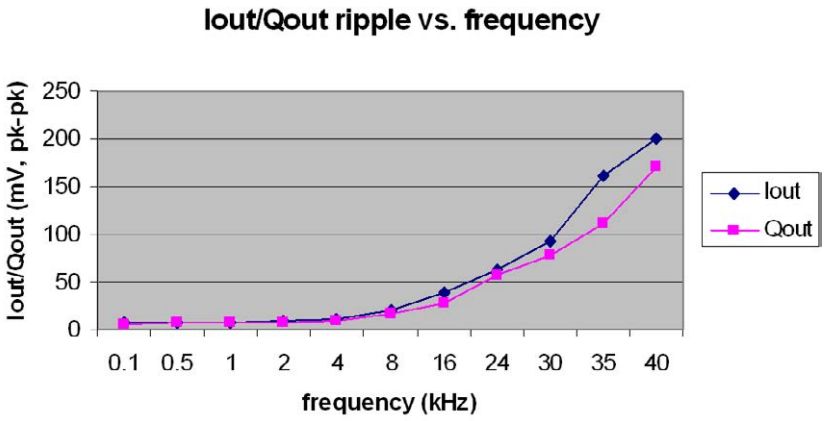

Figure 3.53: Measured I/Q ripple vs. frequency from the phase regulation test

step up to 10.6 kW and phase ripples with different frequencies were imposed on the RF_{out} signal. The cavity voltage was examined with a spectrum analyzer. Because of the phase ripples two additional side-bands appeared on both sides of the carrier frequency indicating the ripples. The magnitude of these side-bands was measured for different ripple frequencies. FIG. 3.52 and FIG. 3.53 show simplified schematics of the test setup and the test results.

As it can be seen in FIG. 3.53, at low frequencies, the feedback loop compensates the ripple almost completely. For example at f_{ripple}=500 Hz, the attenuation factor is about 200 (linear) indicating that only 0.5% of the induced ripple appears on the output while 99.5% is compensated by the feedback loop. This verifies the ability of the ALLRF to compensate phase ripples such as the ones due to the HVPS. As the ripple frequency is increased, larger ripples become visible on the output because of the limited loop bandwidth. For example at f_{ripple}=5 kHz the attenuation factor is about 20 showing that 95% of the induced ripple is compensated by the feedback loop.

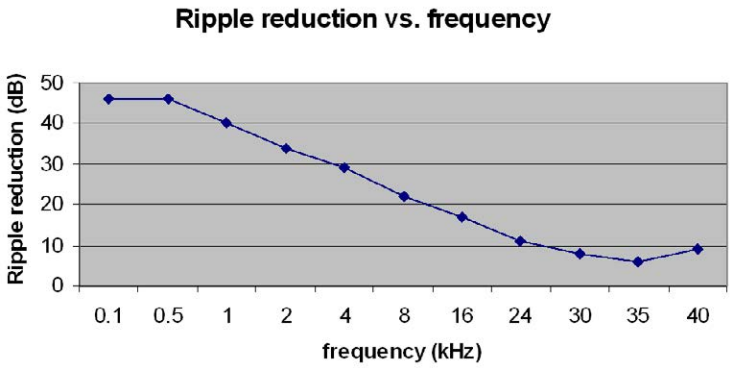

Figure 3.54: Phase ripple reduction vs. frequency (imposed ripple = $-24\ dBc$)

Ramping test

For the ramping test, the RF power was increased step by step to the maximum level. After the vacuum settled, the LLRF was put into operation in ramping mode with a repetition frequency of 35 Hz and maximum level of $I = Q = 1200\ mV$. The results (see FIG. 3.55) show that the cavity voltage closely followed the reference waveforms set by the operator. The measured dynamic range was about 26 dB (3 dB larger than the specifications as shown in TABLE 3.4) and the vacuum was stable throughout the tests.

3.3.3 LLRF tests with *Virtual Beam*

The purpose of this test[28] was to simulate the effect of the beam on the LLRF system in a RF lab where obviously a real beam can not be generated. This test not only gave a very good insight into how the LLRF system should be operated under beam, but also made sure that the electronics had enough voltage margins to counter-act the beam effect which could otherwise push the ICs towards saturation. The beam was simulated by adding a 500 MHz signal with variable amplitude and phase to the amplifier drive as it is shown in FIG. 3.56.

The amplitude and phase of the *Virtual Beam* were adjusted so that it simulated a real one for the LLRF system. The amplifier, however, worked with less power under *Virtual Beam* compared to a real beam[29]. In order to

[28] *Virtual Beam* is the chosen nickname for this kind of test which was done for the first time with a real LLRF, pre-amplifier and cavity but a simulated beam.

[29] This is due to the beam and amplifier effects on the RF cavity. With a real beam, the amplifier injects power into the cavity; part of it will be given to the circulating beam and the other part will be dissipated in the cavity walls. The beam, therefore, tends to reduce the cavity voltage as it absorbs power and the LLRF system counteracts this effect by increasing the amplifier power to keep the cavity voltage at the same level as it was without beam. Using a *Virtual Beam*, on the other hand, the amplifier only needs to provide the power which will be dissipated in the cavity walls as the beam effect is already simulated at the LLRF output. This makes the amplifier work with less power under a *Virtual Beam* compared to a real

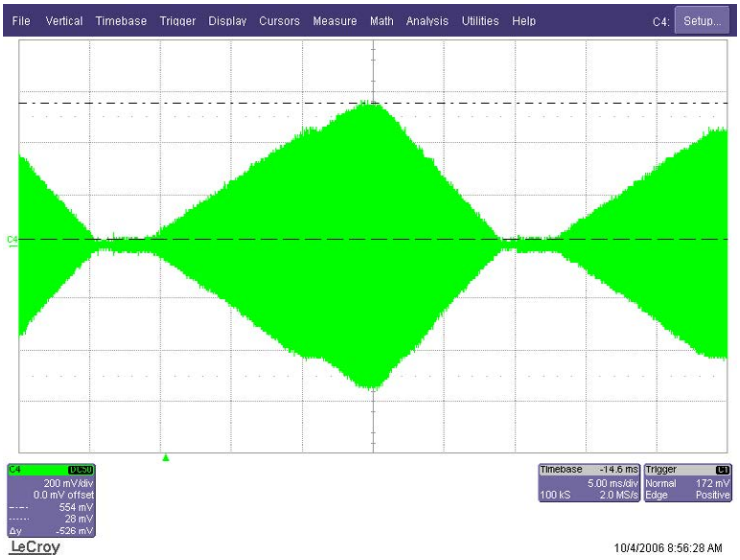

Figure 3.55: Measured cavity voltage in ramping mode with a dynamic range of 26 dB

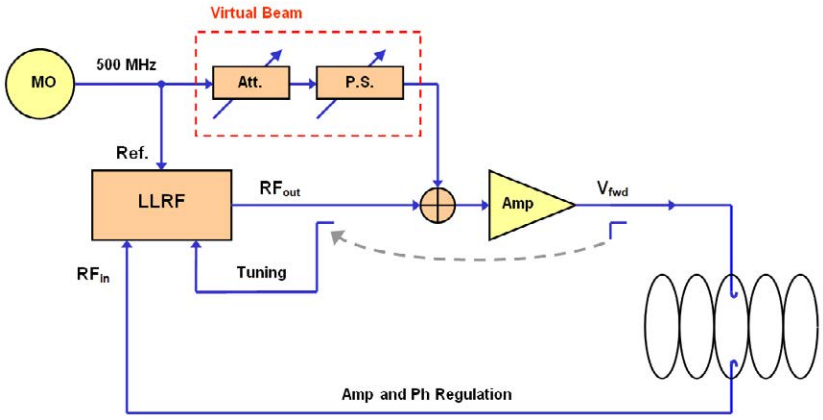

Figure 3.56: Simplified schematics of the setup for amp/ph regulation with a *Virtual Beam*

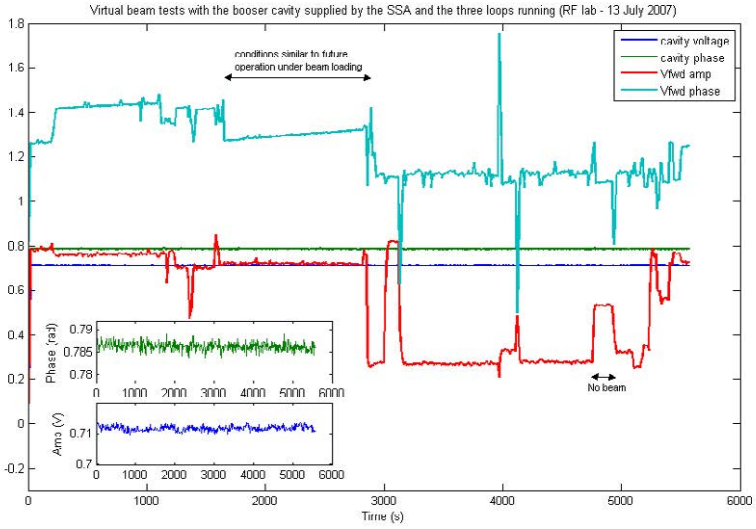

Figure 3.57: Results of the *Virtual Beam* tests with the ALBA booster cavity and a 600 W RF amplifier during 1.5 hours; The two waveforms with little variations are the phase (upper) and amplitude (lower) of the cavity voltage. The two small windows on the lower left show these two waveforms with more details (the height of these windows correspond to the ALBA stability requirements). The two waveforms with large variations are the phase (upper) and amplitude (lower) of the LLRF output.

make the tuning loop work correctly, though, a small change had to be made in the loop configuration; Instead of the cavity forward voltage, the output of the LLRF was fed into the *Tuning/FF Unit*. This is because for the tuning loop, the forward voltage should be measured 'before' the beam.

The system was put into operation for several hours with the IQ and tuning loops running continuously. While the loops were regulating the amplitude/phase of the cavity voltage and its resonant frequency, the amplitude and phase of the *Virtual Beam* were changed to evaluate the performance of the loops. The loop data was then measured by a slow data acquisition system. FIG. 3.57 shows the history of the signals measured during 1.5 hours.

As the figure shows, the amplitude and the phase of the cavity voltage (the two waveforms with no variations) always remained at their set values even though large changes were imposed on the amplitude and phase of the *Virtual Beam*. This can be understood from the large amplitude and phase variations of the LLRF output (the two waveforms with large changes) counteracting the *Virtual Beam* effect. The slow ramps on the LLRF output were due to the

beam, but from a LLRF perspective, the two systems are identical.

cavity warming and the sharp peaks were due to the tuners movements. As the figure shows, none of these disturbances showed up on the cavity voltage thanks to the regulation loops.

The figure also compares the LLRF output voltage without beam to the one simulating a real beam[30]. The difference between the LLRF output voltage in these two cases is the additional voltage that the LLRF system has to provide to compensate the beam loading effect. The two small windows on the bottom left show the amplitude and phase of the regulated cavity voltage with more details. The height of these windows corresponds to 1% and 1° approximately verifying that the actual LLRF stability was well within the specifications.

3.4 Summary and concluding remarks

This chapter has discussed the design, simulation, implementation and experimental results of the ALBA ALLRF system. The specifications of the ALBA RF/LLRF systems are given followed by a description of the ALLRF design for the amplitude and phase loops. In order to simulate the performance of the I and Q loops under beam loading, a baseband-equivalent model for the cavity has been developed in MATLAB-Simulink with the advantage of significantly improving the simulation speed compared to the conventional models available in the literature. Moreover, as this model is based on the cavity equations developed in Chapter 2, it also takes into account the influence of the input coupler on the cavity impedance mismatch, hence provides an effective and reliable test bench for transient-time LLRF simulation and analysis. The model is then applied to the ALBA RF/LLRF to study the effect of the system start-up and phase/delay errors on the performance of the feedback loops under beam loading.

In the continuation, the design of the main circuits comprising the complete ALLRF system has been discussed along with a description of how these circuits are put together to assemble the ALLRF units. Also, the design of the Graphical User Interface of the ALLRF is presented with an explanation of the important LLRF parameters to be monitored and controlled from the ALBA control room. Finally, the experimental results obtained at the CELLS and ELETTRA high power RF laboratories are given. Various types of tests have been done at low and high RF power levels to check the performance of the LLRF loops, hence assert its suitability for the ALBA machine. In the case of amplitude and phase regulation, for example, the results verify the ability of the ALLRF to compensate ripples up to 10 kHz and above in addition to having a short settling time in the order of 20 μs. The ramping tests, on the other hand, show that a highly-linear response in a dynamic range larger than 26 dB is achievable for the cavity voltage. In order the check the ALLRF performance under a simulated beam, a controlled signal with f=500 MHz is added to the LLRF output. The amplitude and phase of this signal have been then adjusted so that

[30]In that case, the relative phase of the *Virtual Beam* with respect to the cavity voltage was adjusted so that it was equal to the ALBA *Synchroneous Phase*.

it simulates a real beam for the LLRF system. The results obtained from these tests, on one hand, have shown that amplitude and phase stabilities down to a fraction of 1% and 1° are achievable and on the other hand have proven that the ALLRF circuits have a large enough voltage range to counteract the beam loading effect without being saturated. Moreover, these tests can be very useful from a training point of view as they give a good insight on how the beam acts on the cavity field and how the ALLRF system should be operated under a real beam.

Chapter 4

DLLRF System for the ESS-Bilbao Linac

4.1 The ESS-Bilbao Linac

The pulsed ESS-Bilbao light-ion Linac which is jointly funded by the Spanish and Basque governments and planned to be built in Leioa (Spain) will consist of two ion sources for light ions such as a Penning trap source for negatively charged H^- and a proton source based upon the ECR[1] principle. The sources are meant to be able to generate beams of around 60 mA. Strong focusing into a four-vane RFQ[2] at present under detailed engineering studies, is then achieved by means of a four-solenoid LEBT[3] system, specifically designed to cater for multi-ion beams. Finally, a chopping device, still within conceptual design stages, will deliver beams into a DTL[4] similar to the one from CERN Linac-4 with an energy of up to 50 MeV[5]. In a second phase, this will be followed by two series of super-conducting double-spoke and triple-spoke cavities driven by several 2.8 MW Klystrons.

Applicationwise, the installation has been dimensioned in the first phase to host a 50 MeV neutron converter, rotating solid target, where neutron production takes place as the result of direct reactions with light nuclei, and several proton extraction lines devoted to experiments on materials processing, radiobiology or nuclear astrophysics.

The total Linac length is estimated at 125 m and the commissioning of the normal-conducting part (up to the end of the DTL) is foreseen for 2015. Fig. 4.1 shows simplified schematics of the normal-conducting part of the ESS-Bilbao linac comprising the ion source, the LEBT, the RFQ and the DTL.The

[1] Electron Cyclotron Resonance
[2] Radio Frequency Quadrupole
[3] Low Energy Beam Transport
[4] Drift Tube Linac
[5] Mega Electron Volt

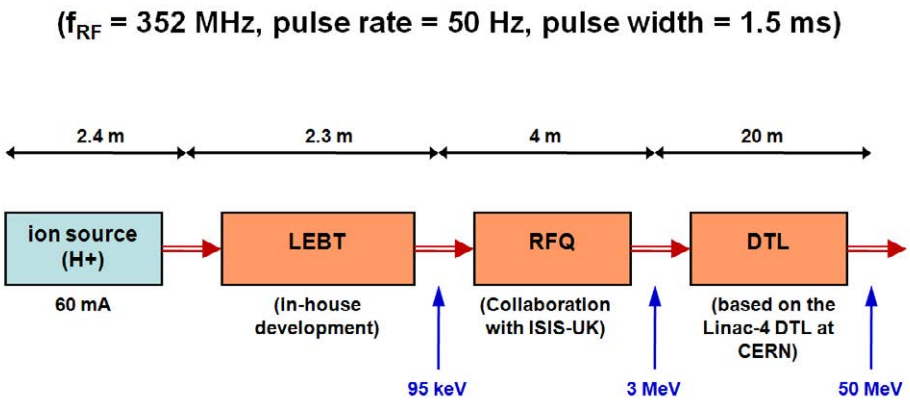

Figure 4.1: Simplified schematics of the normal-conducting part of the ESS-Bilbao linac

Linac will eventually be part of an accelerator research facility for fundamental and applied research using neutron and proton beams.

4.2 Design Description of the ESS-Bilbao DLLRF

An essential part of the Bilbao linac is its RFQ. Table 1 summarizes the main parameters of the ESS-Bilbao RFQ system which is being built in collaboration with RAL[6] - UK [76].

As part of this collaboration, a pulsed digital LLRF system has been designed and developed by the ESS-Bilbao RF group in collaboration with RAL to be used for the RAL FETS[7] and also the future ESS-Bilbao accelerating structures [73, 80].

In order to improve the formation of the beam, avoid an additional beam chopper and reduce operational costs, it is planned to pulse the ion source and the high power RF system. As the beam pulse will be narrower than the RF pulse, the RFQ field should have settled before the beam pulse enters the RFQ so that the beam sees the right voltage and phase. That puts new requirements on the dynamic range, bandwidth and transient response of the LLRF. The LLRF system should also provide a large phase margin to avoid loop instabilities in addition to being compact, modular and easy-to-operate.

LLRF systems for linacs with similar applications have been built in the past in several accelerator facilities. The most recent examples are SNS in the USA and J-PARC in Japan. In the implementation of the SNS LLRF, large effort has been made to keep the latency below 150 ns so that the required bandwidth can be achieved by an all-digital LLRF system. Also, mechanical

[6]Rutherford Appleton Laboratory
[7]Front End Test Stand

Table 4.1: Tentative list of the properties of the ESS-Bilbao RFQ system

Parameter	Value	Unit
RF Frequency	352.209	MHz
RF pulse rate (max)	50	Hz
RF pulse width (max)	1.5	ms
Peak Klystron power	2.8	MW
Beam energy at the RFQ entrance	95	keV
Beam energy at the RFQ exit	3	MeV
Emmitance	0.2π	mm.mrad
Unloaded Q	9000	
Ratio of Copper to beam power	5 to 1	
Amplitude stability	± 0.5	%
Phase stability	± 0.5	$^\circ$
Settling time	≤ 100	μs

modes of the superconducting cavities have been successfully damped out using AFF[8] compensation resulting in significant decrease of the amplitude and phase errors [82]. In the case of J-PARC, a digital LLRF system utilizing feedback and feed-forward control has been made and tested with amplitude and phase stabilities of 0.3% and 0.2° under beam loading [83].

The LLRF system described herein consists of an analog front-end for direct RF conversion to baseband IQ (and vice versa) and an FPGA unit running error compensation and control algorithms. LLRF systems based on the same or similar design principle have been developed for PEP-II B Factory [99], S-DALINAC-Darmstadt [100], SCSS [101] and successfully put into operation, even for the very high RF stability requirements of XFELs [102]. As the accuracy of the probe voltage conversion to I/Q plays an important role in the RF stability, errors associated with the use of analog IQ demodulators have been identified and some FPGA algorithms have been proposed to compensate them, thus meeting the RF stability requirements. Details of the LLRF design for amplitude/phase regulation and cavity tuning are given followed by a description of how the feedback loop parameters should be set to achieve the best performance. Also, a baseband-equivalent model in MATLAB-Simulink is presented to study the time-domain performance of the feedback loop under beam loading in the presence of phase and delay errors. These simulation results and the practical tests performed with a pill-box cavity and an RFQ cold model confirm the ability of the LLRF system to meet the requirements in addition to having a linear response, a configurable bandwidth and an excellent phase margin for loop stability. Furthermore, the effect of the unwanted resonant modes of the ESS-B accelerating structures on the stability of the feedback loop is studied and the LLRF considerations to avoid such instabilities are described verifying that due to the frequency separation of these modes, the klystron bandwidth and the adopted control scheme, such instabilities are very unlikely.

[8] Adaptive Feed Forward

4.2.1 RF Conversion to Digital I and Q

As it was previously mentioned, IQ demodulation is a common and useful method which is widely used in charged particle accelerators for RF field regulation or diagnostics purposes. As an IQ demodulator can precisely measure RF phase in addition to amplitude, it can also be used for cavity tuning purposes, which is based upon RF phase measurements. In a DLLRF system, usually, the cavity probe voltage is converted into digital I and Q components and fed into a digital processor, being typically an FPGA, for operations such as low-pass filtering, phase-shifting, feed-forward control, PID regulation etc. The output I and Q signals are then up-converted using an IQ modulator or a mixer generating the drive signal of the RF amplifier supplying the RF cavity. The I and Q feed-back loops formed in this way then regulate the amplitude and phase of the cavity voltage.

When high RF stabilities are required, the accuracy of the probe voltage conversion to I and Q becomes of great importance as any errors acting on it will have a direct effect on the cavity field without being compensated by the feedback loop. Methods for RF conversion to digital I (In-phase) and Q (Quadrature-phase) components in baseband can be generally classified in three categories:

In the first category, the RF signal ($f = f_{RF}$) is mixed with a reference signal with fixed amplitude and frequency ($f = f_{RF} - f_{IF}$) and low-pass filtered to suppress the upper sideband generated during the mixing process. The obtained signal ($f = f_{IF}$) then conveys, within its bandwidth, the amplitude and phase information originally present on the RF signal. The principal reason for this down-conversion is to reduce the RF signal frequency so that it can be conveniently sampled and converted to digital. In the next stage, the IF signal is sampled by an ADC running at $f = 4f_{IF}$ (or a sub-multiple of it) generating a digital stream of I, Q, -I, -Q... This stream, after being demultiplexed and sign-corrected, will finally result in two data streams being the I and Q components of the RF signal [85]. This method has been widely used in the past years and has become standard for digital LLRF. An extension of this method has been adopted at J-PARC where up to 4 different intermediate frequencies are mixed together and sampled by one ADC with the advantage of reducing the number of required ADC channels [86]. The main drawback of sampling at IF is the need for a precise and complex timing system generating the clock signals needed for down-conversion and ADC sampling. As these clocks must be in tight synchronization, they are usually generated using a PLL (Phase Locked Loop) or a DDS (Digital Data Synthesis) adding to the total cost and complexity of the LLRF system. A few limitations will be imposed on the clock signals generated in this way: The f_{IF} should be determined taking the sample rate of the ADC into account. As this is usually much smaller than the f_{RF}, it implies that the f_{RF} and $f_{RF} - f_{IF}$ should be relatively close, making the generation of $f_{RF} - f_{IF}$ from f_{RF} more complex due to filtering issues. On the other hand, f_{IF} should be large enough so that the required LLRF bandwidth can be achieved. The other drawback of this method is that the generated clocks are

not reconfigurable as changing any of the clock frequencies will probably imply modifying part of the hardware of the timing system.

The second category includes methods in which sampling is done directly on RF without down-conversion to IF. Direct sampling has been tested for the superconducting cavities of the ILC (International Linear Collider) with RF frequency of 1300 MHz, sampling frequency of 270.83 MHz and stability requirements of 0.3% and 0.3° [87]. The I and Q signals are obtained by integrating the sampled values over several RF periods using a trigonometric function [88, 89]. Although sampling in RF has advantages such as increasing the measurement bandwidth and eliminating errors caused by the RF-IF conversion, it still needs precise clock generation and careful choice of the sampling rate so that a reasonable compromise between latency and error can be made [88]. Moreover, such a scheme needs a very fast data acquisition system (both ADC and FPGA) with extremely low clock jitter.

Finally, the third category consists of methods in which sampling is done in baseband. This implies using an analog IQ demodulator for RF conversion to baseband and arbitrarily sampling the I/Q signals at a rate large enough to achieve the required bandwidth. Although sampling in baseband requires two ADC channels for each RF measurement (instead of one for sampling in IF/RF), it is advantageous because of its low latency and simplicity of the front-end and its timing system. With this scheme, the only synchronized clock for down-conversion is either f_{RF} or $2f_{RF}$ depending on the IQ demodulator type. This method has been used at LHC-CERN using a passive IQ demodulator (Merrimac IQG-20E-400) for the compensation of the transient beam loading (revolution frequency sidebands of the RF carrier) where compensation of such frequency cannot be done by the main feedback loop (digital) due to its limited bandwidth [90]. Another implementation has been done at J-PARC where a local analog loop has been used as a complement to the main digital loop to compensate ripples of the HVPS (High Voltage Power Supply) supplying the klystron [84]. Nevertheless, analog IQ demodulation and sampling at baseband has been rarely used in modern LLRF systems for the main feedback loop due to some potential errors such as noise, DC offsets and amplitude/phase imbalance of the I and Q channels.

For the LLRF system of the future ESS-Bilbao RFQ, it has been decided to sample at baseband after simultaneous IQ demodulation and down-conversion due to the simplicity and versatility of this method. However, in order to make sure that the LLRF system will be able to meet the requirements, the IQ data has been further processed in an FPGA to compensate the errors mentioned earlier. The adopted algorithms for these error compensations give better results when applied to modern IQ demodulators which are normally available in the form of RF ICs as they provide the user with less linearity errors and more flexibility in choosing the dynamic range, gain, bandwidth etc. compared to the conventional IQ demodulators which are usually available as passive devices with relatively high insertion losses ([14] and [91] are examples of the first and second types respectively).

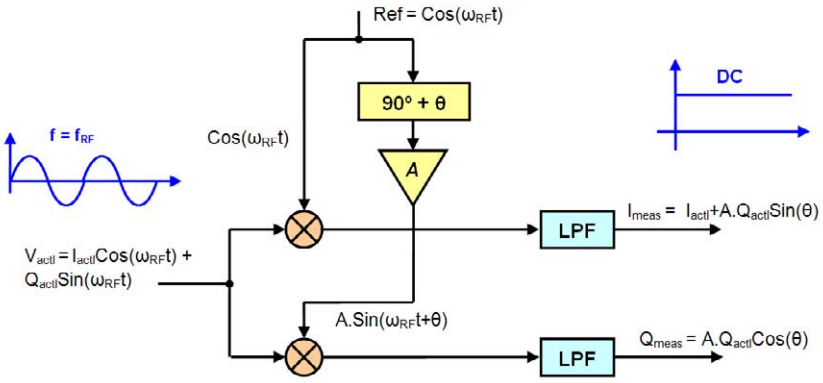

Figure 4.2: Simplified block diagram of an analog IQ demodulator; A and θ represent gain and phase imbalances of the Q channel with respect to the I channel.

4.2.2 Analog IQ demodulator errors

A few effects usually contribute to the accuracy degradation of an analog IQ demodulator, being: gain/phase imbalance between the I and Q channels, DC offsets, noise and gain variations with temperature. Among these, the first two (gain and phase imbalances) are usually more severe as they are internal to the IQ demodulator while the later three can be compensated fully or partially using appropriate FPGA algorithms counter-acting those effects. The datasheet of the AD8348 IQ demodulator which is used in the current design, for example, specifies maximum IQ gain and phase imbalances of ± 0.3 dB and $\pm 0.7^\circ$ respectively [14] resulting in worst-case amplitude and phase errors equal to $\pm 1.75\%$ and $\pm 1^\circ$ which would be unacceptable. In order to minimize the effect of these imbalances on the accuracy of the probe voltage measurement, the phase shifters in the feedback loop are adjusted so that in normal operation, when the cavity phase is desired, the phase of the IQ demodulator input is as close as possible to zero degree (or equivalently any multiple of 90 degrees) as explained in the following section. Then, the gain/phase imbalances will only have negligible effects on the transient response (i.e. before the signals settle) but the steady-state response will be immune to such imbalances improving the IQ demodulator linearity with respect to the input level. In the following, we will also briefly explain the algorithms which were adopted to minimize the effect of the other types of errors mentioned earlier. Given that most of the signal processing of the LLRF system is done by an FPGA, these improvements are just a matter of adding some more lines to the FPGA code.

Gain and phase imbalances

Fig. 4.2 shows simplified block diagram of an analog IQ demodulator.

Here, A and θ are the gain and phase imbalance of the Q channel with respect to the I channel respectively. If we represent the actual (i.e. the input) signal in baseband by (I_{actl}, Q_{actl}), the relation between the measured signal (i.e. (I_{meas}, Q_{meas})) to the actual one can be established as shown in EQ. 4.1 and EQ. 4.2.

$$V_{actl} = I_{actl}.Cos(\omega_{RF}t) + Q_{actl}.Sin(\omega_{RF}t) \tag{4.1}$$

$$\begin{aligned} V_{meas} &= I_{meas}.Cos(\omega_{RF}t) + Q_{meas}.Sin(\omega_{RF}t) \\ &= I_{actl}.Cos(\omega_{RF}t) + AQ_{actl}.Sin(\omega_{RF}t + \theta) \end{aligned} \tag{4.2}$$

where V_{actl} is the actual RF input and V_{meas} is the RF-equivalent of the measured input.

EQ. 4.2 can be rewritten as the following showing how the measured signal is related in baseband to the actual one through the A and θ parameters:

$$\begin{aligned} V_{meas} &= [I_{actl} + AQ_{actl}Sin(\theta)].Cos(\omega_{RF}t) \\ &+ AQ_{actl}Cos(\theta).Sin(\omega_{RF}t) \end{aligned} \tag{4.3}$$

$$\begin{aligned} I_{meas} &= I_{actl} + AQ_{actl}Sin(\theta) \\ Q_{meas} &= AQ_{actl}Cos(\theta) \end{aligned} \tag{4.4}$$

$A = 1$ and $\theta = 0^\circ$ would therefore be the necessary conditions for an error-free measurement resulting in $(I_{meas}, Q_{meas}) = (I_{actl}, Q_{actl})$.

The amplitude and phase of the measured signal $(|V_{meas}|, ph(V_{meas}))$ can be calculated as the following:

$$\begin{aligned} |V_{meas}| &= \sqrt{(I_{actl} + AQ_{actl}Sin(\theta))^2 + (AQ_{actl}Cos(\theta))^2} \\ ph(V_{meas}) &= \arctan\frac{AQ_{actl}Cos(\theta)}{I_{actl} + AQ_{actl}Sin(\theta)} \end{aligned} \tag{4.5}$$

At $ph(V_{actl}) = 45^\circ$ (i.e. $I_{actl} = Q_{actl} = \frac{\sqrt{2}}{2}|V_{actl}|$), this will result in:

$$\begin{aligned} ph(V_{actl}) &= 45^\circ \Longrightarrow \\ |V_{meas}| &= |V_{actl}|\sqrt{\frac{1}{2} + \frac{A^2}{2} + ASin(\theta)} \end{aligned} \tag{4.6}$$

In order to measure the gain imbalance of the IQ demodulator, the phase of the RF input was once set to 0° and another time to 90° with the same amplitude. The gain imbalance A was calculated from the relative value of the two measurements (i.e. $\frac{|V90|}{|V0|}$). The results of these measurements are shown in Fig. 4.3 for several input levels.

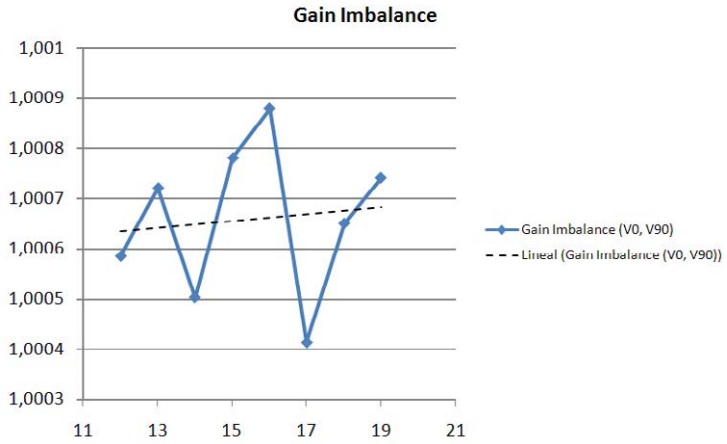

Figure 4.3: Measured gain imbalance with several input levels; the horizontal axis is the input voltage in mV_{RMS} and the vertical one is the measured gain imbalance of the Q channel with respect to the I channel.

The mean value (i.e. $A = 1.00065$) which is considered as the gain imbalance results in an error of 0.065% in the measured amplitude.

In order to measure the phase imbalance, while the amplitude of the input signal was constant, its phase was changed to sweep the complete 2π period and the amplitude of the measured signal was recorded. Having $A = 1.00065$, the phase imbalance was calculated at $ph(V_{actl}) = 45°$ using EQ. 4.6 resulting in $\theta = 0.293°$. Fig. 4.4 shows the results of the amplitude measurements and compares them to the simulated ones obtained with these A and θ values.

As it can be seen in Fig. 4.4, the measured amplitude makes two complete oscillations in one period of the input phase. The phases corresponding to the zero crossings (i.e. $-90°$, $0°$, $90°$, $180°$) result in zero measurement errors due to gain and phase imbalances because at these points the information is carried only by either I or the Q channel while the other channel is at zero volt. The relative gain/phase imbalance of the I/Q channels will therefore play no role in the accuracy of the measurements. Likewise, the $-135°$, $-45°$, $45°$ and $135°$ points result in maximum measurement error as at these phases the information is equally shared between the I and Q channels.

Fig. 4.5 shows the linearity response of the IQ demodulator with the input phase set to $0°$ (optimum) and $45°$ (worst-case) and the input level covering all values from zero to the saturation level of the ADC. The maximum difference which occurs at the peak input level is 15 ADC counts corresponding to an amplitude error of 0.183% which is in agreement with the results shown earlier in Fig. 4.4.

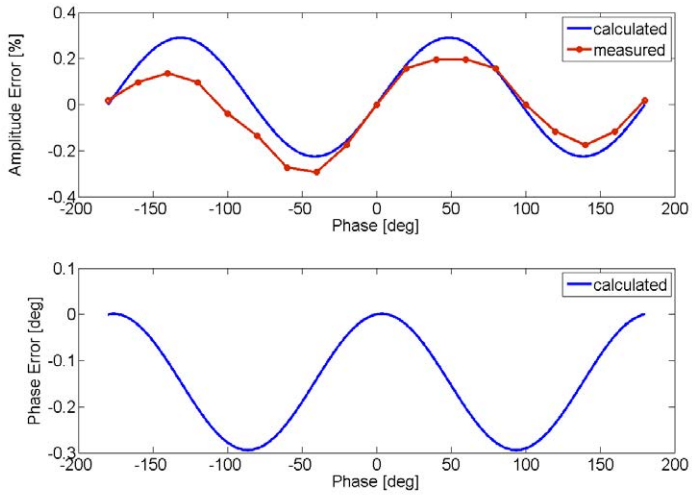

Figure 4.4: Top: comparison between the measured and simulated results of the amplitude error caused by the I/Q gain and phase imbalances, Bottom: simulated results of the phase error caused by the same gain and phase imbalances.

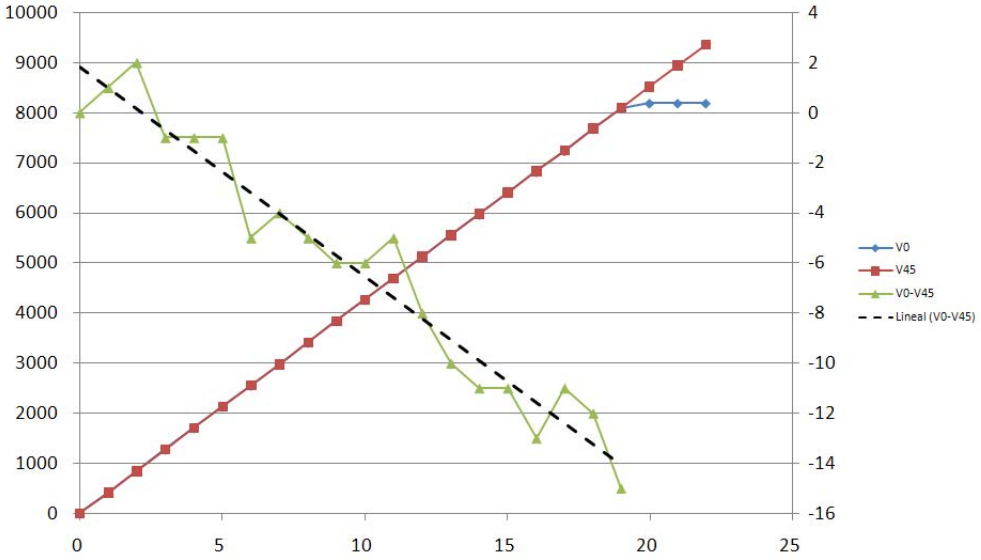

Figure 4.5: Comparison between the IQ demodulator linearity with input phase set to 0° and 45°. The horizontal axis shows the input voltage in mV_{RMS}. The vertical axis on the left shows the ADC counts corresponding to the two measurements and the one on the right the difference between the two waveforms.

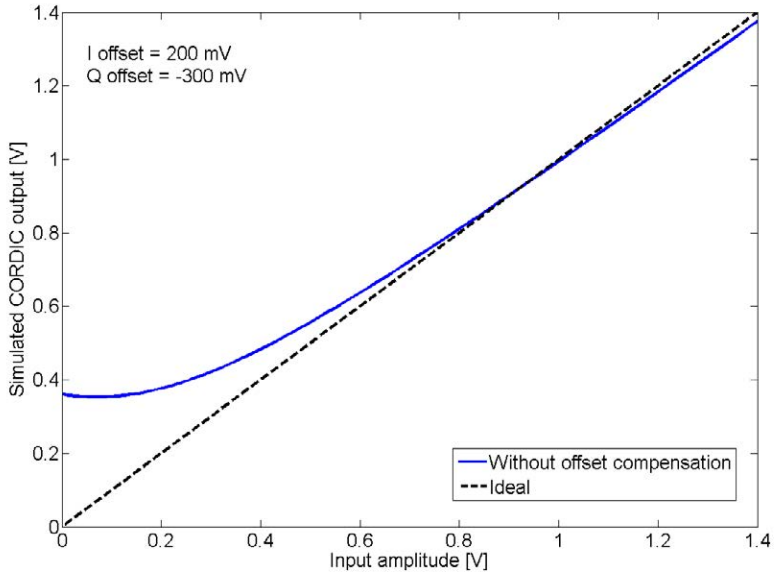

Figure 4.6: Simulated linearity response of the IQ demodulator with I and Q offsets of 200 mV and -300 mV respectively and input phase of 45°.

DC offsets

DC offsets of the I and Q outputs can cause significant non-linearities in the IQ demodulator response if not compensated. The DC offsets of the AD8348 can be as large as ±300 mV in a dynamic range of ±1400 mV. Fig. 4.6 shows the simulated linearity response of the IQ demodulator with I and Q offsets of 200 mV and -300 mV respectively.

As the LLRF system operates in pulsed mode, the voltage that appears on the I/Q channel during the no-pulse period gives the exact value of the overall DC offset (i.e. sum of the IQ demodulator and ADC offsets) of the corresponding channel. These values are then saved in a buffer which is updated in each RF pulse and subtracted from the measured I and Q values to compensate for the DC offsets. As another option, the DC offsets can be manually adjusted using the LLRF GUI (Fig. 4.7). The maximum variation of the offsets during a period of 100 hours was recorded at 5 ADC counts corresponding to maximum error of 0.085% in amplitude.

Noise

The noise of the I and Q signals without shielding was measured at 10 mV_{pp} approximately in a dynamic range of ± 1400 mV. This noise is then reduced significantly in several stages of the LLRF system such as the analog filters of the

front-end unit, averaging blocks in the FPGA and the integrator part of the PI. The cavity noise in the end is dominated not by the IQ demodulator/modulator noise but the RF generator (RF reference) noise as it is shown in the practical results section. In order to protect the electronics against environmental noise, proper enclosures have been designed and built to be used for the final installation.

Gain variations with temperature

The AD8348 includes a VGA (Variable Gain Amplifier) whose gain is controlled by an external voltage [14]. Although care was taken to provide this voltage by a reliable source, it was observed that the gain still had some variations due to temperature fluctuations affecting the regulated cavity voltage (see Fig. 4.35). In order to minimize the gain variations, in the final system setup, it is planned to regulate the electronics temperature and/or fine-tune the demodulator gain based on the measured temperature to compensate these variations.

4.2.3 Amplitude and Phase Loops

Fig. 4.7 shows the simplified schematics of the IQ loops for amplitude and phase regulation.

In this design, an analog IQ demodulator is used to convert the measured cavity voltage into baseband I and Q. The I and Q signals are in the next stage sampled by two 14-bit 104 MSPS ADCs and fed into a model-based Virtex-4 FPGA for the subsequent signal processing. In the first stage of the FPGA program, two averaging blocks acting on the last 30 samples are used to filter out the high frequency noise. The I/Q signals are then offset-compensated (either manually or automatically) and fed into the first phase shifter. This is basically a rotation matrix acting on the rotation angle of the IQ vector by a user-controlled amount. Then, the I/Q signals are compared to their reference values and the I and Q errors (i.e. the difference between the real and the reference I/Q) are fed into their corresponding PI regulators with controllable P and I gains from the LLRF GUI. At the output of the two regulators, a virtual switch is used to operate the system either in open-loop or closed-loop mode. For closed-loop operation, the switch is closed, therefore all the blocks are active and the cavity field is regulated by the two PIs. For open-loop operation, the switch is opened to break the feedback loop and the amplitude and phase are controlled by the Iff and Qff inputs and a second phase shifter which gives the possibility to further rotate the IQ vector. This mode can be particularly useful for test purposes and for making sure that the regulation loops will be stable before they are actually closed. Moreover, by applying appropriate Iff and Qff in addition to the Iref and Qref inputs, one can further improve the step response or compensate for predictable errors such as the beam if needed. At the output stage, the I and Q signals are converted to analog using two 14 bit DACs with maximum sampling rate of 480 MSPS (interpolating). These signals then serve

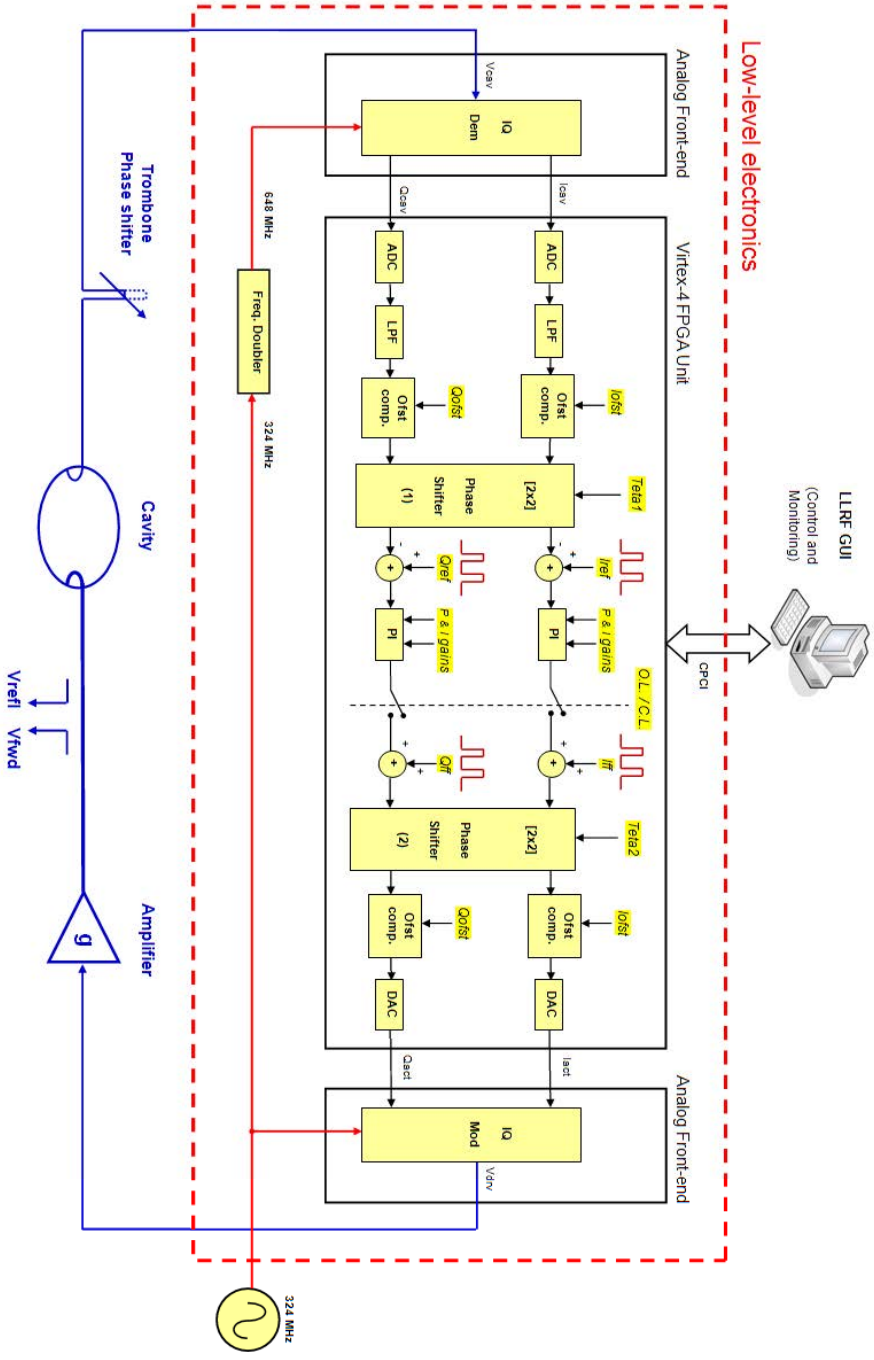

Figure 4.7: Simplified block diagram of the FPGA program for amplitude and phase regulation; The parameters highlighted in yellow and marked as *italic* are set from the control terminal.

as the baseband inputs for the IQ modulator driving the pre-amplifier of the Klystron.

For normal operation in closed-loop mode, the fractional part of the loop delay must be compensated to avoid loop instability. If, for example, the total loop delay from the LLRF output along the RF transmitter, the RFQ and back to the LLRF is 512.3 times the RF period, the phase shifters should be adjusted so that the total phase shift they provide compensates 0.3 RF periods (i.e. -108° of phase shift). Then, the total loop delay will be equivalent to 512 RF periods and the two PI controllers see the IQ vector with correct phase. If the phase shifters are not properly adjusted, the response of the I and Q loops will not be the same and some degradations in the transient response might be seen as well. In the extreme case, if the phase error exceeds the phase margin, the loops will become unstable.

The procedure for the adjustment of the phase shifters is as follows: First, the LLRF system is operated in open-loop mode and the Iff and Qff are set so that $\arctan(\frac{Qff}{Iff})$ corresponds to the desired cavity phase for beam acceleration. Then Phase Shifter (2) is adjusted so that the actual cavity phase is equal to the set value. In the next step, the trombone phase shifter is adjusted so that the read-back cavity phase at the input of Phase Shifter (1) becomes as close as possible to zero degree. Finally, Phase Shifter (1) is adjusted so that the phase at its output (i.e. the input for the two comparators) is the same as the one set by the feed-forward inputs. Having the three phase shifters so adjusted indicates the fractional part of the loop delay is correctly compensated, the phase corresponding to the I/Q set values is the same as the actual cavity phase and the IQ demodulator works at zero input phase in steady state conditions regardless of the voltage amplitude; a condition needed to minimize the effect of the gain and phase imbalance on the regulated cavity voltage as mentioned earlier. Assuming that the loop gain is not too high, the feedback loop can then be closed without loop instability risk. In closed-loop mode, the cavity can be driven only by the reference inputs (Iref and Qref inputs shown in Fig. 4.7) or these inputs in combination with the feed-forward set values. In both cases, the two PI regulators guarantee that the steady-state cavity voltage will be the same as the reference one.

4.2.4 Tuning Loop

Fig. 4.8 shows the schematics of the tuning algorithm which is also based on IQ demodulation.

In this case, two IQ demodulators are used to convert the measured forward and probe voltages to baseband. These signals are then sampled and fed into the FPGA where CORDIC blocks are used to calculate the phase difference between the two RF signals (The FPGA and the IQ demodulator for probe voltage measurement in the tuning loop are physically the same as the ones used for the amplitude and phase loops). RFQ tuning is done by keeping the phase difference as close as possible to its reference where the reference phase is the one giving minimum reflected power from the RFQ in the presence of

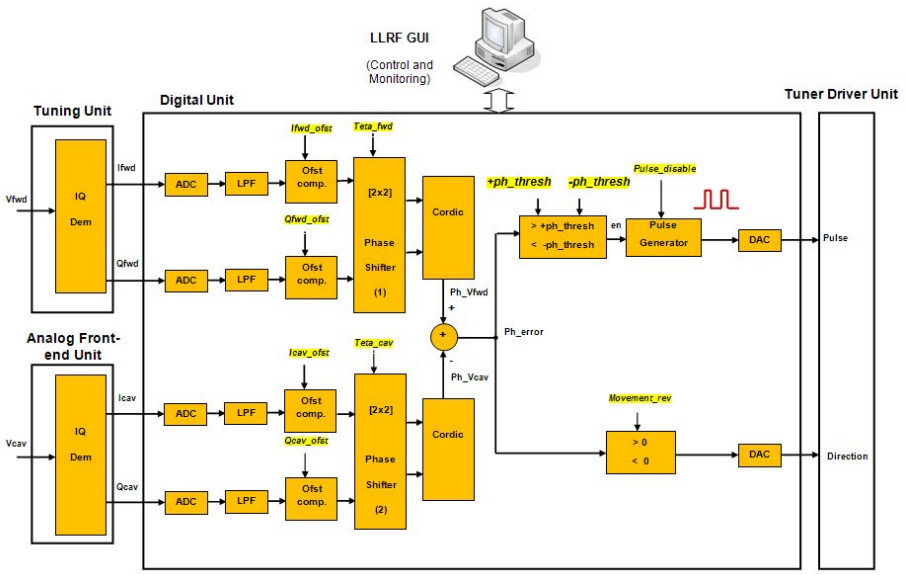

Figure 4.8: Simplified block diagram of the FPGA program for cavity tuning; The parameters highlighted in yellow and marked as *italic* are set from the control terminal.

the beam. This is done by moving the RFQ tuner inward/outward if the phase error (i.e. the difference between the actual phase and the set value) exceeds the upper or the lower thresholds defined by $(+ph_{thresh}, -ph_{thresh})$. If that happens, the tuning loop moves the tuner in the right direction until the error enters the $(+ph_{thresh}, -ph_{thresh})$ again and then leaves the tuner at that position until the next time the error exceeds any of the thresholds. Similar to the amplitude and phase loops, two phase shifters are used in the FPGA to rotate the IQ vectors representing the forward and probe voltages (See Fig. 4.8). By properly adjusting them one should satisfy the following two requirements simultaneously:

1. When the RFQ is tuned (i.e. minimum reflected power), the read-back phase of the forward and RFQ voltages are equal.

2. When the RFQ is tuned, these two phases are as close as possible to zero.

The first condition is required for making sure that regulating the phases to be equal corresponds to having minimum reflected power. The second condition is needed to make sure that moving the tuner from one extreme to the other does not cause any phase jump from +180° to -180° or vice versa in the CORDIC blocks as that can make the tuner move in the wrong direction. This is not an strict requirement though as any phase in the ±30° range would also be acceptable provided that the two phases are equal.

In order to prevent the tuner from an early wear-out due to continuous movement in pulsed operation, the tuning loop is only activated during the pulse after the RFQ phase has settled.

4.3 LLRF simulation in MATLAB-Simulink

Looking at the RFQ from a LLRF perspective, the operating mode can be characterized by its resonant frequency ω_0 and quality factor Q_0; therefore it can be modeled by a RLC circuit. The input coupler is modeled by a step-up transformer where the coupling factor β specifies the impedance matching between the amplifier and the operating mode. Fig. 4.9 shows the baseband-equivalent model of the feedback loop comprising the RFQ, the LLRF and the amplifier in MATLAB-Simulink. This model can be used to study the time-domain performance of the loop where all signals (including the RFQ voltage) are translated to baseband. The model then simulates the envelope of the RF signals (without RF carrier) with the advantage of significantly improving the simulation speed compared to the combined RF-baseband model.

Assuming the drive frequency is the same as the RFQ resonant frequency (i.e. $\omega_{RF} = \omega_0$) the relation between the RFQ voltage V (referred to the primary side) and the amplifier current I presented earlier in EQ. 3.9 can be simplified as the following set of differential equations [81]:

$$\begin{aligned} 2Q_0\frac{dV_i}{dt} + (\beta+1)\frac{dV_q}{dt} + (\beta+1)\omega_{RF}V_i &= Z_0\omega_{RF}\beta.I_i \\ 2Q_0\frac{dV_q}{dt} - (\beta+1)\frac{dV_i}{dt} + (\beta+1)\omega_{RF}V_q &= Z_0\omega_{RF}\beta.I_q \end{aligned} \tag{4.7}$$

Where the i and q subscripts denote the in-phase and quadrature-phase component of the relevant variable respectively. These differential equations can be represented in MATLAB-Simulink as a MIMO (Multi Input Multi Output) system using their equivalent transfer functions shown in Fig. 4.10.

Fig. 4.11 shows the detailed model of the phase shifter simulating the overall phase shift introduced by the three phase shifters shown in Fig. 4.7.

In the simulations, the RF frequency was set to 352 MHz, the unloaded quality factor Q_0 was 9000 and the coupling factor β was set to 1. The gain of the RF amplifier (including the trans-conductance due to voltage-to-current inversion) was assumed to be 50, the total loop delay was set to 500 RF periods and the voltage attenuation caused by the pickup loop was assumed to be 1e-4. The P and I gains were adjusted by trial and error until a satisfactory step response was achieved. With these parameters and assuming a 50 Ω system, setting the reference I (I_{ref}) to 1 V results in 1 MW of peak power in the RFQ.

Fig. 4.12 shows the simulated step response of the loop under beam loading with several values of phase error. Loop instability occurs when the error exceeds $\pm 70^\circ$ marking the phase margin of the system.

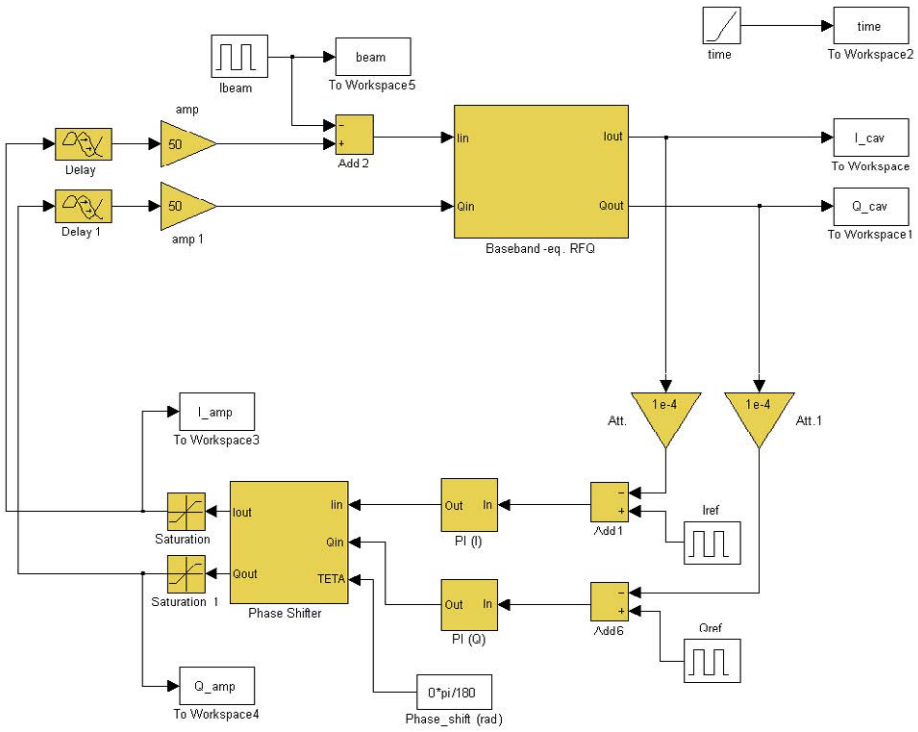

Figure 4.9: Baseband-equivalent model of the feedback loop including the RFQ, the LLRF and the RF amplifier; the model simulates the envelope of the signals in time domain with the advantage of significantly reducing the simulation time compared to the combined RF-baseband model.

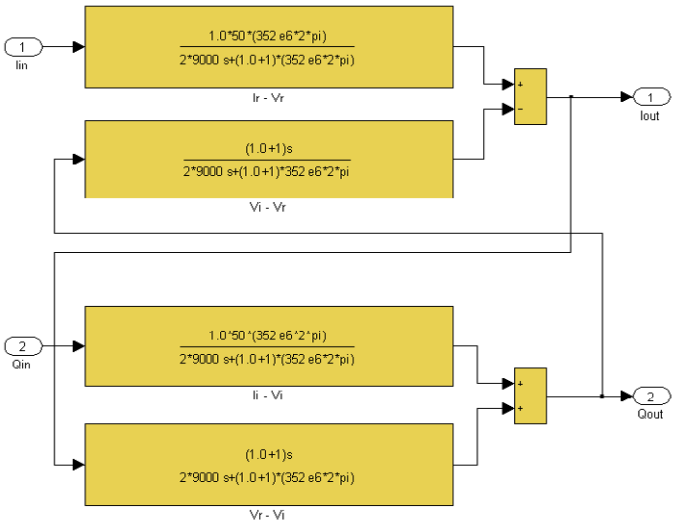

Figure 4.10: Baseband-equivalent model of the RFQ represented as a MIMO system in MATLAB-Simulink

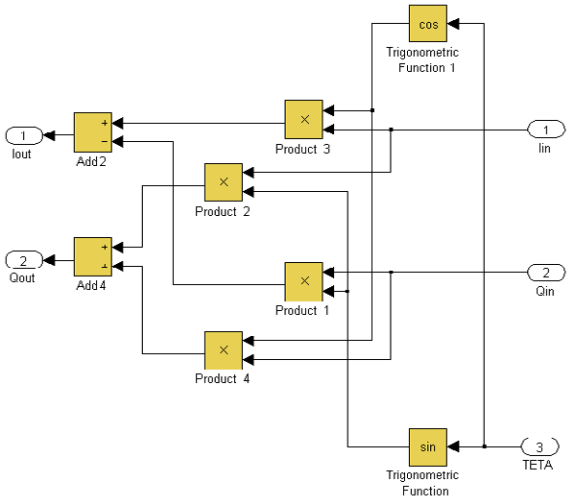

Figure 4.11: MATLAB-Simulink model of the phase shifter

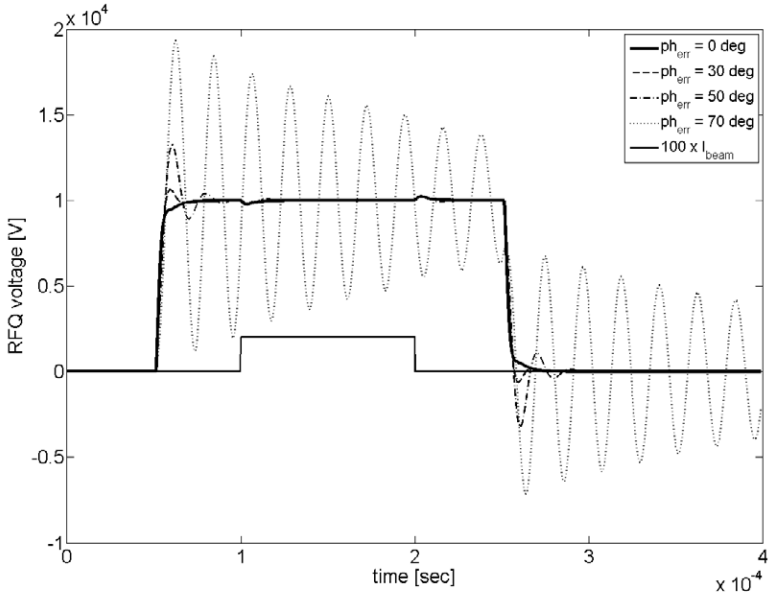

Figure 4.12: Simulated RFQ voltage (referred to the primary side) in closed-loop mode; the pulse width was reduced to 200 μs in the simulations, the beam pulse (not in scale) starts at t=100 μs and ends at t=200 μs.

4.4 Feedback loop instabilities due to other resonant modes

The stability of the LLRF loop could in principle be affected by possible resonant modes adjacent to the cavity main resonant mode. For instance, the effect of the unwanted resonant modes of the 9-cell superconducting RF cavities of the ILC on the feedback loop stability has been discussed in [103]. A more detailed study on this topic has also been done for the XFEL (European Free Electron Laser) which is based on the TESLA (Tera electron volt Energy Superconducting Linear Accelerator) technology [104]. In both cases, the control scheme is based on high-gain proportional controllers so that the feedback loop can significantly suppress fast and non-predictive disturbances. This, however, makes the feedback stability a delicate issue as the other fundamental modes (such as $8/9\pi$ and $7/9\pi$) cause loop instabilities after the introduction of even a small proportional gain. In order to avoid such instabilities, low pass filters (in addition to well-adjusted digital notch filters in case of XFEL) have been used to suppress the difference frequencies of these modes with respect to the desired π-mode. Also, it has been shown that by increasing the delay of the sampled IF signal, the feedback loop goes through successive stable and unstable regions with an interval depending on the difference frequency of each fundamental mode with respect to the π-mode.

In this section, we study these issues and some arising LLRF considerations for the RFQ and the spoke resonators of the ESS-B Linac. First of all, it should be noted that the frequency separation of the operating mode to the nearest undesired resonant mode (known to be >8 MHz from the RFQ electromagnetic simulations and about 42 MHz from cold-model measurement on the double-spoke resonator) is much larger than the typical LLRF bandwidth (limited to a few hundred kHz by the averaging blocks in the FPGA). This, basically makes it impossible for such frequencies to circulate around the feedback loop, hence removes the risk of instabilities due to the other resonant modes. This statement is further reinforced by considering the klystron bandwidth (2 MHz at -1.5 dB [105]) also removing the possibility for such frequencies to get amplified and fed into the cavity.

Contrary to the XFEL and ILC, the adopted control strategy for the ESS-B cavities is based on moderate proportional and integral gains. At the start of each RF pulse, typically 30% - 50% of the drive voltage is provided by the proportional controller while the integral controller gradually increases its output (due to error accumulation) until the RF field reaches its desired level. The introduction of the integral controller (a zero-frequency pole in the transfer function) significantly increases the loop gain at low frequencies but still keeps it at moderate levels at higher frequencies. This not only improves the stability margins of the feedback loops (phase margin of $\pm 55^\circ$ as reported in the LLRF performance section) but also eliminates flat-top steady-state errors in pulsed operation. On the other hand, the design of the LLRF and the adjustment of the P/I gains are so that the feedback loop is able to remove the

highest-frequency disturbance (the 8 kHz ripples and the higher harmonics resulting from the IGBT switching of the klystron modulator as known by far) in addition to having the desired RF settling time (<100 μs).

Unlike the XFEL and ILC LLRF systems, increasing the digital delay in the current design does not make the feedback loop go through stable and unstable regions. This is because increasing the delay of the sampled baseband signal does not cause any phase shift in the resultant RF signal after IQ modulation, while changing the delay of the IF signal changes the phase of the resultant RF signal, hence, can make the loop unstable. In [103, 104] the feedback loop is reported to be made stable by introducing an appropriate digital delay. In our design, however, the loop is made stable by the proper adjustment of the phase shifters as explained in the LLRF Design Description section without imposing an additional delay on the feedback loop.

4.5 Implementation of the ESS-Bilbao DLLRF

The implementation of the ESS-Bilbao DLLRF was done in a modular way. Several units were designed and developed in house each having a certain task. That includes a *Power Supply Unit* generating the required supply voltages for the other LLRF units with very low noise and ripple, *RF Distribution Unit* generating reference RF for the IQ mod/dem, front-ends for the amp/ph and tuning loops and a *Driver Unit* for the cavity tuner. These units were installed in a standard 19 inch rack comprising the complete LLRF system, the prototype cavity and some measurement equipment for the tests. In this subsection, first, the implementation of the LLRF units is presented one by one followed by a brief description of the digital unit and the FPGA program. In the current version, the complete LLRF system is controlled by 27 input parameters which are accessible from the GUI. These parameters are divided into three categories depending whether they are used for the amp/ph loop, the tuning loop or both. The function and range of each of these parameters are then explained along with a description on how these parameters should be properly adjusted by the operator. The section concludes by a brief explanation of how the FPGA program should be generated in MATLAB-Simulink and compiled before being inserted into the cosim model.

4.5.1 LLRF unit design and implementation

LLRF rack

A 19-inch industrial rack with a height of 2 m has been used for the installation of the low-level electronics at the UPV/EHU RF lab. This rack accommodates the LLRF system comprising several units such as Power Supply, RF Distribution, Analog Front-end, Tuning, FPGA and Tuner Driver. The rest of the rack space has been used for some other equipment such as an RF signal generator, laptop computer, oscilloscope, etc. during the system development and test. FIG. 4.13

shows the LLRF rack with the units installed in it. Each of these units is explained in more details in the following subsections.

Power Supply Unit

The *Power Supply Unit* (3U) generates the required supply voltages ($\pm 5\ V$, $+12\ V$) for all the other LLRF units. These are linear type power supplies from Power-one with very low output noise and ripple. In the *Power Supply Unit* care was taken in order not to use switched-mode power supplies as they produce significant amount of high-frequency ripples and that consequently can degrade the short-term RF stability without being compensated by the LLRF. The output voltages are distributed to the other units via the six circular connectors mounted on the rear panel.

RF Distribution Unit

The output signal of the RF signal generator (*Master Oscillator*) is fed into the *RF Distribution Unit* with a typical level of 15 dBm. After frequency doubling and filtering, this unit distributes both f_{RF} and $2f_{RF}$ among the other units. While f_{RF} is needed for the IQ modulator, $2f_{RF}$ is used for the IQ demodulators included in the regulation loops and for RF diagnostics. The components for the implementation of the *RF Distribution Unit* are mainly purchased from Mini-circuits. The schematic view of this unit is shown in FIG. 4.15. FIG. 4.16 shows a picture of the interior of the *RF Distribution Unit*.

Analog Front-End Unit

This unit includes the electronics needed for RF-to-baseband and baseband-to-RF conversion. It is based on an AD8348 [14] Evaluation Board from Analog Devices for IQ demodulation, an in-house developed board based on AD8130 [15] to convert the I/Q outputs of the demodulator from differential to single-ended, another in-house developed board based on AD8132 [16] to convert from single-ended to differential and an AD8345 [17] Evaluation Board for IQ modulation[9]. The schematics of this unit is shown in FIG. 4.17. FIG. 4.18 shows the interior of the unit.

The cavity probe voltage (to be regulated by the LLRF) is fed into the *Analog Front-end Unit* via the *RFin* port. A gain-control input voltage should be provided for the IQ demodulator through the *Gctrl* port. As an alternative, the demodulator gain can be adjusted by the corresponding potentiometer and switch mounted on the demodulator board. This, however, is not the preferred manner of gain adjustment as potentiometers are in general sensitive to temperature variations. In the current configuration, one of the DAC channels is

[9]For the final DLLRF system, the IQ demodulator and the differential-to-single-ended converter board will be combined in a single board. Similarly, the IQ modulator and the single-ended-to-differential board will be combined. The new boards on one hand improve the shielding and on the other hand are optimized for the ESS-Bilbao RF frequency.

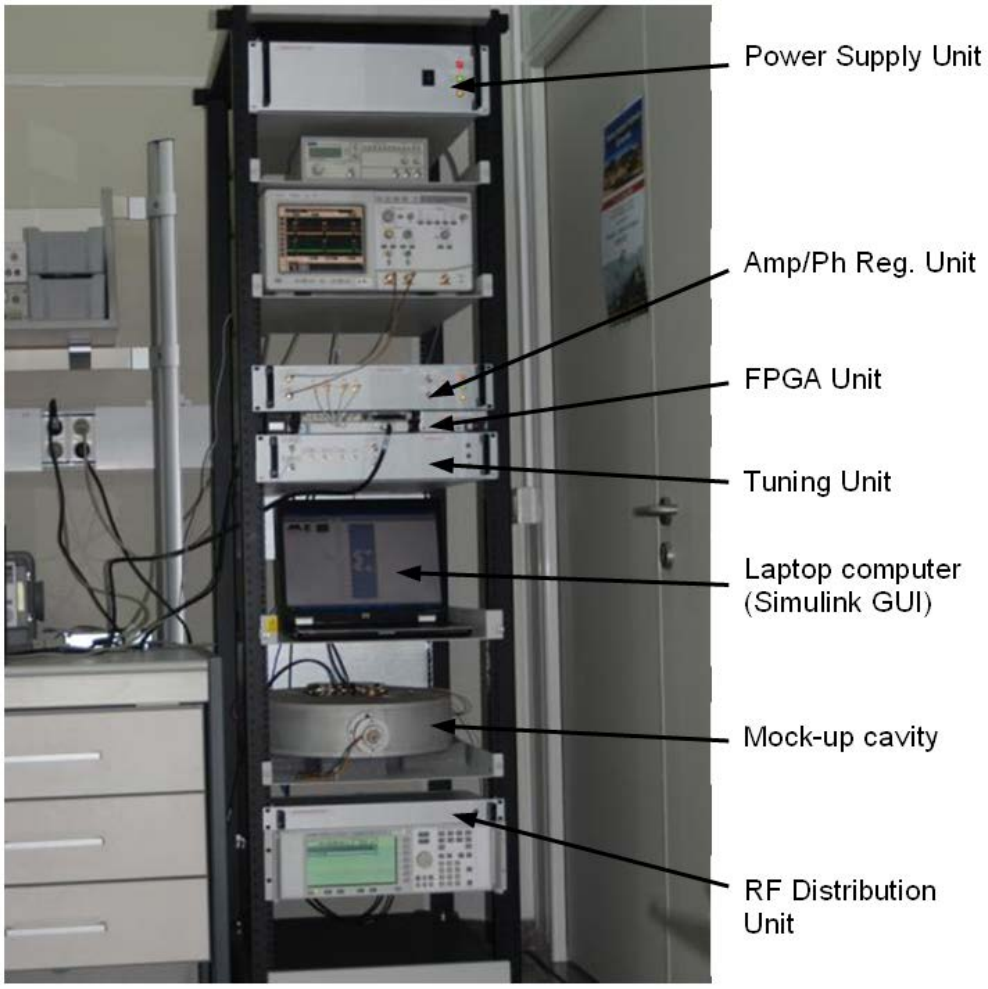

Figure 4.13: The complete DLLRF rack

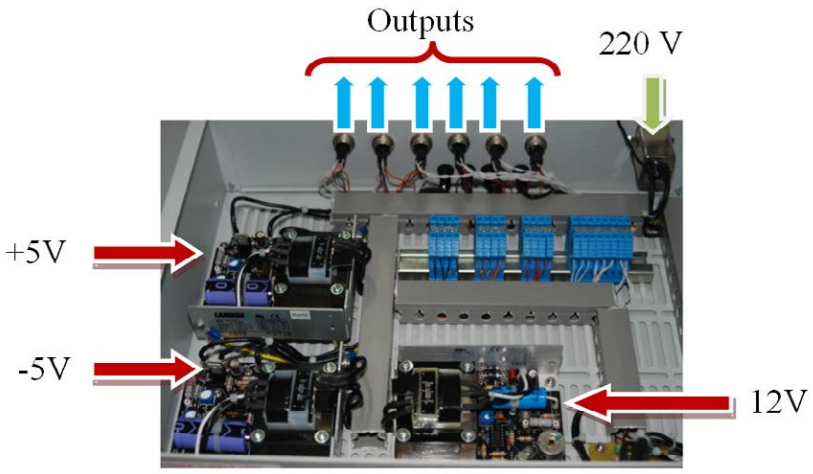

Figure 4.14: Picture of the interior of the *Power Supply Unit*

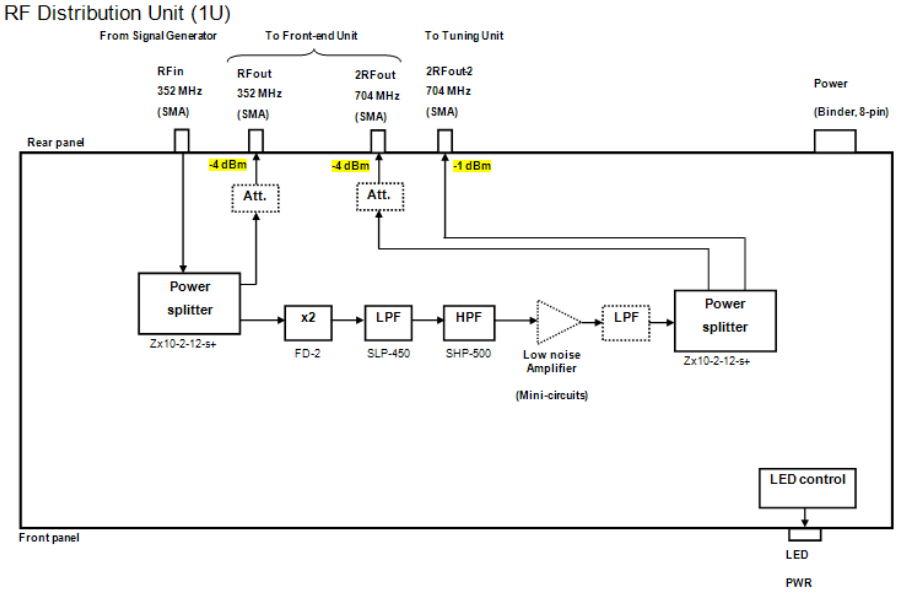

Figure 4.15: Schematics of the RF Distribution Unit

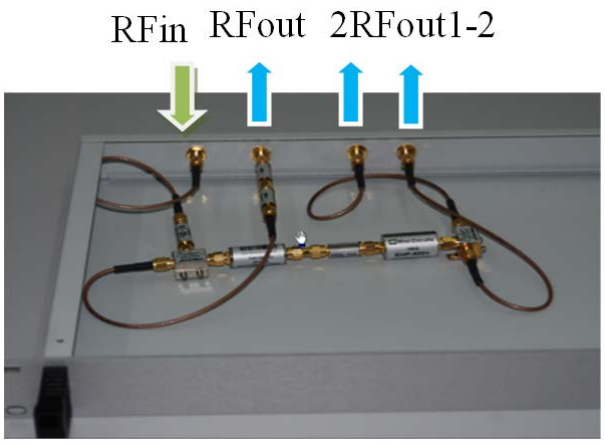

Figure 4.16: Picture of the RF Distribution Unit

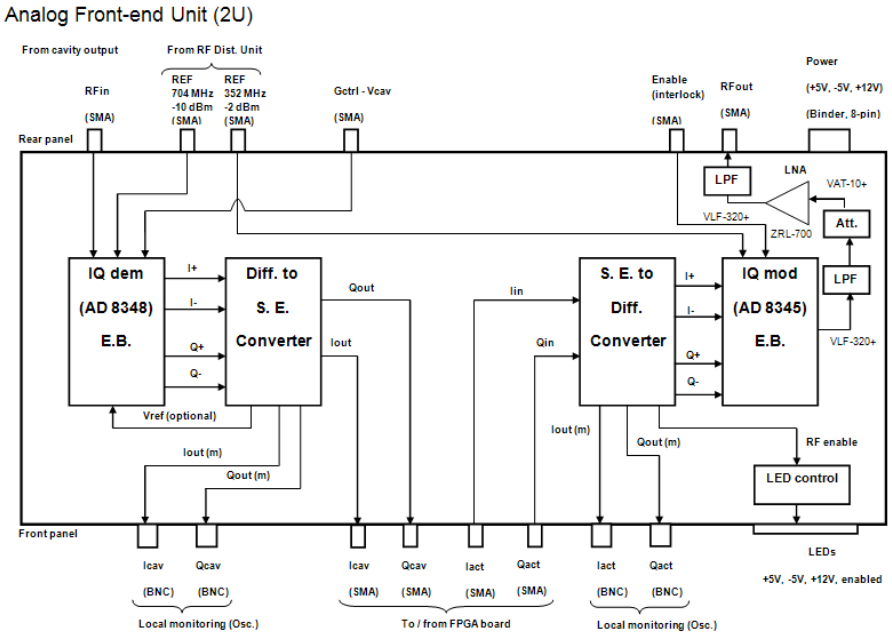

Figure 4.17: Schematic of the Analog Front-End Unit

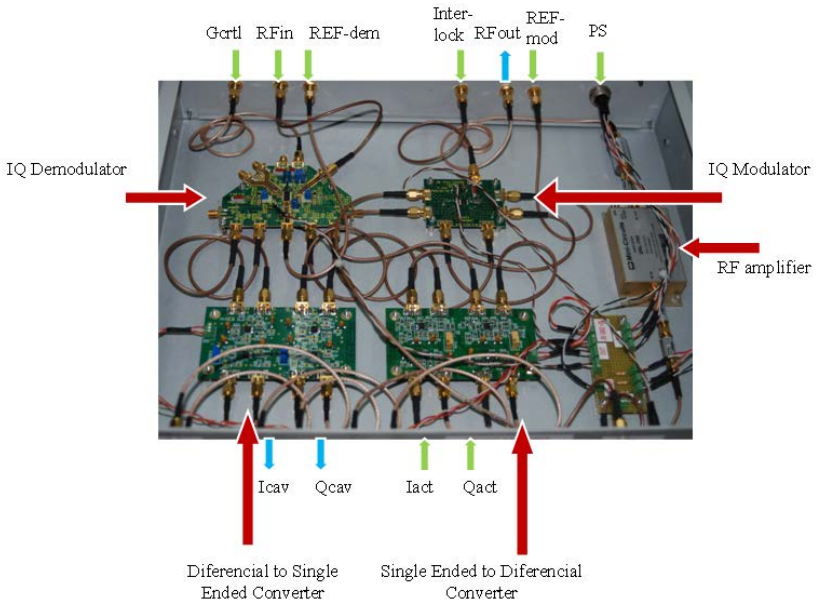

Figure 4.18: Picture of the Analog Front-End Unit

dedicated to gain adjustment of the IQ demodulator. The level of the gain control voltage can be between 0.2 V and 1.2 V but it is normally fixed at 0.65 V approximately via the control computer as that gives best results in terms of output linearity versus gain control voltage. The reference RF ($f = 2f_{RF}$) for the IQ demodulator is provided by the *RF Distribution Unit* with a typical level of -10 dBm. The I and Q outputs of the IQ demodulator, after being converted from differential to single-ended by the corresponding converter board are sent to the SMA connectors on the front panel to be sampled and fed into the FPGA for the subsequent signal processing. Additionally, a buffered copy of the I and Q signals is available on the BNC connectors on the front panel so that they could be measured by an oscilloscope without disturbing the feedback loops. The maximum swing of the I and Q signals is ± 1.4 V but care should be taken in order not to saturate the ADC inputs when these signals are fed into the FPGA unit (the maximum input voltage of the ADCs is only ± 1.25 V). This can be done by inserting appropriate attenuators on the *RFin* of the IQ demodulator and/or fine adjustment of the demodulator gain about 0.65 V.

The I and Q inputs of the IQ modulator (the I/Q drive signals) are fed into the corresponding SMA connectors on the front panel with a buffered copy available on the BNC connectors for local monitoring. The maximum voltage of the I/Q inputs is ± 0.6 V but that whole voltage range might not be used as the DACs have a more limited voltage range (it is only ± 0.32 V). The I and Q signals are in the next stage converted from single-ended to differential and fed into the IQ modulator with the RF reference being provided by the

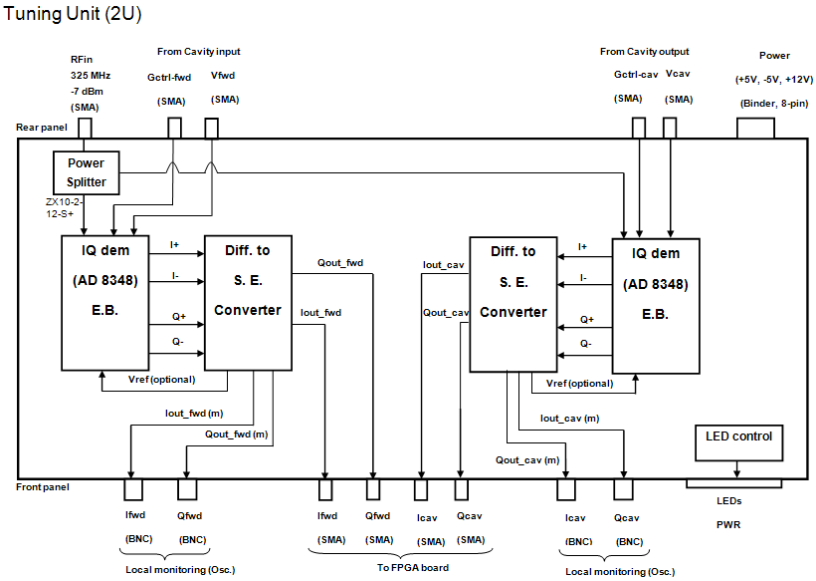

Figure 4.19: Schematics of the Tuning Unit

RF Distribution Unit. Similar to the IQ demodulator, appropriate attenuators should be placed at the RF output of the LLRF so that no LLRF signal becomes saturated within the whole power range of the RF amplifier supplying the cavity. The RF output of the IQ modulator is amplified by a ZLR-700 RF amplifier from Mini-circuits with maximum output power of 25 dBm. However, in order to make sure that the amplifier will always work in its linear region, some attenuators have been placed at the amplifier input; therefore the actual output power of the Analog Front-end Unit is less than the rated power of the amplifier.

An additional port has been provided on the rear panel for enabling/disabling the IQ modulator for interlock purposes with a typical turn-off time of 1.5 μs [17]. The IQ modulator can also be manually enabled and disabled using the corresponding switch mounted on it. A LED on the front panel indicates whether the modulator is enabled or disabled.

Tuning Unit

FIG. 4.19 and FIG. 4.20 show the schematics and the real implementation of the *Tuning Unit* respectively.

This unit basically consists of two AD8348 IQ demodulator boards plus two in-house-developed boards, similar to the one used in the *Front End Unit*, to convert the differential outputs of the IQ demodulators to single ended. The forward voltage and the cavity reflected voltage are fed into the unit via the corresponding connectors on the rear panel to be converted to baseband. The reference RF ($f = 2f_{RF}$) which is provided by the *RF Distribution Unit* is split

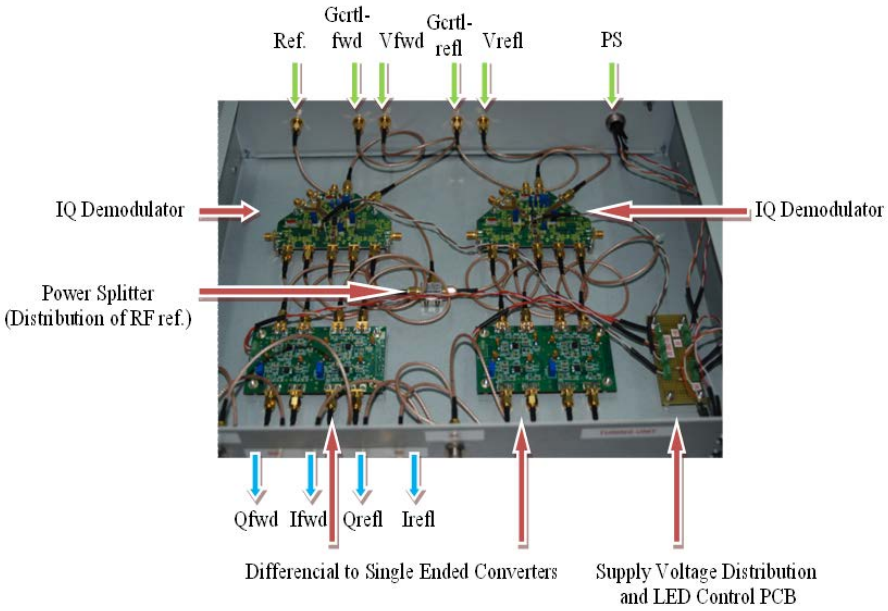

Figure 4.20: Picture of the Tuning Unit

into two by a power splitter and fed into the two boards. The I/Q outputs of the two demodulators are then converted to single-ended by the two converter boards and made available on the corresponding SMA connectors on the front panel to be sampled by the ADCs. The voltage range of these signals is similar to the one of the *Analog Front-end Unit*. Likewise, a buffered copy of the I/Q signals is additionally sent to the BNC connectors on the front panel for local monitoring. The four baseband outputs of the *Tuning Unit* are then sampled and fed into the FPGA running the tuning algorithm.

Two SMA connectors are mounted on the rear panel so that the user can adjust the gain of the IQ demodulators (the preferred voltage though is 0.65 V). Alternatively, the gains can be adjusted using the corresponding potentiometers and switches mounted on the demodulator boards. It should be noted that while measuring V_{fwd} is needed for the tuning loop, the V_{refl} is only used for monitoring the value of the reflected voltage in the control computer. For that reason, in the current version of the FPGA program, a DAC channel is dedicated to the gain adjustments of the V_{fwd} demodulator but the gain of the V_{refl} demodulator is manually fixed at 0.65 V approximately by the gain adjustment potentiometer.

Tuner Driver Unit

This unit consists of the stepper motor driver for cavity tuning and an in-house-developed board which conditions the DAC output signals (Pulse and Direction)

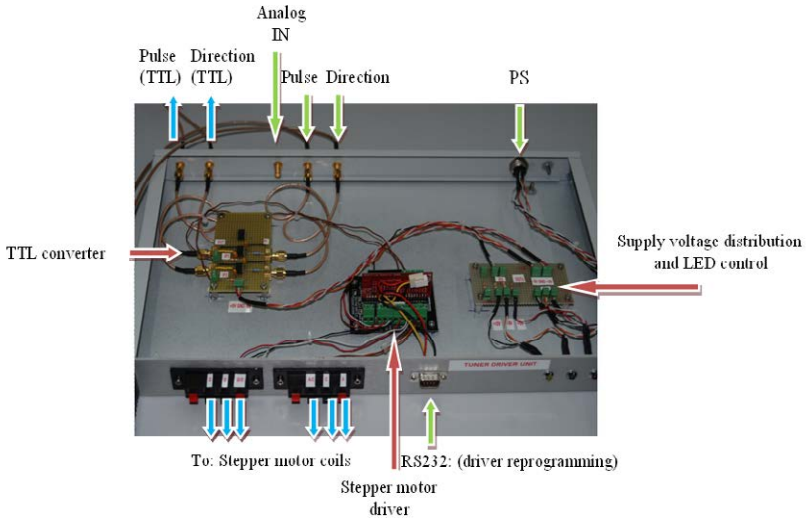

Figure 4.21: Picture of the Tuner Driver Unit

to have TTL levels as this is required for the current driver.

The stepper motor driver is an Easy Step TM 3000 Industrial Interface from Active Robots [23]. The stepper motor of the mockup cavity is a Mclennan 26DBM series DLA's.

FIG. 4.21 shows the *Tuner Driver Unit* with the driver and conditioning boards mounted in it.

The pulse and direction inputs are fed into the *Tuner Driver Unit* via the corresponding SMA connectors on the rear panel. The level of these signals is set in the FPGA program so that the conditioning board generates the required signal levels for the driver board. An analog input port is additionally foreseen so that the driver can also work in analog input mode if needed (with the current design, this port is not used). The pulse and direction signals with TTL levels are made available on the corresponding connectors on the rear panel. These signals can therefore be used if the *Tuner Driver Unit* should control another stepper motor not compatible with the current driver board[10]. The required pulses for the stepper motor coils are accessible via the two quick connect terminals on the front panel. Also, an RS232 port has been foreseen on the front panel to reprogram the driver board if needed [23].

Digital Unit

The *Digital Unit* includes the FPGA board and the ADC and DAC modules. This is a high performance VHS-ADC board from Lyrtech [24] (with cPCI to 4x PCIe interface for PC connection) based on a Virtex-4 FPGA from Xilinx and

[10]In that case only the TTL converter board of the *Tuner Driver Unit* will be used as the stepper motor should be driven by another driver.

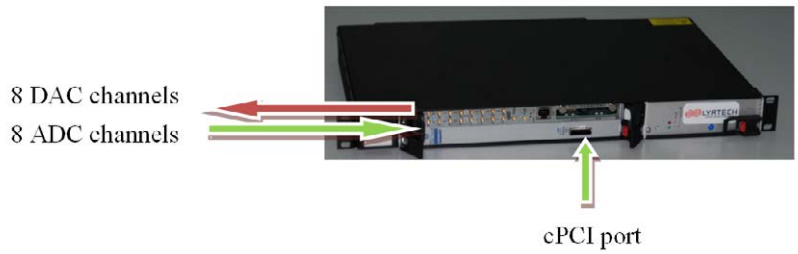

Figure 4.22: Picture of the Digital Unit (Lyrtech)

eight AD6645 ADCs with a resolution of 14 bits and maximum sampling rate of 105 MSPS [21]. The board also incorporates 128 MB of SDRAM for data buffering on the FPGA. In order to provide the FPGA board with 8 additional DAC inputs, an add-on DAC module from Lyrtech has also been purchased and mounted on the FPGA board. These are DAC5687 [22] from Texas Instruments with a resolution of 14 bits and maximum sampling rate of 480 MSPS (interpolating).

The FPGA was programmed using the Xilinx System Generator and the Lyrtech Model Based Design Kit in a MATLAB-Simulink environment. The advantage of this method is that the FPGA programming was eased and the time needed to develop the FPGA code was significantly reduced compared to the VHDL[11] method.

In order to further reduce the time and effort needed for the establishment of the LLRF test bench, it was decided to co-simulate the FPGA hardware in the MATLAB-Simulink environment. With this method, known as HIL[12] co-simulation, the FPGA communicates directly with Simulink blocks; therefore the FPGA hardware can be tested without having to connect it to real-world signals. Then, Simulink source blocks were used to set the LLRF input parameters (such as the PI gains and the offset values) eliminating the need for an additional GUI[13] and a communication protocol, while the I/Q input and output signals were still the real ones coming from the *Analog Front-end Unit* connected to the mock-up cavity. It should be noted that although the HIL co-simulation of the loop proved to be very useful during the system development, test and trouble-shooting, it is not planned to use it for the final deployment as the LLRF system should be integrated into the EPICS[14] control system of the accelerator facility [78].

FIG. 4.22 shows the FPGA card cage with the cPCI communication port and the VHS-ADC and DAC modules mounted in it. For information on these items, please refer to the Lyrtech website [24].

[11] VHSIC (Very High Speed Integrated Circuit) Hardware Description Language
[12] Hardware-In-the-Loop
[13] Graphical User Interface
[14] Experimental Physics and Industrial Control System

PC Unit

A laptop computer (HP EliteBook 8530p, 2.4 GHz with 2 GB of RAM and 250 GB of HD) was used for the development of the FPGA program and later for the LLRF tests with the mock-up cavity.

The following software packages were installed on the laptop computer for system development and tests with the mock-up cavity:

- Software for BSDK[15]: ISE Foundation 9.2
- Software for MBDK[16]: Matlab R2007a and System Generator for DSP[17] 9.2

For detailed information on the required software packages and the installation procedure, please refer to the corresponding User's Manual [24] from Lyrtech.

4.5.2 DLLRF GUI

A MATLAB-Simulink GUI has been made with the cosim block so that the LLRF system could be tested without having to integrate it into the future EPICS control system of the ESS-Bilbao Linac. This GUI allows the user to set the LLRF parameters and additionally monitor all the important variables of the system while it is running. FIG. 4.23 shows a snapshot of the LLRF GUI.

The parameters on the left of the co-simulation block are the control loop parameters while the ones on the right are the read-back values for system monitoring.

The Simulink scope blocks have been used to graphically monitor different parameters versus time such as the amplitudes of the forward and reflected voltages, tuner position, phase error, etc. These scope blocks can be particularly useful when the LLRF system is put into operation during long time periods so that the user can see a history of the data. The numerical displays show current values of the corresponding parameters.

The following color code has been used to easily distinguish the amp/ph blocks from tuning blocks and common blocks:

- Magenta: amplitude and phase loop parameters
- Blue: tuning loop parameters
- Green: common parameters for the amp/ph and tuning loops

Additionally, *Amph*, *Tu* and *Com* prefixes and numbers have been used in front of each parameter name in the cosim block to indicate to which category that parameter belongs.

[15] Board Software Development Kit
[16] Model Based Design Kit
[17] Digital Signal Processor

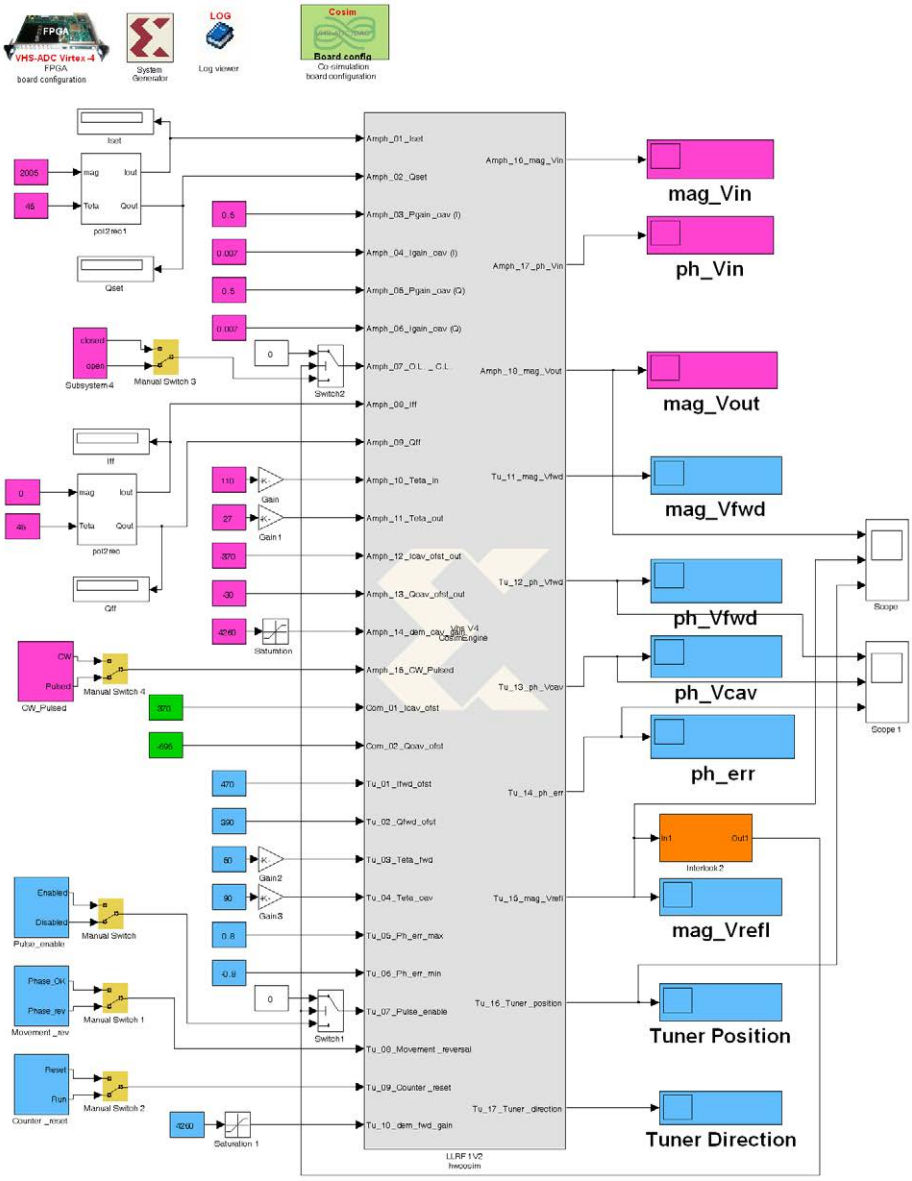

Figure 4.23: DLLRF GUI (MATLAB - Simulink) for the HIL-cosimulation tests

LLRF parameters

Amplitude and phase loop parameters

TABLE 4.2 summarizes the parameters of the amplitude and phase loops as well as their function and range.

Tuning loop parameters

TABLE 4.3 summarize the parameters of the tuning loop as well as their function and range.

Common parameters

TABLE 4.4 summarize the common parameters between the amplitude, phase and tuning loops as well as their function and range.

4.5.3 Setting the LLRF Parameters

Several LLRF parameters must be set properly before the RF system is put into operation under power. That includes the non-negligible DC offsets of the IQ modulator and modulators, the PI gains, the amount of the phase shifts, etc. The setting of these parameters is done via the control computer by inserting appropriate values into the input boxes of the cosim model. The procedure for setting the parameters is as the following:

Amplitude and phase loops

1. **Setting the gain of the input IQ demodulator:** By the *dem_cav_gain* parameter the user can change the IQ demodulator gain and that, in closed-loop mode, scales the RFQ field accordingly. In open loop mode, changing this parameter will not have any effect on the actual RFQ field but, it will scale the read-back value. It is observed that the IQ demodulator response to gain variations is most linear when the gain value is set to 0.65 V app. (4260 steps in the cosim model). Therefore, it is preferred to use the gain control voltage only around 0.65 V for fine adjustment of the RFQ power level when the system is first configured (for coarse power level setting at system setup stage, appropriate attenuators must be placed at the input and output of the LLRF system so that the whole dynamic range of the system can be used while avoiding component damage due to high signal levels). Once an optimum value of the input gain has been found, it should not be changed anymore unless the loop gain should be fine adjusted again (ex. an attenuator value is changed in the loop).

2. **Offset compensation of the IQ modulator (output offset compensation):** This is necessary to ensure that when the set value for the RFQ voltage (in the control computer) is zero, the actual field in the RFQ is also

Table 4.2: Amplitude and phase loop parameters

Parameter	Function	Range
Amph_01_Iset	determines reference value for I component of the cavity field (closed loop mode only)	[-8191,8192]
Amph_02_Qset	determines reference value for Q component of the cavity field (closed loop mode only)	[-8191,8192]
Amph_03_Pgain_cav(I)	proportional gain of the PI controller for I component of the cavity voltage	[-31,32]
Amph_04_Igain_cav(I)	integral gain of the PI controller for I component of the cavity voltage	[-1,2]
Amph_05_Pgain_cav(Q)	proportional gain of the PI controller for Q component of the cavity voltage	[-31,32]
Amph_06_Igain_cav(Q)	integral gain of the PI controller for Q component of the cavity voltage	[-1,2]
Amph_07_O.L_C.L	Changes the operation mode from open-loop to closed-loop and vice versa	Open/Closed
Amph_08_Iff	determines I component of the cavity feed-forward voltage (open-loop and closed-loop)	[-8191,8192]
Amph_09_Qff	determines Q component of the cavity feed-forward voltage (open-loop and closed-loop)	[-8191,8192]
Amph_10_Teta_in	determines rotation angle of the input phase shifter applied to the cavity probe voltage	[-8191,8192]
Amph_11_Teta_out	determines rotation angle of the output phase shifter applied to the cavity drive voltage	[-8191,8192]
Amph_12_Icav_ofst_out	compensates DC offset introduced by the DAC module and the IQ modulator on the I drive signal	[-8191,8192]
Amph_13_Qcav_ofst_out	compensates DC offset introduced by the DAC module and the IQ modulator on the Q drive signal	[-8191,8192]
Amph_14_dem_cav_gain	sets the gain of the demodulator for the cavity probe signal in the Analog Front-end Unit	[-8191,8192]
Amph_15_CW_Pulse	sets LLRF operation mode to CW or Pulsed	Open/Closed
Amph_16_mag_Vin	displays magnitude of the cavity probe voltage	[0,8192]
Amph_17_ph_Vin	displays phase of the cavity probe voltage	[-180,+180]
Amph_18_mag_Vout	displays magnitude of the cavity drive voltage	[0,8192]

Table 4.3: Tuning loop parameters

Parameter	Function	Range
Tu_01_Ifwd_ofst	compensates DC offset introduced by the ADC module and IQ demodulator on the I component of Vfwd	[-8191,8192]
Tu_02_Qfwd_ofst	compensates DC offset introduced by the ADC module and IQ demodulator on the Q component of Vfwd	[-8191,8192]
Tu_03_Teta_fwd	determines rotation angle of the phase shifter applied to the cavity Vfwd	[-8191,8192]
Tu_04_Teta_cav	determines rotation angle of the phase shifter applied to the cavity Vprobe (separate from the one used for the amp/ph loops)	[-8191,8192]
Tu_05_Ph_err_max	sets upper threshold for the phase error (in degrees). If the (Ph(Vprobe)-Ph(Vfwd)) is higher than this value the tuner moves until the error becomes smaller than this threshold.	[-511,512]
Tu_06_Ph_err_min	sets lower threshold for the phase error (in degrees). If the (Ph(Vprobe)-Ph(Vfwd)) is lower than this value the tuner moves until the error becomes larger than this threshold.	[-511,512]
Tu_07_Pulse_enable	Allows the operator to enable or to disable the tuning loop	Enable/Disable
Tu_08_Movement_reversal	changes direction of the tuner movement	Rev/OK
Tu_09_Counter_reset	resets or runs the counter which displays tuner position (in steps)	Reset/Run
Tu_10_dem_fwd_gain	sets the gain of the demodulator for the cavity forward signal in the tuning unit	[-8191,8192]
Tu_11_ph_Vfwd	displays phase of the cavity forward voltage in degrees	[-180,+180]
Tu_12_ph_Vcav	displays phase of the cavity probe voltage in degrees	[-180,+180]
Tu_13_ph_error	displays difference between the phase of forward and probe voltages	[-360,+360]
Tu_14_mag_Vrefl	displays magnitude of the cavity reflected voltage in steps	[0,8192]
Tu_15_Tuner_position	displays current position of the tuner	[-2047,2048]
Tu_16_Tuner_direction	displays direction of the tuner movement as the following: no movement: 0; inwards/outwards: -1/1 or vice versa (depending on Tu_08_Movement_reversal)	[-1;0;+1]

Table 4.4: Common parameters for the Amplitude, phase and tuning loops

Parameter	Function	Range
Com_01_Icav_ofst	compensates DC offset introduced by the ADC module and the IQ demodulator on the I component of the cavity probe signal	[-8192,8192]
Com_02_Qcav_ofst	compensates DC offset introduced by the ADC module and the IQ demodulator on the Q component of the cavity probe signal	[-8192,8192]

zero. In order to do the compensation, the LLRF system must be first put into operation in open-loop mode and the mag_Vfwd must be set to zero. Then the $Icav\_ofst\_out$ and $Qcav\_ofst\_out$ should be changed manually while watching the real output power of the Front-End Unit ($RFout$) using for example an RF power meter or an spectrum analyzer[18]. In this way, right offset values are found so that the LLRF output at the RF frequency becomes as small as possible. This is normally done after a few trials. It should be noted that the output offset consists of two parts: these are the offset of the IQ modulator (it can be as large as 200-300 mV app.) and the offset of the DAC unit (typically a few mV only). Using the method explained above, the overall offset (i.e. the sum of the two offsets) will be compensated at once.

3. **Offset compensation of the IQ demodulator (input offset compensation):** This is necessary to ensure that when the actual RFQ field is zero, the read-back value (in the control computer) will also be zero. Input offset compensation must be done only after the output offset has been compensated (step 2). This is done by first putting the LLRF system into operation in open-loop mode and setting the LLRF output to zero. Then correct $Icav\_ofst$ and $Qcav\_ofst$ values are found by a few trial and errors so that the read-back RFQ field (mag_Vin) also becomes zero.

4. **Setting the phase shifts (i.e. $Teta\_in$ and $Teta\_out$):** In order to ensure that the IQ loops will be stable before they are actually closed, the fractional part of the loop delay must be compensated. This is done by adjusting either $Teta\_in$ or $Teta\_out$ (or both). If, for example, the total delay from the LLRF output along the RF transmitter and the RFQ to the LLRF and the two PI controllers is 512.3 times the RF period, the phase shifters must be set so that the overall phase shift (i.e. the sum of the two phase shifts) compensates 0.3 RF periods (i.e. -108° of phase shift). Then the IQ vector enters at the input of the PIs with correct phase. If the phase shift value is not properly set, the response of the

[18]This implies disconnecting the LLRF output temporarily in order to connect it to the power meter.

I and Q loops will not be the same and some degradations in the step response might be seen as well. In the extreme case, if the phase error exceeds the phase margin of the loop, the loop will become unstable (in the preliminary tests, the phase margin was measured at $\pm 55^\circ$ about the optimum phase giving a very large margin for loop stability). Having two phase shifters (one at the LLRF input and another one at the output) gives the possibility to maintain the loops stable while additionally rotate the read-back IQ vector so that the monitored phase is the same as the actual RFQ phase (or the phase of any other RF signal along the loop path which is of interest for the operator).

In order to find optimum phase shift values, the LLRF system must be put into open-loop operation while the mag_Vfwd set to a non-zero value. Then either $Teta\_in$ or $Teta\_out$ is changed so that the read-back phase of Vin is the same as the set value (for example both are 45°). That guarantees that the I and Q loops will be stable (assuming the PI and loop gains are not too high) and the response of both loops will be equal provided that the other parameters of the two loops are also equal. Once the optimum value for the phase shift is found, it should not be changed anymore unless there is a change in the loop delay (ex: a cable is changed) which implies finding a new value for the phase shift(s).

5. **Setting the PI gains:** The PI gains for the I and Q loops are normally set to be equal. In order to adjust the PI gains, the LLRF system should be put into operation in closed-loop (pulsed mode). It is important to note that improper PI gains can make the loops oscillatory or even unstable; therefore care should be taken to avoid instabilities when the loops are closed around the RFQ for the first time. Loop instability can be avoided by setting the integral gain to zero and the P gain to relatively low values at first[19]. After the loop is successfully closed, optimum P and I gains can be found by a few trials so that the loop response becomes acceptable[20]. A simple way for gain adjustment could be the following: first the I gain is set to zero and the P gain is set so that the real RFQ field is almost half of the set value. Then the I gain is increased step by step until the loop response is just about to undergo an overshoot. Once the PI controllers are properly adjusted, the gain values should not be changed anymore unless there is degradation in the step response (for example if the loop gain is changed).

Tuning loop

The tuning loop should be disabled if the RFQ field during the pulse is too small; because then the phase of the RF signals cannot be measured and that makes the movement of the tuner unpredictable. Therefore, before the RFQ

[19] This implies that the real amplitude of the RF pulse will smaller than the set value.

[20] This normally corresponds to a response which is as fast as possible but does not undergo any overshoot or oscillations.

is powered, the tuning loop should be disabled using the $Pulse\_enable$ switch in the cosim model. If for any reason (such as improper setting of the tuning loop parameters) the tuner moves in the wrong direction, the movement can be reversed by the $Movement\_rev$ switch in the cosim model. The procedure for setting the tuning loop parameters is as the following:

1. **Setting the gain of the input IQ demodulator for forward voltage measurement (dem_fwd_gain):** As this IQ demodulator is only used for phase measurement purposes, normally its gain does not need any fine adjustment. Therefore, its gain control input can be set to 0.65 V (i.e. 4260 in the cosim model) which is the optimum value in terms of IQ demodulator output linearity versus gain.

2. **Input offset compensation:** Two IQ demodulators are needed for the tuning loop. These are used to measure the phase of the forward and cavity voltages. As the IQ demodulator for the cavity phase measurement is physically the same as the one used for amplitude and phase loops, once its offset has been compensated for amp/ph regulation (step 3 in the previous subsection) that setting will also be valid for the tuning loop. The procedure for compensating the IQ offsets of the forward voltage is similar: once the system is put into operation in open-loop mode, the magnitude of the RFQ voltage is set to zero ($Iff = Qff = 0$), then the $Ifwd\_ofst$ and $Qfwd\_ofst$ parameters are changed by a few trial and errors until the read-back value of the $Vfwd$ becomes minimum (as close as possible to zero).

3. **Setting the phase shifts (i.e. $Teta\_fwd$ and $Teta\_cav$):** In the FPGA program, two phase shifters are used for the forward and cavity voltages (they are separate from the ones used for the amplitude and phase loops). They should be adjusted so that the following two conditions are met simultaneously:

   (a) When the reflected voltage is minimum (i.e. the cavity is properly tuned) the read-back values of the forward and cavity phases are equal.

   (b) When the reflected voltage is minimum, the two read-back phases are close to zero[21].

   The first condition is necessary to make sure that regulating the phase difference at zero degree corresponds to having minimum reflected voltage. The second condition is needed for having enough margin to avoid any phase discontinuity (i.e. phase jump from $+180^\circ$ to -180° or vice versa) even if the tuner moves from one extreme to another. Bearing in mind that the output phase of the cordic blocks in the FPGA program changes

[21] That is not an strict requirement though as any value in the range of $\pm 30^\circ$ would also be fine provided that the two values are equal.

in the $\pm 180^\circ$ range, by meeting the second condition one can avoid any phase discontinuity which can otherwise make the tuners move in the wrong direction.

4. **Setting the upper and lower phase error thresholds:** The tuning loop moves the tuner only when the phase error (i.e. the difference between the forward and cavity phases after the corresponding phase shifts of these signals) exceeds either the upper or the lower phase error thresholds. The movement continues until the phase error enters the (Ph_err_max, Ph_err_min) window and then the tuning algorithm leaves the tuner at that position until the next time the error exceeds any of the two thresholds. Setting a narrower window for the phase error means that the cavity will be more precisely tuned (less reflected power in average), but then the tuner will move more frequently. If the phase error window is too narrow, the tuner will vibrate at its position due to the noise on the measured signals.

4.5.4 FPGA programming procedure

Here, we briefly explain the different steps which should be followed each time the FPGA should be reprogrammed and/or the control algorithm has to be modified. For detailed information on how to program the FPGA, please refer to the corresponding user's manual from Lyrtech [24] and Xilinx [25].

Definition of the FPGA algorithm in Simulink

As mentioned earlier, with the model-based approach, the FPGA is programmed in the MATLAB-Simulink environment. The algorithm for the regulation loops is therefore defined using appropriate blocks from the Lyrtech, and Xilinx libraries. This option also allows the user to perform simulations and timing analysis in order to identify errors in the control algorithms and check the control system viability before compiling the program. The FPGA source program in MATLAB-Simulink is named as `LLRF` followed by its version. For example `LLRF1V2.mdl` refers to version 1.2 of the program. FIG. 4.24 shows the top-level FPGA program containing two main blocks for the amp/ph and tuning loops.

FIG. 4.25 and FIG. 4.26 show the design of the FPGA program for amp/ph regulation and tuning with more details (the yellow boxes are programmed in-house).

Compilation

Once the FPGA program has been defined and successfully tested in MATLAB-Simulink, the program has to be complied to create the `cosim` block. This is done by double clicking the System Generator Block in the `.mdl` program and choosing the options that correspond to the actual hardware and parameters values. Depending on the program size and complexity, it can take up to one hour approximately until the compilation is finished. The compilation will stop

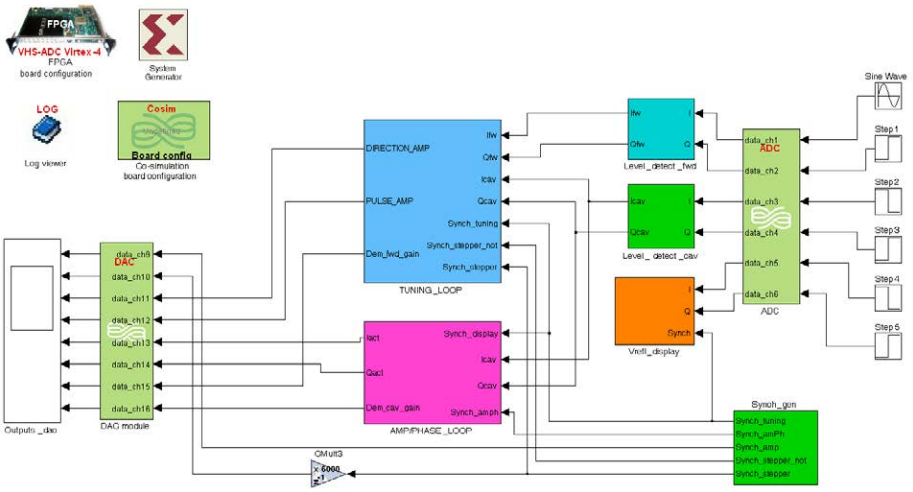

Figure 4.24: Top level view of the FPGA program

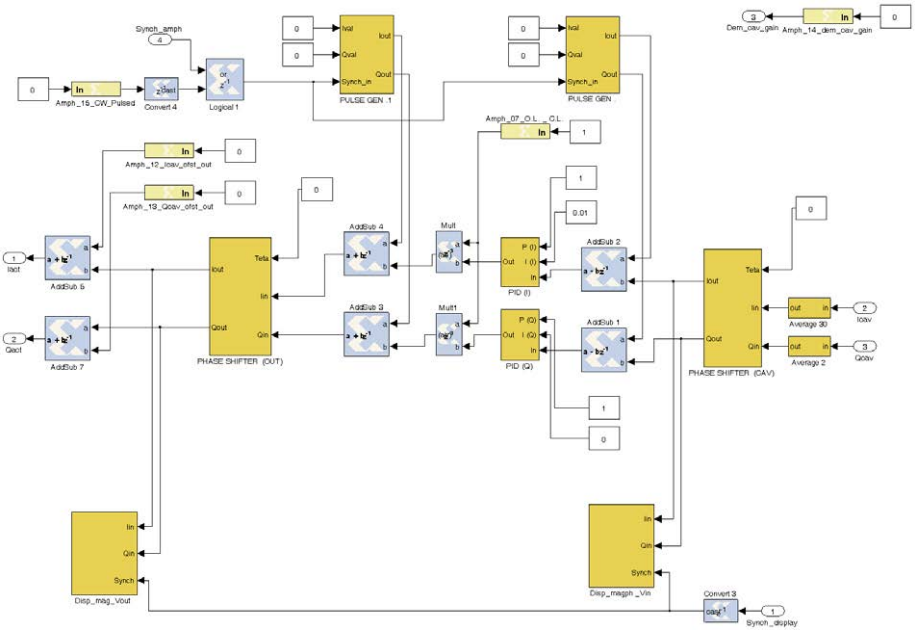

Figure 4.25: Design of the FPGA program for the amp/phase loops

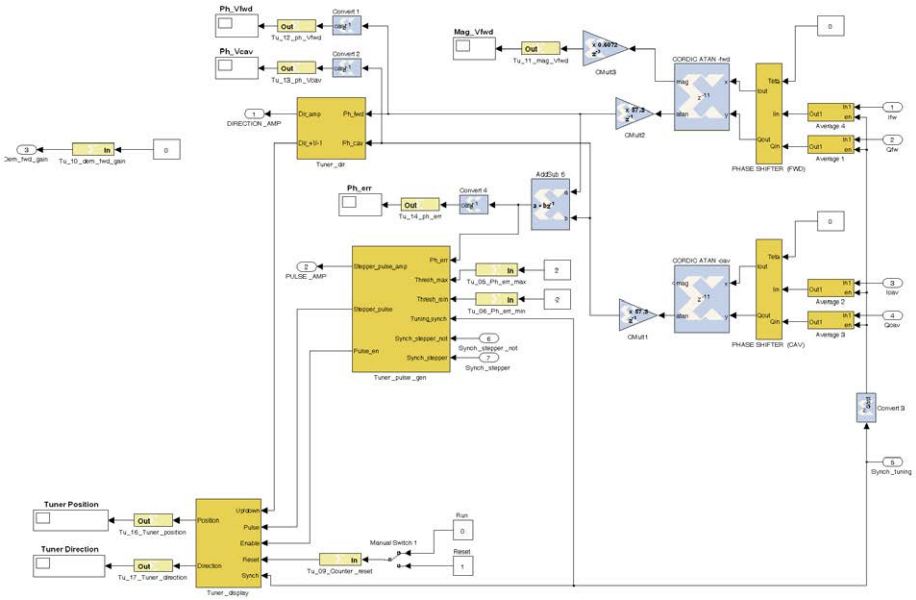

Figure 4.26: Design of the FPGA program for the tuning loop

before finishing if the System Generator finds any unresolved error in the FPGA program. If that happens, the user can refer to the error log file generated during compilation so that the error can be identified and removed before starting a new compilation.

If the compilation finishes successfully, a new window appears with the co-simulation block automatically named as the program name followed by `hw_cosim_lib.mdl`. The cosim block can then be saved in the cosim library to be used in the cosim model.

This co-simulation block contains all the input ports defined in the FPGA program as well as the output parameters to be monitored either numerically or graphically in the cosim model.

Inserting the cosim block into a cosim model

In order to define the input values and output displays for the cosim block, another MATLAB-Simulink file will be needed. This file is named as the original program file followed by `_cosim.mdl`. Then, the cosim block can be inserted into the `_cosim.mdl` file together with all other MATLAB-Simulink blocks which are needed to define the inputs and outputs or further manipulate the data if needed. This, in fact, will be the GUI that the user should work with during the HIL co-simulation (please refer to FIG. 4.23 for a snapshot of the GUI).

If any modification is made in the loop design, a new co-simulation block has to be generated and that implies new compilation of the design file. Then,

the operator has to substitute the old co-simulation block by the new one in the final `_cosim.mdl` file and readjust the input parameters if necessary.

Programming the FPGA

Having the cosim block inserted into the cosim model and the input and output variables properly connected to Simulink source and sink blocks, the user can now run the `_cosim.mdl` file to start a HIL co-simulation. In this model, the user can set the values of all the loop parameters and monitor the system performance while it is running.

4.6 Experimental Results of the ESS-Bilbao DLLRF

Two series of tests were done in a laboratory environment to evaluate the LLRF performance being: 1) low power tests with a mock-up cavity with a resonant frequency of 327.14 MHz and unloaded quality factor of 1000 approximately and 2) tests with the RFQ cold model at the Imperial College London with 60 W of RF power. The experimental setup was the same as the one shown in Fig. 4.7 and Fig. 4.8 except the trombone phase shifter which was missing in the tests. The control loop parameters were adjusted following the procedures explained in the LLRF design description sections. Several tests were then carried out to measure the amplitude and phase stability, linearity, loop delay, transient response, loop stability and finally long-term performance. These tests not only assured the ability of the LLRF system to work in accordance with the specifications but also were very useful in terms of giving a good insight of how the system should be operated with a real RFQ system running under power. The section begins by a description of the experimental setup, discussion of the significance and results of each of the measured parameters and finally comparison between the specifications and the practical results.

4.6.1 System set-up

In order to perform the different tests to check the LLRF performance, the measurement system of FIG. 4.27 was set up in the RF laboratory of the Electronics and Electricity Department at the University of the Basque Country (UPV/EHU).

As can be seen, the signal generator provides the reference RF signal ($f_{RF} = 327.14\ MHz$) to the *RF Distribution Unit*. At the same time this unit distributes both f_{RF} and $2f_{RF}$ to the rest of units. The upstream directional coupler at the input of the cavity is used to take a sample of the forward voltage to be demodulated in the *Tuning Unit*. The cavity field sample to be monitored on the power meter is taken from one output of the power splitter connected directly at the cavity output (i.e. the pickup loop). The other splitter output goes into the downstream circulator. This circulator acts as an isolator since a matched load is connected to its third port. A second sample of the cavity field

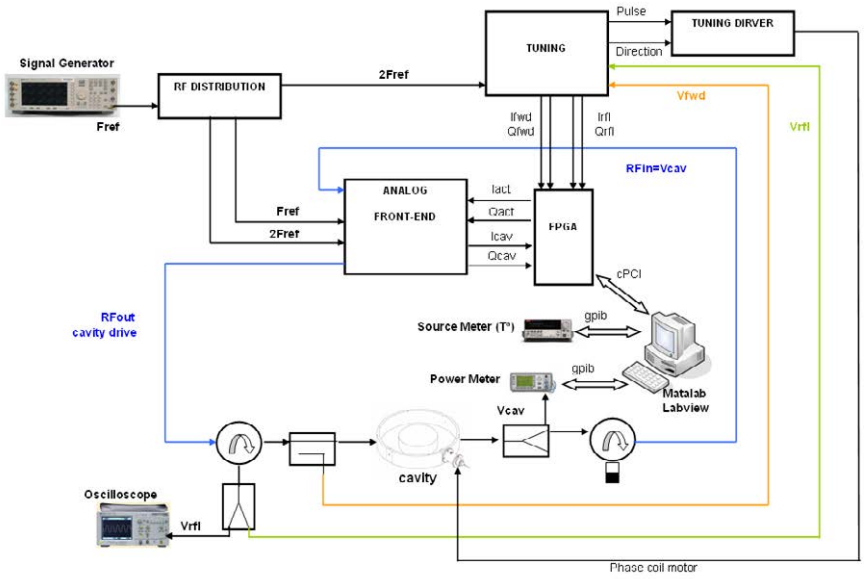

Figure 4.27: Schematics of the the DLLRF test set-up

is taken from the circulator output port. This signal, after being demodulated in the *Analog Front-End Unit*, is compared to its set-point and regulated in the FPGA. Moreover, the FPGA program provides the possibility of demodulating and digitally monitoring the reflected power, using the power splitter connected at the third port of the upstream circulator. The other output of the same power splitter is connected directly to an oscilloscope to monitor the reflected power.

The RF power meter is connected via the GPIB port to a PC with Labview program to monitor the long-term stability of the cavity field. At the same time, the Labview controls a Source Meter connected to a PT100 temperature sensor so that the ambient temperature can also be recorded for the long term tests.

Apart from the laboratory instruments shown in FIG. 4.27, some other equipments have been required. A Network Analyser has been used to characterize the cavity parameters while couplings and tuning parameters were adjusted. On the other hand, phase noise tests and power spectrum measurements have been performed with a Spectrum Analyzer, as it will be explained in more details in the next section.

The laboratory instruments used for the tests were the following:

- Signal Generator: Agilent ESG 4417A
- Oscilloscope: Agilent Infinium 54833 DSO

Table 4.5: Measured parameters of the mock-up cavity

Parameter	Value	Unit	Note
Resonance freq.	327.14	MHz	centered tuner
Tuning range	≈ 1	MHz	
Q_0 (unloaded Q)	≈ 1000		
Attenuation	≈ 15	dB	from input to pickup output

- Spectrum Analyzer: Agilent E4410A
- Power Meter: Agilent E4417A
- Power Meter Sensor: Agilent E9327A
- Network Analyzer: Agilent E8358A
- Source Meter: Keithley 2602 used with a PT100 temperature sensor

4.6.2 Tests results with the mock-up cavity

This section presents the main results obtained from the LLRF tests with the mock-up cavity.

Re-entrant mock-up cavity tests

The cavity parameters were measured by connecting the cavity input and output (i.e. the signal from the pickup loop) to the Network Analyzer measuring the S parameters. The results are shown in TABLE 4.5 and FIG. 4.28.

LLRF delay measurements

The total loop delay was measured at 800 ns approximately. That was due to the delay of the ADCs and DACs (500 ns), baseband low pass filters (200 ns) in the FPGA and the control program and cable lengths (100 ns). It is important to note that large loop delays can make the loop response oscillatory or even unstable; therefore care was taken to reduce the loop delay as much as possible by utilizing fast electronics and short signal paths.

Phase noise measurements

The phase noise was measured by a Spectrum Analyzer with the LLRF system being operated in CW mode. The selected bandwidth for the measurement was $3\ Hz\ -\ 300\ kHz$ which is larger than the cavity bandwidth (i.e. $\approx$200 kHz). FIG. 4.29 shows the noise level of the cavity field in dBc/Hz. As this is almost equal to the signal generator noise, one can conclude that the phase noise introduced by the LLRF is lower than that of the signal generator. Therefore, the overall phase noise can be improved by utilizing a better RF source.

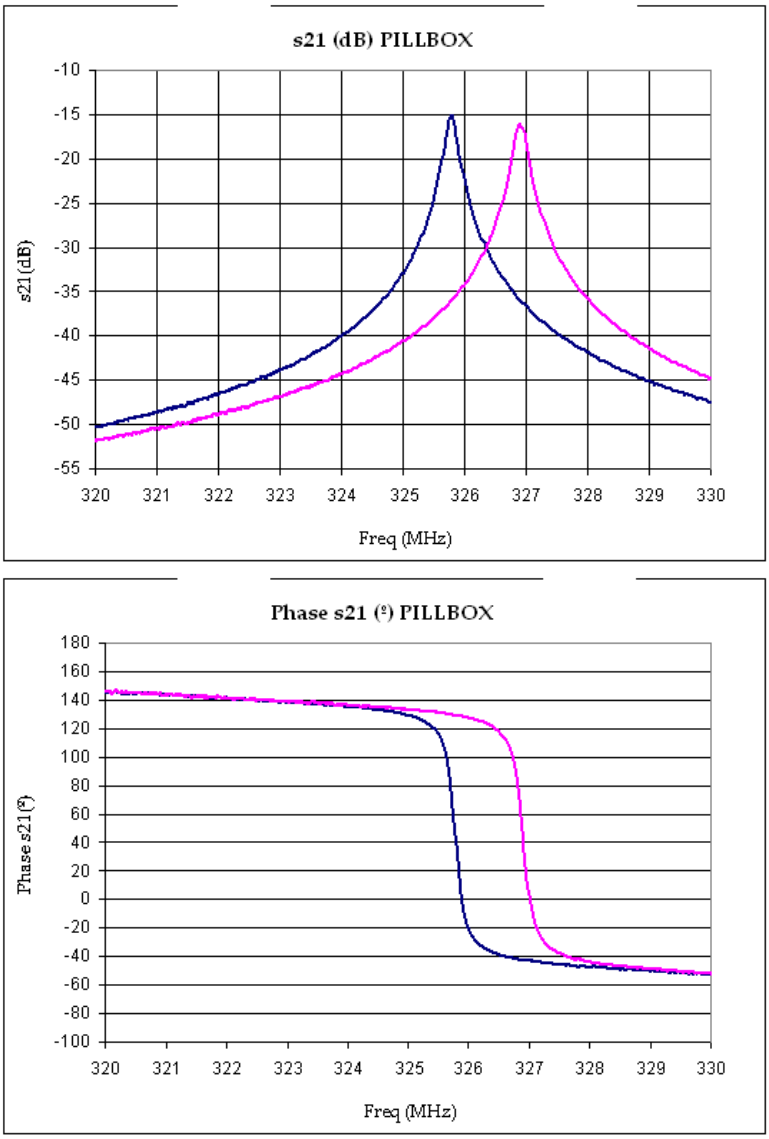

Figure 4.28: S21 measurements of the mock-up cavity with the tuner on both extremes, above: amplitude, below: phase

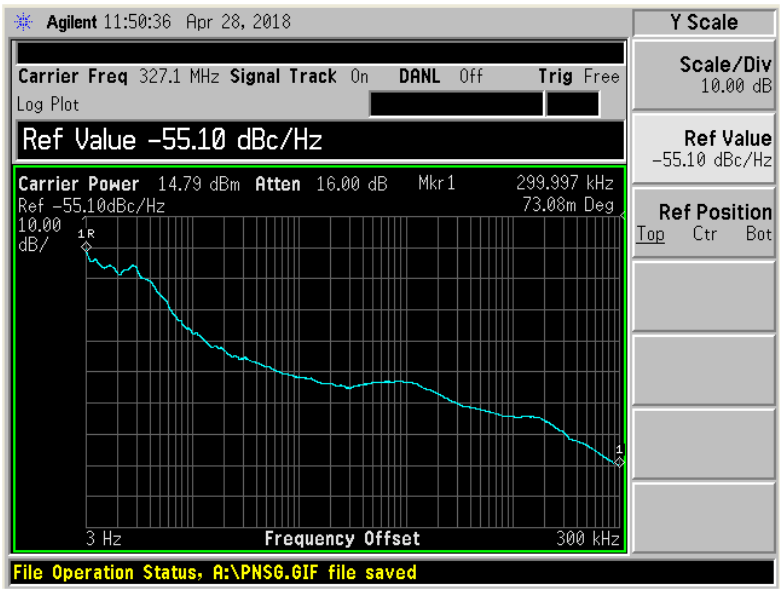

Figure 4.29: Measured phase noise of the cavity field; The integrated phase noise in the cavity single sideband is measured at 0.073°

FIG. 4.30 compares the power spectral density of the RF Signal Generator to that of the cavity pickup signal in pulse mode. As there is a close resemblance between the two waveforms at the RF frequency, this graph also confirms that the phase noise was mainly due to the RF generator.

LLRF linearity measurements

Linearity becomes an important issue when the RF field is changing such as in ramping or pulsed RF applications. System nonlinearities cause actual amplitude/phase of the cavity to deviate at some point from its set value degrading the system accuracy. Also, strong nonlinearities push feedback loops towards becoming unstable. The main contribution to the overall system nonlinearity is usually due to the LLRF or the RF amplifier depending on its type. Klystron amplifiers, for example, are known to have significant nonlinearities at their peak power level. These nonlinearities will therefore be seen in open-loop operation. In closed-loop, however, the nonlinearity of the RF amplifier will be automatically compensated by the integrator part of the regulator (for example, if a PI regulator has been utilized for the feedback loop) provided that no signal becomes saturated. The nonlinearity of the signal path from the cavity pickup loop to the PI regulator will then determine the overall system nonlinearity. This implies that the input stage of the LLRF system, which usually converts the measured cavity voltage to baseband, should be as linear as possible while the linearity of the output stage is of less importance. FIG. 4.30 presents the

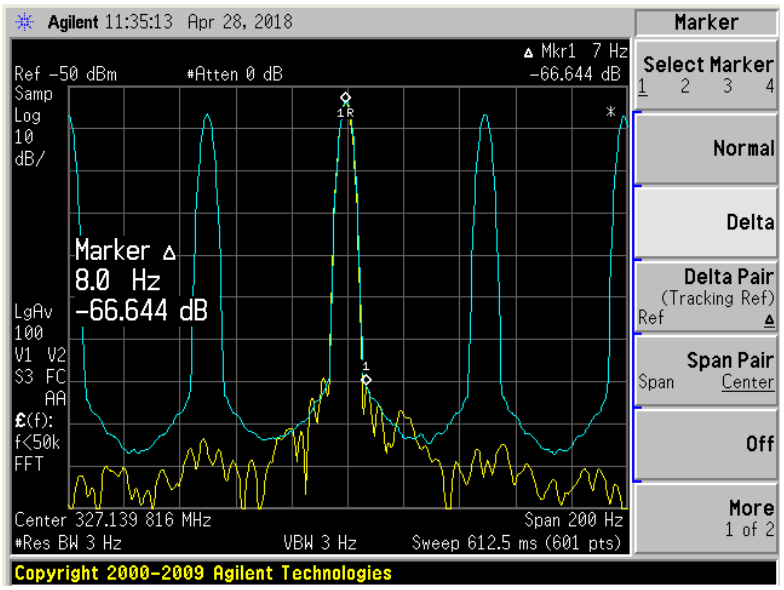

Figure 4.30: Measured power spectral density of the cavity field (upper waveform) and the Signal Generator (lower waveform)

linearity of the regulation loop showing a very good response up to the saturation level of the DACs generating the drive voltage for the IQ modulator. The signal levels are therefore configured so that the maximum amplifier power can be achieved before the DAC becomes saturated.

Transient response in pulsed mode

Transient response deals with issues related to the evolution of the cavity field with time upon a change in the reference level [81]. Also, the response of the regulation loops to the disturbance caused by the beam is studied under this topic [44, 49, 63]. A figure which is widely used to express the speed of field evolution is the time constant assuming that the RF field follows an exponential path when the reference level changes. The cavity transient response, in general, needs to be as fast as possible but should not undergo any overshoot or oscillation. This requirement implies that the LLRF bandwidth should be larger than the cavity bandwidth by a factor of 5-10 and the delay of the electronics be short. Then, the time constant of the feedback loop can be reduced through the adjustment of the regulator gains to be almost equal to the natural time constant of the cavity. Also, the response of the loop to the beam, which acts as disturbance, will be similar to the one of the reference change because the loop dynamics is the same in both cases. FIG. 4.32 and FIG. 4.33 show the pulsed cavity voltage in closed-loop mode and an expanded view of the pulse at the rising edge. The measured settling time is 1.9 μs which is almost the

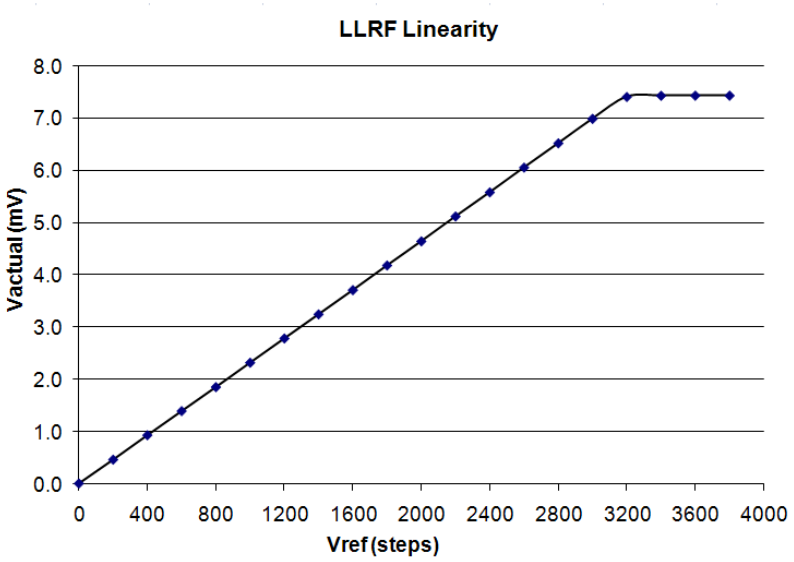

Figure 4.31: Linearity response of the LLRF system in closed-loop mode. The horizontal axis is the reference value of the cavity voltage and the vertical one is the actual cavity voltage measured by a Spectrum Analyzer configured directly in mV unit.

same as the one due to the natural step response of the mock-up cavity. The pulse rise time can be further reduced by injecting more power into the cavity at the rising edge using feed forward control with the hard limit being the maximum available power from the RF amplifier. The PI regulators then guarantee that the field settles at its desired level after the transient period has passed. Similarly, FIG. 4.34 shows the cavity I and Q signals in pulsed mode with the reference cavity phase being set to 45° [22].

LLRF loop stability

A feedback loop in some circumstances becomes unstable. That can happen, for example, if the loop gain is too high, or the loop has severe nonlinearities or long delays. As the loop gets closer to the instability point, larger oscillations become visible on the signals and the amplitude of the oscillations grows until the signals saturate or the interlock system eventually intervenes and stops the plant.

The phase margin of the system was measured simply by changing the amount of the phase shift introduced by the phase shifters shown in Fig. 4.7 and loop instability was observed at ±55° about the optimum phase. Although this is smaller than the simulated phase margin with the mock-up cavity (i.e. ±73°

[22]The instantaneous cavity phase is equal to $arctan(\frac{Q}{I})$.

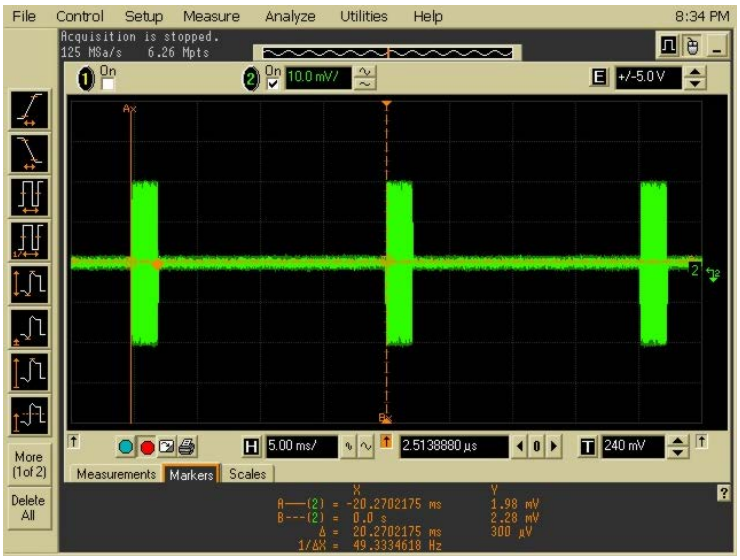

Figure 4.32: Measured cavity voltage in pulsed mode with a pulse rate of 50 Hz and pulse width of 2 ms

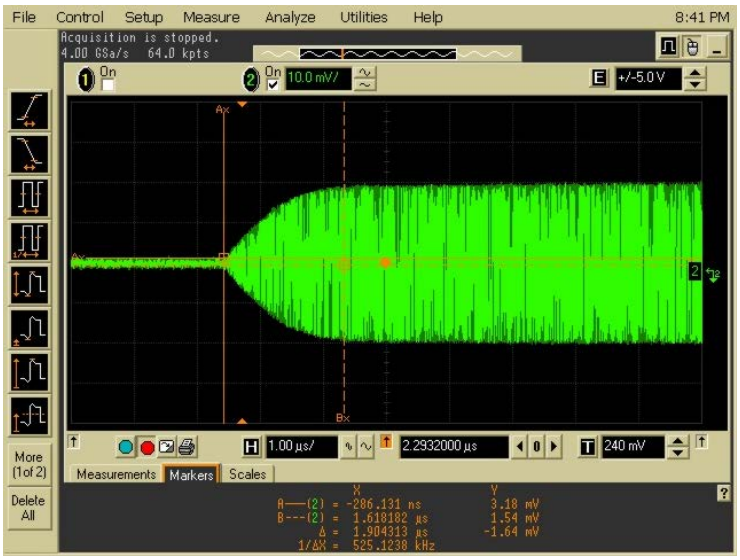

Figure 4.33: Zoomed view of the cavity pulse at the rising edge with a settling time of 1.9 μs

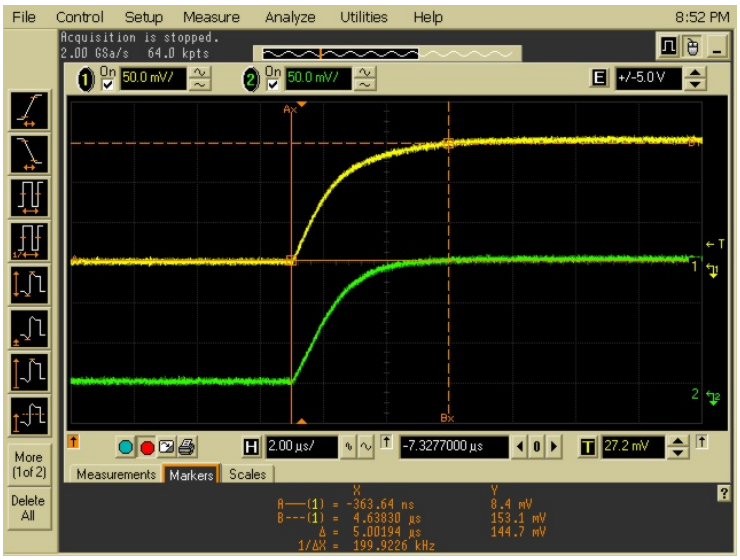

Figure 4.34: Cavity I and Q at the rising edge of the RF pulse with the reference phase being set to 45°

with 800 ns of loop delay), it still provides a very large margin to ensure the loop stability. The difference between the simulated and the measured phase margins is believed to be due to the errors and dynamics which were ignored in the simulations such as the amplifier nonlinearity and the filter dynamics.

Long term tests

The HIL co-simulation of the LLRF system in the Matlab-Simulink environment allows the user to monitor any of the output parameters of the cosim block using the Simulink numerical and graphical displays. In this case, among others, three parameters have been recorded: the LLRF output (i.e, the cavity drive signal), the reflected voltage and the tuner position. Several long term tests were performed in order to check the accuracy of the LLRF system. These tests were done during a period of 100 hours in an unregulated temperature environment with maximum temperature variation of $4°C$. The sample time for all the recorded signals was 15 sec. approximately. The cavity field was measured using the power meter communicating with the Labview program. At the same time, the ambient temperature was recorded using a PT100 temperature sensor and a source meter controlled by Labview as well. The results of these tests are shown in FIG. 4.35.

Note to FIG. 4.35 results:

- These measurements were done using an external FPGA clock running at

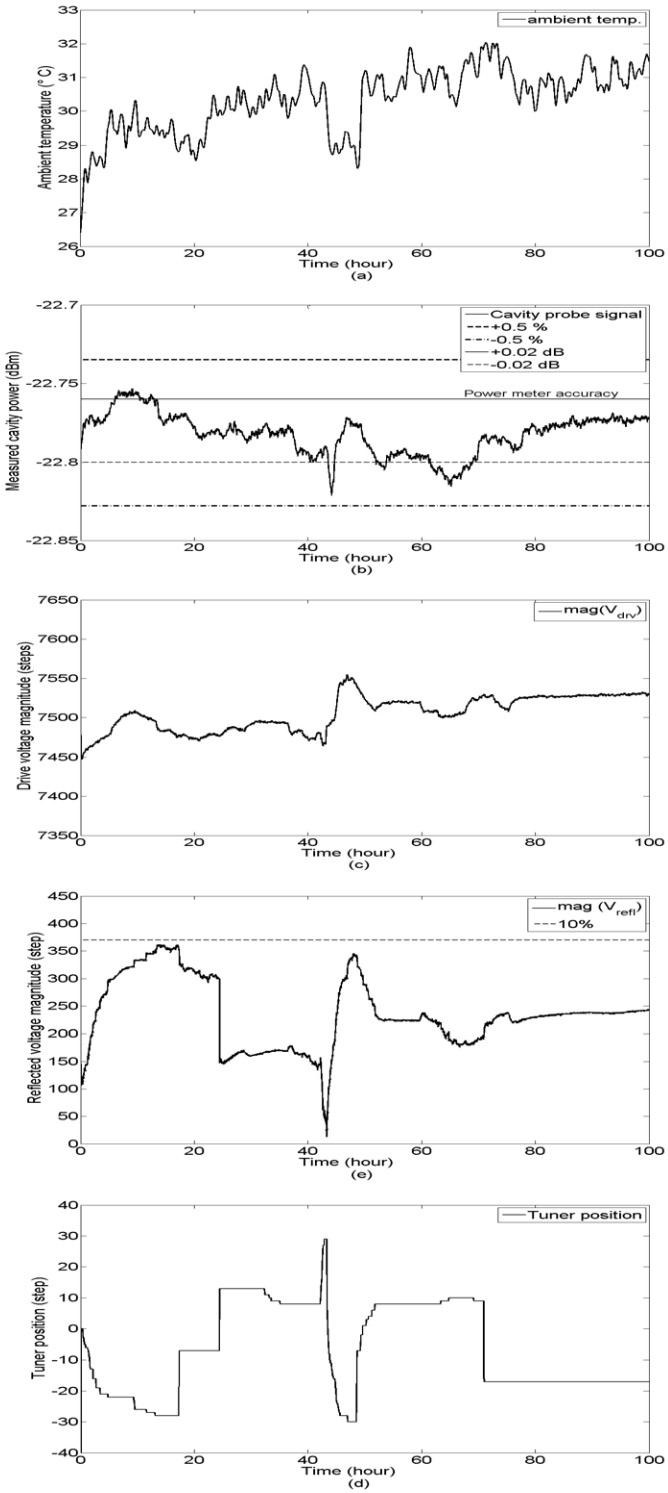

Figure 4.35: 100-h long term stability measurements; from top to bottom: a) ambient temperature, b) cavity power (The $\pm 0.5\%$ lines show the stability requirement and the $\pm 0.02\ dB$ lines correspond to the power meter accuracy) c) amplitude of the forward voltage, d) amplitude of the reflected voltage, e) tuner position (The steps correspond to the resolution of the stepper motor.)

104 MHz.

- The cavity was manually pressed at $t = 18\ h$ to test the tuning loop against mechanical perturbations.
- $Teta\_fwd$ was increased by $3°C$ at $t = 25\ h$ to decrease the reflected voltage.
- The cooling system of the lab. was switched on at $t = 43\ h$ and switched off at $t = 48\ h$ approximately.

From these graphs a few effects degrading the long term stability can be identified. For example, the cooling system of the RF laboratory was switched on at $t = 43\ h$ and switched off at $t = 48\ h$. The effect of these temperature variations on the long-term stability of the cavity field can be seen in the Pcav graph where the $\pm 0.5\%$ stability requirements and the power meter accuracy have also been shown for comparison. Also, it was observed that all the signals were much more stable during nights and weekends as the temperature variations and vibrations caused by the laboratory staff resulted in some stability degradations. This can be clearly seen during $t = 75\ -100\ h$ which corresponds to a weekend. For the final installation, it is planned to minimize these unwanted effects by regulating the ambient temperature and installing the RF transmitter and the cavity in a vibration-free place.

During these tests, the cavity reflected voltage was always below 10% (i.e. 1% of reflected power) as it can be seen in the last figure. The reflected voltage can be further reduced by choosing a narrower error window at the expense of moving the tuner more frequently. If the window is too narrow, the tuner will vibrate at its position due to the noise on the measured phases. In the LLRF tests, tuner vibrations were observed with $(+ph\_thresh, -ph\_thresh) = (+0.2°, -0.2°)$. For normal operation, the error window was set to $(+0.4°, -0.4°)$.

More long term tests were performed with the FPGA being clocked by its internal oscillator. As these tests gave similar results, for simplicity reasons, they are not included here.

4.6.3 Tests with the RFQ cold model

The design/manufacturing of the RFQ cold model, which was used for the LLRF tests, is the same as the one intended for the future RAL-FETS except the length which is 40 cm instead of the desired length of 1 m for each RFQ section. Because of this and due to the effect of the flat end plates the resonant frequency and the unloaded quality factor of the cold model are different from the final ones (319 MHz and 7773 instead of the expected 324 MHz and 9000 for the final RAL-FETS RFQ) [95]. The preliminary results obtained from these tests are similar to the ones from the mock-up cavity except the settling time which is significantly longer due to the increase of the quality factor (see Fig. 4.36). Looking at the rising edge of the pulse, two time constants can be distinguished. The shorter one ($\tau \approx 6\ \mu s$) which happens first is due to the

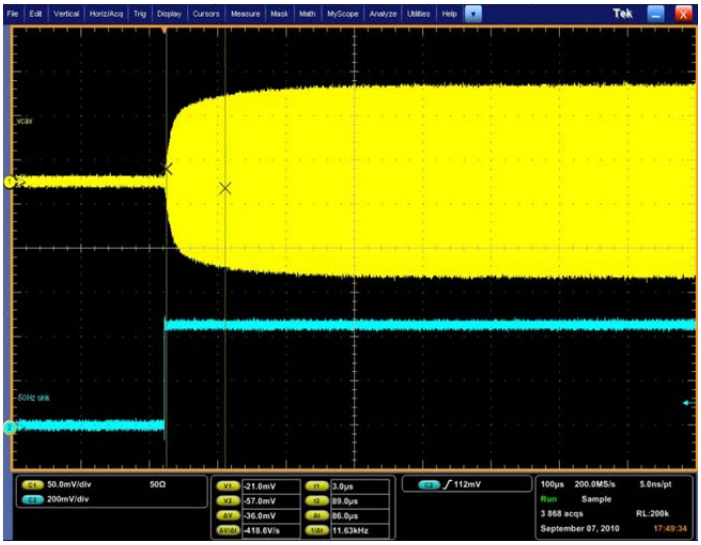

Figure 4.36: Measured RFQ voltage in pulsed mode; the settling time (100 μs approximately) can be further reduced by a readjustment of the PI gains and/or feed-forward control.

RFQ and amplifier dynamics when the P control has dominant effect while the longer one is due to the integral part of the PI regulator (it can be reduced through a readjustment of the PI gains).

Tuning an RFQ is not a trivial task due to its mode spectrum. While in a pillbox cavity it is rather easily to lock on the desired (lowest TM01) resonant mode which is usually far from higher modes, in an RFQ three independent azimuthal modes exist being one quadrupole and two dipole modes. The quadrupole mode is formed by the magnetic flux from each vane splitting in two halves each flowing around the tip of the vane and returning in the two adjacent quadrants. The dipole modes, on the other hand, are formed by each pair of the opposite vanes [93]. From flux conservation, the azimuthal sum of the fluxes in the four quadrants is equal to zero. When the RFQ is properly tuned, the amplitudes of the fluxes in all the four vanes are equal minimizing the amplitude of the dipole modes and resulting in best approximation to a pure quadrupole operating mode. If the RFQ is not well tuned, the amplitudes of the four fluxes are not equal and the cavity mode will be an admixture of the quadrupole mode and the two dipole modes. In the RFQ mode spectrum, it can be seen that the frequency of the dipole modes lies typically a few percent lower than that of the operating quadrupole mode introducing the possibility of accidentally exciting a higher longitudinal mode of the dipole family [93].

The tuning tests with the RFQ cold model were done with one motorized tuner mounted in one RFQ quadrant and three manual tuners on the other three quadrants. It was then observed that at a specific position of the motorized

Table 4.6: DLLRF performance summary

Parameter	Spec.	Actual	Unit
Operation mode	Pulsed	CW/Pulsed	
Settling time	≤ 100	< 100	μs
Loop delay		800 app.	ns
Phase noise	± 0.5	$< \pm 0.1$	$^\circ$
Short-term amp. stability	± 0.5	$< \pm 0.1$	%
Long-term amp. stability	± 0.5	$< \pm 0.5$	%
Linearity		100 app.	%
Dynamic range		> 30	dB
Phase margin		$\geq \pm 55$	$^\circ$
Max. reflected power		< 1	%

tuner there was a sudden jump in the $ph(V_{fwd}) - ph(V_{cav})$ due to the excitation of the dipole modes causing tuner vibrations. This usually happened half an hour after the system start-up when the RFQ temperature rose up and the motorized tuner reached that specific point. Due to this reason, for the case of RAL RFQ, it is foreseen to replace the manual tuners with motorized ones so that all the four tuners move in parallel, hence keep a good separation between the quadrupole and dipole modes [94]. Similarly, in the case of ESS-Bilbao RFQ, it is planned to move the tuners of the RFQ together (at least the ones belonging to the same RFQ section) so that a large separation between the quadrupole and dipole modes is preserved[23].

TABLE 4.6 summarizes the main LLRF parameters measured during the tests and compares them to the specifications[24].

4.7 Summary and concluding remarks

Design, simulation, implementation and experimental results of the ESS-Bilbao DLLRF have been discussed in this chapter. A general description of the ESS-Bilbao Linac is given followed by the specifications of its RFQ system. The designs of amplitude/phase and tuning loops which are based on an analog front-end and an FPGA unit have been discussed in detail. As the accuracy of the probe voltage conversion to baseband I/Q plays a significant role in the performance of the proposed DLLRF, errors inherent to analog IQ demodulators have been identified and compensated by FPGA algorithms and proper setting of the control loop parameters. The LLRF feedback loop is then simulated in MATLAB-Simulink for pulsed operation using the cavity equations developed in Chapter 2. Moreover, the effect of the other resonant modes on the stability of the feedback loops has been studied and compared to some other machines such as the ILC and the European XFEL. These results show that due to the large

[23]This is supposed to be larger than 8 MHz from the RFQ electromagnetic simulations.
[24]The settling time with the final RFQ is estimated at 30-50 μs.

separation of the undesired resonant modes from the operating mode, klystron bandwidth, DLLRF design and the adopted control strategy, such instabilities are very unlikely for the ESS-Bilbao accelerating structures.

In the continuation, details of the units comprising the complete DLLRF system are given followed by a description of the FPGA program and the procedure for the setting of the control loop parameters. The validity of the proposed design is ensured by experimental tests with a 324 MHz mock-up cavity at the RF laboratory of the UPV/EHU University and an RFQ copper model at the Imperial College London. The important LLRF parameters such as the short and long term stabilities, linearity, bandwidth, transient response and phase margin have been measured and compared to the specifications. The stability tests verify the DLLRF ability to meet the $\pm 0.5\%$ stability requirements even in an environment subjected to temperature variations and vibrations. Furthermore, it has been shown that the stability can be further improved provided that the temperature changes and vibrations are minimized. The linearity tests show a highly-linear response in a dynamic range larger than 30 dB thus verifying the effectiveness of the error compensation algorithms. Moreover, the transient response tests verify that a large loop bandwidth in the order of few hundred kHz would be achievable to suppress the HVPS ripples and other disturbances. These tests also show that due to the high bandwidth of the analog and digital circuits a settling time smaller than 100 μs would be easily achievable with the RFQ. Finally, the tests show a phase margin as large as $\pm 55^{\circ}$ thus providing adequate safety margin to ensure the loop stability.

Chapter 5

Concluding remarks and future works

5.1 Concluding remarks

5.1.1 RF cavity modeling and simulation

RF cavities modeling and simulation in the context of particle accelerators has been discussed in Chapter 2. The accelerating RF cavity and its input power coupler, in their general form, have been modeled as a shunt RLC circuit and a step-up transformer respectively. The RF amplifier has been modeled as a current source supplying the cavity through a transmission line with a characteristic impedance Z_0. Although this generic model can explain some of the most important aspects of the cavity, two additional considerations are still required so that the model leads to correct and informative results. These are 1) cavity impedance mismatches to the transmission line and 2) cavity transient response. In the existing articles on cavity modeling and simulation, however, one or both of these issues are often overlooked depending whether the cavity is being looked at from a high-power or a LLRF perspective. These drawbacks have been resolved in this chapter by calculating the cavity transfer function using the Laplace notation and taking into account the effect of the input coupler on the cavity impedance. Considering the cavity model, the following two conditions will be required for making sure that all the forward power enters the cavity without beam: 1) the turn ratio of the transformer should be chosen so that it matches the cavity shunt impedance to Z_0 (i.e. coupling factor equal to one) and 2) the cavity resonant frequency should be equal to the RF frequency (i.e. detuning equal to zero). Any coupling factor and detuning other than these, will then cause part of the amplifier power to reflect from the cavity. Moreover, in the transient simulations it can be seen that changing the coupling factor and detuning can degrade the cavity transient response due to voltage overshoots and oscillations. These issues have been discussed in detail both

analytically and by computer simulations.

In the continuation, the cavity model has been modified so that it also represents the beam loading effect. This has been done by adding another current source, representing the beam, to the cavity model and applying the superposition theorem to calculate the total cavity voltage due to the amplifier and the beam. As the previous values of the coupling factor and detuning only result in zero reflected power under no-beam conditions, new values for these parameters have been calculated to suppress the reflected power for a certain beam current and phase. The results have been verified by computer simulations and a few examples using the ALBA RF parameters. The developed model has been used in the following chapters for closed-loop simulations of the ALBA RF cavity and the ESS-B RFQ.

5.1.2 ALLRF system for the ALBA booster

In chapter 3 the design, simulation, implementation and experimental results of the ALBA ALLRF system have been discussed. The specifications of the ALBA RF/LLRF systems are given followed by a description of the ALLRF design for the amplitude and phase loops. In order to simulate the performance of the I and Q loops under beam loading, a baseband-equivalent model for the cavity has been developed in MATLAB-Simulink with the advantage of significantly improving the simulation speed compared to the conventional models available in the literature. Moreover, as this model is based on the cavity equations developed in Chapter 2, it also takes into account the influence of the input coupler on the cavity impedance mismatch, hence provides an effective and reliable test bench for transient-time LLRF simulation and analysis. The model has been then applied to the ALBA RF/LLRF to study the effect of the system start-up and phase/delay errors on the performance of the feedback loops under beam loading. In the continuation, design of the main circuits comprising the complete ALLRF system has been discussed along with a description of how these circuits are put together to assemble the ALLRF units. Also, the design of the Graphical User Interface of the ALLRF has been presented with an explanation of the important LLRF parameters to be monitored and controlled from the ALBA control room. In the continuation, the experimental results obtained at the CELLS and ELETTRA high power RF laboratories are given. Various types of tests have been done at low and high RF power levels to check the performance of the LLRF loops, hence assert its suitability for the ALBA machine. In the case of amplitude and phase regulation, for example, the results have verified the ability of the ALLRF to compensate ripples up to 10 kHz and above in addition to having a short settling time in the order of 20 μs. The ramping tests, on the other hand, have shown that a highly-linear response in a dynamic range larger than 26 dB is achievable for the cavity voltage. In order the check the ALLRF performance under a simulated beam, a controlled signal with f=500 MHz has been added to the LLRF output. The amplitude and phase of this signal have been then adjusted so that it simulates a real beam for the LLRF system. The results obtained from these tests, on one hand, have

shown that amplitude and phase stabilities down to a fraction of 1% and 1° are achievable and on the other hand have proved that the ALLRF circuits have a large enough voltage range to counteract the beam loading effect without being saturated. Moreover, these tests have been found to be very useful from a training point of view as they give a good insight on how the beam acts on the cavity field and how the ALLRF system should be operated under a real beam.

5.1.3 DLLRF system for the RAL-FETS RFQ and the future ESS-Bilbao linac

In chapter 4 the design, simulation, implementation and experimental results of the ESS-Bilbao DLLRF system have been discussed. A general description of the ESS-Bilbao linac has been given followed by the specifications of its RFQ system. The designs of amplitude/phase and tuning loops which are based on an analog front-end and an FPGA unit have been discussed in detail. As the accuracy of the probe voltage conversion to baseband I/Q has been found to play a significant role in the performance of the DLLRF, errors inherent to analog IQ demodulators have been identified and compensated by FPGA algorithms and proper setting of the control loop parameters. The LLRF feedback loop has been then simulated in MATLAB-Simulink for pulsed operation using the cavity equations developed in Chapter 2. Moreover, the effect of the other resonant modes on the stability of the feedback loops has been studied and compared to some other machines such as the ILC and the European XFEL. These results have shown that due to the large separation of the undesired resonant modes from the operating mode, klystron bandwidth, DLLRF design and the adopted control strategy, such instabilities are very unlikely for the ESS-Bilbao accelerating structures.

In the continuation, details of the units comprising the complete DLLRF system have been given followed by a description of the FPGA program and the procedure for the setting of the control loop parameters. The validity of the proposed design has been ensured by experimental tests with a 324 MHz mock-up cavity at the RF laboratory of the UPV/EHU University and an RFQ copper model at the Imperial College London. The important LLRF parameters such as the short and long term stabilities, linearity, bandwidth, transient response and phase margin have been measured and compared to the specifications. The stability tests have verified the DLLRF ability to meet the $\pm 0.5\%$ stability requirements even in an environment subjected to temperature variations and vibrations. Furthermore, it has been shown that the stability can be further improved provided that the temperature changes and mechanical vibrations are minimized. The linearity tests have shown a highly-linear response in a dynamic range larger than 30 dB thus verifying the effectiveness of the error compensation algorithms. Moreover, the transient response tests have shown that a large bandwidth in the order of a few hundred kHz would be achievable to suppress the HVPS ripples and other disturbances. These tests have also shown that due to the high bandwidth of the analog and digital circuits a settling time smaller than 100 μs would be easily achievable with the RFQ. Finally, the stability tests have

shown a phase margin as large as $\pm 55^{\circ}$ thus providing adequate safety margin to ensure the loop stability. In general it has been found that the proposed digital solution for the LLRF problem has many advantages with respect to pure analog solutions, in terms of versatility, flexibility and robustness, while fullfilling the required specifications of the accelerating structures to which it will be applied.

5.2 Future works

The following works are suggested for the follow-up of the current thesis:

5.2.1 Cavity modeling and simulation

The RLC model presented in chapter 2 only considers the operating mode of the cavity. This model can therefore be expanded taking into account the cavity HOMs[1]. Although HOMs don't have to be dealt with in normal LLRF operating conditions, they will become of great importance for beam stability studies. Also, based on the transient HOM model, a feedback loop can be designed for damping the undesired HOMs to provide a larger stability margin for the beam. The feedback loop for HOM damping can then be used as a replacement of the traditional HOM dampers which are usually available in the form of special couplers absorbing the RF power confined in a series of undesired resonant modes and dissipating them in a load with a potential undesired effect on the operating mode.

5.2.2 Analog LLRF

Although the ALLRF system was originally designed and developed for the ALBA booster, because of its versatility, low cost and ease of use it could also be a suitable candidate for other LLRF applications with a wide range of RF frequencies when moderate amplitude and phase stabilities in the order of 1% and 1° are required. It is therefore worth studying in more detail the suitability of using this LLRF for other applications. This is believed to be possible after making minor modifications in the LLRF design/implementation.

The results presented in chapter 3 were obtained with the prototype ALLRF system with home-made PCBs and a minimum shielding for the electronics. Therefore, they can be further improved if the circuits are replaced with professionally-fabricated ones with adequate shielding. Also, a high quality RF signal generator can improve the short term stability because of its lower output noise.

The results presented in the Experimental Results section (section 3.3) were obtained without beam. Therefore, it would be very interesting to repeat them in a synchrotron ring to check the LLRF performance under a real beam.

The results presented under the *Virtual Beam* topic can be very useful from a training point of view. As the presence of the beam pushes the electronics

[1] Higher Order Modes

towards saturation, it is important to ensure that the electronics have enough dynamic range so that they can successfully counter-act the beam loading effect. On the other hand, it is a good practice to simulate the beam loading effect for the LLRF before operating it under a real beam to see how it would change the amplitude and the phase of the cavity voltage if not compensated and how the feedback loop parameters should be properly adjusted to remove that disturbance.

5.2.3 Digital LLRF

The closed-loop model which is presented in section 4.3 only deals with the most important parts of the feedback loop with the biggest impact on the LLRF performance. Although this is sufficient for the current analysis, a more detailed model can be created considering, for example, the klystron nonlinearities, the filter dynamics and the amplitude/phase imbalances of the IQ demodulator.

Although the experimental tests proved that the DLLRF system can work successfully with different types of cavities, its performance can still be improved by slightly modifying the design especially in the FPGA program. For example, in the current version, little effort has been made in using less FPGA resources for the control loop implementation such as the number of Simulink blocks and the input and output ports for the FPGA. Also, it is possible to further reduce the group delay by a more careful use of the system generator blocks and the routing of the signals.

The current results are obtained in a laboratory environment with a minimum shielding for the electronics. In real operating conditions in the future linac, the environmental noise will be significantly higher; therefore a better protection of the electronics against noise will be a must. Also, many other issues will have to be addressed when the LLRF system is connected to the RF transmitter and the cavity and operated under high power. These issues should therefore be studied in details in the future when the high power parts will become available.

Similar to the ALLRF, it would be highly interesting to repeat the tests in the future with the real RF transmitter and the real RFQ, when they become available, and compare them to the ones obtained with the mock-up cavity and the RFQ cold model.

5.2.4 BPM system

Appendix A presents the preliminary design of the beam position monitoring system for the ESS-Bilbao linac. The developed electronics for this BPM system is based on an analog front-end including an IQ demodulator and a FPGA digital unit. Due to the similarity of the BPM electronics to the DLLRF, this system is briefly discussed and summarised in the Appendix A. Although the first results obtained from the BPM electronics and its test bench are promising, the system still needs to go through a long process of modification and improvement so that

it becomes suitable for being used in the future ESS-Bilbao linac. In this respect, the following improvements are proposed for each part of the BPM system:

As it is mentioned in the Appendix A.1, a strip-line detector would be a better choice for the ESS-Bilbao proton linac compared to the capacitive button detector which was used in the tests. It is therefore suggested to replace the current detector with a strip-line one properly designed and built for the linac.

Similar to the LLRF systems, the front-end electronics still need some improvements so that they become suitable for being used under real operating conditions. This includes shielding for the circuits, properly mounting them in units with a solid ground for the signals and minimizing the temperature variations to prevent the signals from floating.

The current FPGA program for beam position calculation is very basic. Some important part of the program such as linearization and calibration are either missing or under development. These parts should therefore be added to the program in the newer versions. Also, the current FPGA program is only intended for one BPM while in the future, one FPGA unit is planned to be used for up to 3 BPMs. These issues should therefore be taken into account in the future versions of the FPGA program.

Appendix A

BPM System for ESS-B and IFMIF-EVEDA

A.1 Introduction

The objective of this project, which is being done in collaboration with CIEMAT-Madrid, is to design and develop a BPM system for the IFMIF-EVEDA accelerator and the future ESS-B linac[1]. Due to the similarity of the BPM electronics to the LLRF system, it was later decided to append to this thesis some basic contents of this project so that it also covers the basic design of the BPM system and the preliminary results obtained with a BPM test bench at the RF laboratory of the UPV/EHU University.

The BPM system described herein can be used to measure the transversal position of the beam center in the beam pipe. This is done by measuring the amplitude of the voltages induced in the BPM detector with the passage of each bunch and calculating the X and Y positions using the well-known delta-over-sigma method. Two types of detectors are commonly used in particle accelerators being electrostatic (capacitive) buttons and strip-lines. Although the strip-line detector is in general a better choice for relatively long bunches due to the larger induced voltage [113, 115], as the first step, a button-type test bench was used for the tests because of the collaboration agreement with Ciemat [79]. The capacitive detector, however, is planned to be replaced in the future with a strip-line detector as that will increase the level of the induced voltages, thus improving the signal to noise ratio. The amplitudes of the voltages induced in the four buttons are then measured using an analog front-end unit based on logarithmic amplifiers. The baseband outputs of the front-end unit are in the next stage sampled by fast ADCs and fed into a FPGA unit for the required signal processing including low-pass filtering, offset compensation, X and Y calculation and linearization purposes. This, in the end gives the beam

[1]The BPM system described herein is a project defined in the frame of the ESS-B RF and diagnostics groups.

Table A.1: Main IFMIF-EVEDA BPM parameters

Parameter	Value	Unit
Beam energy	5-9	MeV
Beam current	90-126	mA
RF pulse width	200-CW	μs
Duty cycle	0.1-CW	%
Position resolution	10	μm
Position precisin (absolute)	100	μm
Phase resolution	0.3	$^\circ$
Phase precision (absolute)	2	$^\circ$
Number of buttons per BPM	4	
Input power range	50	dB
Maximum input power w/o att.	+30	dBm
Maximum input power with att.	-10	dBm
Minimum input power	-60	dBm

position with a resolution of 10 μm or better.

In addition to the beam position measurement, the current BPM system can be used to measure the beam current and phase (with respect to the master oscillator). This is done by adding together samples of the four signals from the detector and feeding the resultant signal into an IQ demodulator in the front-end with the I/Q signals being fed into a CORDIC block in the FPGA. The amp/ph outputs of the CORDIC block will then give an estimate of the beam current and phase.

In this appendix, first, a brief description of the BPM system consisting of the detector, the analog electronics and the FPGA unit is given followed by the implementation of these parts and finally, the results obtained on a test stand with a simulated beam.

A.2 Main Parameters and system description

TABLE A.1 summarizes the main parameters of the beam, precision requirements and signal levels at the entrance of the BPM electronics [114]. These parameters are therefore used in the design of the BPM electronics which is presented in the following subsections.

The BPM electronics consists of an analog front-end where the BPM signals are filtered, conditioned and converted to base-band and a digital unit to sample the baseband signals and calculate the beam position, current and phase.

For the final deployment, the digital unit will have a cPCI connection to an industrial PC running under Linux where the required EPICS drivers will be installed. The interface between the industrial PC and the global EPICS control system will be Ethernet. For the BPM test bench, though, the industrial PC has been replaced by a local PC connected to the FPGA unit via the PCIe port from

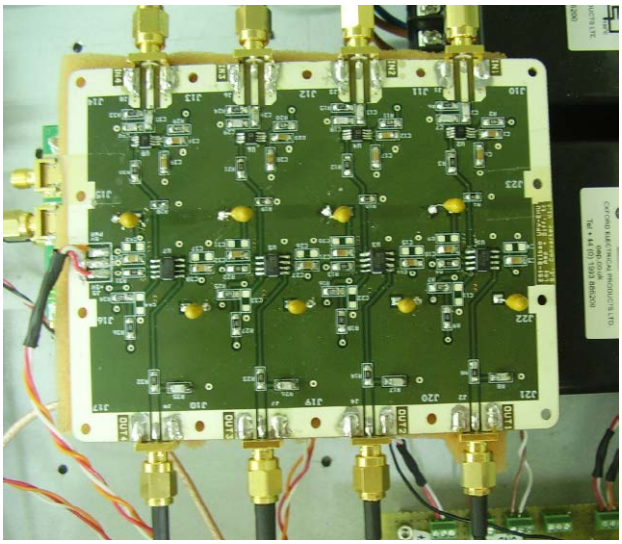

Figure A.1: Picture of the log-amp board, The amplitudes of the induced voltages in the BPM buttons are measured by four AD8310 logarithmic amplifiers and then buffered and conditioned by four AD8130 differential amplifiers before being sampled and fed into the FPGA.

where the operator can control the whole BPM system in a MATLAB-Simulink environment.

The BPM system consists of an Analog front-end, a digital unit and a test-bench as explained in the following:

A.2.1 The Analog Front End (AFE) Unit

This unit consists of an in-house developed board comprising 4 logarithmic amplifiers (AD8310 [117]) and 4 four differential-receiver amplifiers (AD8130 [15]) as shown in Fig. A.1.

The induced voltage on each button is fed into one input channel of the front-end unit to measure its amplitude. The logarithmic amplifier has a dynamic range of 95 dB, bandwidth of DC - 440 MHz and a typical rise time of 15 ns. The input channels have been designed to have an impedance of 50 Ohm, hence avoid signal degradations due to impedance mismatches and reflections. The analog front-end unit additionally includes one IQ demodulator (AD8348 [14]) to measure the beam phase and intensity. In this case, four directional couplers are used giving samples of the button voltages before being fed into the log-amp board. These four signals are then added together and used as the RF input of the IQ demodulator board. The resultant I and Q signals, after being buffered and conditioned by a home-made board (based on AD8130), are converted to digital and fed into the FPGA for the subsequent processing.

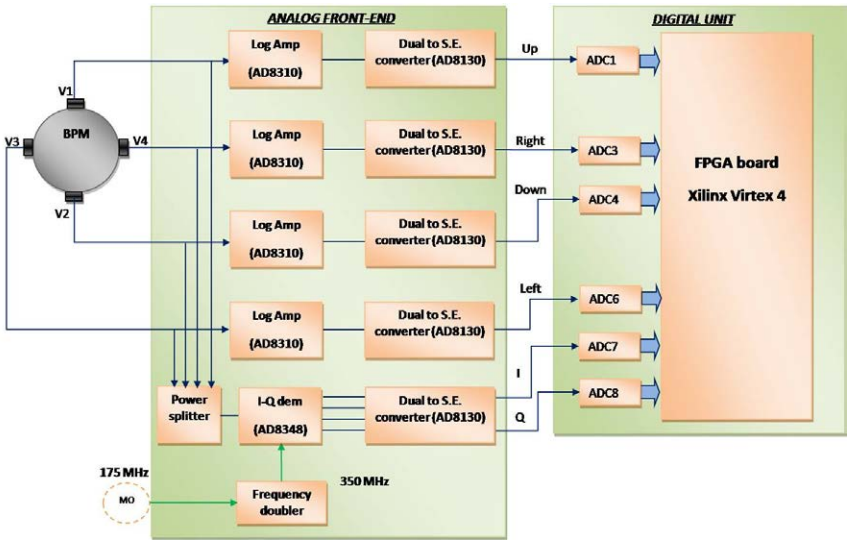

Figure A.2: Simplified schematics of the BPM detector and its electronics; the amplitude of the induced voltages on the buttons are measured by the logarithmic amplifier board and then fed into the digital unit to calculate the X and Y position. Similarly, samples of the four signals are added together and used as the input of an IQ demodulator to calculate the beam intensity and phase.

FIG. A.2 shows a simplified schematic view of the BPM electronics.
FIG. A.3 shows a picture of the analog front-end unit.

A.2.2 The Digital Unit

The Digital Unit includes the FPGA and the ADC boards (VHS-ADC from Lyrtech). This is a high performance cPCI digital board (with cPCI to 4x PCIe interface for local PC connection) based on a Virtex-4 FPGA from Xilinx and eight AD6645 ADCs with a resolution of 14 bits and maximum sampling rate of 105 MSPS [21]. The board also incorporates 128 MB of SDRAM for data buffering on the FPGA. In order to provide the FPGA board with 8 additional ADC channels, an add-on ADC module has also been purchased and mounted on the FPGA board. Each digital unit can then be used to fully measure up to two BPMs simultaneously or alternatively up to three BPMs if only one BPM out of these three is used for beam phase and intensity measurements. For FPGA programming, the model-based approach [24] and the Xilinx System Generator [25] have been used as this significantly shortens the programming time and effort compared to the VHDL method.

The FPGA program consists of several parts including offset compensation blocks, filtering, gain adjustment, and delta-over-sigma for X and Y position measurements in CW/pulsed modes. The program also includes the required

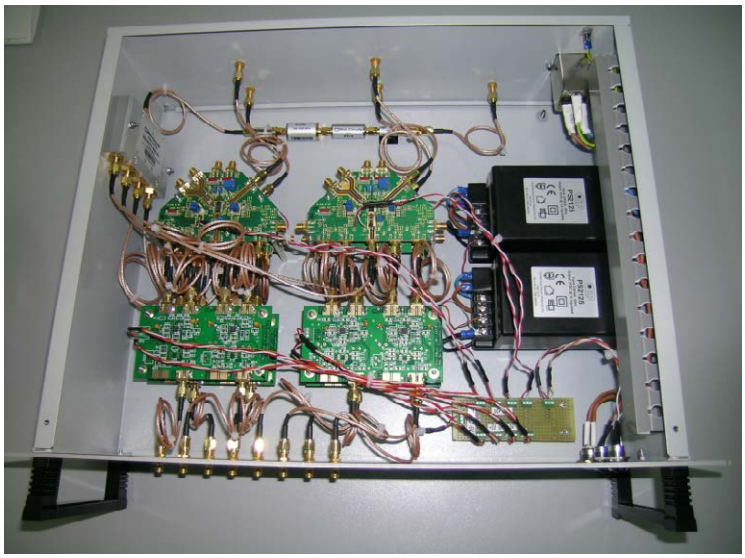

Figure A.3: Picture of the first version of the analog front-end unit

blocks to measure the beam current and phase and a linearization algorithm currently under development.

A.2.3 BPM test bench

In order to test the performance of the BPM electronics with a simulated beam, a test bench is needed. This is basically a table with a moveable tube where the four BPM buttons are mounted and a fixed internal tube fed by an RF generator to simulate the beam as shown in Fig. A.4.

The test bench is connected to the AFE and digital units explained earlier to calculate the beam position, phase and intensity and finally a local computer communicating with the digital unit to monitor the FPGA output and/or set the input parameters. The design of the BPM test bench is so that it provides a good impedance match to the RF generator, hence minimizes power reflections from the tests bench. The X and Y position of the internal tube are changed with respect to the outer tube using the corresponding knobs and that accordingly changes the amplitude of the induced voltages on the buttons due to the changes in the distance between the internal tube and each button.

A.3 Practical Results

Fig. A.5 shows the measured resolution of the BPM electronics verifying that beam displacements down to 5 μm could be measured with the current system.

Likewise, Fig. A.6 shows the BPM response after applying the linearization

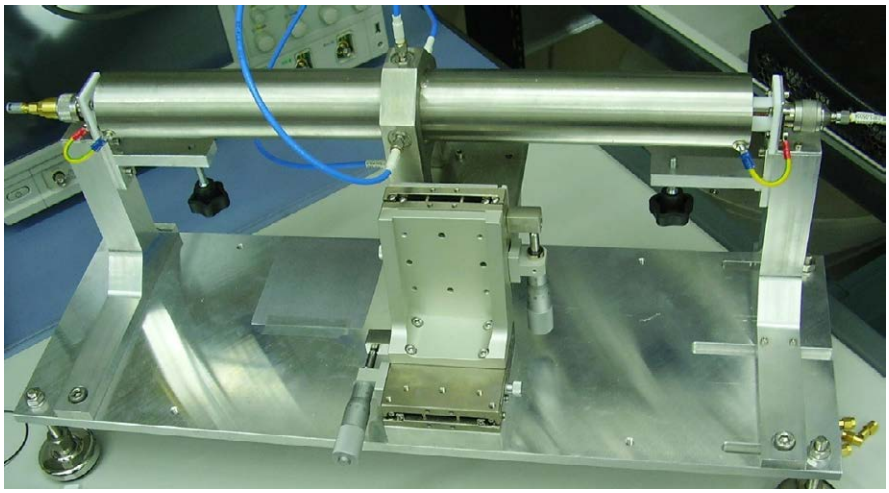

Figure A.4: Picture of the BPM test bench

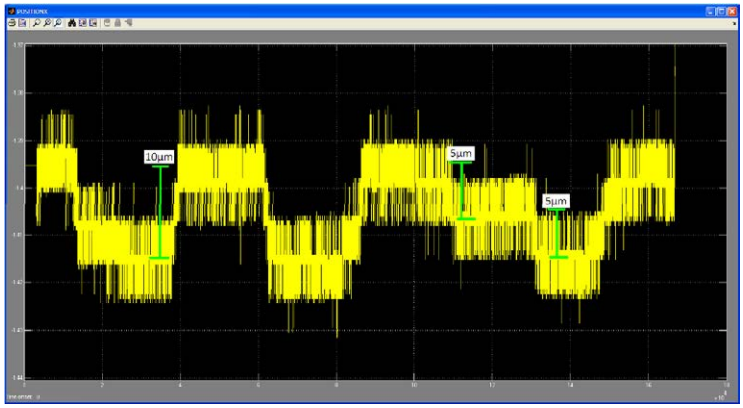

Figure A.5: Measured X position with displacements of 5 μm and 10 μm

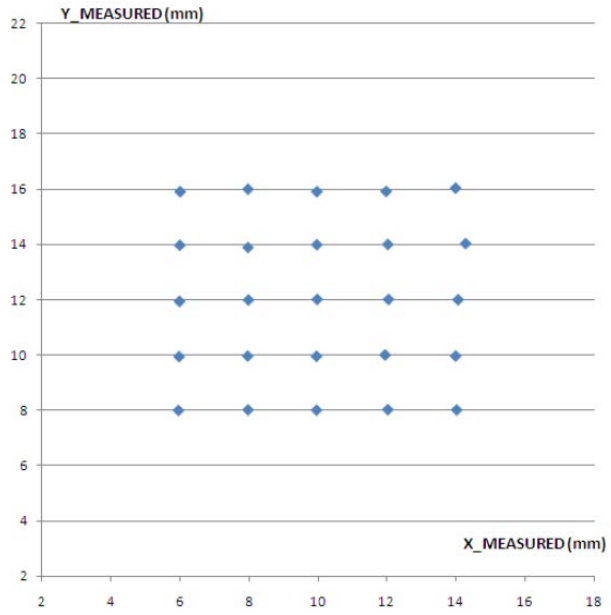

Figure A.6: Measured linearity response of the BPM system after applying the linearization algorithm; the graph shows the measured X and Y positions while the actual X and Y positions were incremented by 2 mm in each step.

algorithms with the actual X position changing from 6 mm to 14 mm and actual Y from 8 mm to 16 mm. The imperfections of the results are due to the positioning and measurement errors (they will be removed in the final version).

In order to check the accuracy of the measurement, the system was put into operation continuously during a period of 14 hours. The maximum drift of the measured X and Y positions were recorded at 50 μm and that of the beam phase was measured at 1.3° verifying that the actual results meet the requirements (100 μm and 2° respectively). These results, however, are supposed to be further improved in the future as more modifications will be made in the design and the setting of the parameters.

TABLE A.2 presents a summary of the BPM measurements and compares these results to the specifications verifying the viability of the BPM system to meet the specifications.

Table A.2: BPM performance summary

Parameter	Measured	Specifications	Unit
X position resolution	$\leq$5	10	μm
Y position resolution	$\leq$5	10	μm
X position precision (absolute)	49	100	μm
Y position precision (absolute)	50	100	μm
Phase resolution	0.2	0.3	$^\circ$
Phase precision (absolute)	1.3	2	$^\circ$

Appendix B

List of publications

- H. Hassanzadegan, N. Garmendia, V. Etxebarria, F.J. Bermejo, *Low level rf system for the European Spallation Source's Bilbao linac*, Physical Review Special Topics - Accelerators and Beams, **Vol. 14**, n.5, pp. 052803-1, 052803-16 (2011), DOI: 10.1103/PhysRevSTAB.14.052803

- D. Belver, I. Arredondo, M. del Campo, P. Echevarria, J. Feuchtwanger, N. Garmendia, H. Hassanzadegan, L. Muguira, F.J. Bermejo, V. Etxebarria, J. Jugo, and J. Portilla, *Overview of the BPM system of the ESS-Bilbao*, Proceedings of the 10th European Workshop on Beam Diagnostics and Instrumentation for Particle Accelerators DIPAC2011. Hamburg, Germany, 16-18 May (2011)

- P. Echevarria, I. Arredondo, D. Belver, M. del Campo, N. Garmendia, H. Hassanzadegan, L. Muguira, V. Etxebarria and J. Jugo, *Multipurpose controller based on a FPGA with EPICS integration*, Proceedings of the 2011 Particle Accelerator Conference PAC'11. New York, 28 March-1 April, pp. WEOBN4-1-3 (2011)

- H. Hassanzadegan, R. Griñó, *A Transient Model for RF Cavity Analysis under Beam Loading*, Nuclear Instruments and Methods in Physics Research A **615**, p. 143-157, (2010)

- V. Etxebarria, J. Lucas, J. Feuchtwanger, A. Sadeghzadeh, H. Hassanzadegan, N. Garmendia and J. Portilla, *Very High Sensitivity Displacement Sensor Based on Resonant Cavities*, IEEE Sensors Journal, **Vol. 10**, No. 8,(2010)

- I. Bustinduy, D. De Cos, S. Jolly, J.K. Pozimski, P. Savage, J. Feuchtwanger, F.J. Bermejo, V. Etxebarria, N. Garmendia, H. Hassanzadegan, J. Portilla, A.P. Letchford, *Beam Dynamics Studies on the Radio-Frequency Quadrupole for the Bilbao Accelerator*, Proceedings of the 1st International Particle Accelerator Conference IPAC'10. Kyoto, Japan, 23-28 May, pp. 4214-4216 (2010)

- H. Hassanzadegan, M. Eguiraun, N. Garmendia, F. J. Bermejo, V. Etxebarria, D. Findlay, A. Letchford, *Design and Implementation of a Pulsed Digital LLRF System for the RAL Front End Test Stand*, Proceedings of the 1st International Particle Accelerator Conference IPAC'10. Kyoto, Japan, 23-28 May (2010), pp. 1458-1460

- A.P. Letchford, M.A. Clarke-Gayther, D. Faircloth, S.R. Lawrie, M. Perkins, P. Wise, A. Kurup, S. Alsari, S. Jolly, D.A. Lee, P. Savage, J.K. Pozimski, C. Gabor, C. Plostinar, J. Back, F.J. Bermejo, R. Enparantza,I. Ariz, P. Romano, A. Sedano, V. Etxebarria, H. Hassanzadegan, N. Garmendia, M. Eguiraun, *Status of the RAL Front End Test Stand*, Proceedings of the 1st International Particle Accelerator Conference IPAC'10. Kyoto, Japan, 23-28 May, pp. 642-644 (2010)

- I. Arredondo, P. Echevarria, H. Hassanzadegan, N. Garmendia, J. Jugo and V. Etxebarria, *Controlador multipropsito basado en FPGA con integracin EPICS para un linac de protones*, Actas de las XXXI Jornadas de Automtica. Universidad de Jaen, 8-10 Septiembre (2010)

- H. Hassanzadegan, M. Garmendia, V. Etxebarria, F. J. Bermejo, and I. del Campo, *Design and implementacion of the pulsed digital LLRF system of the ESS-Bilbao ion source test stand*, Proceedings of the 12th International Conference on Accelerator and Large Experimental Physics Control Systems ICALEPCS 2009. Kobe, Japan, 12-16 October (2009)

- H. Hassanzadegan, R. Griñó, D. Einfeld, *Transient Analysis of RF Cavities under Beam Loading*, Proceedings of PAC09, Vancouver, BC, Canada (2009)

- H. Hassanzadegan et. al., *Analogue LLRF of the ALBA Booster*, EPAC08, Genoa, Italy, 23-27 June (2008)

- H. Hassanzadegan et. al., *Analogue and Digital LLRF for the ALBA Synchrotron*, EPAC06, Edinburgh, Scotland, 26-30 June (2006)

- F. Perez, B. Baricevic, H. Hassanzadegan, A. Salom, P. Sanchez, D. Einfeld, *New Developments for the RF System of the ALBA Storage Ring*, Proceedings of EPAC06, Edinburgh, Scotland (2006)

- D. Einfeld, E. Al-Dmour, M. Attal, G. Vignola, H. Hassanzadegan, H. Tarawneh, *SESAME, a Synchrotron Light Source for the Middle East Region*, Proceedings of APAC 2004, Gyeongju, Korea (2004)

- D. Einfeld, R.H. Sarraf, M. Attal, K. Tavakoli, H. Hashemi, H. Hassanzadegan, E. Al-Dmour, B. Kalantari, A. Aladwan, H. Tarawneh, S. Varnasery, *SESAME, a 2.5 GeV Synchrotron Light Source for the Middle East Region*, Proceedings of the 2003 Particle Accelerator Conference (2003)

Bibliography

[1] R. Brinkmann, *Linear Collider Projects at DESY*, proc. EPAC'98

[2] P. Faugeras, *The LHC Project: Status and Prospects*, proc. APAC'01, Beijing, China (2001)

[3] F. Schonfeld et. Al., *A Cavity With Circular Waveguides for HOM Damping*, Available at: http://epaper.kek.jp/

[4] M. Langlois et. Al., *Impedance Measurements on ALBA Storage Ring Pre-series Cavity DAMPY 0*, CELLS internal report, Aug. 2007

[5] D. L. Trumper, et. Al, *A Loop Shaping Perspective for Tuning Controllers with Apaptive Feedforward Cancellation*, Precision Eng. 29, PP 27-40, 2005

[6] P. Mattews, et. Al, *Storage Ring Cavity Higher-Order Mode Dampers for the Advanced Photon Source*, IEEE 1996, http://accelconf.web.cern.ch/

[7] S. Kwiatkowski et. Al, *HOM Dampers for ALS Storage Ring RF Cavities*, Proc. PAC 2003

[8] R. Garoby, *Low Level RF and Feedback*, CERN. PS/RF note

[9] A. Gamp, *Servo Control of RF Cavities under Beam Loading*, http://www.desy.de/

[10] T. Weis, *Interaction between RF-system, RF-cavity and Beam*, Presentation in Riezlern, Austria, 2005, http://athene.delta.uni-dortmund.de

[11] T. Czarski et al. *Cavity Control System Models Simulations for TESLA Linear Accelerator*, TESLA report, Sep. 2003 http://tesla.desy.de/

[12] *ELETTRA website*, ELETTRA website http://www.elettra.trieste.it/

[13] *HASYLAB website*, HASYLAB website http://hasylab.desy.de/

[14] *AD8348 data sheet*, Analog Devices www.analog.com

[15] *AD8130 data sheet*, Analog Devices www.analog.com

[16] *AD8132 data sheet*, Analog Devices www.analog.com

[17] *AD8345 data sheet*, Analog Devices www.analog.com

[18] *AD8056 data sheet*, Analog Devices www.analog.com

[19] *AD835 data sheet*, Analog Devices www.analog.com

[20] *AD8302 data sheet*, Analog Devices www.analog.com

[21] *AD6645 data sheet*, Analog Devices www.analog.com

[22] *DAC5687 data sheet*, Texas Instruments http://www.ti.com/

[23] *Easy Step TM 3000 Industrial Interface*, Active Robots http://www.active-robots.com/

[24] *Lyrtech website*, Lyrtech http://www.lyrtech.com/

[25] *Xilinx website*, Xilinx http://www.xilinx.com/

[26] H. Hassanzadegan et. al., *Analogue and Digital LLRF for the ALBA Synchrotron*, EPAC06, Edinburgh, Scotland, 26-30 June 2006

[27] H. Hassanzadegan et. al., *Analogue LLRF of the ALBA Booster*, EPAC08, Genoa, Italy, 23-27 June 2008

[28] H. Hassanzadegan, *Report on the ALLRF tests at ELETTRA*, CELLS internal report, 13 Oct. 2006

[29] H. Hassanzadegan, *Report on ALLRF Tests with the 5-cell cavity at CELLS*, CELLS internal report, 10 Feb. 2007

[30] S. Michizono et. a.l, *Digital RF Control System for 400-MeV Protron Linac of JAERI/KEK Joint Project*, Proc. LINAC2002, Gyeongju, Korea, 2002

[31] A. Rohlev et. al. *All Digital IQ Servo-System for CERN Linacs*, EPAC03, June 2003

[32] E. Onillon, *Low Level RF Feedback Loop Design*, http://icfa-nanobeam.web.cern.ch/

[33] S. N. Simrock, *Design of the Digital RF Control System for the TESLA Test Facility*, (1996), http://accelconf.web.cern.ch

[34] J. R. Delayen, *Determination of Low Level RF Control Requirements for Superconducting Cavities From Microphonics Measurements*, EPAC03, June 2003

[35] C. Schwartz, A. Nassiri, Y. Kang, R. L. Kustom,*Simulation of the APS Storage-Ring RF System*, PAC97, May 1997

[36] L. R. Doolittle, *Low Level RF Modeling for the MEBT Rebunchers*, SNS Tech Note FE-EE-021, June 2001

[37] P. Krejcik et al, *RF Feedback for Beam Loading Compensation in the SLC Damping Rings*, proc. PAC93 (1993)

[38] S. Michizono, *Design of the Low Level RF Control for the TESLA Superstructure*, Proc. PAC01

[39] P. Corredoura, *Commissioning Experience with the PEO-II Low-Level RF System*, Proc. PAC97

[40] M. Liepe et al, *A New Digital Control System for CESR-C and the CORNELL ERL*, Proc. PAC03

[41] P. Corredoura, *Architecture and Performance of the PEP-II Low-Level RF System*, Proc. PAC99

[42] C. Rossi et. al., *The Low Level RF System of ELETTRA*, Proc. EPAC89

[43] T. Czarski et. al., *Cavity Control System Essential Modeling for TESLA Linear Accelerator*, TESLA Report 2003-08

[44] M. G. Minty et. al., *Klystron Power Specifications Based on Transient Beam Loading Analysis in Damping Rings*, (1995), http://ieeexplore.ieee.org/

[45] S. N. Simrock, *Transient Beam Loading Based Calibration of the Vector-Sum for the TESLA Test Facility*, (1996), http://accelconf.web.cern.ch/

[46] W. K. Lau et. al., *Analysis of the Superconducting RF Cavity Under Heavy Beam Loading at Taiwan Light Source*, Proc. EPAC'02

[47] S. N. Simrock et. al., *Operational Aspects of the RF Control System for the TESLA Test Facility*, (1996), http://accelconf.web.cern.ch/

[48] P. Corredoura et. al., *The Proposed NLC Linac LLRF System*, Proc. EPAC 2000

[49] M. G. Minty, R. H. Siemann, *Transient Beam Loading in the SLC Damping Rings*, (1995), http://ieeexplore.ieee.org/

[50] T. S. Rohlev et. al., *Frequency Response Measurements of the LEDA RF Control System*, XX International Linac Conference, Monterey, California, (2000)

[51] P. Baudrenghien, *Low Level RF Systems for Synchrotrons*, Contribution to the CAS RF School, Seeheim, 8-16 May 2000

[52] M. G. Minty, *Low Level RF System Design for the Next Linear Collider Damping Rings*, 1998 http://ieeexplore.ieee.org/

[53] *Conceptual Design Report for the Upgrading of SESAME to 2.5GeV*, May 2000, http://www.sesame.org.jo/

[54] P. Corredoura, *Low Level RF Systems for the PEP-II B Factory*, Proc. PAC95

[55] T. Czarski et. al., *Cavity Digital Control Testing System by Simulink Step operation Method for TESLA Linear Accelerator and Free Electron Laser*, TESLA Report 2003-20

[56] A. Vardanyan et. al., *An Analysis Tool for RF Control for Superconducting Cavities*, http://tesla.desy.de/

[57] F. Wang et. al., *Low Level Control RF System for SSRF*, Proc. 2nd APAC, Beijing, China, (2001)

[58] L. Doolittle et. al., *The SNS Front End LLRF System*, Proc. LINAC 2002, Gyeongju, Korea

[59] M. S. de Jong et. al., *Performance of the MIT-Bates South Hall Ring 2856 MHz CW RF Cavity System*, http://epaper.kek.jp/

[60] R. Tighe et. al., *RF Feedback Simulation Results for PEP-II*, (1995), http://ieeexplore.ieee.org/

[61] C. Schwartz et. al., *Simulation of the APS Storage-Ring RF System*, http://epaper.kek.jp/

[62] A. Gallo et. al., *Experimental Tests of the DANE RF Feedback System*, (1996), http://accelconf.web.cern.ch/

[63] W. T. Weng, S. Y. Zhang, *Beam Loading Issues for SNS Storage Ring*, (1998), http://accelconf.web.cern.ch/

[64] D. Teytelman, *Survey of Digital Feedback Systems in High Current Storage Rings*, Proc. PAC'03

[65] J. M. Brennan et. al., *RF Beam Control System for the Brookhaven Relativistic Heavy Ion Collider, RHIC*, Proc. EPAC'98

[66] M. G. Minty et. al., *Low-level RF System Design for the Accelerator Test Facility (ATF) Damping Ring*, (1997), http://ieeexplore.ieee.org/

[67] S. Holmes et. al., *Low-level RF Signal Processing for the Next Linear Collider Test Accelerator*, Proc. PAC'97

[68] Sung-Il Kwon et. al., *Frequency Shift Observer for an SNS Superconducting RF Cavity*, IEEE Transactions on Nuclear Science, VOL. 50, No 1, Feb. 2003

[69] W. Ross et. al., *Gap Voltage Feed-Forward Module for PEP-II Low Level RF System*, Proc. PAC'97

[70] T. Schilcher et. al., *A Design and Performance Analysis Tool for Superconducting RF Systems*, http://epaper.kek.jp/

[71] S. N. Simrock et. al., *Design of the Digital RF Control System for the TESLA Test Facility*, (1996), http://accelconf.web.cern.ch/

[72] *Conclusions Report of the ESS-Bilbao Initiative Workshop*, Bilbao (Spain), March 2009. Available at http://www.essbilbao.com

[73] H. Hassanzadegan, M. Eguiraun, N. Garmendia, F. J. Bermejo, V. Etxebarria, D. Findlay, A. Letchford, *Design and Implementation of a Pulsed Digital LLRF System for the RAL Front End Test Stand*,Proceedings of the 1st International Particle Accelerator Conference IPAC'10. Kyoto, Japan, 23-28 May, pp. 1458-1460

[74] H. Hassanzadegan, M. Garmendia, V. Etxebarria, F. J. Bermejo, and I. del Campo, *Design and implementacion of the pulsed digital LLRF system of the ESS-Bilbao ion source test stand* Proceedings of the 12th International Conference on Accelerator and Large Experimental Physics Control Systems ICALEPCS 2009. Kobe, Japan, 12-16 October (2009)

[75] A.P. Letchford, M.A. Clarke-Gayther, D. Faircloth, S.R. Lawrie, M. Perkins, P. Wise, A. Kurup, S. Alsari, S. Jolly, D.A. Lee, P. Savage, J.K. Pozimski, C. Gabor, C. Plostinar, J. Back, F.J. Bermejo, R. Enparantza,I. Ariz,

P. Romano, A. Sedano, V. Etxebarria, H. Hassanzadegan, N. Garmendia, M. Eguiraun, *Status of the RAL Front End Test Stand* Proceedings of the 1st International Particle Accelerator Conference IPAC'10. Kyoto, Japan, 23-28 May, pp. 642-644 (2010)

[76] I. Bustinduy, D. De Cos, S. Jolly, J.K. Pozimski, P. Savage, J. Feuchtwanger, F.J. Bermejo, V. Etxebarria, N. Garmendia, H. Hassanzadegan, J. Portilla, A.P. Letchford, *Beam Dynamics Studies on the Radio-Frequency Quadrupole for the Bilbao Accelerator* Proceedings of the 1st International Particle Accelerator Conference IPAC'10. Kyoto, Japan, 23-28 May, pp. 4214-4216 (2010)

[77] I. Arredondo, P. Echevarria, H. Hassanzadegan, N. Garmendia, J. Jugo and V. Etxebarria, *Controlador multipropsito basado en FPGA con integracin EPICS para un linac de protones* Actas de las XXXI Jornadas de Automtica. Universidad de Jaen, 8-10 Septiembre.

[78] P. Echevarria, I. Arredondo, D. Belver, M. del Campo, N. Garmendia, H. Hassanzadegan, L. Muguira, V. Etxebarria and J. Jugo, *Multipurpose controller based on a FPGA with EPICS integration* Proceedings of the 2011 Particle Accelerator Conference PAC'11. New York, 28 March-1 April, pp. WEOBN4-1-3 (2011).

[79] D. Belver, I. Arredondo, M. del Campo, P. Echevarria, J. Feuchtwanger, N. Garmendia, H. Hassanzadegan, L. Muguira, F.J. Bermejo, V. Etxebarria, J. Jugo, and J. Portilla, *Overview of the BPM system of the ESS-Bilbao* Proceedings of the 10th European Workshop on Beam Diagnostics and Instrumentation for Particle Accelerators DIPAC2011. Hamburg, Germany, 16-18 May (2011).

[80] H. Hassanzadegan, N. Garmendia, V. Etxebarria, F.J. Bermejo, *Low level rf system for the European Spallation Source's Bilbao linac*, Physical Review Special Topics - Accelerators and Beams, **Vol. 14**, n.5, pp. 052803-1, 052803-16 (2011), DOI: 10.1103/PhysRevSTAB.14.052803

[81] H. Hassanzadegan, R. Griñó, *A Transient Model for RF Cavity Analysis under Beam Loading*, Nuclear Instruments and Methods in Physics Research A, **615**, p. 143-157, (2010)

[82] H. Ma, M. Champion, M. Crofford, K. Kasemir, M. Piller, L. Doolittle, A. Ratti, *Low-level RF Control of Spallation Neutron Source: System and Characterization*, Physical Review Special Topics - AB, **9**, 032001 (2006)

[83] Z. Fang, S. Anami, S. Michizono, S. Yamaguchi, T. Kobayashi, H. Suzuki, *RF Feedback Control Systems of the J-PARC Linac*, proc. PAC'07, (2007)

[84] S. Anami et al, *Control of the Low Level RF System for the J-PARC Linac*, proc. LINAC 2004, (2004)

[85] C. Ziomek, P. Corredoura, *Digital I/Q Demodulator*, proc. PAC'95, (1995)

[86] T. Matsumoto, S. Fukuda, H. Katagiri, S. Michizono, T. Miura, Y. Yano, *Performance of Digital Low-level RF Control System with Four Intermediate Frequencies*, proc. LINAC'08, (2008)

[87] H. Katagiri, S. Fukuda, T. Matsumoto, T. Miura, S. Michizono, Y. Yano, M. Yoshida, *High Speed Data Acquisition System Using FPGA for LLRF Measurement and Control*, proc. LINAC'08, (2008)

[88] S.N. Simrock, M. Hoffmann, F. Ludwig, M. K. Grecki, T. Jezynski, *Considerations for the Choice of the Intermediate Frequency and Sampling Rate for Digital RF Control*, proc. EPAC'06, (2006)

[89] M. Grecki, T. Jezynski, A. Brandt, *Estimation of IQ Vector Components of RF Field - Theory and Implementation*, proc. MIXDES'05, (2005)

[90] P. Baudrenghein et al, *The LHC Low Level RF*, proc. EPAC'06, (2006)

[91] *Merrimac IQG-20E-400 data sheet*, Merrimac Industries Inc. http://www.merrimacind.com/

[92] T. Mastorides, C. Rivetta, J.D. Fox, D. Van Winkle, PAC'09, (SLAC-PUB-13631), (1999)

[93] T. P. Wangler, *RF Linear Accelerators, second edition*, WILEY-VCH, ISBN: 978-3-527-40680-7 (2008)

[94] C. Cheng, P. Savage, A. Kurup, J. Pozimski, A. Letchford, *RFQ Cold Model RF Measurements and Waveguide-to-coaxial Line Transition Design for the Front-end Test Stand at RAL*, proc. PAC'07, (2007)

[95] S. Jolly, A. Kurup, D. Lee, P. Savage, J. Pozimski, A. Letchford, Y. Cheng, *Detailed Study of the RF Properties of the FETS RFQ Cold Model*, proc. EPAC'08, (2008)

[96] http://cern.ch//LLRF05, S. N. Simrock, LINAC'04, Lubeck, 2004, p. 523, D. Teytelman, PAC'03, Portland, 2003, p. 318, M.E. Angoletta, EPAC'06, 1848, (2006)

[97] D. Makowski, W. Koprek, T. Jezynski, A. Piotrowski, Member, IEEE,G. Jablonski, W. Jalmuzna, and S. Simrock, IEEE Trans. Nucl. Sci., **56**, 2814 (2009)

[98] S. Simrock, M. Grecki, W. Jalmuzna, T. Jezynski, W. Koprek, and P. Pucyk, *Proc. 15th IEEE-NPSS Real-Time Conf.*, 2007, Batavia, IL, p. 1, (2007)

[99] P. Corredoura, L. Sapozhnikov, R. Tighe, *RF Feedback Development for the PEP-II B Factory*,4th European Particle Accelerator Conference, London, UK, 27 Jun - 1 Jul 1994, pp.1954 (1994)

[100] A. Araz, U. Bonnes, R. Eichhorn, F. Hug, M. Konrad, A. Richter, *The Bseband Low Level RF Control for the S-DALINAC: A Flexible Solution for Other Frequencies?*, proc. SRF 2009, Berlin, Germany (2009)

[101] Y. Otake, H. Maesaka , M. Kitamura , T. Shintake, T. Ohshima, N. Hosoda, T. Fukui, T. Ohata, *SCSS RF Control Toward 5712 MHZ Phase Accuracy of One Degree*, proc. APAC07, Indore, India (2007)

[102] H. Maesaka, T. Ohshima, N. Hosoda, T. Fukui, T. Inagaki, Y. Otake, H. Tanaka, S. Takahashi, T. Hasegawa, S. Tanaka, M. Kitamura, *Precise RF Control System of the SCSS Test Accelerator*, proc. EPAC08, Genoa, Italy (2007)

[103] T. Miura, H. Katagiri, T. Matsumoto, S. Michizono, Y. Yano, S. Fukuda, *Measurements of Feedback Instability due to 8/9π and 7/9π Modes at KEK-STF*, proc. LINAC'08, (2008)

[104] E. Vogel, *High Gain Proportional RF Control at TESLA Cavities*, Physical Review Special Topics - Accelerators and Beams **10**, 052001 (2007)

[105] Communications and Power Industries, *Proposal for the Development and Manufacture of a 352.2-MHz, 2.8-MW Klystron*, dated 30 March 2010

[106] G. Dome, *RF theory*, CERN Accelerator School proc. 92-93, **1**, (1992)

[107] W. Weingarten, *Superconducting Cavities*, CERN Accelerator School proc. 92-93, **2**, (1991)

[108] P. B. Wilson, *High Energy Electron Linacs: Application to Storage Ring RF Systems and Linear Colliders*, AIP conf. proc. 87, eds. R.A. Carrigan, F.R. Huson and M. Month, American Institute of Physics, New York, SLAC-PUB-2884, (1982)

[109] M. G. Minty, R. H. Siemann, *Heavy Beam Loading in Storage Ring Radio Frequency Systems*, Nuclear Instruments and Methods in Physics Research, A **376**, p. 310-318, (1996)

[110] H. Ma, J. Rose, *Low-Level Radio Frequency System Development forthe National Synchrotron Light Source II*, Brookhaven Natl. Lab. , report No. BNL-82322-2009-CP, (2009)

[111] T. Mastorides, C. Rivetta, J.D. Fox, D. Van Winkle, PAC'09, (SLAC-PUB-13631), (1999)

[112] T. Schilcher, *Vector Sum Control of Pulsed Accelerating Fields in Lorentz Force Detuned Superconducting Cavities*, PhD thesis, Hamburg University (1998)

[113] R. E. Shafer, *Beam Position Monitoring*, Los Alamos National Laboratory (1990)

[114] I. Podadera, *Requirements for the Electronics of the IFMIF-EVEDA BPM System*, Ciemat Internal Report, Oct. (2009)

[115] M. Cohen-Solal, *Design, Test and Calibration of an Electrostatic Beam Position Monitor*, Physical Review Special Topics Accelerators and Beams, **13**, 032801 (2010)

[116] R. B. Shurter et. Al., *Analog Front-end Electronics for Beam Position Measurement on the Beam HALO Measurement*, proc. PAC01 (2001)

[117] *AD8310 data sheet*, Analog Devices