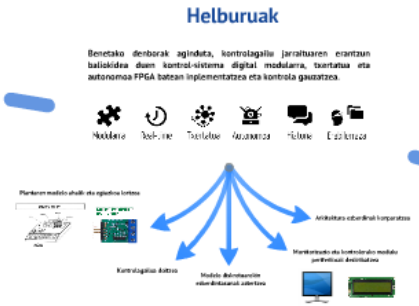

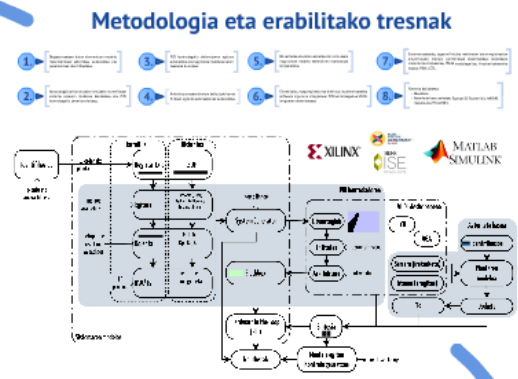

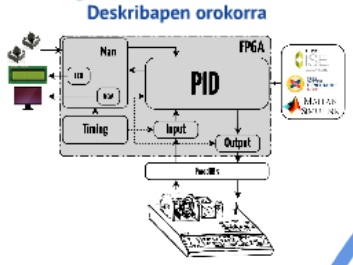

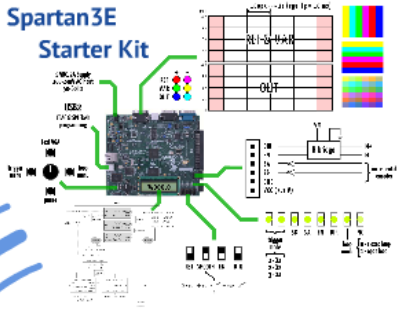

Laburbilduz

- Abstrakzio-maila baxuko garapen osoa.
- Esperimentalki balidatutako sistema.
- Azterketa bibliografiko zabala.
- Irudien eta bestelako baliabideen biltegi irekia.
- Plataforma ezberdinetan, tresna ireki eta askeekin egindako dokumentazioa.

Universidad del País Vasco — Euskal Herriko Unibertsitatea

APES

INDUSTRIA INGENIARITZA TEKNIKOKO UNIBERTSITATE ESKOLA
ESCUELA UNIVERSITARIA DE INGENIERIA TÉCNICA INDUSTRIAL

Kontrol esparruan ikasketa eta garapenerako oinarrizko ingurune praktiko, ireki eta askea

discrete_control, PID, real_time, matlab_simulink, xilinx_ise, fpga_spartan3

IKASLEAREN DATUAK

Unai Martinez Corral

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ZUZENDARIAREN DATUAK

Koldo Basterretxea Oyarzabal

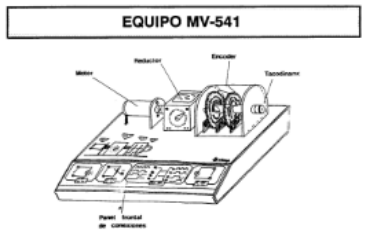
koldo.basterretxea@ehu.es

Helburuak

Benetako denborak aginduta, kontrolagailu jarraituaren erantzun baliokidea duen kontrol-sistema digital modularra, txertatua eta autonomoa FPGA batean inplementatzea eta kontrola gauzatzea.

Modularra Real-time Txertatua Autonomoa Hiztuna Erabilerraza

Plantaren modelo ahalik eta egiazkoa lortzea



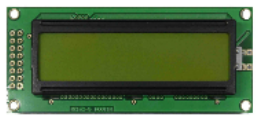
Digilent PmodHB3™
2A H-Bridge

Kontrolagailua doitzea

Modelo diskretuarekin ezberdintasunak aztertzea

Arkitektura ezberdinak konparatzea

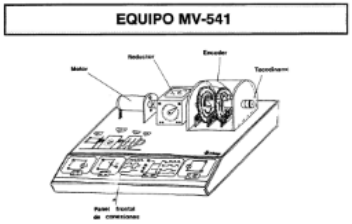
Monitorizazio eta kontrolerako modulu periferikoak deskribatzea



autonomoa FPGA batean inplementatzea eta kontrola gauzatzea.

Modularra Real-time Txertatua Autonomoa Hiztuna Erabilerraza

Plantaren modelo ahalik eta egiazkoa lortzea



Arkitektura ezberdinak konparatzea

Monitorizazio eta kontrolerako modulu periferikoak deskribatzea

Kontrolagailua doitzea

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Modularra

Real-time

Txertatua

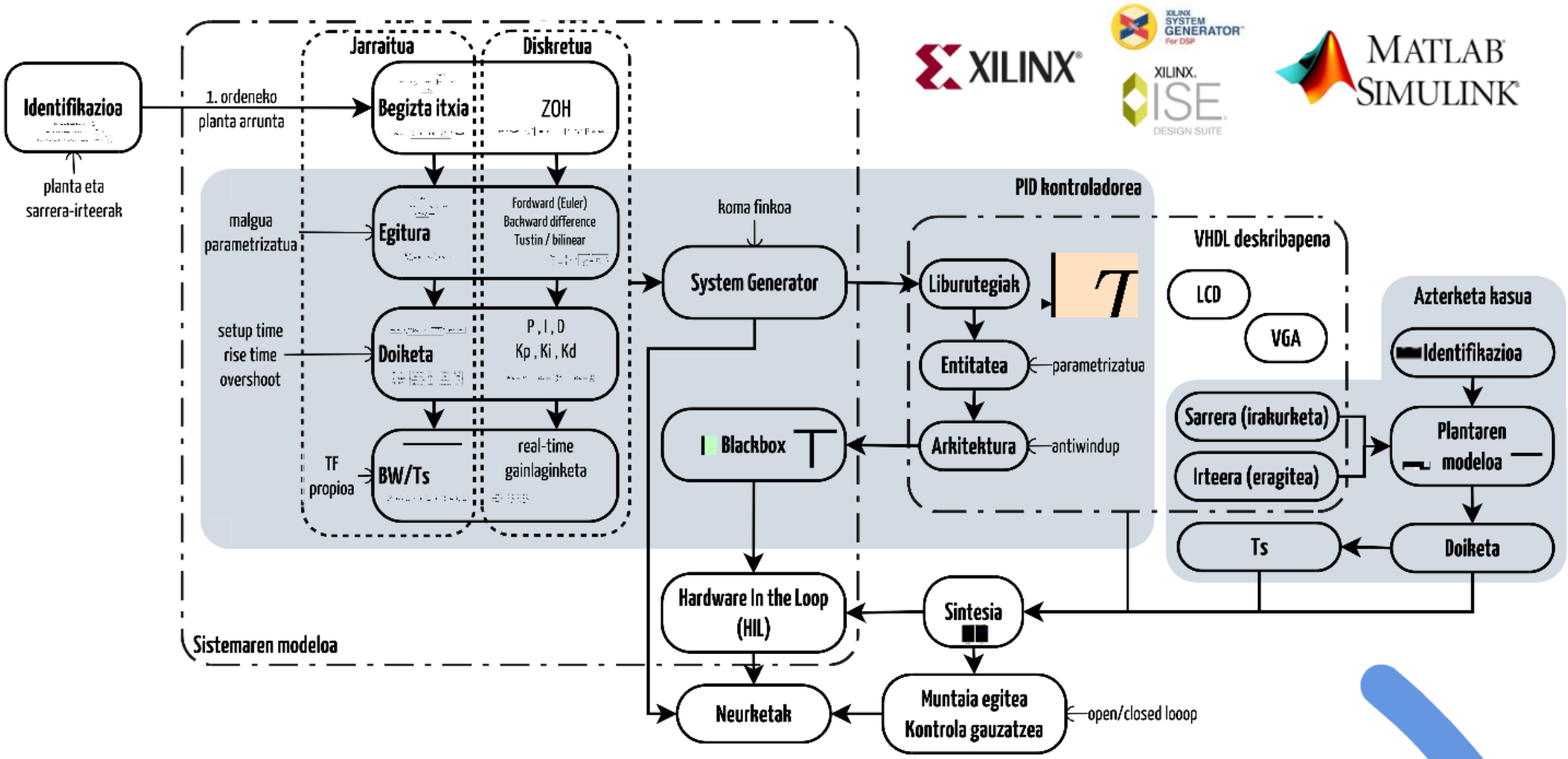
Autonomoa

Hiztuna

Erabilerraza

Metodologia eta erabilitako tresnak

1. Begizta osatzen duten elementuen modelo matematikoak aztertzea, aukeratzea eta parametroak identifikatzea.
2. Konputagailuz burututako simulazio numerikoaz sistema osoaren modeloa balidatzea eta PID kontrolagailu jarraitua doitzea.
3. PID kontrolagailu diskretuaren egitura aukeratzea eta laginketa-maiztasunaren ikasketa burutzea.
4. Arkitektura ezberdinetan kalkuluak koma finkoan egiteko adierazpenak aukeratzea.
5. Bit-zehatza eta ziklo-zehatza den simulazio ingurunean modelo ezberdinen erantzunak konparatzea.
6. Sintesirako, mapa egiteko eta diseinua inplementatzeko software ingurune integratuan PID kontrolagailua VHDL lengoaian deskribatzea.
7. Sistema osatzeko, egoera finituko makinetan eta erregistroetan oinarritutako modulu periferikoak deskribatzea: kodetzaile inkremental birakariak, PWM modulagailua, H-zubia babesteko logika, VGA, LCD...
8. Sistema balidatzea:
   - Blackbox
   - Azterketa kasu zehatza: Spartan3E Starter Kit, MV541 maketa eta PmodHB3.



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uutoyia et

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d eraVillak

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tresnak

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XILINX SYSTEM GENERATOR™ For DSP

MATLAB®

1. matematikoak aztertzea, aukeratzea eta parametroak identifikatzea.

3. aukeratzea eta laginketa-maiztasunaren ikasketa burutzea.

5. ingurunean modelo ezberdinen erantzunak konparatzea.

7. [illegible] inkremental birakariak, PWM modulagailua, H-zubia babesteko logika, VGA, LCD...

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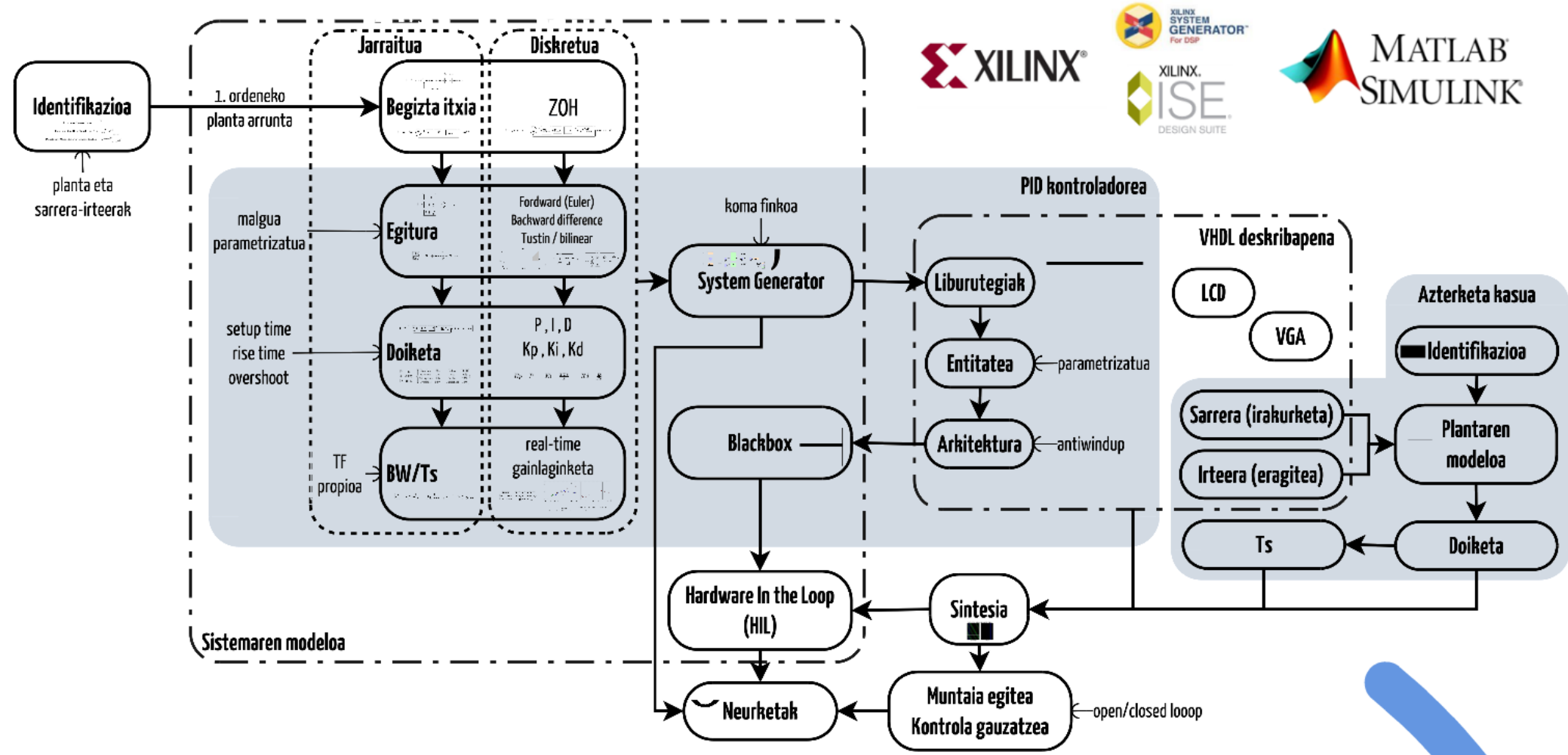

De

Identifikazioa

First Order Transfer function: $\frac{K}{\tau s + 1}$

First Order Plus Delay Transfer function: $\frac{K}{\tau s + 1} e^{-\alpha s}$

Discrete First Order Plus Delay Transfer function: $z^{-\text{round}(\frac{\alpha}{T_s})} \frac{\frac{K \cdot T_s}{\tau}}{z - e^{\frac{-T_s}{\tau}}}$

planta eta sarrera-irteerak

entiRazio

First Order Transfer function: $\frac{K}{\tau s + 1}$

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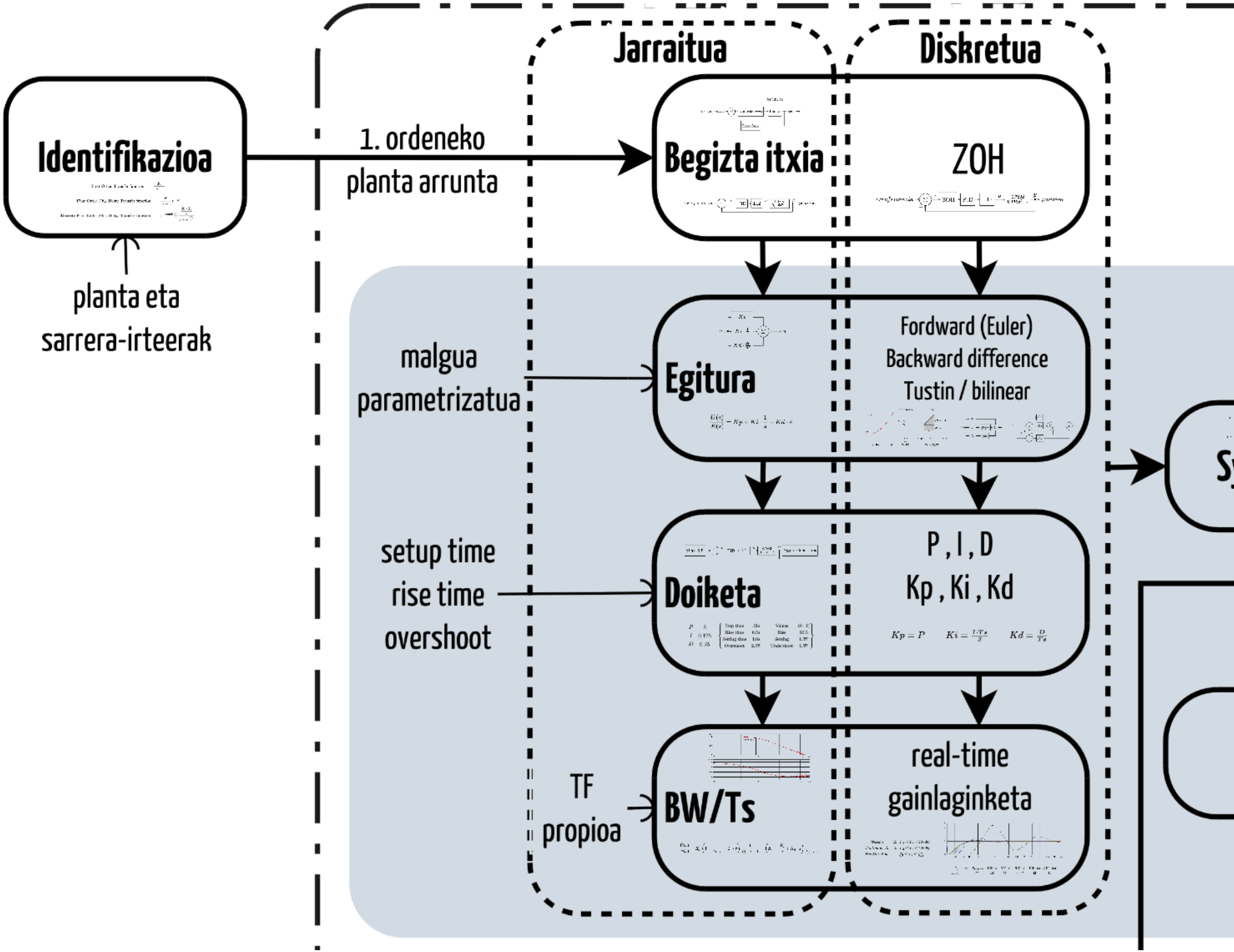
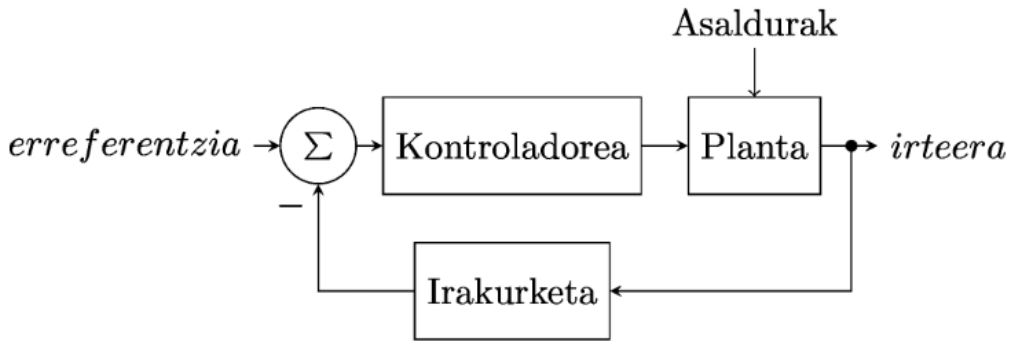
Discrete First Order Plus Delay Transfer function: $z^{-\text{round}(\frac{\alpha}{T_s})} \frac{\frac{K \cdot T_s}{\tau}}{z - e^{\frac{-T_s}{\tau}}}$

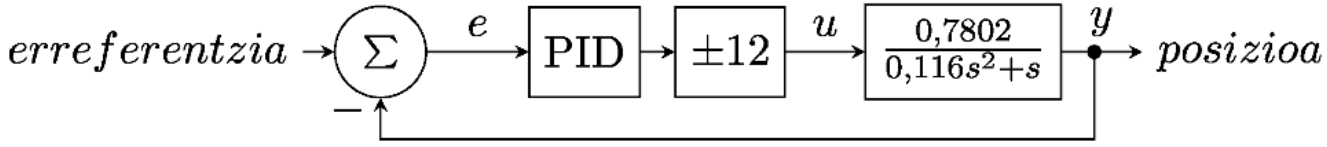

Identifikazioa
planta eta
sarrera-irteerak
1. ordeneko
planta arrunta
Jarraitua
Diskretua
Begizta itxia
ZOH
malgua
parametrizatua
Egitura
Fordward (Euler)
Backward difference
Tustin / bilinear
setup time
rise time
overshoot
Doiketa
P , I , D
Kp , Ki , Kd
TF
propioa
BW/Ts
real-time
gainlaginketa

1. ordeneko

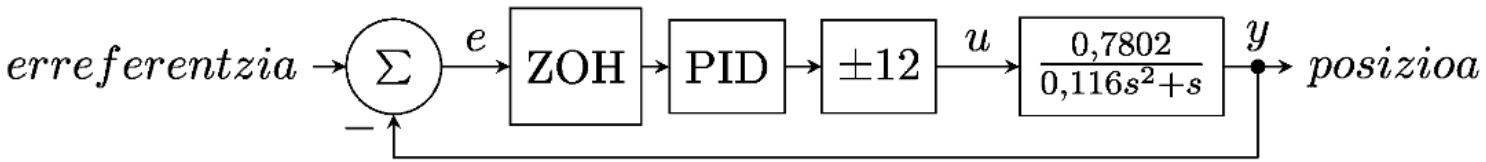
planta arrunta



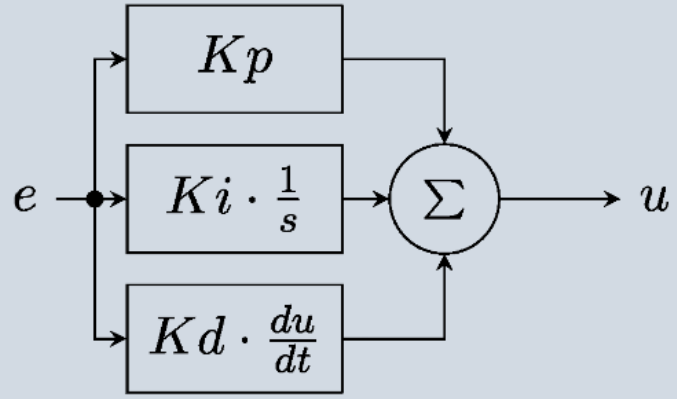
Begizta itxia



ZOH



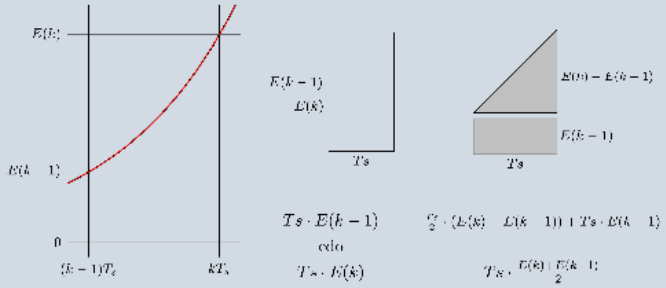
malgua
parametrizatua

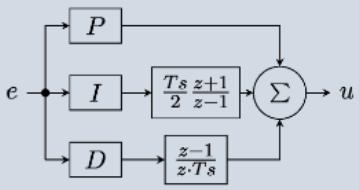


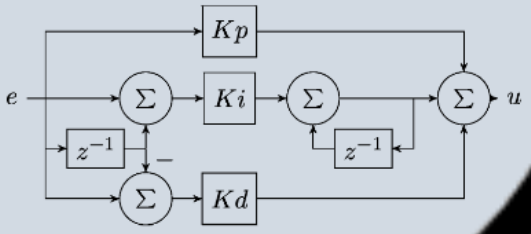
Egitura

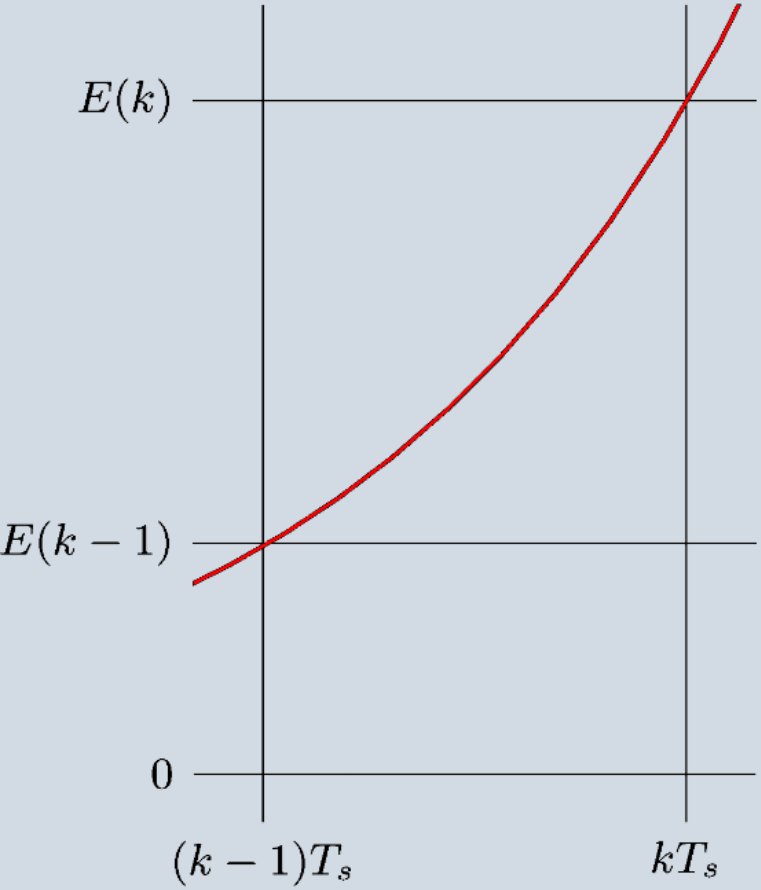
$$\frac{U(s)}{E(s)} = Kp + Ki \cdot \frac{1}{s} + Kd \cdot s$$

Fordward (Euler)
Backward difference
Tustin / bilinear

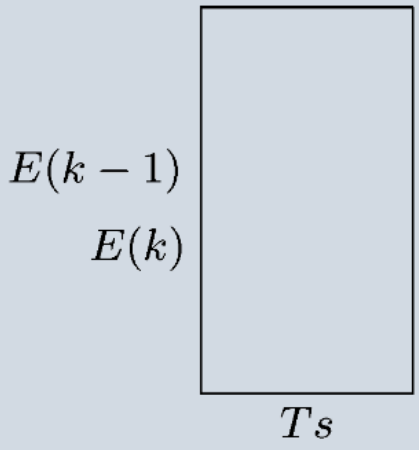








Euler / Backward

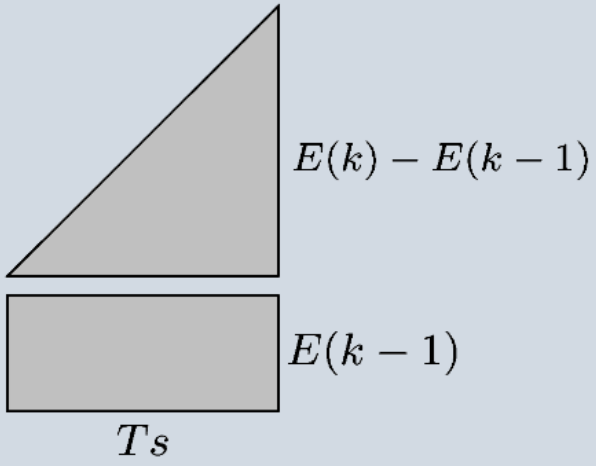


$$Ts \cdot E(k-1)$$

edo

$$Ts \cdot E(k)$$

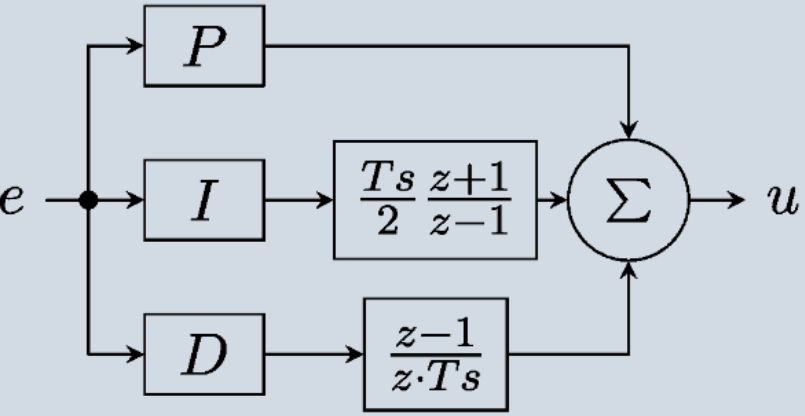
Tustin

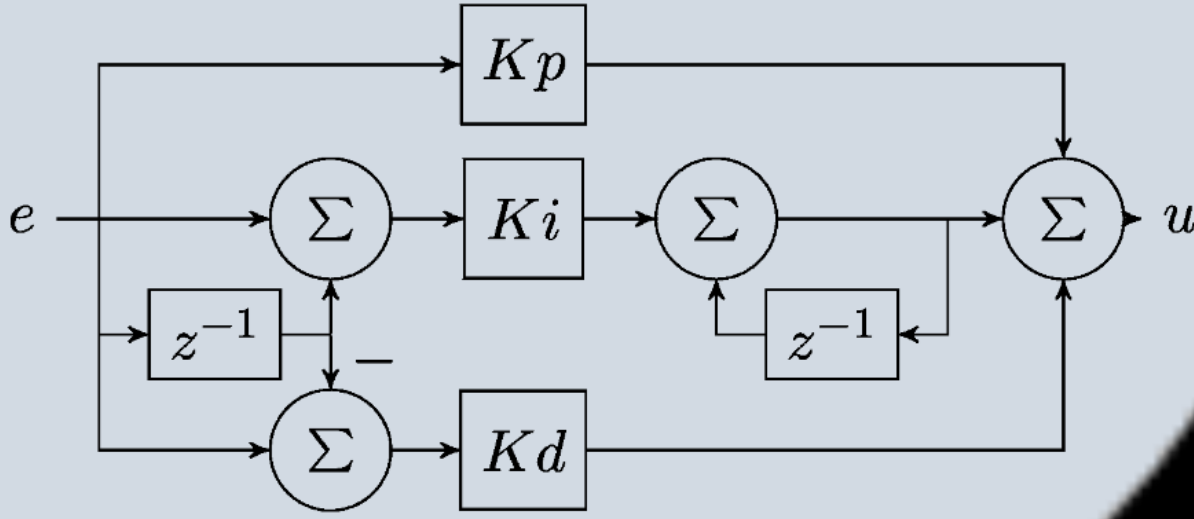


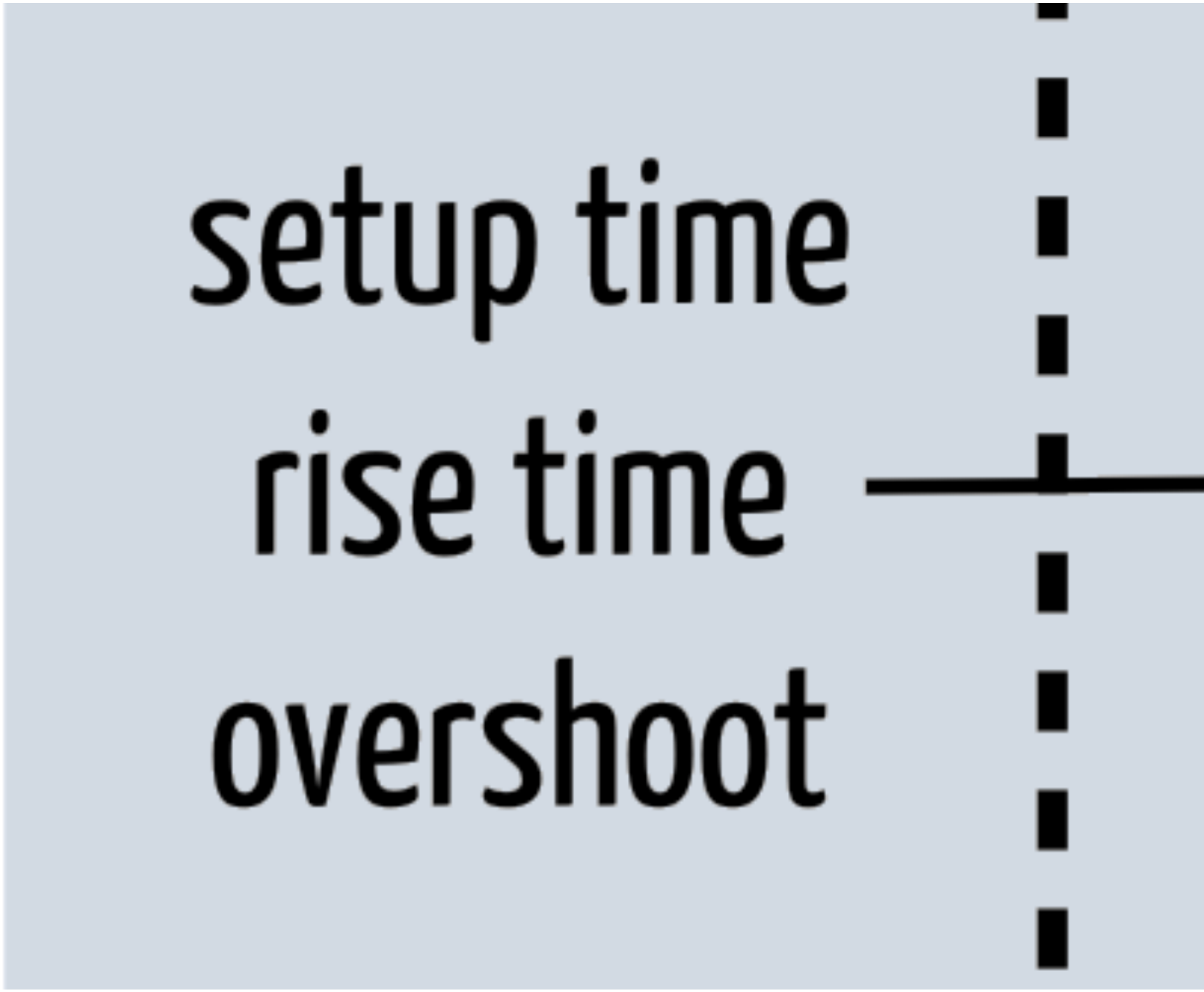
$$\frac{Ts}{2} \cdot (E(k) - E(k-1)) + Ts \cdot E(k-1)$$

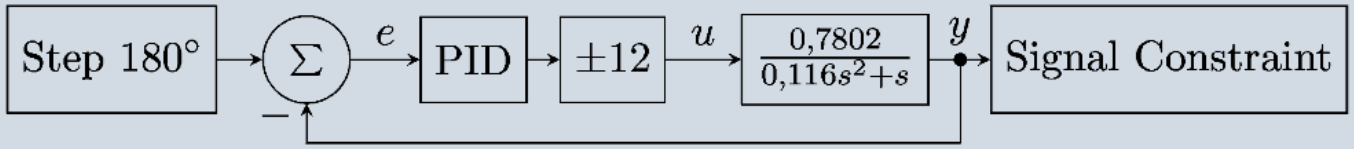
$$Ts \cdot \frac{E(k)+E(k-1)}{2}$$

/ bilinear


P
I
D
e
$\frac{Ts}{2}\frac{z+1}{z-1}$
$\frac{z-1}{z \cdot Ts}$
Σ
u


Kp
e
Σ
Ki
Σ
Σ
u
z^{-1}
z^{-1}
−
Σ
Kd


setup time
rise time
overshoot



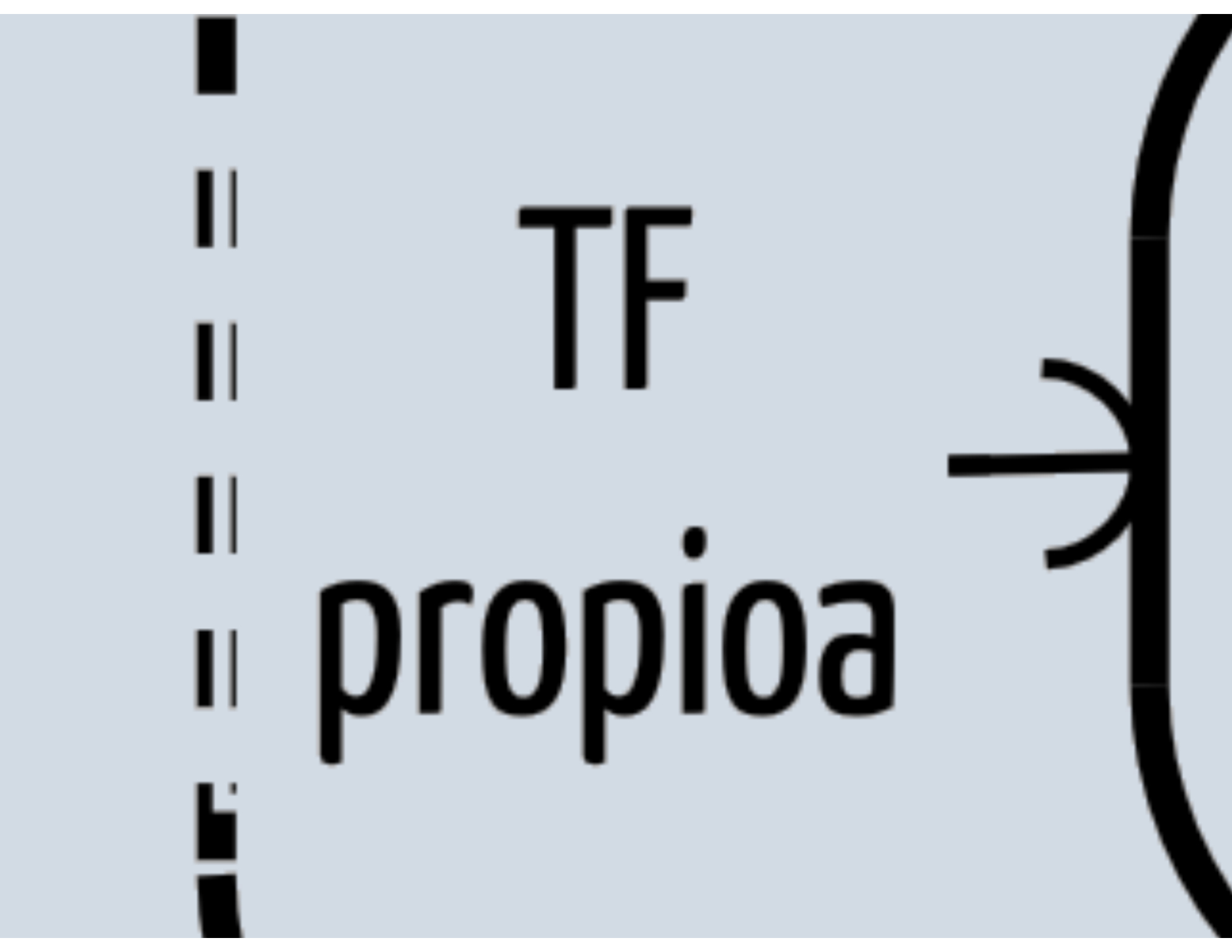
Doiketa

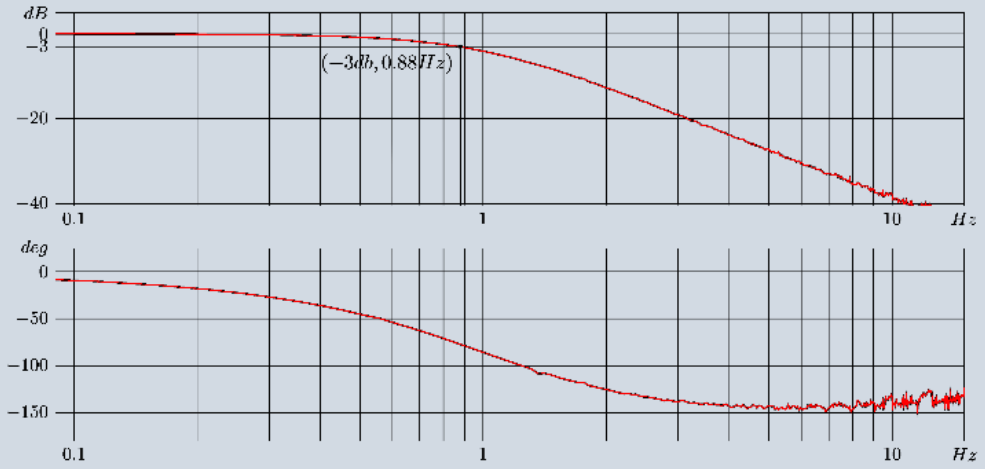
P	6	Step time	$.01s$	Values	$(0:1)$
I	0.125	Rise time	$0.5s$	Rise	90%
D	0.25	Setting time	$1.0s$	Setting	1.5%
		Overshoot	2.5%	Undershoot	1.5%

P , I , D

Kp , Ki , Kd

$$Kp = P \qquad Ki = \frac{I \cdot Ts}{2} \qquad Kd = \frac{D}{Ts}$$


TF
propioa

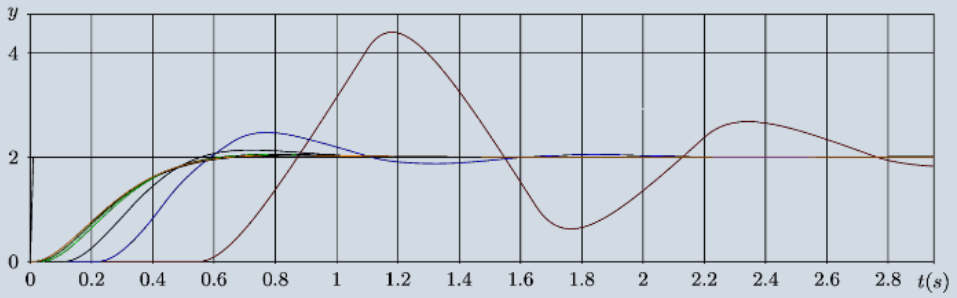


BW/Ts

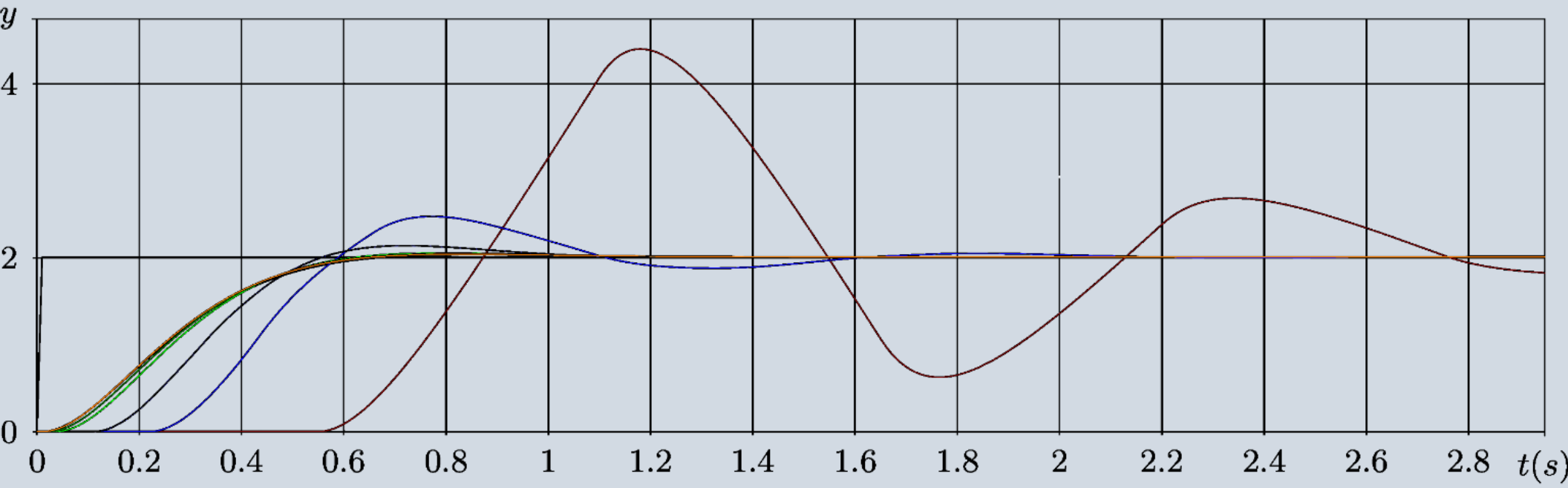
$$\frac{U(s)}{E(s)} = K_p \left(1 + \frac{1}{T_i \cdot s} + T_d \cdot s\right) \frac{1}{T_f \cdot s + 1} = \left(K_p + \frac{K_i}{s} + K_d \cdot s\right) \frac{1}{T_f \cdot s + 1}$$

real-time gainlaginketa

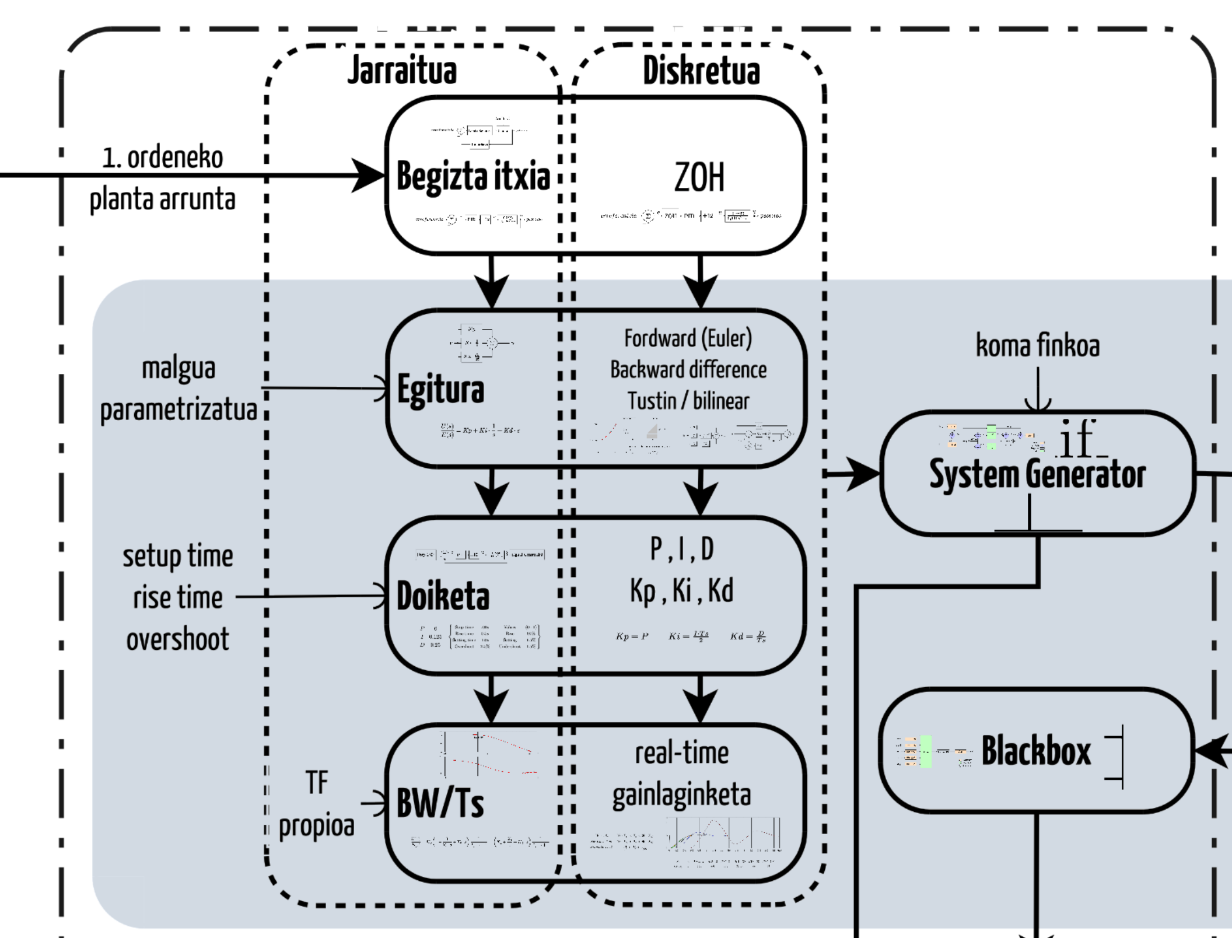
Wescott	$10 \cdot F_{cl} < F_s < 20 \cdot F_{cl}$
Santina et al.	$10 \cdot F_{cl} < F_s < 40 \cdot F_{cl}$
Franklin et al.	$\frac{\omega_0}{0,3} < F_s < \frac{\omega_0}{0,08}$



F_s	∞	$F_{Shannon}$	$BW \cdot 5$	$BW \cdot 10$	$BW \cdot 30$	$BW \cdot 50$	$BW \cdot 100$
T_s(ms)	0	550	220	110	36,67	22	11

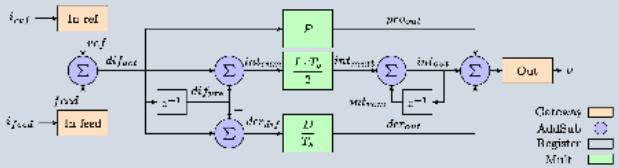


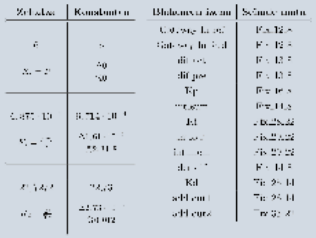
F_s	∞	$F_{Shannon}$	$BW \cdot 5$	$BW \cdot 10$	$BW \cdot 30$	$BW \cdot 50$	$BW \cdot 100$
T_s(ms)	0	550	220	110	36,67	22	11


Jarraitua
Diskretua
1. ordeneko
planta arruna
Begizta itxia
ZOH
malgua
parametrizatua
Egitura
Fordward (Euler)
Backward difference
Tustin / bilinear
koma finkoa
System Generator
setup time
rise time
overshoot
Doiketa
P , I , D
Kp , Ki , Kd
Blackbox
TF
propioa
BW/Ts
real-time
gainlaginketa

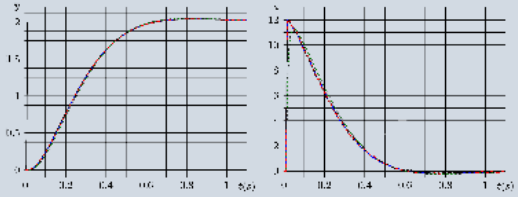
koma finkoa

koma finkoa

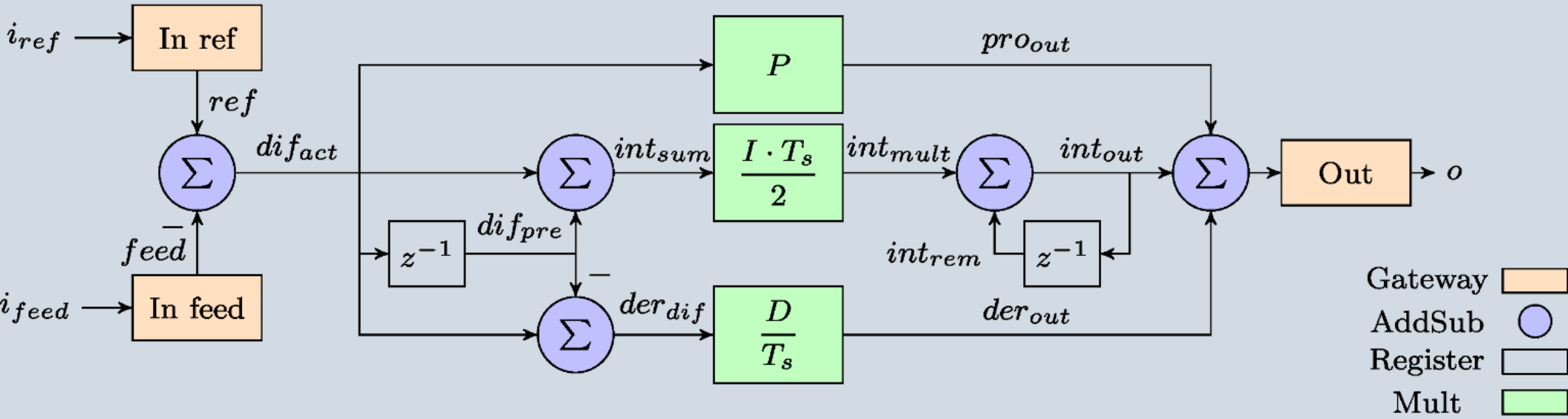




System Generator

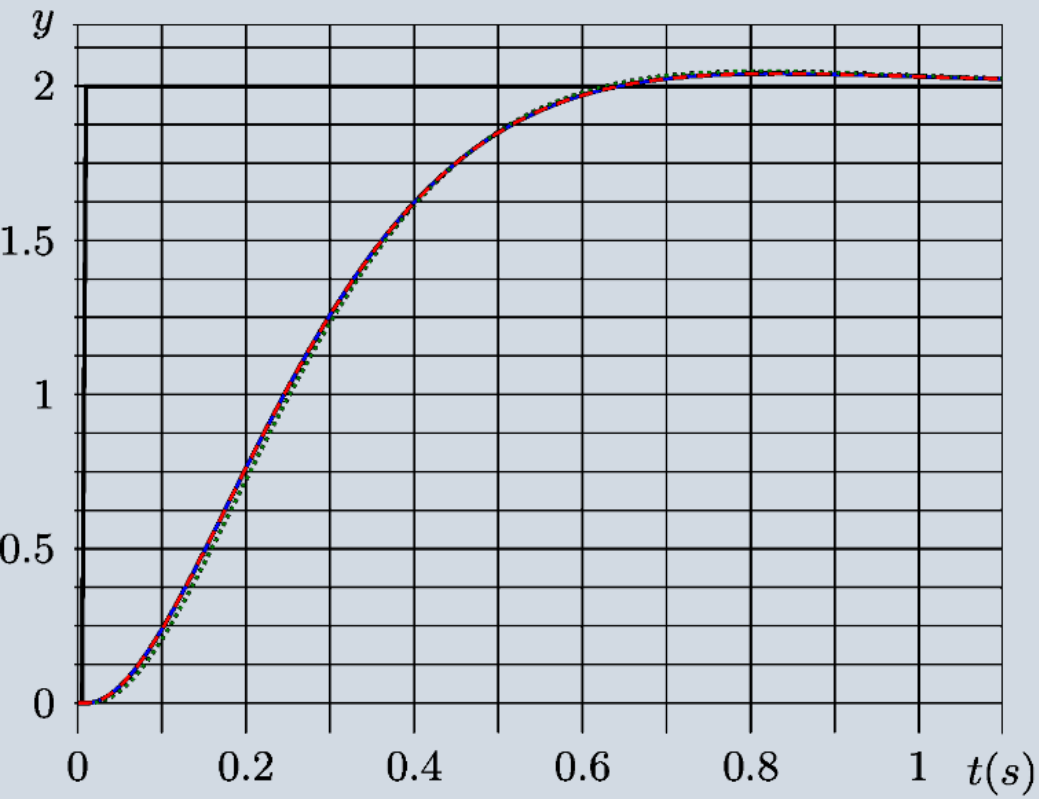


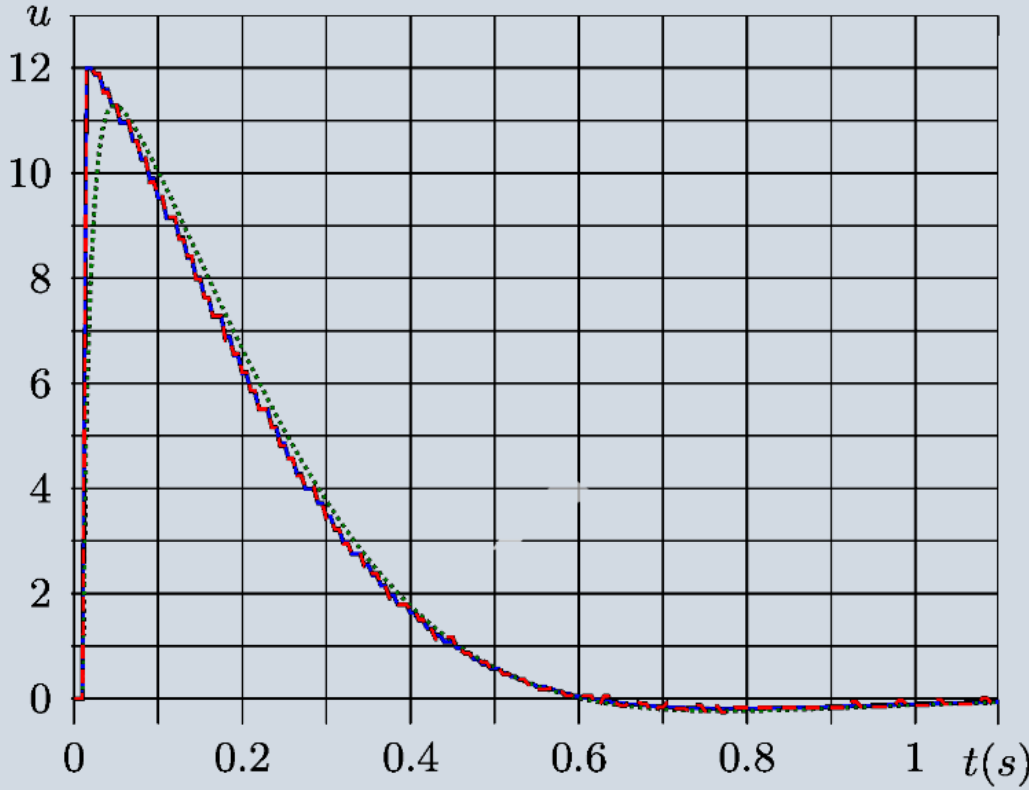
Jarraitua Iragazia Diskretua Diskretua (sysgen)


i_{ref}
In ref
ref
dif_{act}
$feed$
i_{feed}
In feed
z^{-1}
dif_{pre}
P
pro_{out}
int_{sum}
$\frac{I \cdot T_s}{2}$
int_{mult}
int_{out}
int_{rem}
z^{-1}
Out
o
der_{dif}
$\frac{D}{T_s}$
der_{out}
Gateway
AddSub
Register
Mult

Zehatza	Konstantea
6	6
$K_p = P$	$\Delta 0$ $\%0$
$6,875 \cdot 10^{-4}$	$6,714 \cdot 10^{-4}$
$K_i = \frac{I \cdot Ts}{2}$	$\Delta 1,61 \cdot 10^{-5}$ $\%2,3418$
$22,7272$	$22{,}73$
$K_d = \frac{D}{Ts}$	$\Delta 2,73 \cdot 10^{-3}$ $\%0,012$

Blokearen izena	Seinale mota
Gateway In ref	Fix_12_8
Gateway In feed	Fix_12_8
dif_act	Fix_13_8
dif_pre	Fix_13_8
Kp	Fix_16_8
int_sum	Fix_14_8
Ki	Fix_28_22
int_out	Fix_29_22
int_mem	Fix_29_22
der_dif	Fix_14_8
Kd	Fix_25_14
add_out1	Fix_26_14
add_out2	Fix_35_22

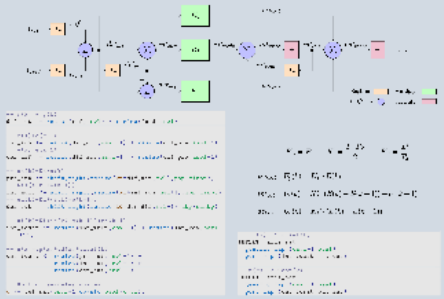




Jarraitua Iragazia Diskretua Diskretua (sysgen)

PID kontroladorea

Liburutegiak



Entitatea ← parametrizatua

Arkitektura ← antiwindup

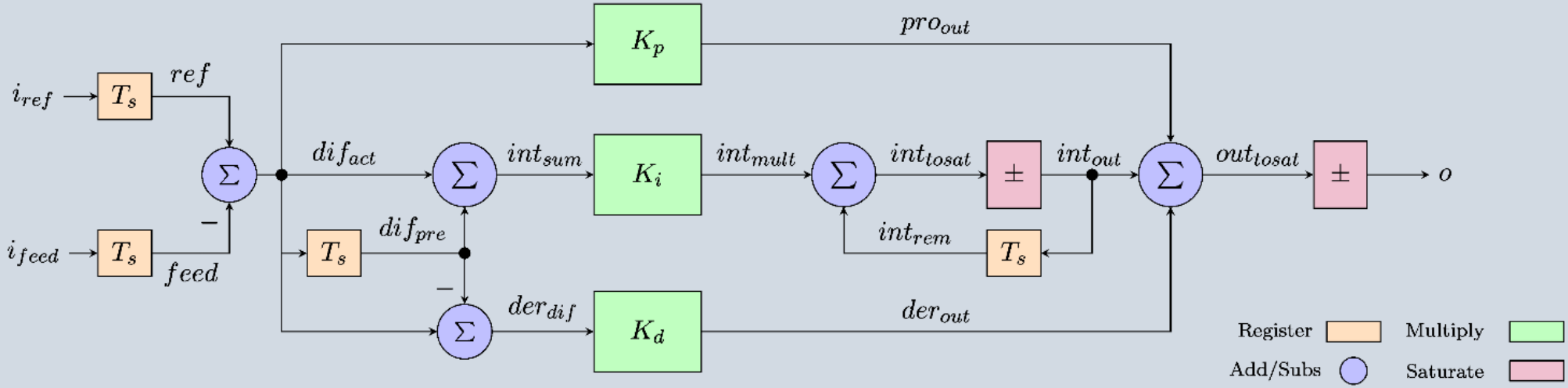
VHDL deskribapena

LCD

VGA

Sarrera (irakurketa)

Irteera (eragitea)




```
-- r(k) - y(k)
dif_act <= resize(ref,aswl) - resize(feed,aswl);

-- e(k)+e(k-1)
int_sum <= resize(dif_act,aswl+1) + resize(dif_pre,aswl+1);
-- e(k)-e(k-1)
der_dif <= resize(dif_act,aswl+1) - resize(dif_pre,aswl+1);

-- up(k)=Kp*e(k)
pro_out <= shift_right(resize(kp*dif_act,mwl),pbp-minbp);
-- Ki*(e(k)+e(k-1))
int_mult <= shift_right(resize(ki*int_sum,mwl+1),ibp-minbp);
-- ud(k)=Kd*(e(k)-e(k-1))
der_out <= shift_right(resize(kd*der_dif,mwl+1),dbp-minbp);

-- ui(k)=Ki*(e(k)+e(k-1))+ui(k-1)
int_tosat <= resize(int_mult,oswl+1) + resize(int_rem,oswl
    +1);

-- u(k)=up(k)+ud(k)+uisat(k)
out_tosat <= resize(pro_out,oswl+1) +
             resize(int_out,oswl+1) +
             resize(der_out,oswl+1);

-- Kontrol seinalea moztea
o <= out_sat(oswl-1 downto oswl-o_wl);
```

$$K_p = P \qquad K_i = \frac{I \cdot Ts}{2} \qquad K_d = \frac{D}{T_s}$$

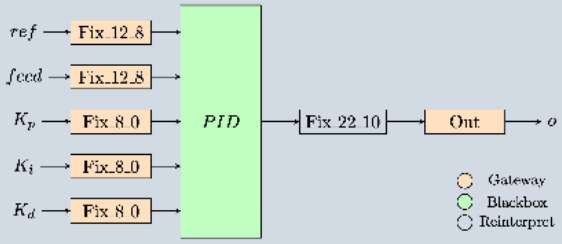
$$pro_{out} \quad U_p(k) = Kp \cdot E(k)$$

$$int_{out} \quad U_i(k) = Ki \cdot (E(k) + E(k-1)) + U_i(k-1)$$

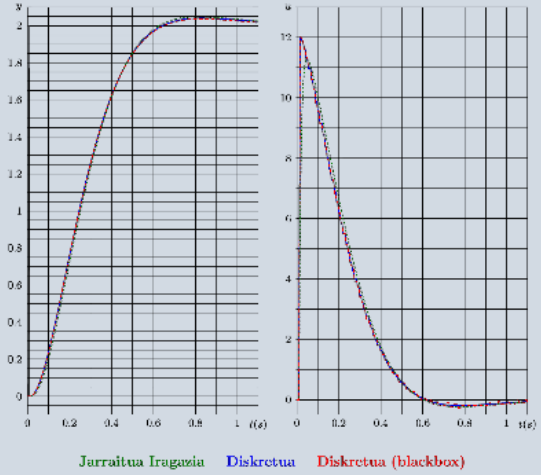
$$der_{out} \quad U_d(k) = Kd \cdot (E(k) - E(k-1))$$

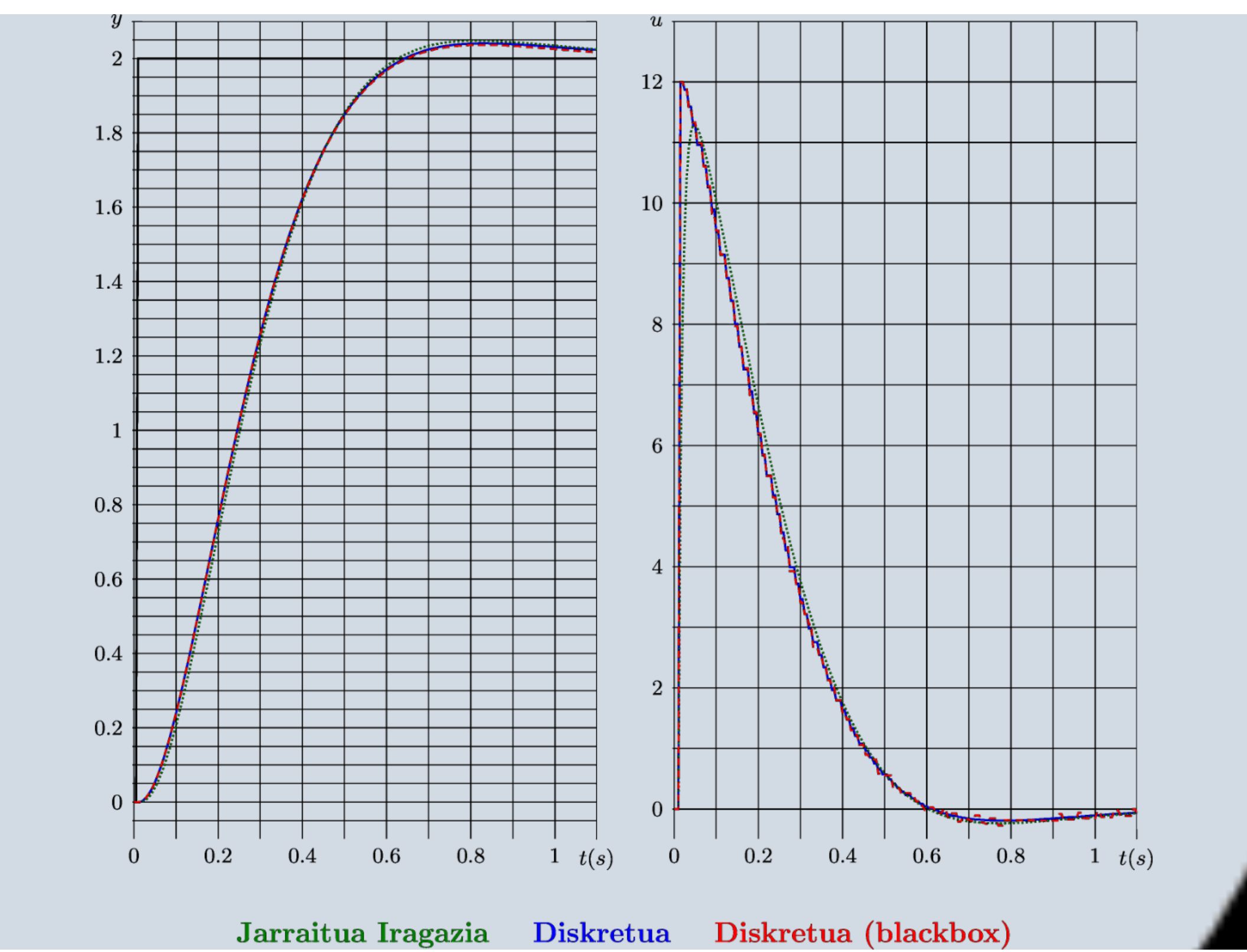
```
-- ui(k) -> uisat(k)
INTSAT: anie_sat
  generic map (oswl+1,oswl)
  port map (int_tosat,int_out);

-- u(k) -> usat(k)
OUTSAT: anie_sat
  generic map (oswl+1,oswl)
  port map (out_tosat,out_sat);
```


ref
Fix 12.8
feed
Fix_12.8
K_p
Fix 8.0
K_i
Fix_8.0
K_d
Fix 8.0
PID
Fix 22.10
Out
o
Gateway
Blackbox
Reinterpret

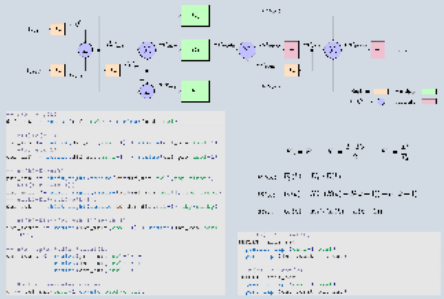
Blackbox


Jarraitua Iragazia
Diskretua
Diskretua (blackbox)


y
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
0.2
0.4
0.6
0.8
1
t(s)
u
12
10
8
6
4
2
0
0
0.2
0.4
0.6
0.8
1
t(s)
Jarraitua Iragazia
Diskretua
Diskretua (blackbox)

PID kontroladorea

Liburutegiak



Entitatea ← parametrizatua

Arkitektura ← antiwindup

VHDL deskribapena

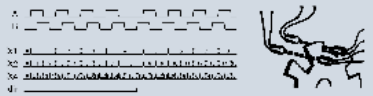
LCD

VGA

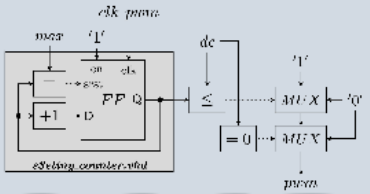
Sarrera (irakurketa)

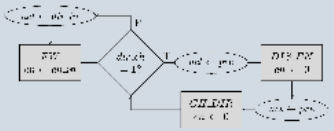
Irteera (eragitea)

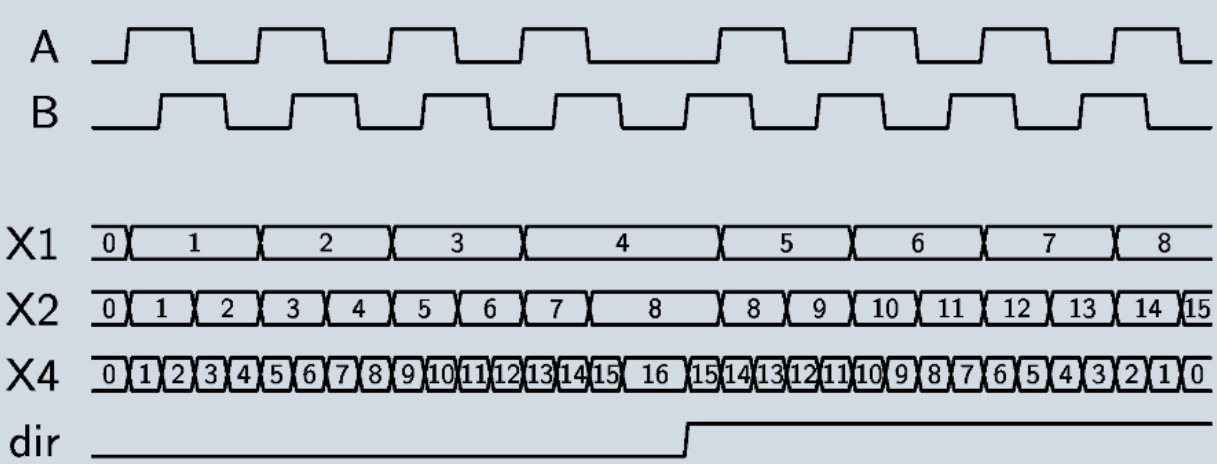
Sarrera (irakurketa)

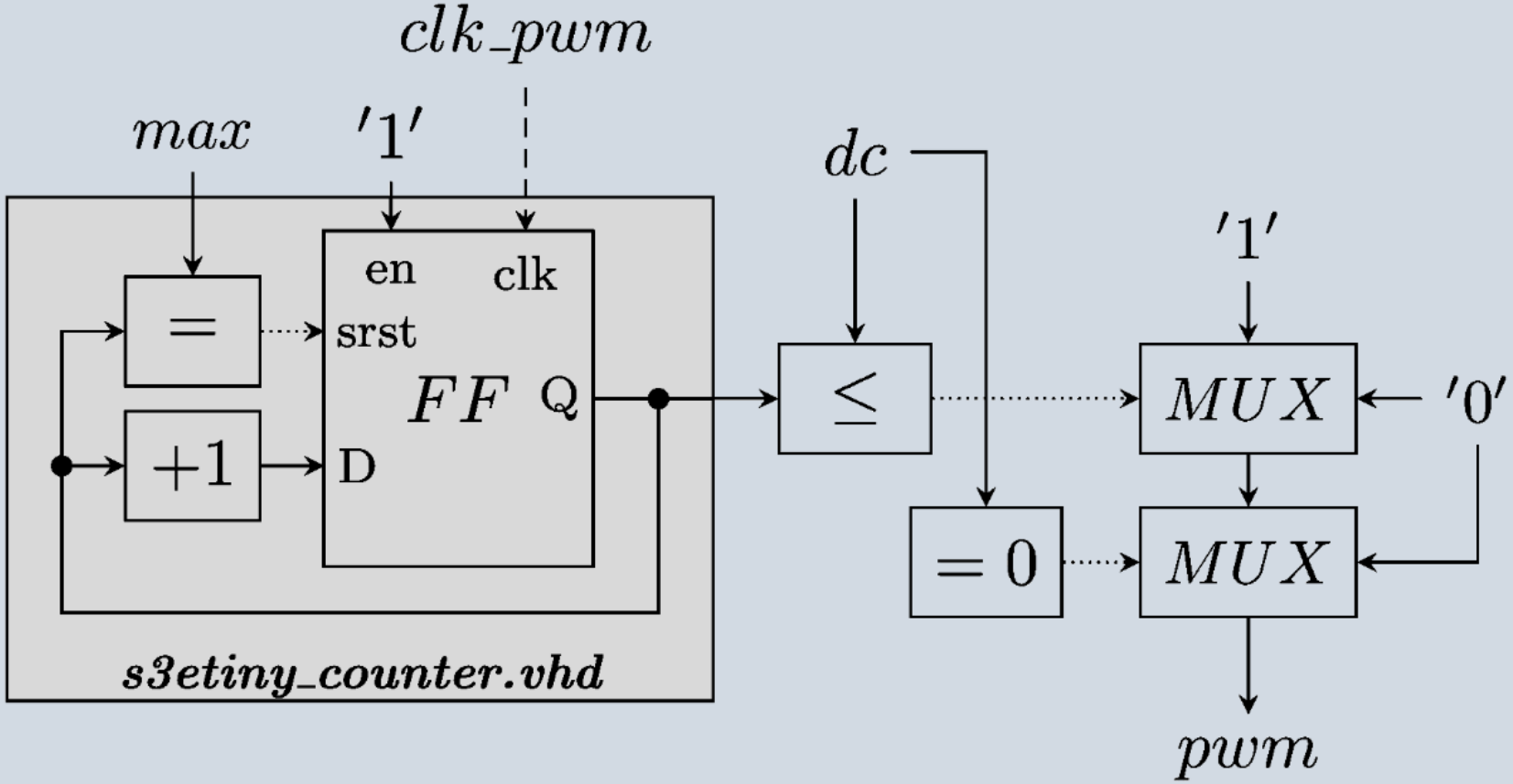


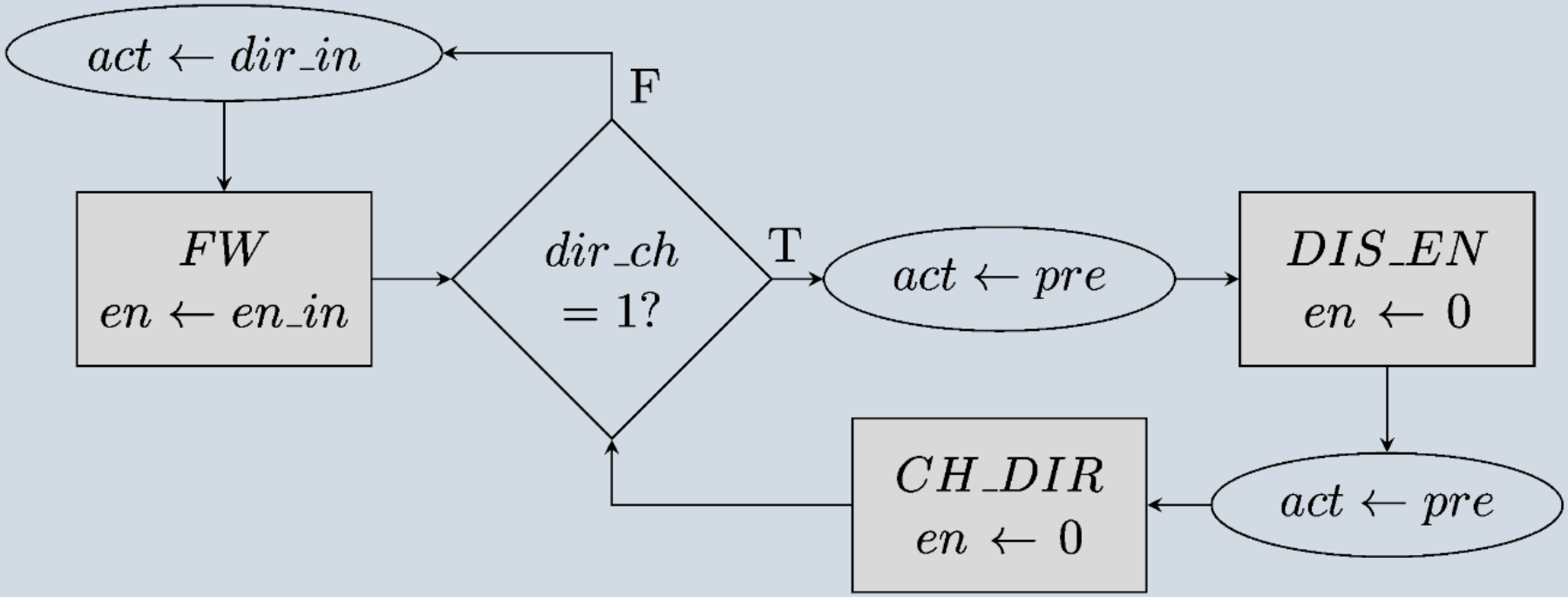
Irteera (eragitea)





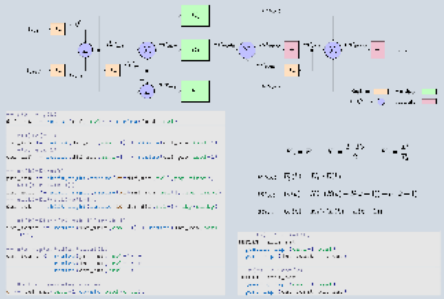

A
B
X1
0 1 2 3 4 5 6 7 8
X2
0 1 2 3 4 5 6 7 8 8 9 10 11 12 13 14 15
X4
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
dir


clk_pwm
max
'1'
dc
'1'
en
clk
=
srst
FF
Q
+1
D
≤
MUX
'0'
= 0
MUX
s3etiny_counter.vhd
pwm


$act \leftarrow dir\_in$
F
FW
$en \leftarrow en\_in$
dir_ch
$= 1?$
T
$act \leftarrow pre$
DIS_EN
$en \leftarrow 0$
$act \leftarrow pre$
CH_DIR
$en \leftarrow 0$

PID kontroladorea

Liburutegiak



Entitatea ← parametrizatua

Arkitektura ← antiwindup

VHDL deskribapena

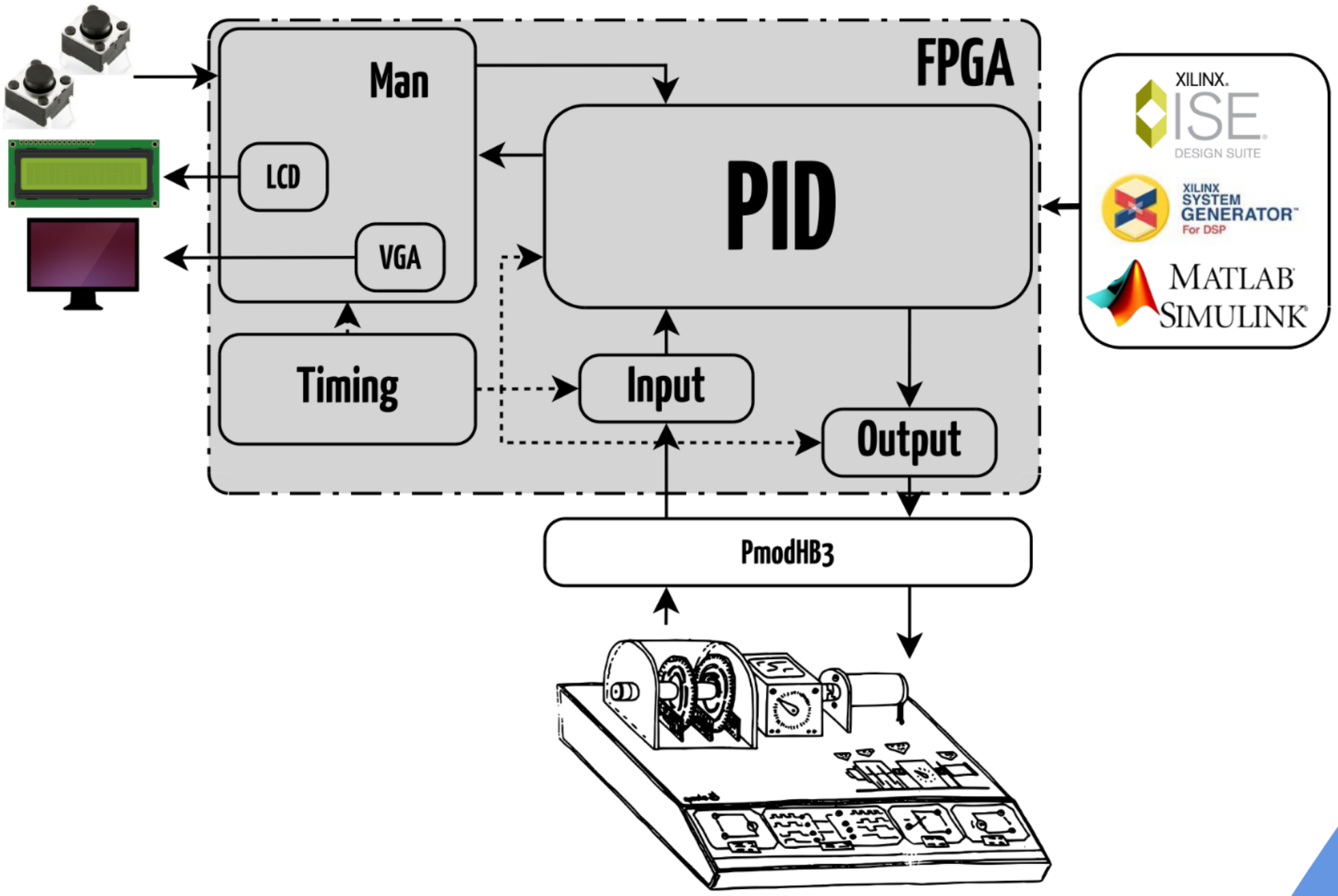
LCD

VGA

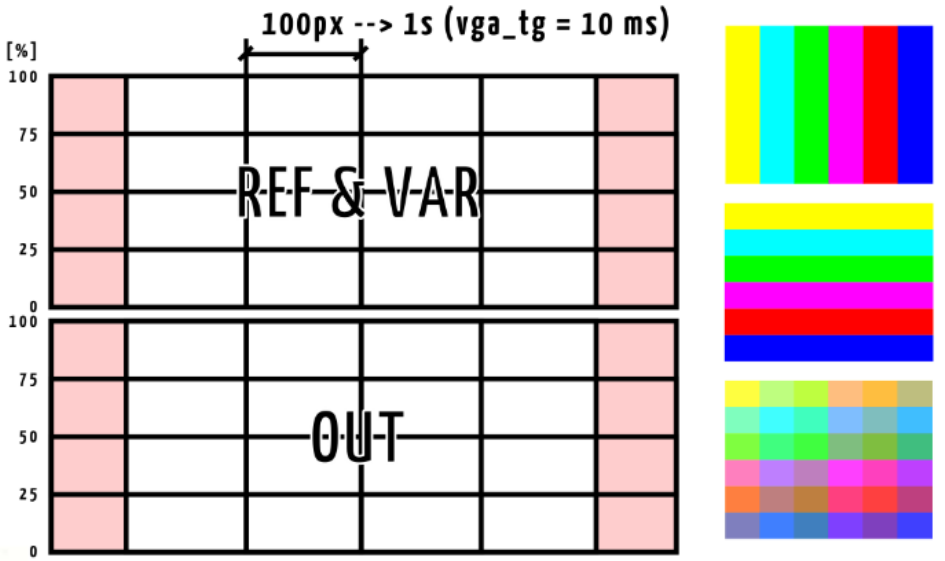
Sarrera (irakurketa)

Irteera (eragitea)

Deskribapen orokorra



Spartan3E Starter Kit



5 VDC, 2A Supply
100-240V AC Input
50-60 Hz

USB2
JTAG & SPI Flash programming

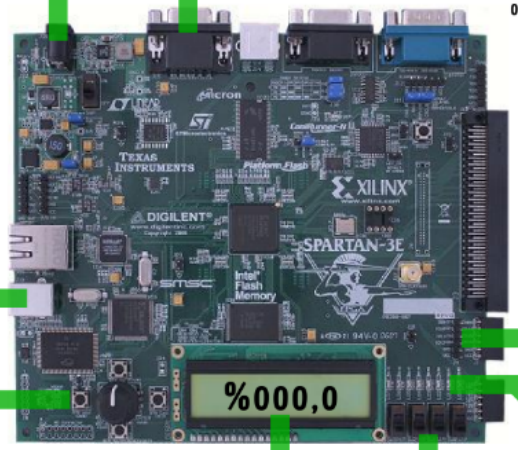
REF
VAR
OUT
\+ -

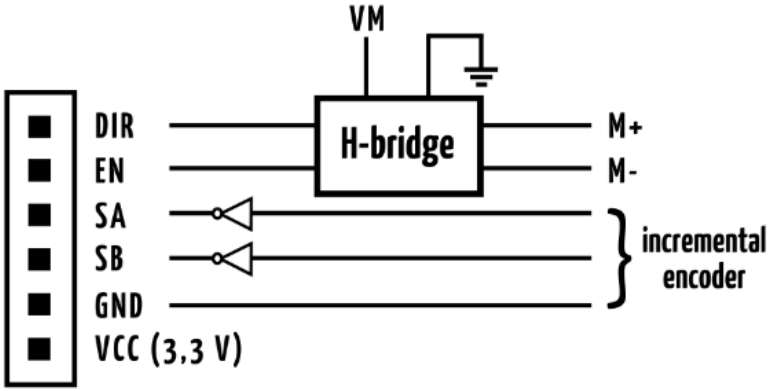
test VGA

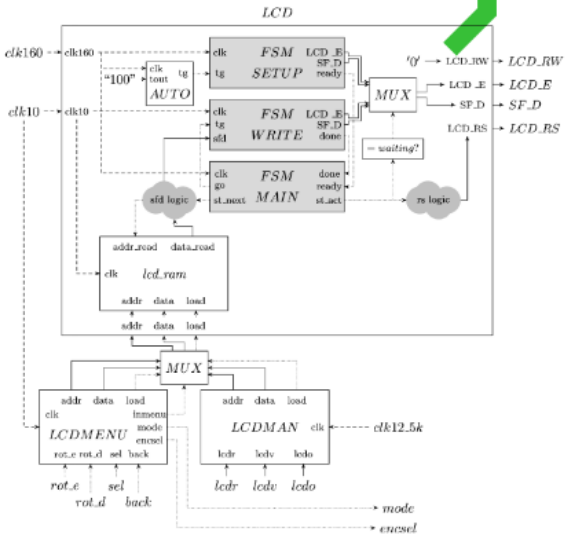
trigger menu

loop menu

pause







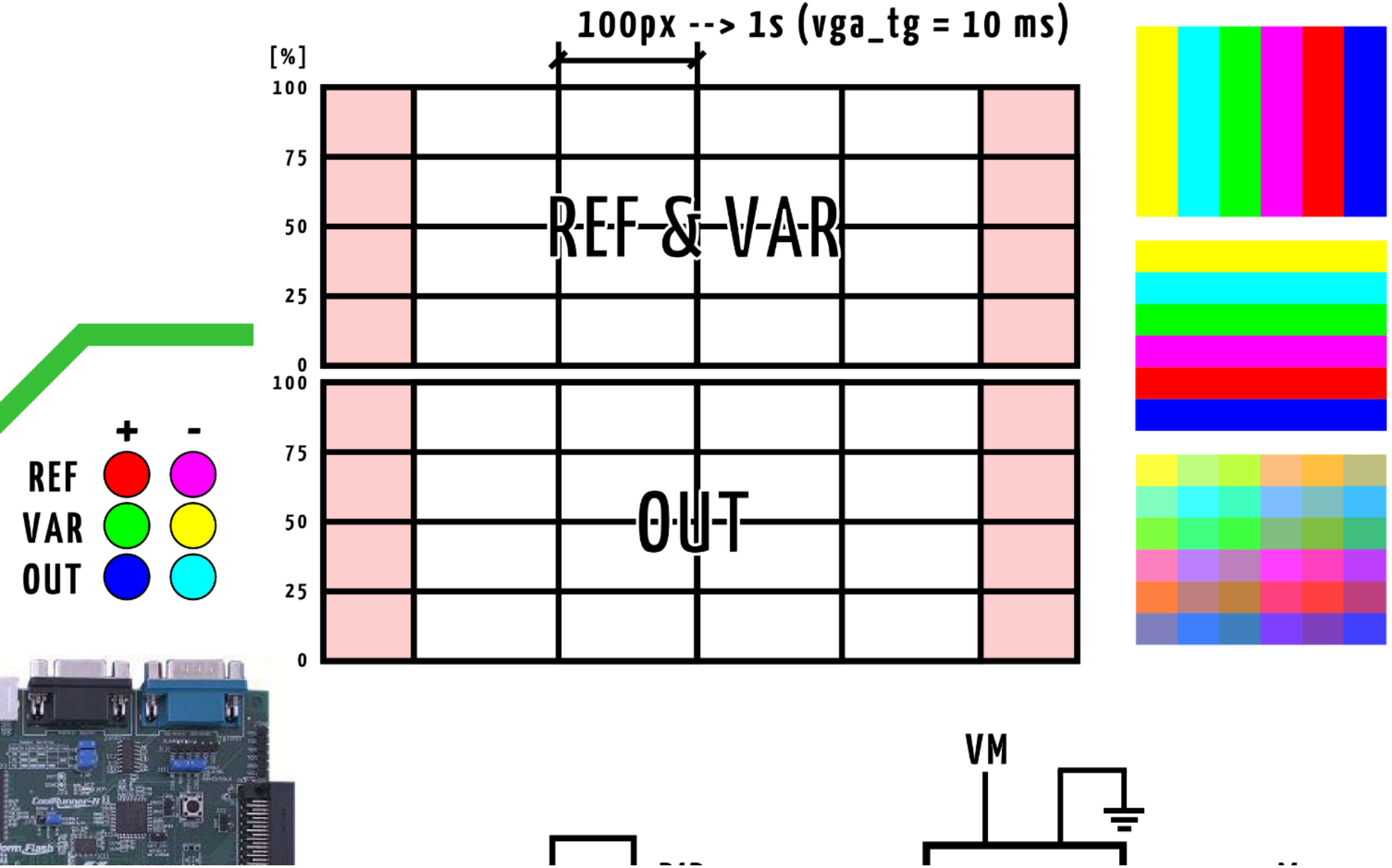
RST SMOOTH EN DIR

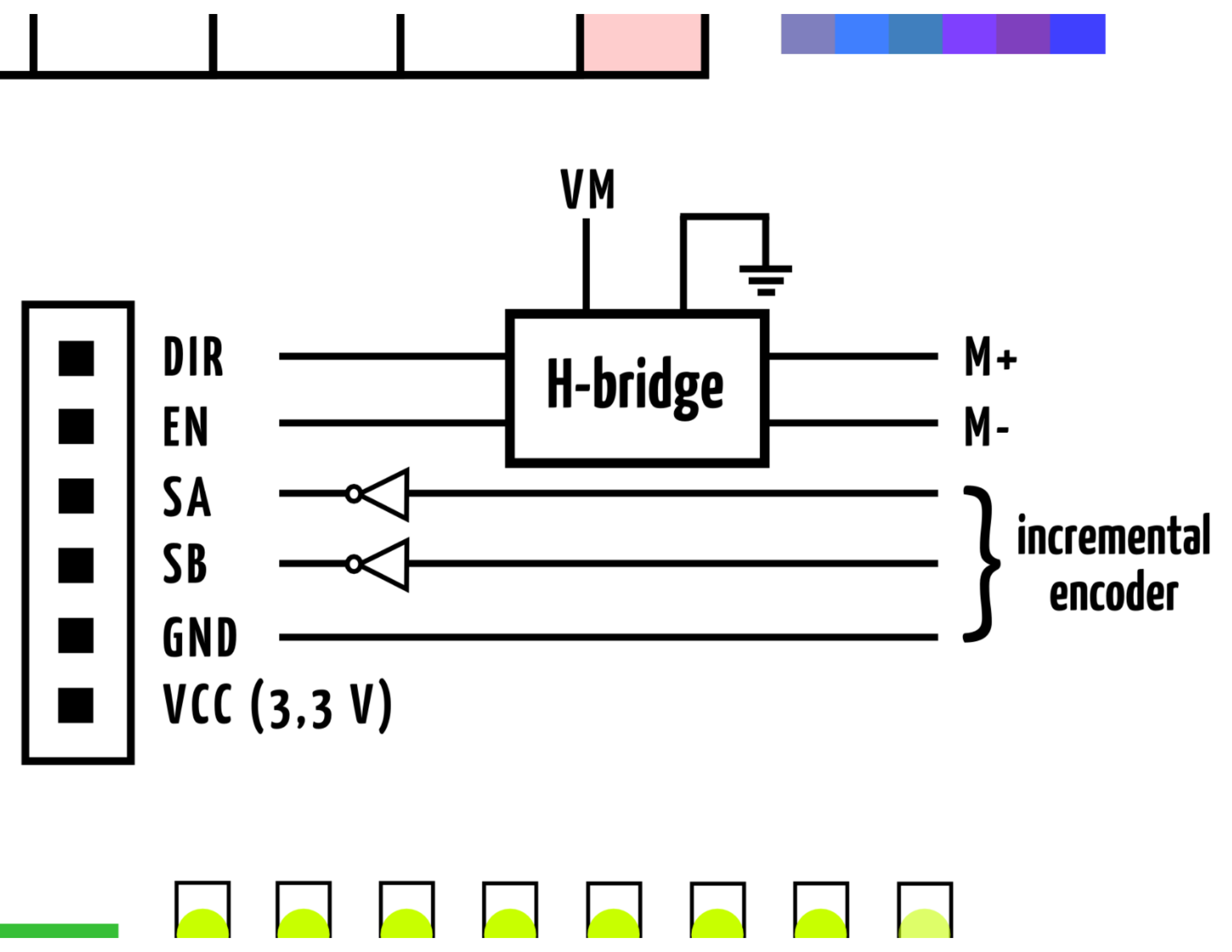
$$\frac{2 \cdot var + var \cdot z^{-1} + var \cdot z^{-2}}{4}$$

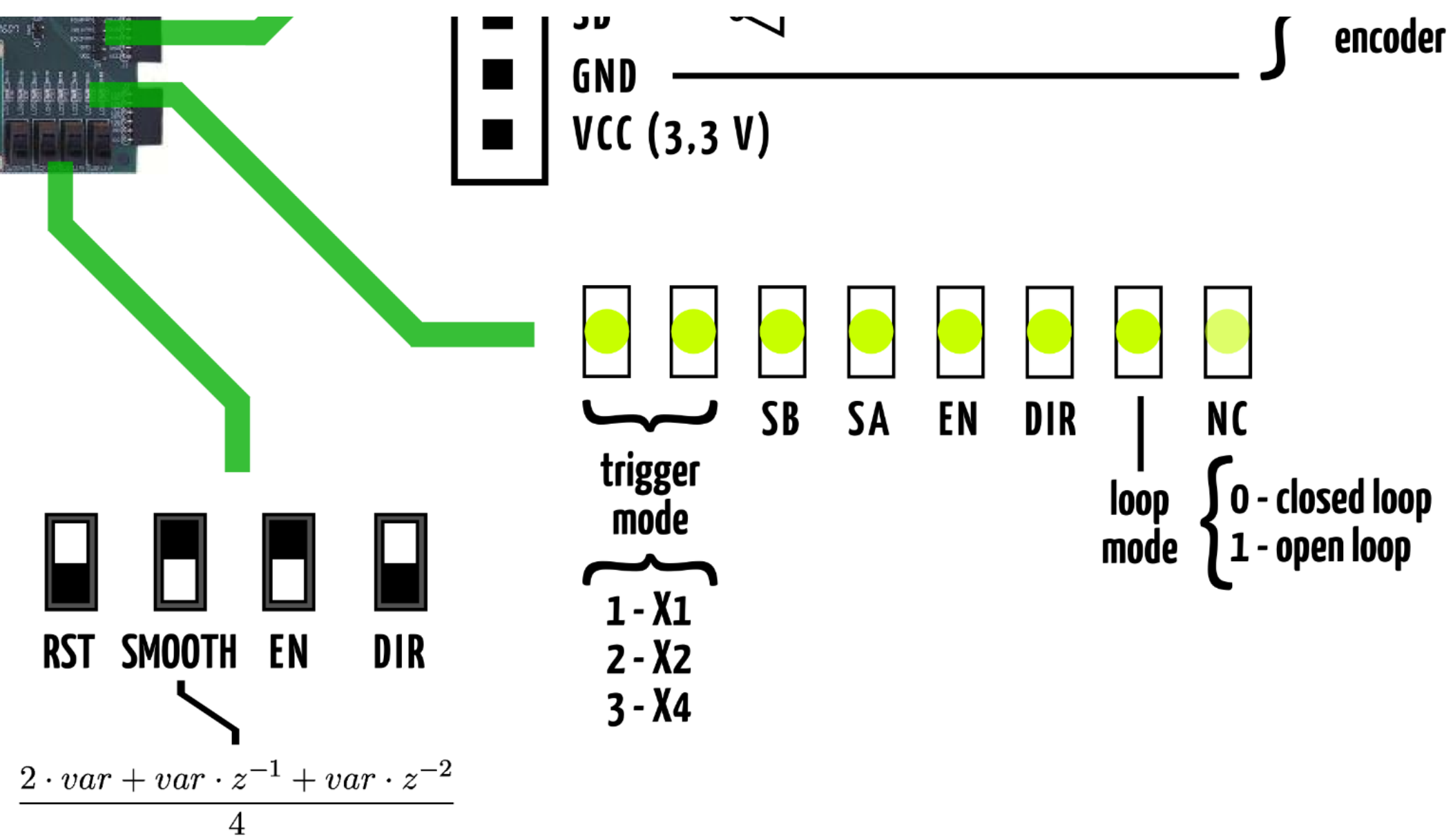
SB SA EN DIR NC

trigger mode
1 - X1
2 - X2
3 - X4

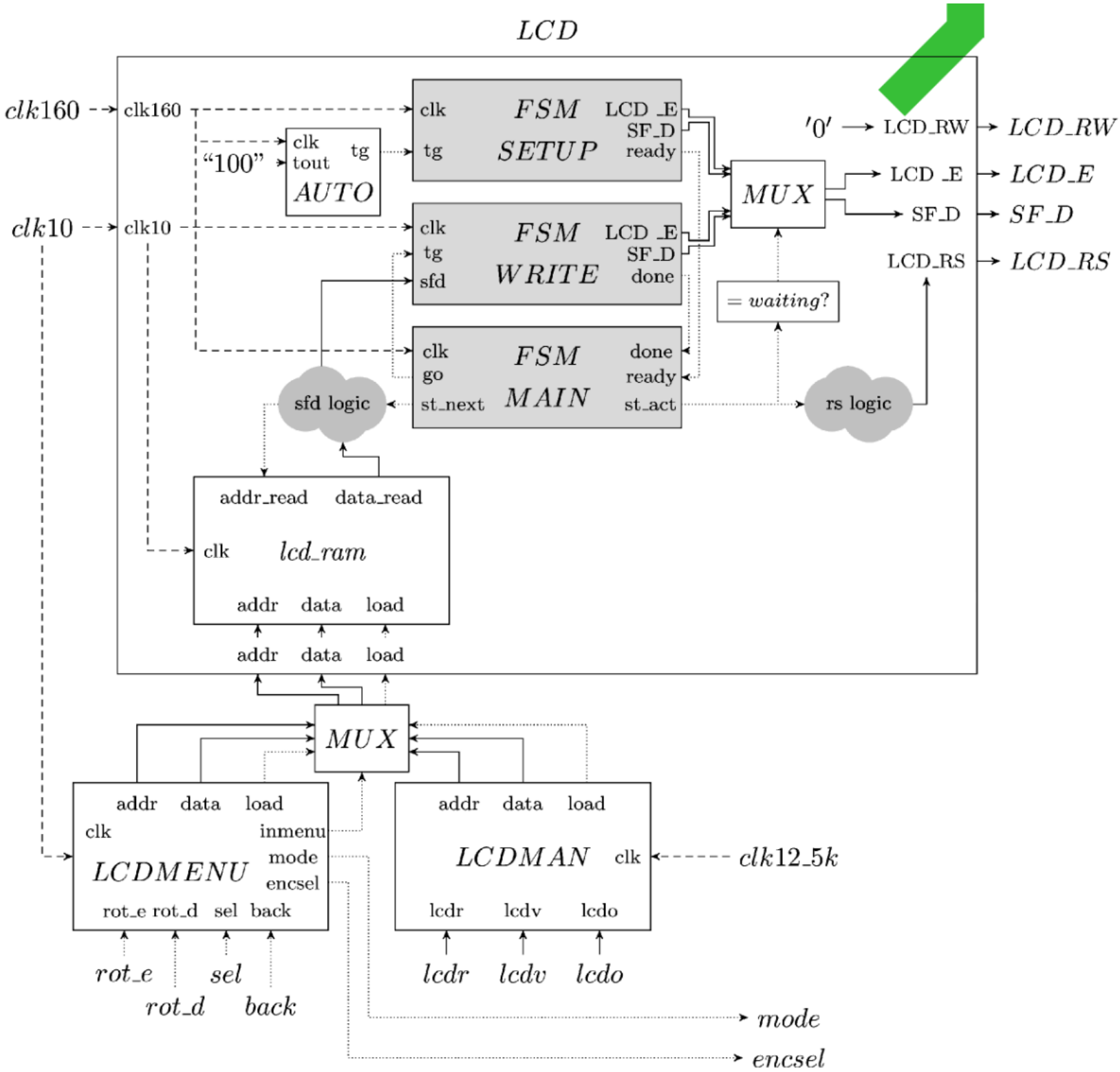
loop mode
0 - closed loop
1 - open loop

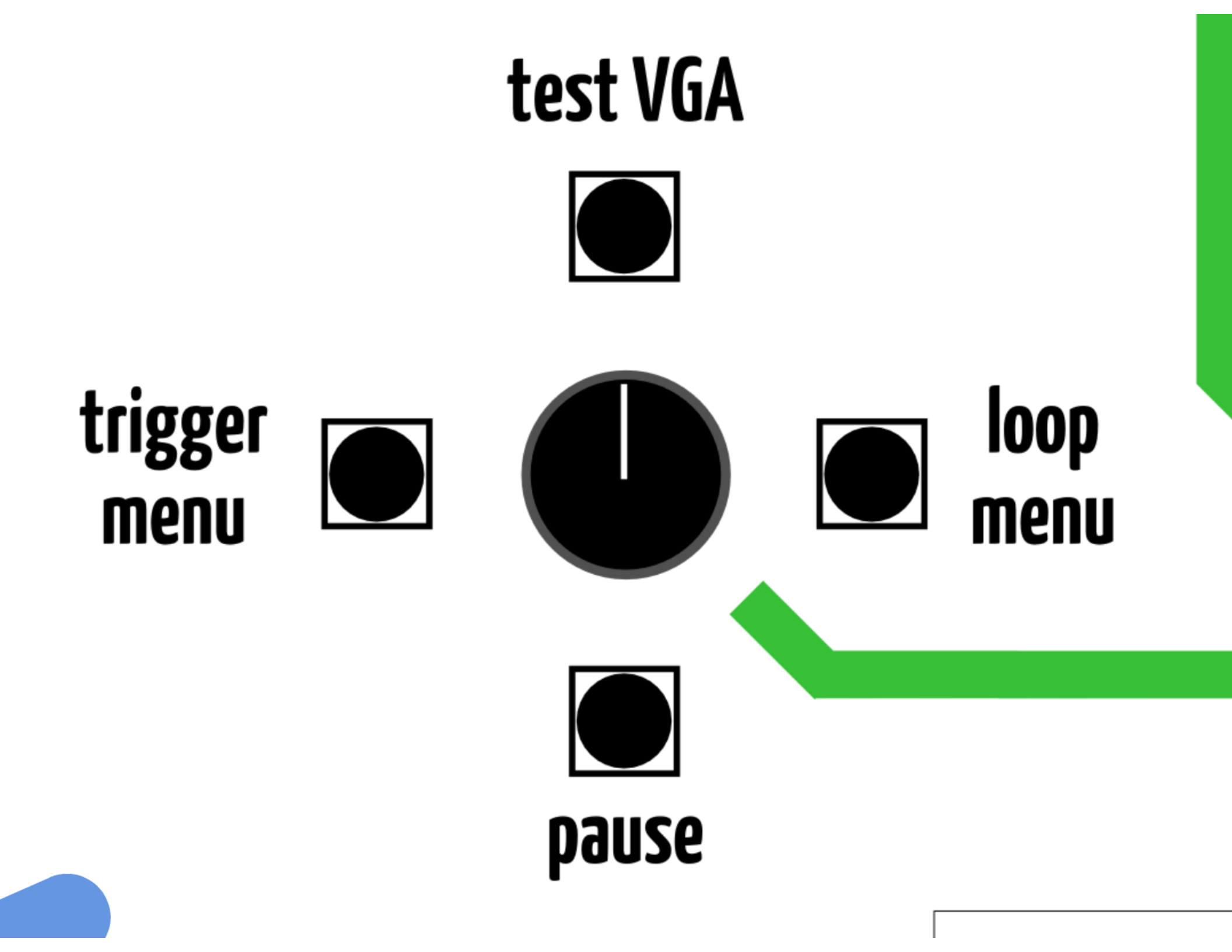

100px --> 1s (vga_tg = 10 ms)
[%]
100
75
50
25
0
REF & VAR
100
75
50
25
0
OUT
+
-
REF
VAR
OUT
VM


VM
H-bridge
DIR
EN
SA
SB
GND
VCC (3,3 V)
M+
M-
incremental
encoder

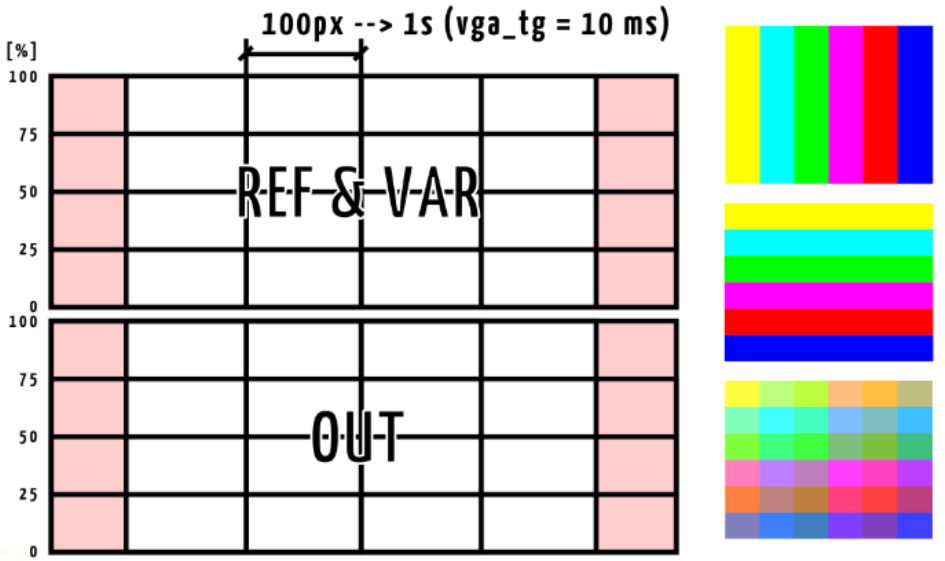


$$\frac{2 \cdot var + var \cdot z^{-1} + var \cdot z^{-2}}{4}$$


LCD
clk160
clk10
clk160
clk10
"100"
clk
tout
tg
AUTO
clk
tg
FSM
SETUP
LCD _E
SF_D
ready
clk
tg
sfd
FSM
WRITE
LCD _E
SF_D
done
clk
go
st_next
FSM
MAIN
done
ready
st_act
sfd logic
rs logic
= waiting?
'0'
MUX
LCD_RW
LCD _E
SF_D
LCD_RS
LCD_RW
LCD_E
SF_D
LCD_RS
addr_read
data_read
clk
lcd_ram
addr
data
load
addr
data
load
MUX
addr
data
load
clk
inmenu
LCDMENU
mode
encsel
rot_e
rot_d
sel
back
addr
data
load
LCDMAN
clk
clk12_5k
lcdr
lcdv
lcdo
rot_e
rot_d
sel
back
lcdr
lcdv
lcdo
mode
encsel


test VGA
trigger menu
loop menu
pause

Spartan3E Starter Kit



5 VDC, 2A Supply
100-240V AC Input
50-60 Hz

USB2
JTAG & SPI Flash programming

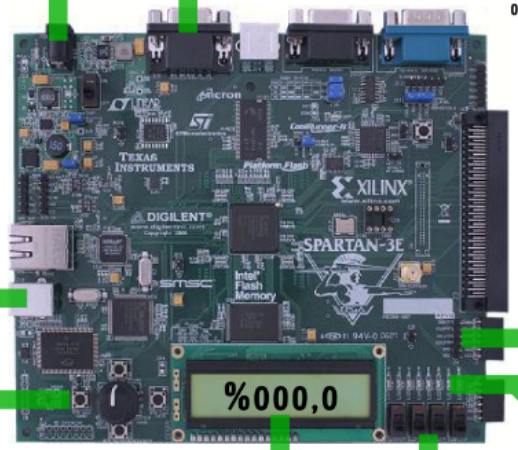
REF
VAR
OUT
\+ -

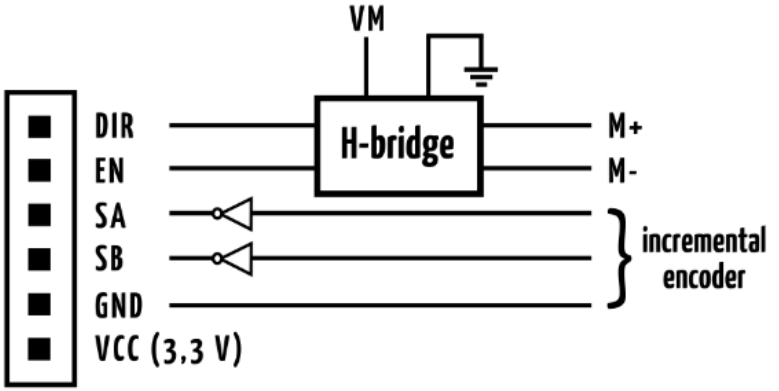
test VGA

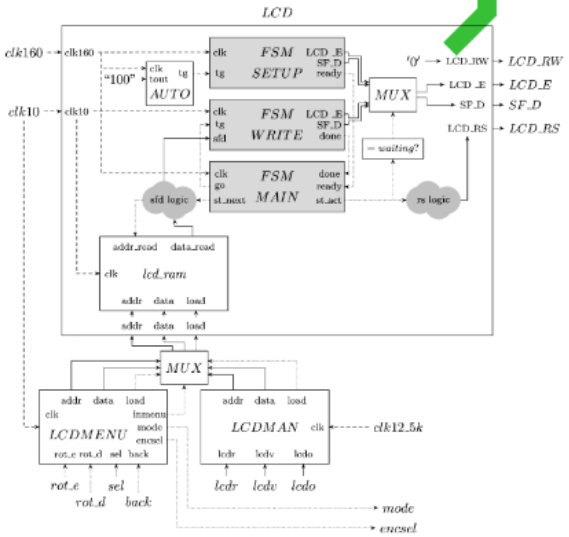
trigger menu

loop menu

pause







RST SMOOTH EN DIR

$$\frac{2 \cdot var + var \cdot z^{-1} + var \cdot z^{-2}}{4}$$

SB SA EN DIR NC

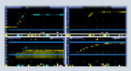
trigger mode
1 - X1
2 - X2
3 - X4

loop mode
0 - closed loop
1 - open loop

LCD

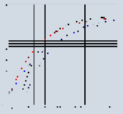
VGA

Azterketa kasua



Identifikazioa

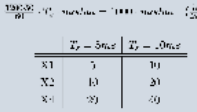
Sarrera (irakurketa)

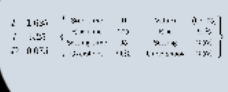


Plantaren modeloa

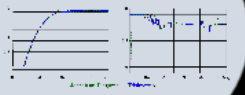
Irteera (eragitea)

Ts

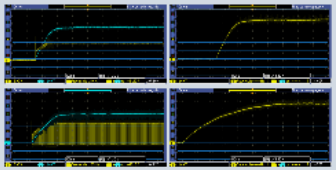




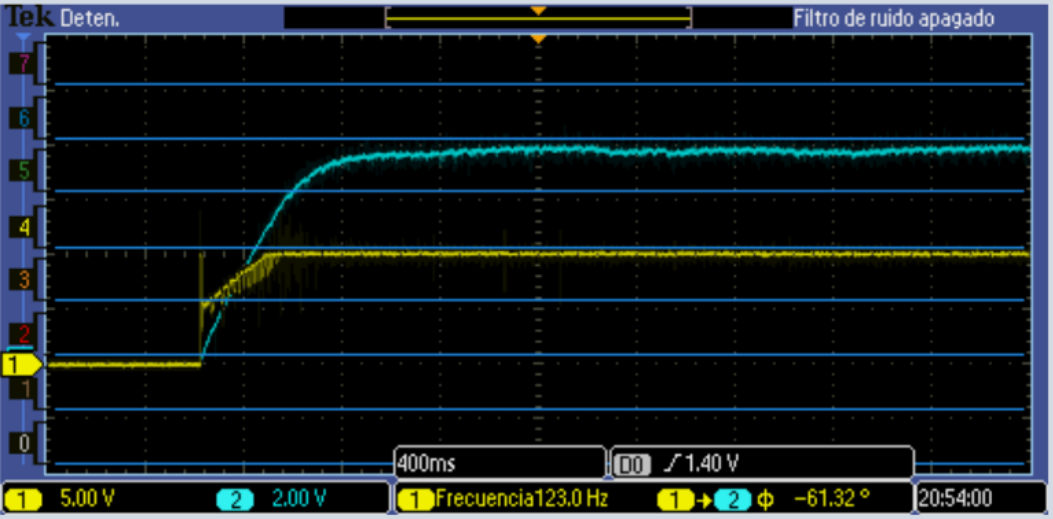
Doiketa

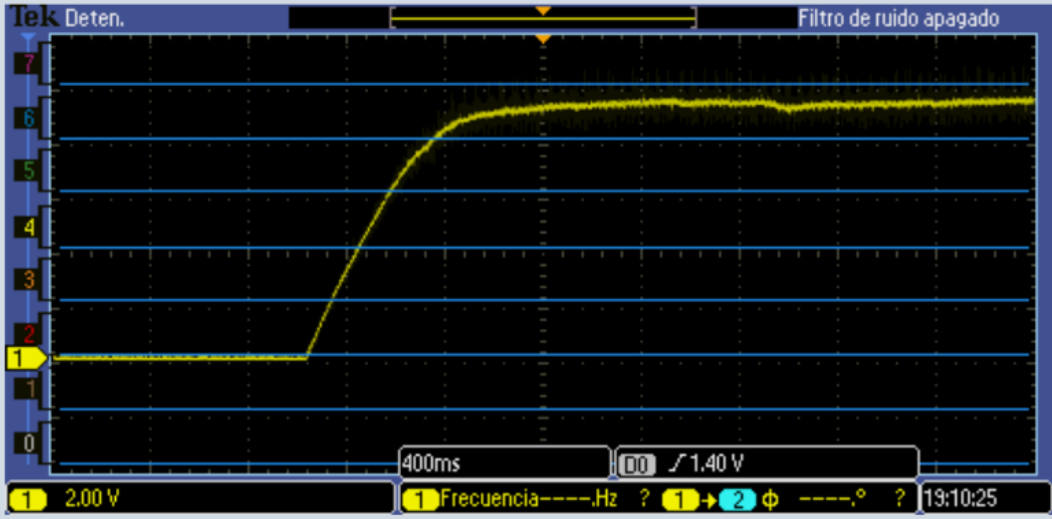


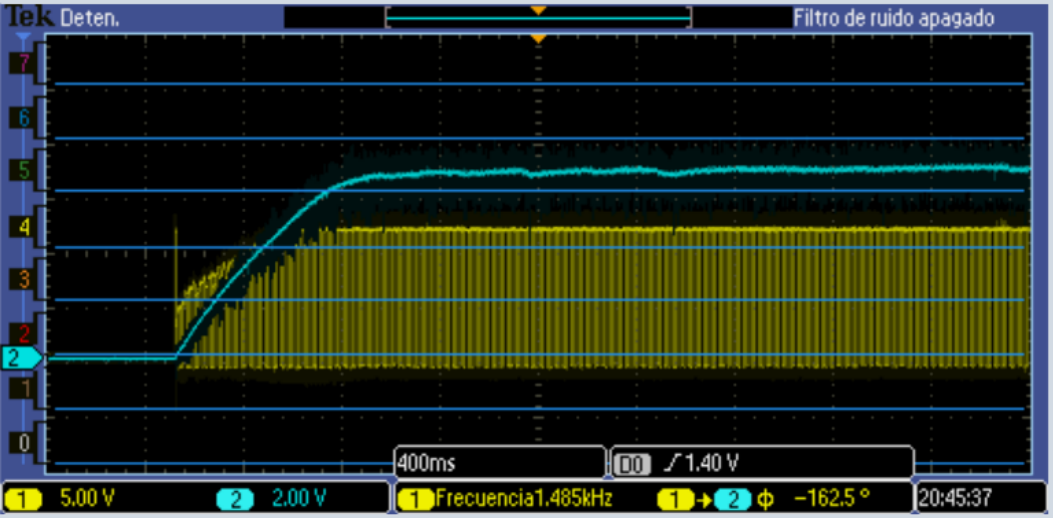
Azterketa Rasua

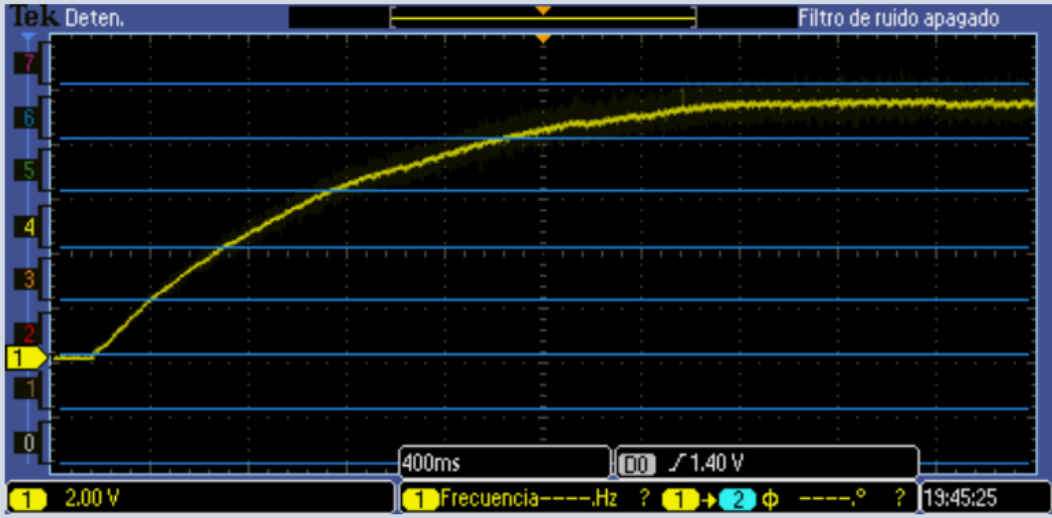


Identifikazioa

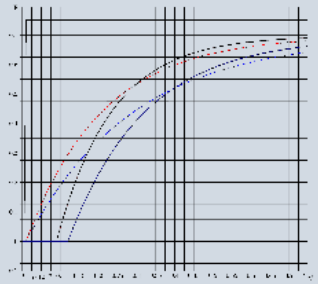

Tek Deten.
Filtro de ruido apagado
400ms
1.40 V
5.00 V
2.00 V
Frecuencia123.0 Hz
−61.32 °
20:54:00

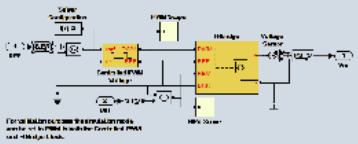

Tek Deten.
Filtro de ruido apagado
400ms
1.40 V
2.00 V
Frecuencia----.Hz
----.°
19:10:25

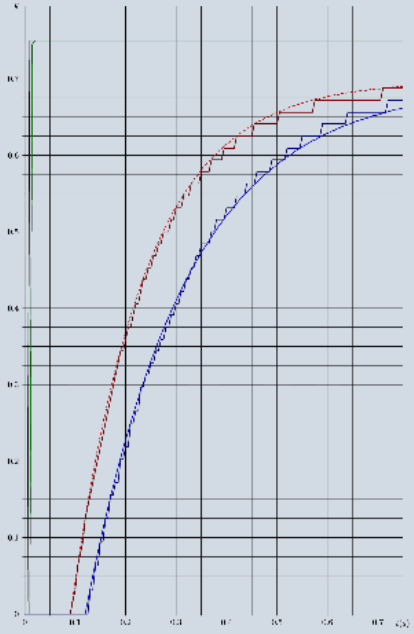

Tek Deten.
Filtro de ruido apagado
400ms
1.40 V
5.00 V
2.00 V
Frecuencia1.485kHz
−162.5 °
20:45:37

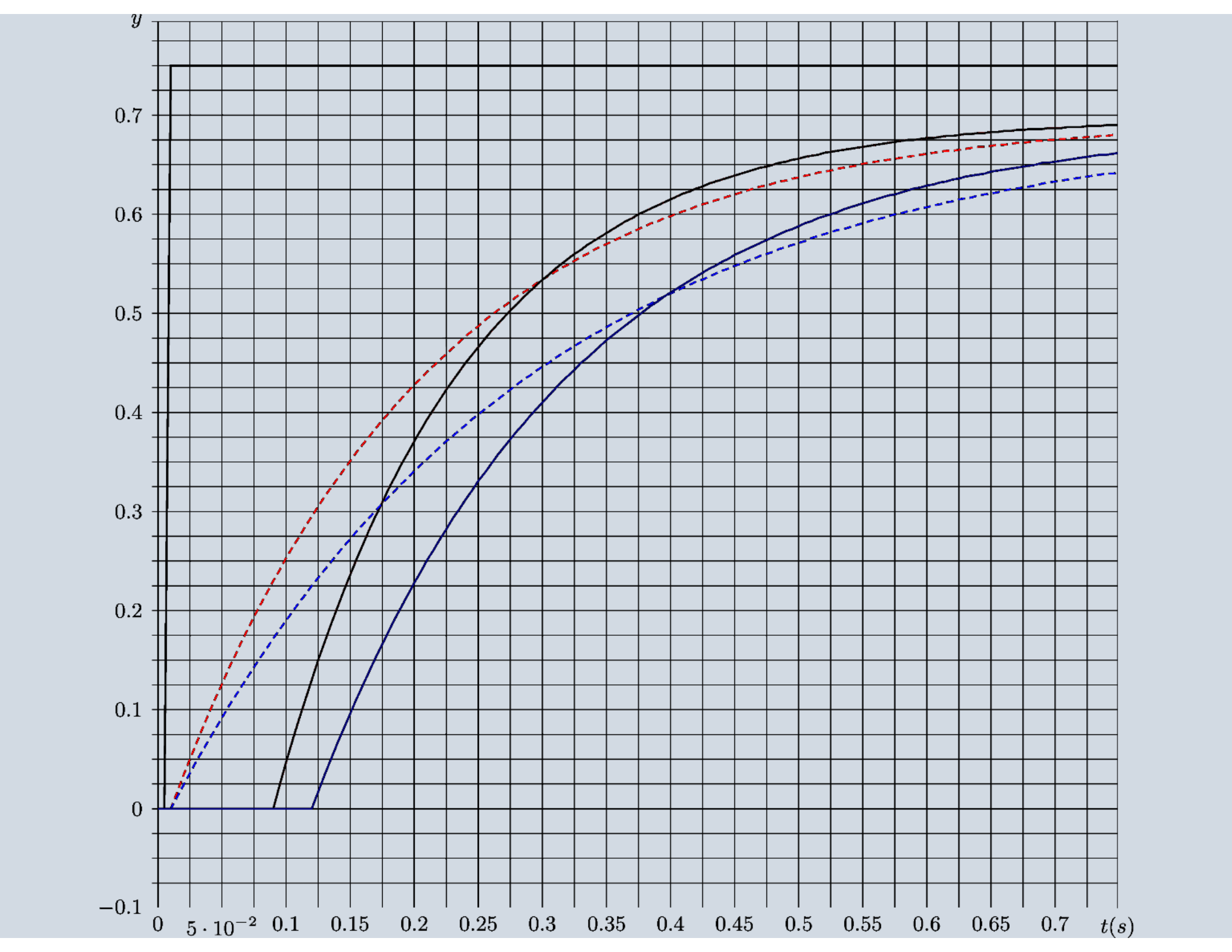

Tek Deten.
Filtro de ruido apagado
400ms
1.40 V
2.00 V
Frecuencia----.Hz
----.°
19:45:25

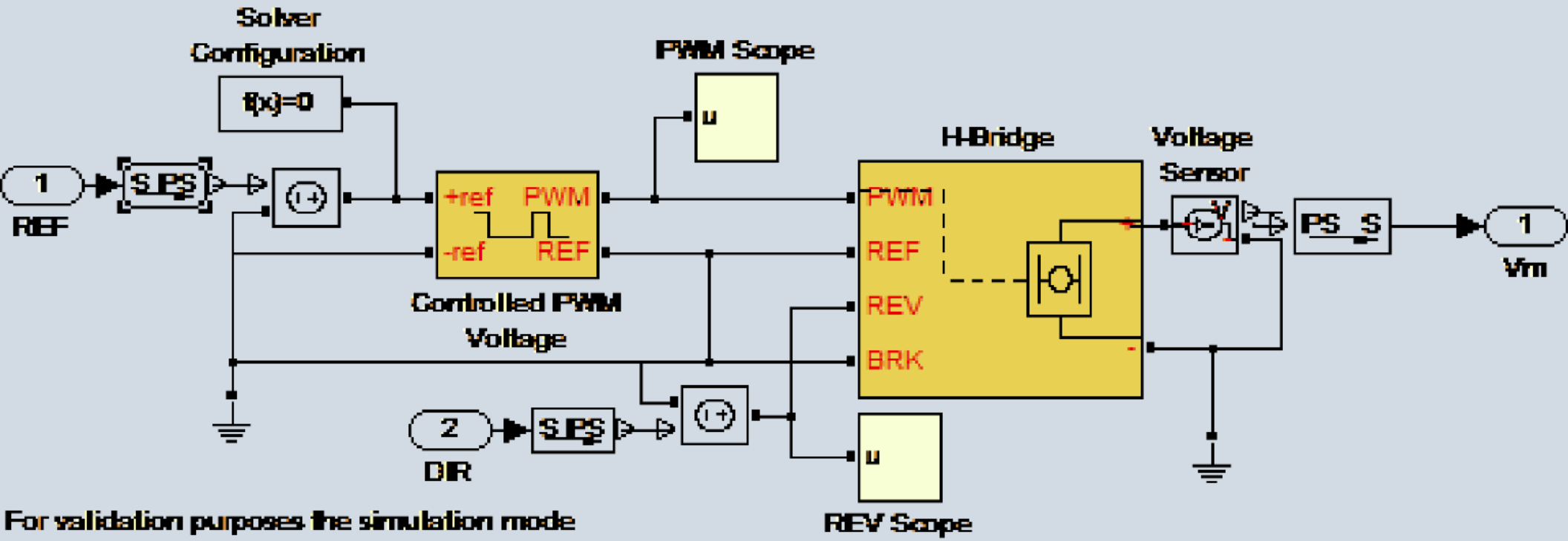
Plantaren modeloa



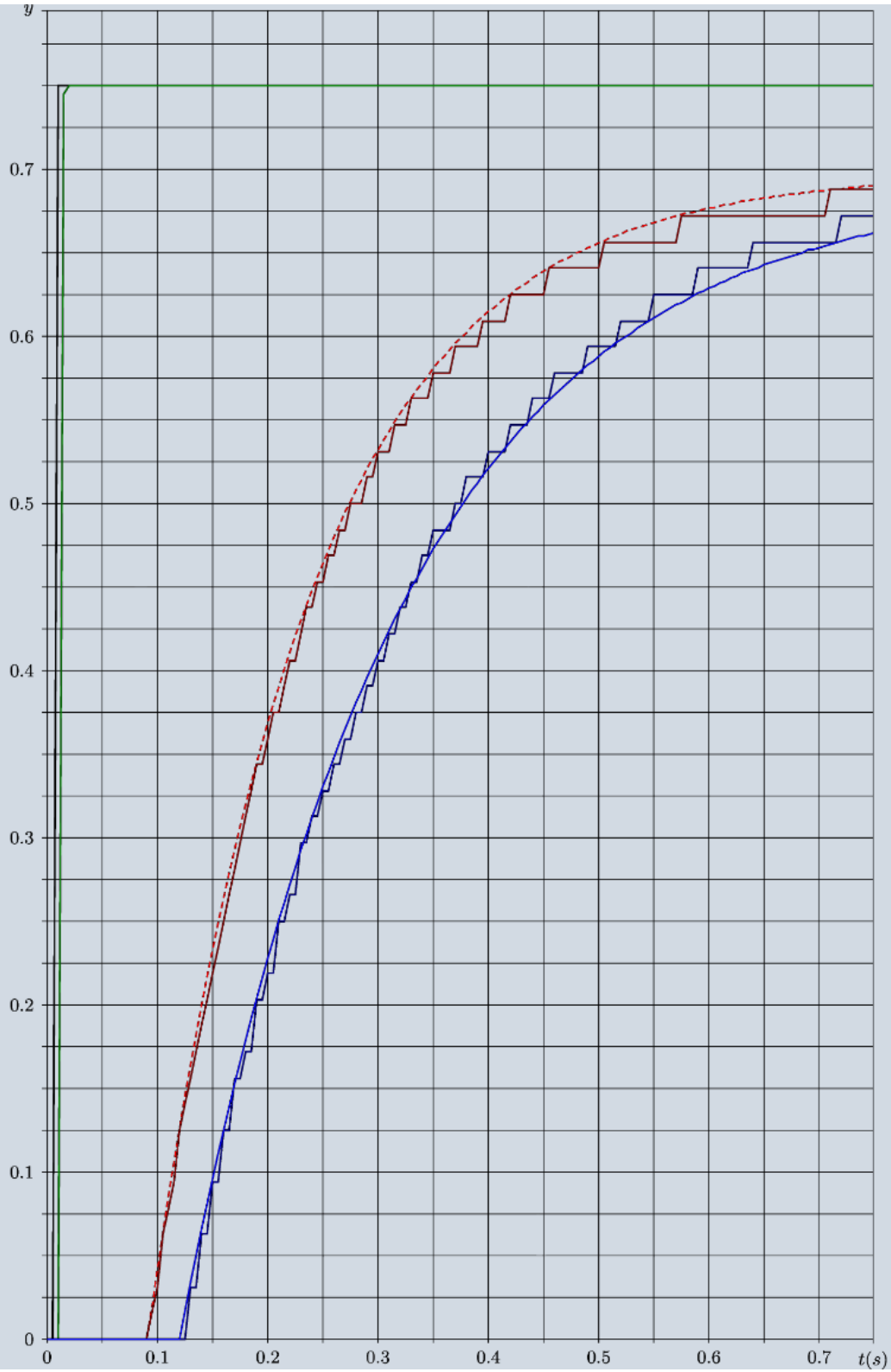





y
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
−0.1
0
5 · 10^−2
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6
0.65
0.7
t(s)



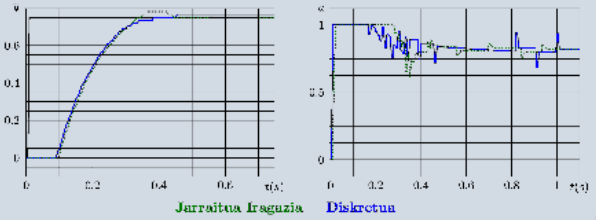
For validation purposes the simulation mode can be set to PWM in both the Controlled PWM and H-Bridge blocks.

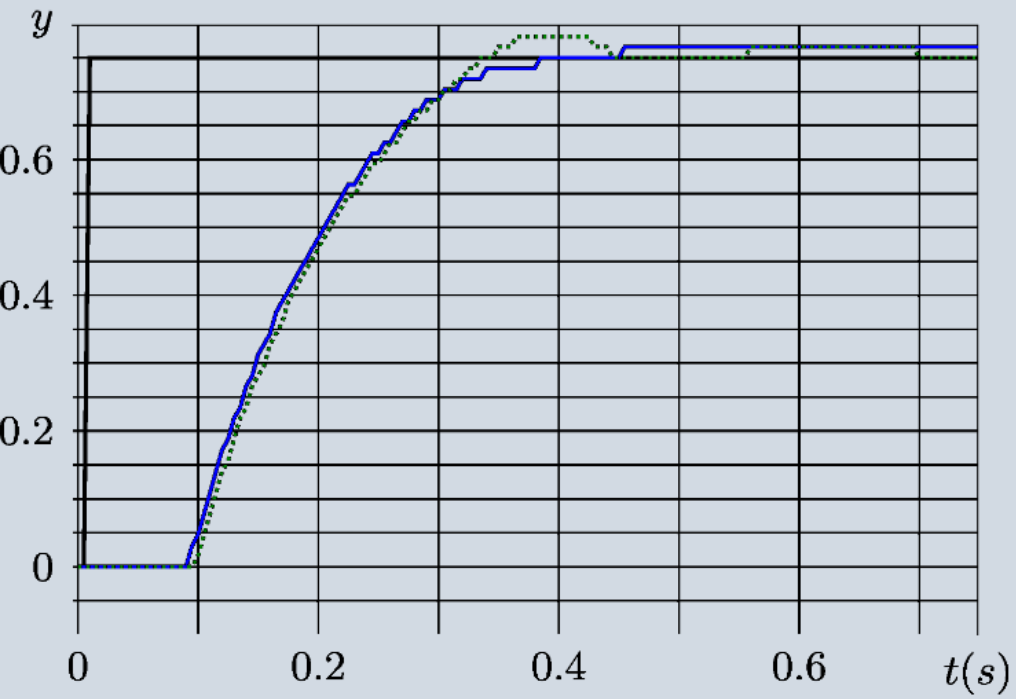

y
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
t(s)

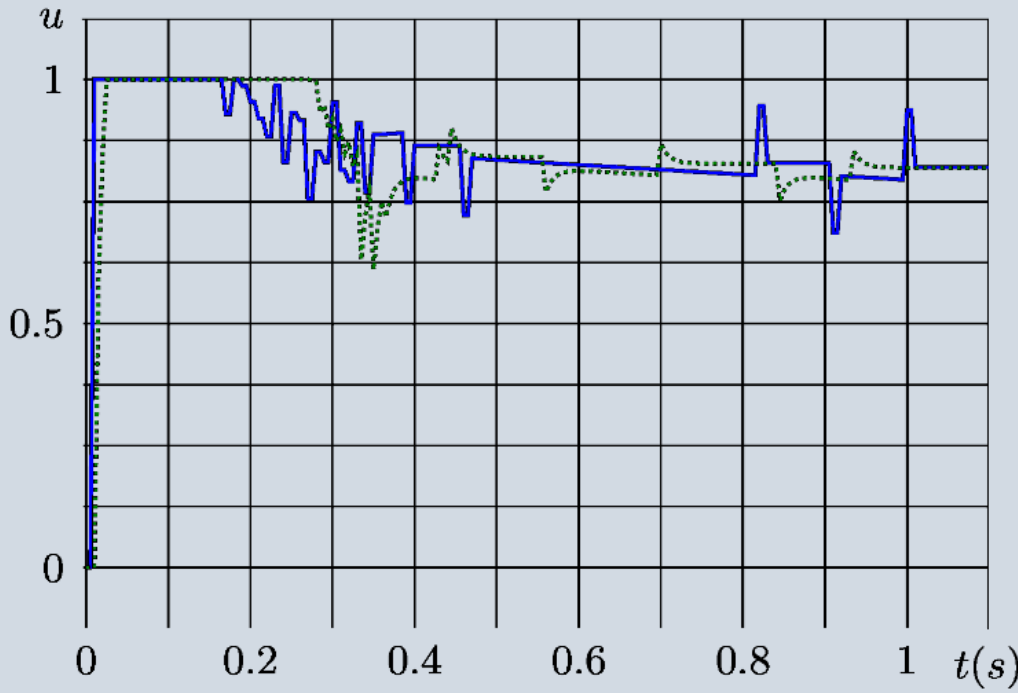
P 1.625
I 6.25
D 0.075

Step time	.01	Values	(0 : .75)
Rise time	.275	Rise	90%
Setting time	.65	Setting	2.5%
Overshoot	2.5%	Undershoot	2.5%

Doiketa







Jarraitua Iragazia **Diskretua**

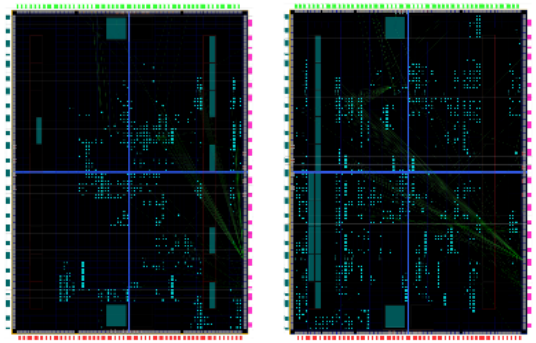
Ts

$$\frac{1200 \cdot 50}{60} \cdot T_s \cdot modua = 1000 \cdot modua \quad (\frac{inpultsu}{laginketa})$$

	$T_s = 5ms$	$T_s = 10ms$
X1	5	10
X2	10	20
X4	20	40

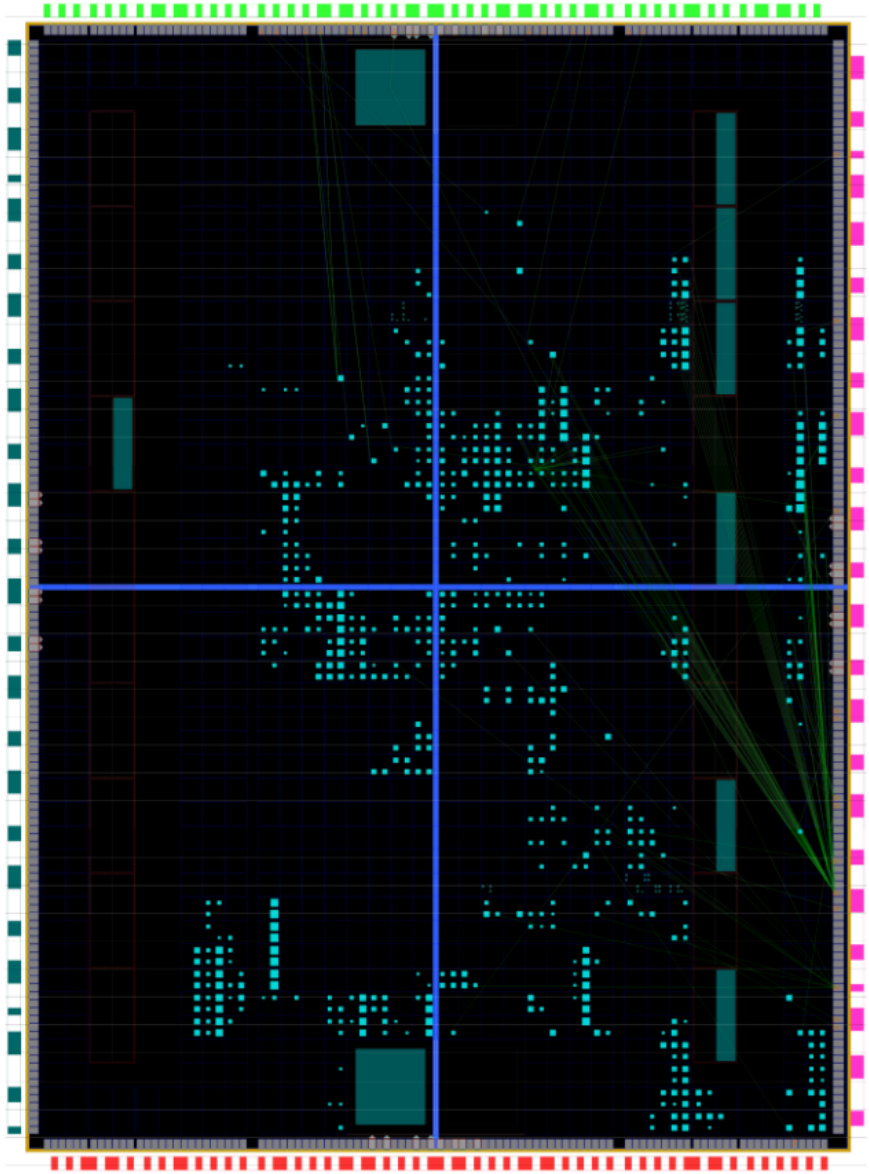
Sintesia

Inplementazio fisikoaren ikuspegi teknologikoa

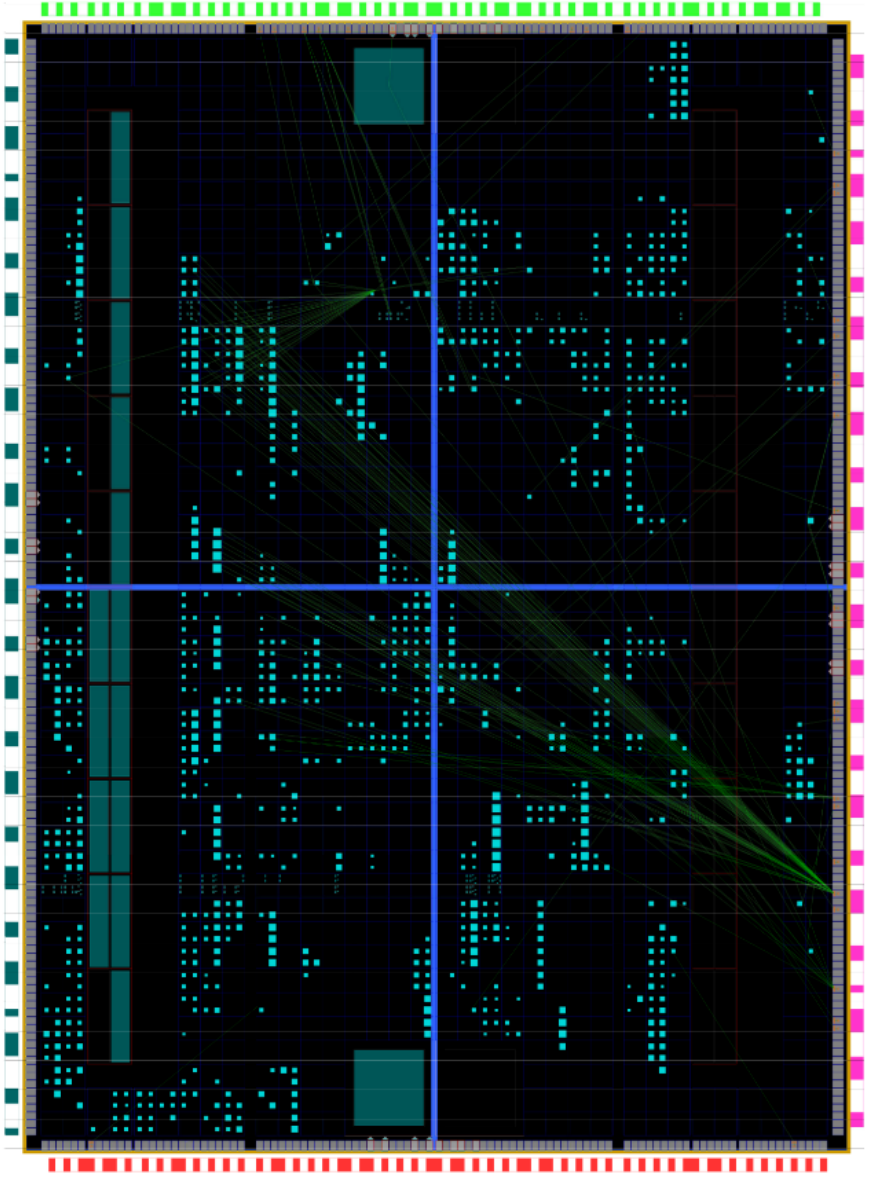


anie-tiny anie

Inplementazio fisikoaren ikuspegi teknologikoa

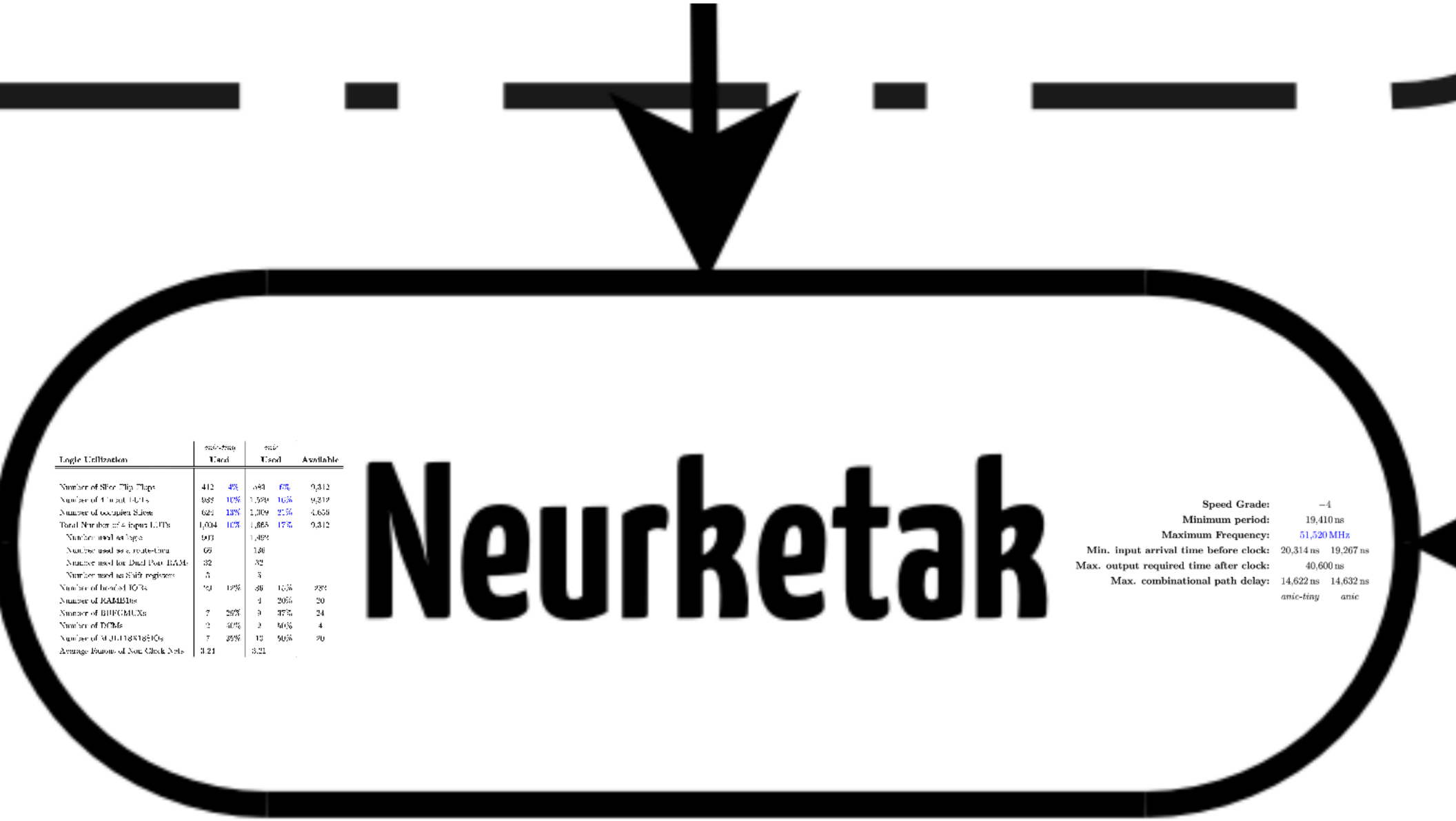


anie-tiny



anie


anie-tiny
anie
Muntaia egitea
Kontrola gauzatzea

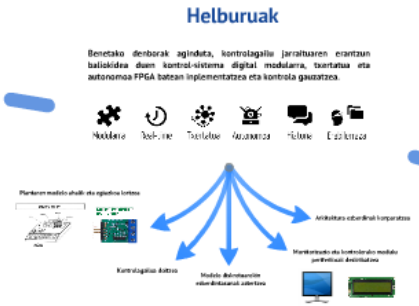


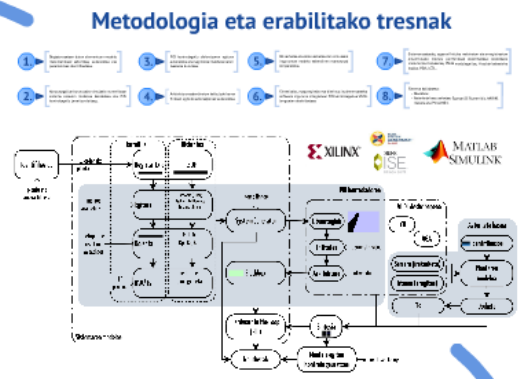
Logic Utilization	anic-tiny Used		anic Used		Available
Number of Slice Flip Flops	412	4%	580	6%	9,312
Number of 4 input LUTs	988	10%	1,529	16%	9,312
Number of occupied Slices	621	13%	1,009	21%	4,656
Total Number of 4 input LUTs	1,004	10%	1,865	17%	9,312
Number used as logic	903		1,489		
Number used as route-thru	69		136		
Number used for Dual Port RAMs	32		32		
Number used as Shift registers	5		5		
Number of bonded IOBs	91	12%	86	11%	934
Number of RAMB16s			4	20%	20
Number of BUFGMUXs	7	29%	8	33%	24
Number of DCMs	2	50%	2	50%	4
Number of PLL18X18SIOs	7	35%	18	90%	20
Average Fanout of Non-Clock Nets	3.21		3.21		

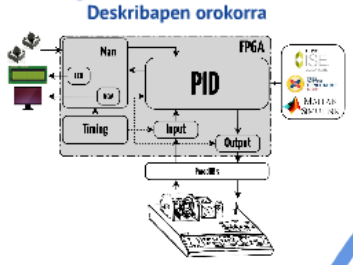
Speed Grade:	−4	
Minimum period:	19,410 ns	
Maximum Frequency:	51,520 MHz	
Min. input arrival time before clock:	20,314 ns	19,267 ns
Max. output required time after clock:	40,600 ns	
Max. combinational path delay:	14,622 ns	14,632 ns
	anic-tiny	*anic*

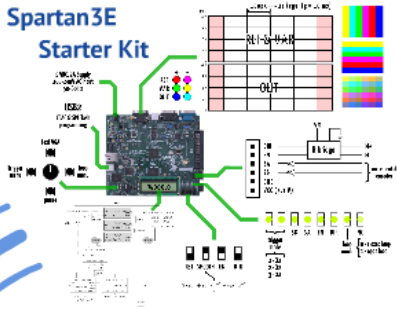
Logic Utilization	*anie-tiny* Used		*anie* Used		Available
Number of Slice Flip Flops	412	4%	583	6%	9,312
Number of 4 input LUTs	938	10%	1,529	16%	9,312
Number of occupied Slices	624	13%	1,009	21%	4,656
Total Number of 4 input LUTs	1,004	10%	1,665	17%	9,312
Number used as logic	903		1,492		
Number used as a route-thru	66		136		
Number used for Dual Port RAMs	32		32		
Number used as Shift registers	3		5		
Number of bonded IOBs	29	12%	36	15%	232
Number of RAMB16s			4	20%	20
Number of BUFGMUXs	7	29%	9	37%	24
Number of DCMs	2	50%	2	50%	4
Number of MULT18X18SIOs	7	35%	10	50%	20
Average Fanout of Non-Clock Nets	3.24		3.21		

Speed Grade:	−4	
Minimum period:	19,410 ns	
Maximum Frequency:	51,520 MHz	
Min. input arrival time before clock:	20,314 ns	19,267 ns
Max. output required time after clock:	40,600 ns	
Max. combinational path delay:	14,622 ns	14,632 ns
	anie-tiny	*anie*









Laburbilduz

- Abstrakzio-maila baxuko garapen osoa.
- Esperimentalki balidatutako sistema.
- Azterketa bibliografiko zabala.
- Irudien eta bestelako baliabideen biltegi irekia.
- Plataforma ezberdinetan, tresna ireki eta askeekin egindako dokumentazioa.