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Advanced Techniques for Diagnostics and Control Applied to Particle Accelerators

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by

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Laburpena

Tesi honek jorratzen du partikula-azeleragailuen diagnostiko eta kontrol tresnei zuzenduriko teknika eta teknologia aurreratuen gaia. Aipaturiko tresnentzako bi aplikazioen inguruan zentraturik dago nagusiki: sorta-posizioaren monitore (BPM, Beam Postion Monitor ingelesez) bat alde batetik, eta maila baxuko RF (LLRF, Low Level-RF ingelesez) izeneko kontrol sistema bat bestetik.

Partikula-azeleragailuak ezinbesteko tresnak dira zientzia ulertzeko eta anbizio handiko erronka zientifikoei aurre egiteko. Hala ere, mota honetako makinen erabilera ez da bakarrik proiektu zientifiko handien esparrura mugatzen. Izan ere, azeleragailu gehienak aplikazio mediko eta industrialetara zuzendurik daude.

Makina hauen konplexutasun handia dela eta, erronka teknologiko oso handia dira, eta beraz, oso bizia da haien inguruko tresneria eta teknologia berrien ikerketa eta garapena.

Diagnostikoak eta RF kontrola, edozein partikula-azeleragailuren funtsezko atalak dira. Diagnostikoak ezinbestekoak dira makinaren doiketan eta funtzionamendu normalean. Makinaren osagai eta prozesu askoren inguruko informazio inportantea eskaintzen dute. Neurtu nahi den aldagaiaren edo azeleragailu motaren arabera, hainbat fenomeno fisikotan oinarriturik egon daitezke. Diagnostiko tresna askok, prezisio altuko neurketak burutu behar dituzte informazio erabilgarria eskaini ahal izateko.

Beste alde batetik, RF kontrol sistemak nahitaezkoak dira partikulen azelerazio prozesuan. Sistema hauen diseinu eta garapenean, ezinbestekoa suertatzen da kontrol automatikoaren eta RF-aren jakintza arloen elkarlana, kontrolatu beharreko aldagaiak abiadura altuko seinaleak baitira, ehunka MHz-ren ordenakoak. Azelerazio egokia emateko, partikulak garraio-uhinarekin sinkronizatu behar dira. Horrek eskatzen du seinalearen anplitude eta fasearen kontrol azkar eta zehatza.

Honela, tesi honen motibazioa izan da partikula-azeleragailuentzako diagnostiko eta kontroleko tresna flexible, modular eta berkonfiguragarri berrien garapena. Horretarako, soluzio digitaletan oinarritzea erabaki da. Horrek, diseinuan aldaketa handiak burutzea ahalbidetzen du, esaterako, funtzionalita-

teak gehitu edo aldatu, programaren kodea baino ez aldatuz. Ezaugarri hau oso abantaila handia da prototipazioari begira, garapen denbora murriztu eta errekerimendu berriei aurre egitea ahalbidetzen baitu.

Hau guztia kontuan hartuta, National Instruments-eko PXIe plataforma aukeratu da proposaturiko aplikazio berrien garapenaren arkitektura nagusi bezala. PXIe-k, mota askotako moduluak eskaintzen ditu. Esaterako, data eskuraketa, data sorrera, FPGA teknologia, timing-a, etab. Arkitektura honen beste abantaila handi bat da sistema osoa ingurugiro berdinpean integratzeko aukera, LabVIEW bitartez operatua. Ezaugarri honek errazten du hardware gailu anitzen integrazioa, driver-en garapena, puntuz-puntuko komunikazioa edota DMA bitartezko transferentziak bezalako prozesuen konplexutasuna gutxituz. Aipatzekoa da ere, LabVIEW-ren erabilpenak ahalbidetu duela FPGA-n oinarrituriko txartelak programatzea ahalbidetu duela maila-baxuko VHD kodea erabili barik, modu honetan garapena erraztuz denbora eta esfortzuaren ikuspegitik.

Proposaturiko ideiarekin jarraituz, gailu analogikoak ekiditea izan da lan honen helburuetako bat, ahal den heinean. Hau erronka bat da, RF-ko seinaleak erabiltzen baitira, haien frekuentzia harmarka edo ehunka MHz-takoa izanik. Garaturiko aplikazioetan, RF seinaleak zuzenean lagintzen dira, seinalea eta ADC-en artean inolako tarteko etaparik gabe.

Ohiko laginketa teknikak erabiltzea oso laginketa abiadura azkarren beharra suposatzen du lan arlo honetan, ekipamendu garestiaren erabilpena dakarrena. Hain abiadura azkarrak ekiditeko asmoz, eta ondorioz, soluzio merkeagoak eraiki ahal izateko, azpilaginketa (subsampling ingelesez) izeneko laginketa teknika aurreratu bat aztertu eta inplementatu da. Teknika hau aliasing deituriko fenomenoaz baliatzen da frekuentzia baxuetan kokaturiko informaziotik seinaleak berreraikitzeko, modu honetan abiadura gutxiagoko ADC-ak erabiltzea ahalbidetuz. Teknika honen erabilpena, garaturiko diagnostiko eta kontrol tresnetako oso parte garrantzitsua da.

Modu honetan, tesi honen kontribuzio aipagarrienak dira BPM baten eta LLRF kontrol sistema baten garapena, biak era flexible eta berkonfiguragarrian eratuta eta hardware digitalean oinarrituta. Aurkeztutako soluzioak, diseinatuak izan dira laborategi-prototipaziorako lagungarriak diren tresnak eratzeko helburuarekin, aldi berean instalazio erreal batean modu errazean integragarriak izanik. Lortutako aplikazioek bete egiten dute helburu hau, modularitate handia eta prototipazio azkarra bezalako ezaugarri baliotsuak edukirik. Diseinaturiko sistemen balidazio esperimentala burutzeko, laborategi-muntaiak eraiki dira, modu honetan aipaturiko tresnak laborategian frogatu ahal izateko. Haien

bitartez, hainbat esperimentu burutu dira, emaitza egokiak lortu direlarik.

Horrez gain, tesi honetan aurkezturiko beste ikerketa lerro batek jorratzen ditu aipaturiko tresnek eskaintzen dituzten datuak EPICS-en integratzeko soluzioak, hau izanik partikula-azeleragailu askotan erabilitako kontrol teknologia garrantzitsuenetarikoa.

Resumen

Esta tesis versa en torno a tecnologías y técnicas novedosas orientadas al diagnóstico y control para aceleradores de partículas. Se centra principalmente en el desarrollo de dos aplicaciones para dicho propósito: un monitor de posición de haz (beam position monitor o BPM en inglés) por un lado, y un control de RF denominado sistema de RF de bajo nivel (low-level RF o LLRF en inglés) por el otro.

Los aceleradores constituyen herramientas fundamentales para el estudio de la ciencia y para ayudar a afrontar algunos de los retos científicos más ambiciosos. Aún así, el uso de este tipo de máquinas no se limita a grandes proyectos científicos. De hecho, la gran mayoría de los aceleradores están orientados a aplicaciones médicas e industriales.

Debido a la gran complejidad de estas máquinas, representan un gran reto tecnológico, y por lo tanto, la investigación y el desarrollo de nuevas tecnologías en este área es muy dinámico.

Los diagnósticos y el control RF son aspectos esenciales en cualquier acelerador de partículas. Los diagnósticos son clave en el ajuste y la operación normal de la máquina. Proporcionan información relevante relacionada con numerosos procesos y componentes de la máquina, y pueden estar basados en diferentes fenómenos físicos dependiendo en la variable que se desea medir o el tipo de acelerador. Muchas de estas herramientas de diagnóstico necesitan efectuar medidas de gran precisión para poder generar información útil.

Por otro lado, los sistemas de control RF son vitales para el proceso de aceleración de las partículas. En el diseño y desarrollo de estos sistemas, la colaboración entre las áreas de conocimiento del control automático y las RF es necesaria, ya que las variables que se requiere controlar son señales de alta velocidad, habitualmente del orden de centenas de MHz. Para una aceleración correcta, las partículas deben sincronizarse con la onda viajera, lo que requiere un control rápido y preciso de la amplitud y la fase de la señal.

Así, la motivación de esta tesis ha sido el desarrollo de nuevas herramientas flexibles, modulares y reconfigurables para el diagnostico y control para aceleradores de partículas. Para este propósito, se ha tomado la decisión de basarlas

en soluciones digitales. Esto permite introducir cambios sustanciales en el diseño, así como añadir o cambiar funcionalidades simplemente modificando el código del programa. Esta característica es una gran ventaja a la hora de prototipar, ya que reduce el tiempo de desarrollo y permite una rápida adaptación a nuevos requerimientos.

Considerando esto, se ha escogido la plataforma PXIe de National Instruments como la arquitectura principal para el desarrollo de las aplicaciones descritas. PXIe proporciona una gran variedad de módulos de muy diversa índole, como adquisición de señal, generación de señal, tecnología FPGA, temporización, etc. Otra gran ventaja de trabajar con esta arquitectura es que todo el sistema puede ser integrado bajo un entorno común operado en LabVIEW. Esto facilita la tarea de integrar una gran cantidad de dispositivos hardware, reduciendo el esfuerzo empleado para tareas complejas como el desarrollo de drivers, el uso de comunicaciones punto-a-puto o transferencias por DMA entre otras. También cabe destacar que el uso de LabVIEW ha permitido programar tarjetas basadas en FPGA en lenguaje estándar de LabVIEW, evitando el uso de VHD a bajo nivel, lo que ha facilitado el desarrollo en términos de esfuerzo y tiempo.

Siguiendo con la idea propuesta, uno de los objetivos de este trabajo ha sido evitar en lo posible el uso de componentes analógicos en el diseño de la herramientas propuestas. Esto supone un reto debido a que se emplean señales de RF, cuya frecuencia se encuentra en el rango de las decenas o centenas de MHz. En las aplicaciones desarrolladas, las señales RF son muestreadas directamente, evitando cualquier etapa intermedia entre la señal y los ADCs.

El uso de técnicas convencionales de muestreo conlleva la necesidad de velocidades de muestreo muy altas en el presente área, lo que se traduce en el empleo de equipamiento costoso. Con el objetivo de evitar tan altas velocidades de muestreo y por lo tanto construir soluciones más económicas, se ha estudiado e implementado una técnica de muestreo avanzada conocida como submuestreo (subsampling en inglés). Esta técnica hace uso del fenómeno denominado *aliasing* para reconstruir señales desde la información alojada en frecuencias bajas, abriendo la puerta al uso de ADCs de menor velocidad. La aplicación de esta técnica juega un papel central en las soluciones de diagnostico y control desarrolladas.

De esta manera, las principales contribuciones de esta tesis son el desarrollo de un BPM y un sistema de control LLRF altamente flexibles y reconfigurables, estando ambos basados en hardware digital. Las soluciones presentadas han sido diseñadas para crear herramientas que faciliten las labores de prototipado en laboratorio, aún siendo fácilmente integrables en una instalación real. Las

aplicaciones obtenidas cumplen este objetivo, mostrando características especialmente valiosas como una rápida etapa de prototipado y alta modularidad. Para la validación experimental de los sistemas diseñados, se han desarrollado completos bancos de pruebas, permitiendo de esta manera el testeo de las mencionadas soluciones en el laboratorio. Haciendo uso de ellos, las soluciones desarrolladas han sido testeadas en diversos experimentos, obteniendo resultados satisfactorios.

Adicionalmente, otra linea de investigación presentada en esta tesis se centra en la integración de los datos proporcionados por las mencionadas herramientas en redes EPICS, una de las principales tecnologías de control empleadas en muchos aceleradores de partículas.

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CHAPTER 1

Introduction

This PhD dissertation has been carried out under the guidance of Professor Josu Jugo, from the Department of Electricity and Electronics of the University of Basque Country UPV/EHU. It deals with advanced techniques and technologies oriented towards diagnostics and control for particle accelerators. It is mainly focused on the development of two applications for these purposes, a beam diagnostic application on the one hand and a RF control in the other. In addition, complete laboratory testbenches have been developed, thus allowing for the testing of the solutions developed in our laboratory. The study of sampling and digital processing techniques to be applied also play an important role in this thesis work.

The main contributions of this thesis are the development of a beam position monitor and a Low-Level control system that are highly flexible and reconfigurable because they are based on digital hardware. The solutions developed have been designed with the goal of creating tools specially suited for research purposes in the laboratory. The applications developed are highly focused on this objective, showing very valuable features such as fast prototyping stages or modularity.

Another line of the present thesis works is devoted to the study of advanced sampling and digital processing techniques, which are later on implemented in the mentioned applications. Finally, the last part of this work deals with the integration of the information produced by the diagnostic developed and control tools in EPICS, a control systems tool widely used in the field of particle accelerators.

Particle accelerators constitute fundamental tools to understand fundamental science and to help face some of the most ambitious scientific challenges. Yet, the usage of this kind of machines is not limited to large scientific projects. In fact, the vast majority of accelerators are oriented to industrial and medical applications.

Due to the huge complexity of these devices, they represent a great technologic challenge and, thus, the research and and the development of new technologies for them is very dynamic.

Figure 1.1. – Aerial view of the projected European Spallation Source (ESS).

1.1. Context of the Thesis

The present work is focused in the development of new technologies oriented towards diagnostics and control tools for of particle accelerators, work area of the *GAUDEE Experimental Control Research Group* and *RF and Microwave Research Group* of the department of Electricity and Electronics of the University of the Basque Country UPV/EHU. It must be remarked that the research in the

field of particle accelerators science and technology has been recently declared as strategic by both the University of the Basque Country and the Basque Government, and those institutions has signed an agreement for the collaboration in such field.

The diagnostics, control and RF fields are essential aspects in every accelerator. Diagnostics are key for the adjustment and normal operation of the machine. They provide useful information related to several processes and components of the machine, and they can be based on different physical phenomena depending on the variable to be measured and the accelerator type. This way, different diagnostics are obtained, such as emittance, beam loss or beam position. Many of this diagnostic tools need to perform high accuracy measurements in order to generate valuable information. Due to the scientific relevance of this kind of devices, the project "Tecnologías para diagnóstico y aceleración de haces de partículas -6-12-TK-2012" funded by the Provincial Council of Bizkaia was signed in order to develop a beam position monitor system along with a compact testbench by the *GAUDEE Experimental Control Research Group* and *RF and Microwave Research Group* in UPV/EHU.

On the other hand, RF control systems are vital for the particle acceleration process. In the design and development of these systems, the collaboration of the knowledge areas of automatic control and RF is necessary, as the variable that are intended to be controlled are high speed signals, usually in the order of hundreds of MHz. For a proper acceleration, particles must be synchronized with the travelling wave, which requires a very precise and fast control of the amplitude and phase of the signal. In this sense, the project called "ACELTEC, Tecnologías de fabricación de aceleradores lineales superconductores de alta intensidad para irradiación de sistemas" funded by the CDTI by meams of the FEDER Innterconecta plan, was conceived to develop a LLRF control system for the control of a RF cavity. The project also implied the building of a complete testbench of the LLRF system, including the design and development of an aluminium reentrant RF cavity.

An introduction to the diagnostics and control in the field of particle accelerators is presented in Chapter 2.

1.2. Objectives of the Thesis

The main motivation of the current thesis is to develop new flexible, modular and reconfigurable tools for diagnostics and control in particle accelerators. For this purpose,the decision was made to build a solution that is mostly digital in

Figure 1.2. – A Penning ion source of the the Front End Test Stand (FETS) experiment at the Rutherford Lab.

nature. This brings the opportunity to easily introduce substantial changes in the design or to add or modify functionalities by simply changing the program's code. This feature is a great advantage for the prototyping process, as it reduces the implementation time and allows to quickly adapt to new requirements.

Considering this, the PXIe platform of National Instruments has been selected as the main architecture for the development of the proposed applications. PXIe provides a large variety of modules of very different types, like data acquisition, signal generation, FPGA technology, timing, to name a few. Another big advantage of working with this architecture is that all the system is integrated under a common environment operated in LabVIEW. This eases the task of integrating a wide amount of hardware devices, thus reducing the effort employed in complex tasks such as driver development, use of peer-to-peer streaming or DMA transfers among others. It is also worth pointing out that LabVIEW allows to program FPGA based cards in standard LabVIEW language, not requiring the development of low level VHD code, a fact that eases the development of programs in terms of effort and time.

So, one of the main goals of this work is to avoid as many analog components in the design as possible. This represents a great challenge when dealing with RF signals in the range of dozens or hundreds of MHz. In the developed

applications, RF signals are directly sampled, avoiding any intermediate analog stage of downconversion between the signal and the ADCs.

The usage of conventional sampling techniques lead to very high sampling rates in the current working area, what directly translates in the need for expensive equipment. With the aim of avoiding such high sampling rates and therefore be able of building a more cost effective solution, an advanced sampling technique known as subsampling has been studied and implemented in the applications developed. This technique takes advantage of the aliasing phenomenon to reconstruct signals from the information located at low frequencies, bringing the opportunity of employing lower sampling speed ADCs. The application of this technique plays a central role in the solutions developed.

Another research line presented in this thesis is centered on the integration of the data provided by the mentioned diagnostic and control tools in EPICS, which is the main control technology used in many particle accelerators.

The main objectives can be summarized as follows:

- The research for developing new technologies in the field of diagnostic and control tools for particle accelerators.
- The design and development of solutions for the aforementioned fields, resulting in highly modular, flexible and reconfigurable tools.
- The design and development of tools based on digital solutions, minimizing the usage of analog components.
- The development of a BPM and a LLRF control system following the previous specifications and their testing using complete testbenchs in thel laboratory. In addition, the realization of a performance test of a nonstandard EPICS fast controller for the integration of the developed tools in EPICS networks.

1.3. Structure of the Thesis

This thesis is divided in six chapters and one appendix:

- This thesis work begins with a brief introduction to the field of particle accelerators in Chapter 2, followed by a more detailed description of diagnostic tools, centered around beam diagnostics. Here the fundamentals of capacitive-effect based beam position monitors are explained. This

Chapter also introduces RF control, Low-Level RF control systems in particular, describing their function and structure.

- Chapter 3 deals with the description of the selected technology for digital signal processing. All the hardware employed along with the main software platform is presented, justifying the selection. The second part of this Chapter presents a detailed study of the subsampling technique with the aim of facilitating its understanding for the later implementation.

- Next, one of the most important contribution of the present thesis is described in Chapter 4. This corresponds to the design and development of a digital beam position monitor application. In addition, a compact testbench is presented, which is used to test the previously mentioned solution in the laboratory. The results obtained are also shown.

- In Chapter 5, the other principal contribution of this thesis is introduced. This is a digital Low-Level RF control system, with its respective fast feedback loops for phase and amplitude regulation and the slower one to tune the resonance frequency of the cavity. Two different approaches are proposed and developed for each type of loop, each one with it own advantages an drawbacks, pursuing different goals. To test the LLRF developed, a complete testbench is also presented, consisting mainly of a resonant RF cavity. With this, the LLRF control system is tested and results obtained. The resulting laboratory testebench is useful for the development and test of realistics LLRF systems and for the research on avanced techniques to be applied in the control of such systems.

- The 6th Chapter deals with the integration of the aforementioned applications, which are based on the PXIe architecture and LabVIEW in EPICS networks. Here, a performance test is carried out in order to test the validity of a nonstandard EPICS fast controller for the developed diagnostic and control tools based in this technology, in terms of repeatability and stability.

- Finally, the main contributions and concluding remarks obtained from the present thesis are summarized in Chapter 7.

There is also an appendix giving additional technical information.

CHAPTER 2

Diagnostics and RF Control in Particle Accelerators

Particle accelerators are a widely used machines in both scientific research and industry. These are complex systems that can require a huge number of devices and tools for both their development and operation. Therefore, the research and innovation in technologies applied to particle accelerators is very active and dynamic, resulting in new tools, applications and improvements from year to year. Among these technologies, those focused on the RF control and diagnostics are specially relevant, as they play a key role in the particle beam acceleration and the correct operation of the whole machine.

This chapter introduces the particle accelerator basics, as well as describing the role, principles and main types of diagnostic and RF control tools in this field.

2.1. Introduction

A particle accelerator is a machine that increases the kinetic energy of charged particles, making it possible to reach extremely high energies (of the order of TeV [55]). These can be elementary particles like protons or electrons, or whole atoms (heavy ions). Accelerators are key tools in the development of science and technology, and any country that is reference in this fields operates several of this large scientific facilities. They are considered the hallmark of highly technological societies. Accelerators were invented in the 1930s [16] as means of providing energetic particles to investigate and understand the structure of the atomic nucleus. This first early accelerator was the Cockcroft-Walton accelerator [16], which consisted in a voltage multiplier that used an intricate stack of capacitors connected by rectifying diodes as switches. By opening and closing switches in proper sequence, they could build up a potential enough to accelerate protons to send them against a lithium target, this way they found that protons disintegrated a lithium nucleus into two alpha particles. It has been a long way since then, and many aspects of the particle physics have been discovered and studied thanks to them.

Although particle accelerators are at times associated with big physics, it is worth pointing out that the vast majority of them are used in medical and industrial fields. In the year 2000, a worldwide inventory set the particle accelerator number at 15000 [7], and up to 26000 in 2014 [11], and in both cases, the percentage of them oriented to pure nuclear and particle physics research only represented 1%.Figure 2.1 shows how particle accelerators are distributed depending on its application.

Regarding the physical principle on which are based, particle accelerators can be split into two fundamental types, electrostatic accelerators and oscillating field accelerators [41]. The first accelerators, such as the Cockcroft-Walton accelerator and the Van de Graaff generator [24], are examples of electrostatic accelerators. These, based on the electrostatic field, require very large electric fields in order to obtain the energy required to accelerate particles, making them very difficult and dangerous to operate. This big disadvantage led to the development of the oscillating field accelerators. Almost all the particle accelerators belong to this type nowadays. The main categories of oscillating field machines are detailed below:

- The Linear Accelerator (Linac): as the name suggest, in this kind of machines, particles are accelerated along a linear beamline. They are capable of accelerating larger ions than circular accelerators and it is

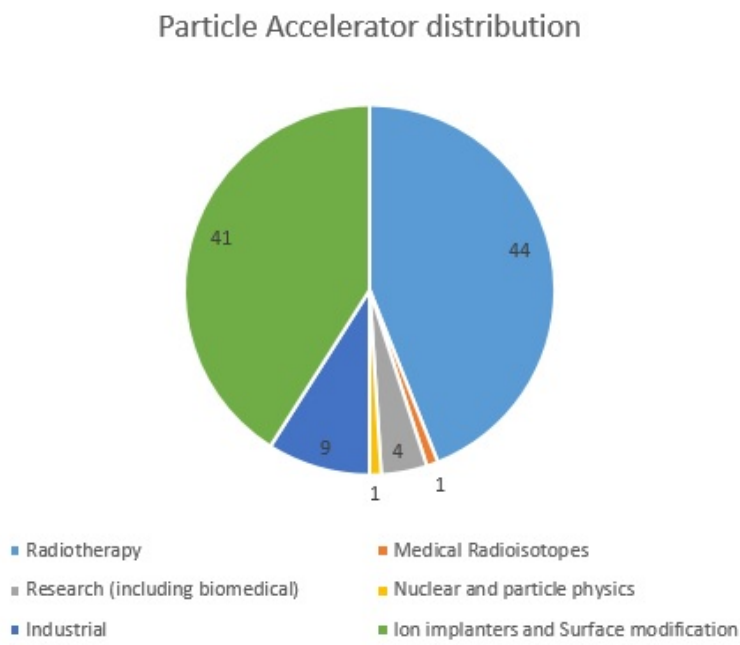

Figure 2.1. – Particle accelerator distribution worldwide based on its application.

easier to produce high energy electron beams, as they do not use a circular path [43]. Some examples of Linacs are found in the Stanford Linear Accelerator Center (SLAC) [74] or the projected European Spallation Source (ESS) [66].

- The Cyclotron: here, charged particles accelerate outwards from the center along a spiral path. They were conceived as a improvement over the linear accelerators, being more cost- and space-effective.

- The Betatron: this consists of a main ring, a doughnut shaped vacuum chamber, known as the doughnut chamber, in which electrons (produced by an electron gun within the chamber) are accelerated. The main limitation of the betatrons is that the maximum energy that betatron can impart is limited by the strength of the magnetic field due to the saturation of iron and by practical size of the magnet core [27].

- The Microtron: similar to the cyclotron, but based on classical mechanics. This implies some limitations in the energy that can be achieved, but

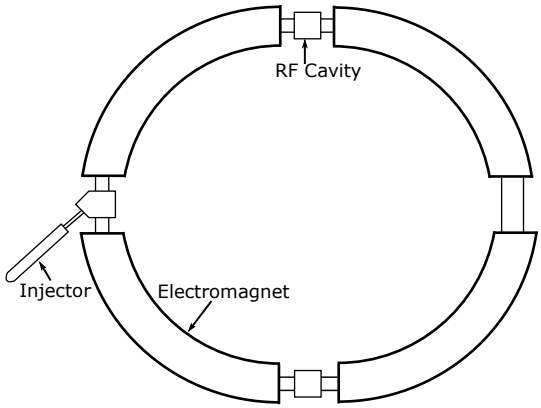

Figure 2.2. – Simplified scheme of a proton synchrotron accelerator.

it must be remarked that microtrons are still in operation today, e.g. Mainzer Mikrotron (MAMI) [71].

- The Synchrocyclotron: conceived as a modification of the cyclotron with the goal of overcoming the relativistic limitations of its predecessor. The main difference with the classic cyclotron is that instead of maintaining the AC voltage employed constant, it synchronizes with the orbit frequency of the accelerated particles [14].

- The Synchrotron: this machines synchronize the magnetic field strength with the energy of the accelerated particles in order to maintain the accelerated particles at a constant orbital radius. This way, as the particles are accelerated and gain energy, the magnetic field increases, thus keeping the particles orbit constant [50]. A simplified structure of a synchrotron can be found in Figure 2.2. The development of the Synchrotron led to the construction of large scale accelerators, as in a Synchrotron the components can be divided in different sections. Examples of big scale synchrotrons are the European Synchrotron Radiation Facility (ESRF) [65] or the Advanced Photon Source (APS) [59].

- The Storage Ring Collider: this kind of accelerators can be considered a special type of synchrotron. Colliders store and then accelerate two counterrotating beams of charged subatomic particles before bringing them into head-on collision with each other. Because the net momentum of the oppositely directed beams is zero, all the energy of the colliding

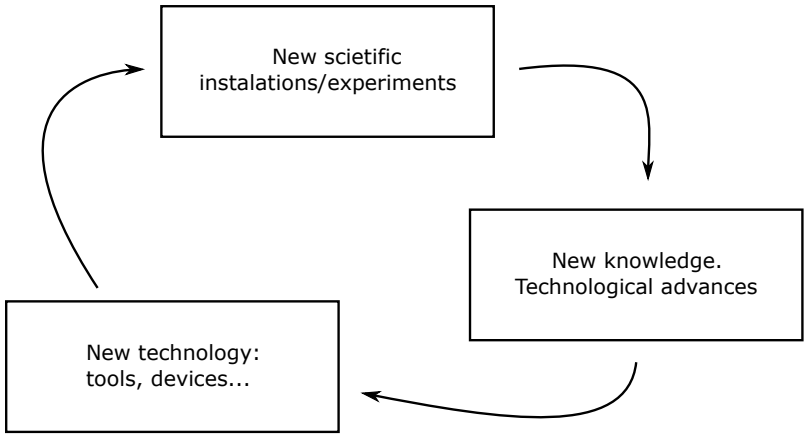

Figure 2.3. – The feedback loop between scientific research and technological development in the field of particle accelerators.

beams is available to produce very-high-energy particle interactions [21]. Two remarkable examples of colliders are the Deutsches Elektronen-Synchrotron (DESY) [61] and the Large Hadron Collider (LHC) [69] at CERN.

No matter what the type or final application is, particle accelerators share many common principles, being their main job to speed up and increase the energy of a particle beam. This is achieved by generating electric fields that accelerate the particles, and focusing them by means of magnetic fields. This implies extremely complex machines, which represent a huge scientific and technologic challenge. The research and development of new tools, devices and techniques in this field is very dynamic. The relation between technology and scientific research is fully bidirectional (as seen in Figure 2.3), meaning that they rely on each other to grow and advance, forming a virtuous cycle.

In particle accelerators, technologies of very different nature coexist, which are employed for a wide variety of applications: from the vacuum system or the cryogenics to the human safety. This chapter focuses in two of them: beam diagnostics and RF control, as those topics are the main ones in this work. The tools presented in Chapters 4 and 5 correspond to these areas.

2.2. Diagnostics and RF control

Among the different technologies involved in particle accelerators, two of them can be highlighted, due to their vital importance in the proper operation of the whole system. These are the beam diagnostics and the RF control system.

Accelerator performance depends critically on the ability to carefully measure and control the properties of the accelerated particle beams, making a good understanding of diagnostics essential for achieving the required performance. Beam diagnostics are conformed by the following elements:

- The measuring device.
- Related conditioning electronics and hardware.
- High-level processing.

A deeper description of beam diagnostics, especially beam position monitoring is given in the next section.

RF control, is also an essential part of accelerators. It plays a key role in the particle acceleration process, governing the energy transfer required to speed up the particles in a proper way. To accelerate a particle bunch, RF cavities are used. These are metallic chambers that contain an electromagnetic field supplied by an RF power generator. These radio frequency waves interact with the passing particle bunches, transferring some of the energy from the radio waves to the particles every time a beam passes the electric field in the RF cavity, thus pushing them forwards [15]. Additionally, the particle bunches are formed and shaped in the cavities, accordingly to the RF signal.

The RF cavity is designed and built to a specific size and shape so that electromagnetic waves become resonant at a given frequency (depending on the particle type to be accelerated) and build up inside the cavity. Charged particles passing through the cavity feel the overall force and direction of the resulting electromagnetic field, which transfers energy to nudge them forwards along the accelerator, but only if the needed synchronization is achieved. Figure 2.6 represents a transverse cut of a cavity and the orthogonal components of the electromagnetic field. Many cavity resonators are derived from the simple cylindrical cavity. This type of cavities are particularly interesting because there exist a mode of the beam of electromagnetic radiation [18] in which the resonance frequency is independent of the cavity's length, which is a great advantage when designing the physical cavity. This mode is called a *transverse-magnetic mode*, referred as TM_{010} in the conventional literature, because the z

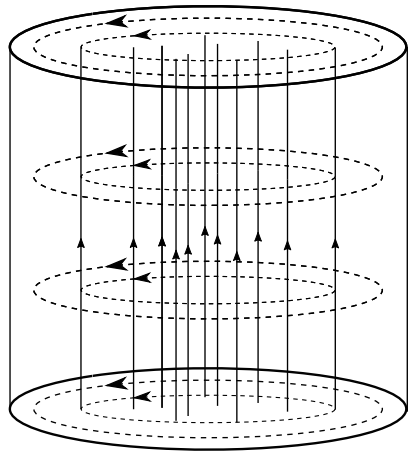

Figure 2.4. – The electric and magnetic fields for TM_{010} mode.

component of the wave's magnetic field is zero [52]. So, the wave's magnetic field is parallel to the cavity's bottom and perpendicular to the electric field, as shown in Figure 2.4.

The cylindrical cavity resonator can be analogous to a parallel RLC resonant circuit, see Figure 2.5. From this, the input impedance of the cavity can be expressed as:

$$Z_{in} = \frac{R}{1 + j\frac{R}{L}\left(\frac{\omega}{\omega_0} - \frac{1}{\omega}\right)} \tag{2.1}$$

where ω_0 is the resonance frequency. For frequencies near the resonance, $\omega \approx \omega_0$, impedance can be written:

$$Z_{in} = \frac{R}{1 + jQ_0 2\Delta} \tag{2.2}$$

being $\Delta = \frac{\omega - \omega_0}{\omega_0}$ and $Q_0 = \frac{R}{\omega_0 L}$. Q_0 is the unloaded quality factor of the cavity, that is, the Q for the cavity resonator without connection of the external circuit. The quality factor (Q-value) is an essential parameter for estimating the quality of cavity resonators [44]. A high Q-value indicates high accuracy and narrow bandwidth of the cavity resonator.

The voltage demanded by some high energy applications can rise to a point where copper cavities become uneconomical, due to ohmic power losses [46]. An analog situation happens in applications that demand a long RF pulse length,

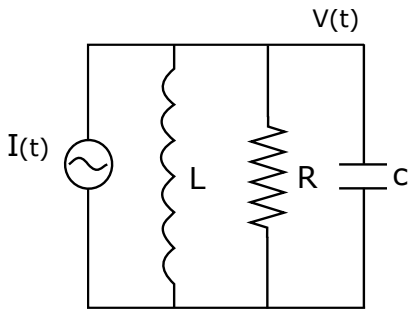

Figure 2.5. – Circuit model of a cavity resonator.

or a high RF duty factor [40]. In this cases, superconducting RF cavities (SRF) are used, as the surface resistance of this kind of cavities is many orders of magnitude lower than that of copper. These cavities require a cryogenic system to achieve the required conditions for superconductivity. Another important advantage of SRFs is that they cause a less disruptive effect on the beam [39].

The energy gained by a particle in a cavity is given by [42]:

$$\Delta \mathrm{W} = \int q \cdot E_z(s) \cdot cos\left(\Phi(\mathrm{s})\right) \cdot ds \tag{2.3}$$

with

$$\Phi(s) = \Phi_o + \omega t = \Phi_o + \frac{\omega}{t} \int_{s_0}^{s} \frac{ds}{\beta_z(s)} \tag{2.4}$$

being q the elementary charge constant, E_z the module of the electric field longitudinal with the velocity of the particle, Φ the phase and β the speed of the beam relative to the speed of light. Note that, starting from a continuous beam, the RF signal groups the particles, forming particle bunches, which must be in phase with next RF signals, in order to get an acceleration.

The energy gain can be expressed as:

$$\Delta \mathrm{W} = q_0 \cdot V_0 \cdot T \cdot cos\Phi_p \tag{2.5}$$

being $V_0 = \int |E_z(s)| \cdot ds$ the cavity voltage, Φ_p the average phase and T the transit-time factor.

Equation 2.5 evidences the importance of the cavity's voltage and the phase parameters in the energy transfer process, vital for the correct acceleration of the

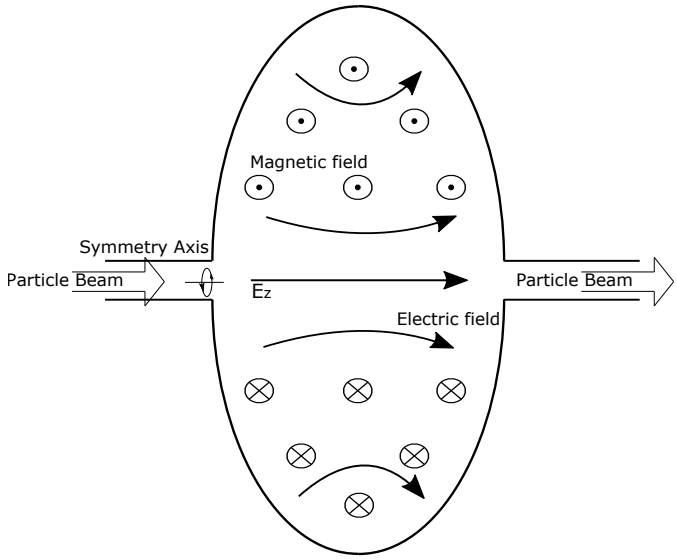

Figure 2.6. – Cross section of a cavity, where the orthogonal magnetic and electric components of the RF fields can be seen.

particle beam. That is one of the main reasons why RF control is so essential for particle accelerators. The control system that regulates the voltage amplitude and the phase of the RF fields inside the cavities is known as Low-Level Radio Frequency (LLRF). These system are described in detail in a section bellow.

So, being the diagnostics and RF control key features of an accelerator machine, the development of new technologies for these purposes has a huge importance. New devices, techniques and approaches enhance the capabilities of diagnostics and control tools, boosting the overall performance and operation of such complex machines. The following two section introduce both tools, describing their principles and main types.

2.3. Particle accelerator beam diagnostics

Beam diagnostics are essential in any accelerator. These systems are in charge of sensing what properties a beam has and how it behaves in the accelerating machine. Those diagnostics give essential information needed in the commissioning phase, when adjusting the initial beam characteristics, and in the production phase, for a correct operation of the beam.

It is a very wide field, where a great variety of physical effects are made use of and where research and new ideas are very dynamic. Consequently, the characteristics of the accelerated particle and the implemented acceleration technology are relevant. Therefore, a vast choice of different types of diagnostics devices exist, each usually in several forms.

In the next paragraphs, the most common diagnostics of the accelerators are briefly described.

Position pickup monitors (PU)

Very extended, since is a non-destructive diagnostic tool, this kind of devices are in charge of measuring the transverse beam position. They are based on different physical effects, the most common being those based on electrostatic, magnetic or electromagnetic effects. Electrostatic PUs are mostly used in circular accelerators and the most common implementations are the shoe-box and the button type electrodes. Its mechanism is based on the measurement of the induced electric charges on metallic electrodes. This type will be deeply studied in the next sections as the Beam Position Monitor presented corresponds to this kind of diagnostics device.

In proton machines, where secondary emission from the electrodes can be a problem if strong beam losses occur, magnetic PUs are usually installed [33].

In addition, electromagnetic PUs are commonly used in single-ring colliders, where two beams are circulating at the same time [12]. The previous types of PU only allow to observe one beam in the presence of the other. On the one hand, electromagnetic PUs measure the electric charge of the passing beam induces a charge on them. On the other, the magnetic field created by the beam current is also measured. These two effects result in a sum in the direction of the beam, while in the opposite direction they cancel.

Beam Loss Monitors (BLM)

BLMs are distributed along the machine in order to detect the magnitude and the location of losses in the beam. Although technically these devices do not measure a property of the beam, they provide an essential information for the particle accelerator operation and safety, as minimal losses in the particle beam can cause excessive radiation and produce radioactivity. In addition, a high radiation is an indirect measurement of a malfunction of the machine.

Among the most widely used BLMs, ionization chambers, scintillator plus photomultiplier (PM) and aluminum cathode electron multiplier (ACEM) must

be highlighted [56].

Secondary Emission Monitors (SEM)

This devices are presented as arrays or grids of thin wires that measure the transverse density distribution of the beam. The beam profile is obtained from sequential displays of the signals obtained from the wires. It can be considered as a nearly non-destructive diagnostic tool.

The underlying technology behind SEMs is the phenomenon known as secondary emission. It describes how when beam particles impact on a solid material, electrons are ejected from the surface, creating a current flow [48]. Those diagnostics require a well designed electronics system for signal conditioning, since the currents obtained by secondary emission are very low. They are vital part of the BLMs, and are present in every particle accelerator [19].

Faraday Cup

A Faraday cup is the most direct and primitive beam diagnostic method. It was the first implementation of this kind of tools and consists of capturing the beam and driving the current flow through a meter, consequently destroying the beam. Nowadays, it is used at low energies, usually no higher than some keV [20].

When the mentioned collector receives the beam, the metallic plate suffers from perturbations caused by secondary electron emission. Faraday cups are used in order to avoid liberated electrons escape and therefore, prevent losses.

Beam (Current) transformers (BT)

The most basic measurement on a beam is its intensity. The beam transformers allow to determine the electric current that constitutes a beam. The simplest BT consists of a coil mounted over a ceramic piece. They are usually used for AC signals at frequencies under 100MHz [53]. More evolved designs, known as DC Current Transformers (DCCT), allows BT measuring DC currents[37].

Wall-Current Monitors (WCM)

When the longitudinal shape of the bunches want to be observed at frequencies beyond the 100 MHz usually achieved with BTs, WCMs are used. At such high frequencies, for example when working with electrons or positrons, bunches

become very short and the usage of WMCs becomes necessary as in the case of the Compact Lineal Collider (CLIC) of CERN, [60, 38].

They are based on the measurement of the "wall-current", which is the induced current in the vacuum chamber by the beam, of equal magnitude and opposite direction. The implementation consists of a ceramic insertions in the chamber. The created insulating gap forces the wall-current to pass through so can be driven to a coaxial cable and this way monitorized.

Wire-Scanners

SEMs may excessively disturb the beam under study. In this case, a single wire is used. This is quickly moved across the beam and the beam profile is obtained from the composition of successive mesaurements. In addition to secondary-emission wire-scanners, they can also be found based in radiation detectors reading γ and secondary particles. Nowadays, wire-scanners can be implemented using focused laser pulses to measure micron-scale beam sizes, as the found in the Koo Energy Ken (KEK) accelerator [6].

Measurement targets

Sometimes, the most reliable information of a beam requires a destructive diagnostic method. Particle beam can be intercepted using a target to study the product of the scattered particles. As said before, it is a destructive and slow method, but provides a highly accurate information of the particle distribution of the beam. It is used in many type of accelerators and different applications, as neutron scattering [51].

Table 2.1 summarizes the aforementioned diagnostic tools and its main features.

2.3.1. Beam Position Monitoring

In this section main principles of non-intercepting electromagnetic beam position monitoring is discussed.

The most common method to monitor the position of a beam composed by charged particles is to couple the electromagnetic field of the beam. As a beam is strictly a current, it is accompanied by a magnetic and an electric fields. If for any reason the beam deviates from the center of a hollow conducting enclosure, the measured magnetic and electric fields vary accordingly. The study of this changes allow to accurately determine the beam position.

Instrument	Physical Effect	Measured quantity	Effect on beam
Pickup	- Electric/Magnetic field	-Position	-Non destructive
SEM	-Secondary electron emission	-Transverse size/shape, emittance	-Disturbing -Destructive at low energies
Faraday Cup	-Charge collection	-Intensity	-Destructive
BT	-Magnetic field	-Intensity -Size/Shape -Emittance	-Non destructive
WCM	-Image current	-Intensity - Longitudinal shape	-Non destructive
Wire-Scanner	-Secondary particle creation	-Size/shape	-Slightly disturbing
BLM	-Luminosity -Gas-ionization ...	-Position -Size/Shape -Emittance	-Non destructive
Target	-Particle collision	-Particle distribution	-Destructive

Table 2.1. – Main diagnostic tools found in particle accelerators and its main characteristics

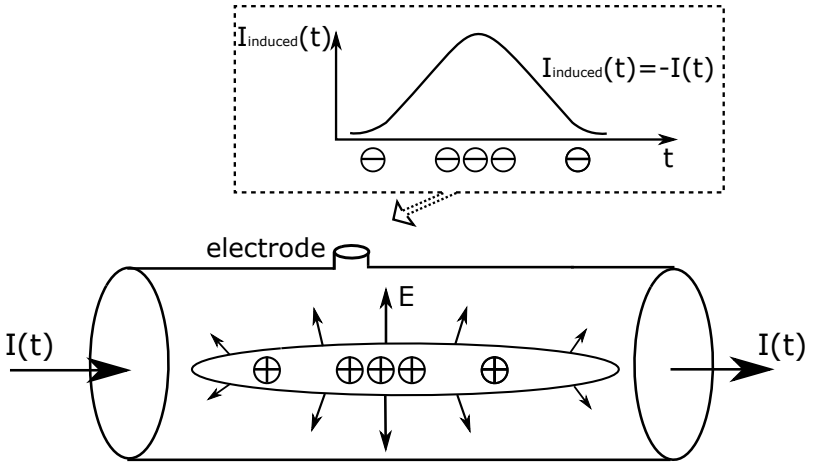

Figure 2.7. – The image current induced by the beam particle electric field.

Most pickups electrodes cannot directly sense DC electric or magnetic fields, so they are based on induced charges. This induced signals are produced by a time-varying component of the beam. Depending on source operation mode, the carrier for the beam position information can be the frequency of the periodic particle bunches (for continuous train of bunches) or the derivative of the instantaneous beam current (for a single bunch).

The most widely used beam position pickup structure is composed by a pair of electrodes, or two pairs, if position is both transverse planes is needed, where signals are induced. The ratio of the amplitudes of the induced signals at the carrier beam bunching frequency is uniquely related to the beam position.

Pick-ups

The position of a particle beam as well as the longitudinal bunch shape are often determined using pick-up plates, [49]. As mentioned before, it is carried out by measuring the charges induced by the electric field of the particle beam on an insulated metal plate, as shown in Figure 2.7. In pulsed sources, electric field of the beam is time dependent, so the signal read on the plates is a RF AC signal.

The goal with this tools is to determine the center of mass of the particle beam, which means its position. In order to do so, pick-up pairs are used. The voltage difference read in each pair provides the center of mass in the respective direction.

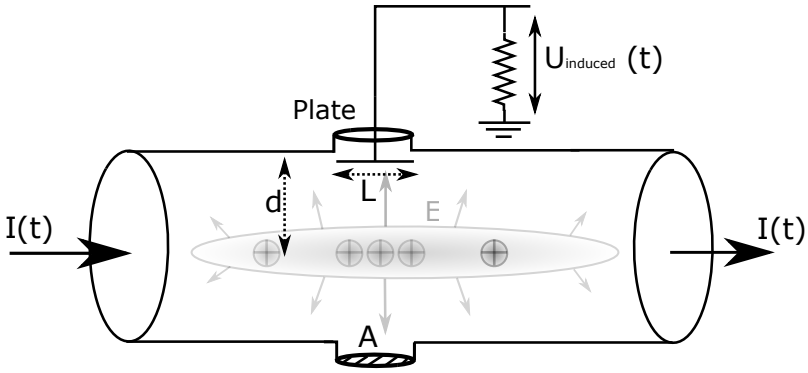

Figure 2.8. – Schematic description of the insulated metallic plates (pick-ups) inside the beam pipe.

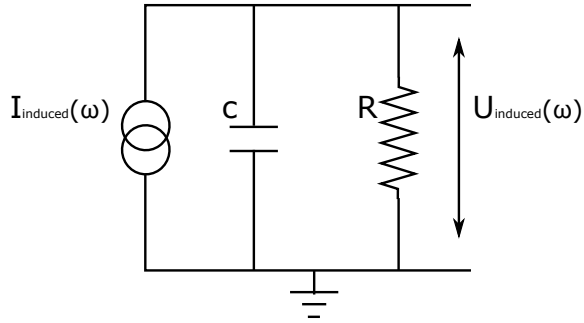

Figure 2.9. – The equivalent circuit of the capacitive pick-ups.

This section is centered around the description of capacitive (also called electrostatic) pick-ups, which is the type chosen for the development of the compact BPM system presented in the next chapter, These kind of pick-ups consist of a ring inserted in the hollow beam pipe. In order to acquire the data produced by the induced image charge of the beam, the sensors are Rf coupled.

A plate with an area of A and a longitudinal length of L in a pipe with radius d is assumed, as shown in Figure 2.8. Its equivalent electrical circuit is represented in Figure 2.9.

The image charge on a plate is given by:

$$Q_{image}(\omega) = \frac{\text{Pick-up Area}}{\text{Pipe Circumference}} \cdot \rho(\omega) \tag{2.6}$$

being $\rho(\omega)$ the linear charge density. So, the induced image current out of the pick-up is given by:

$$I_{image}(\omega) = \frac{dQ_{image}}{dt} = \frac{\text{Pick-up Area}}{\text{Pipe Circumference}} \cdot \frac{d\rho}{dt} \tag{2.7}$$

If the linear charge density is expressed in terms of the beam current and assuming that the beam acts as a perfect current source:

$$\rho(\omega) = \frac{I(\omega)}{\beta c} \tag{2.8}$$

being βc the beam velocity. So,

$$\frac{d\rho}{dt} = \frac{1}{\beta c} \cdot \frac{dI}{dt} = \frac{i\omega}{\beta c} \cdot I(\omega) \tag{2.9}$$

and the induced image current can be expressed as:

$$I_{image}(\omega) = \frac{A}{2\pi d} \cdot \frac{i\omega}{\beta c} \cdot I(\omega) \tag{2.10}$$

Regarding the voltage seen in the pick-ups, it corresponds to the product of the current out of the electrode and the impedance seen by this current. The major contributions to this impedance come from the impedance of the cable derived by the reactance of some parasitic capacitance C_b between the pick-up and the walls of the beam duct [49].

$$Z = Z_{coaxial} \Big|\Big| \frac{1}{i\omega C_b} \tag{2.11}$$

This way,

$$V_{pick-up} = Z \cdot I_{image}(\omega) = \frac{A}{2\pi d} \cdot \frac{\omega}{\beta c} \cdot Z(\omega) \cdot I(\omega) \tag{2.12}$$

Position measurement with capacitive/electrostatic pick-ups

In order to measure the deviation of the particle beam under study relative to the center of the pipe, four isolated metal plates are used. They are crosswise placed around the hollow beam pipe. From the voltage difference obtained from the opposite sensors (see Figure 2.10) of each perpendicular pair, the center of mass in both vertical and horizontal directions can be obtained,

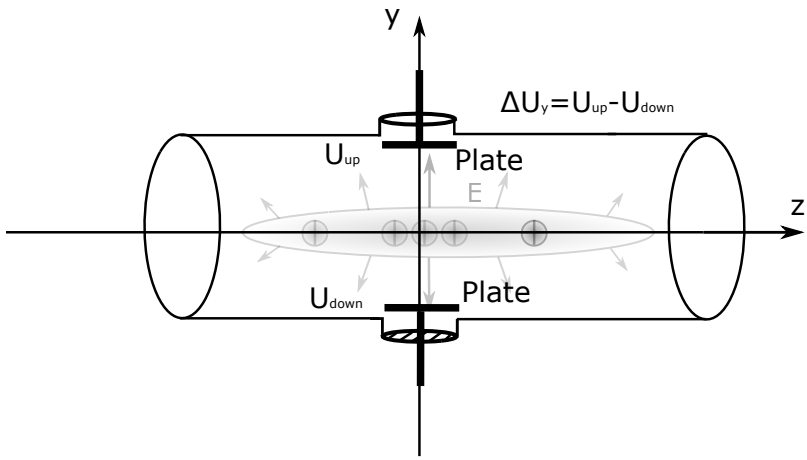

Figure 2.10. – Schematic description of the measurement of the vertical position of a capacitive type BPM using the proximity effect

$$\Delta U_x = U_{right} - U_{left} \tag{2.13}$$

$$\Delta U_y = U_{up} - U_{down} \tag{2.14}$$

Due to the "proximity effect", the closer distance to one of the plates leads to a higher induced voltage.

The vertical and horizontal displacement is independent of the beam intensity and can be written as [22]:

$$x = \frac{1}{S_x}\frac{U_{right} - U_{left}}{U_{right} - U_{left}} + \delta_x = \frac{1}{S_x}\frac{\Delta U_x}{\Sigma U_x} + \delta_x \tag{2.15}$$

$$y = \frac{1}{S_y}\frac{U_{up} - U_{down}}{U_{up} - U_{down}} + \delta_y = \frac{1}{S_y}\frac{\Delta U_y}{\Sigma U_y} + \delta_y \tag{2.16}$$

where S_x and S_y constants are defined as position sensitivity and represent the difference between the measured normalized voltage difference and the real beam displacement. It is given in [%/mm]. δ_x and δ_y are the offset correction for the deviation of the electrical center, given in [mm].

Key characteristics in the BPM design

In the development of this kind of devices, the study of some key characteristics is essential to obtain the best possible measuring system. The understanding of this features allows to take the necessary compromises to go from an ideal beam position monitor to a realizable one.

One of the most important characteristics is the measurement accuracy. This is defined as the ability to determine the position of the beam relative to the device being used to measure. This feature is affected by several perturbation sources such as mechanical-related errors, attenuation in cables, temperature changes, calibration errors of the electronic devices interferences and overall noise of the built system.

Another characteristic that has to be taken into account is the resolution. In this case, this is the capacity to measure small variances of the beam position. The maximum resolution of a beam positioning system determines the minimum displacement of the beam that can be measured. This parameter is typically higher than accuracy. For example, if the beam jitter (motion) needs to be measured (resolution), this can be quantified in a scale hundreds of times higher than the beam position (accuracy).

Dynamic range of the diagnostic tool must be also carefully studied. This refers to the range of the beam intensity over which the measurement system can respond. In digital systems, larger dynamic ranges of acquisition devices lead to lower resolution.

In pulsed sources, the beam is in the form of short bunches with a multiple of the period of the RF system being used to accelerate it. In this cases, beam bunching is an essential feature. It refers to the temporal attributes of the beam current modulation.

There are a few more characteristics of the diagnostics systems that is worth mentioning, like the beam DC current, the bandwidth of the system or the signal-to-noise ratio (SNR) of the acquired data. In particular, the SNR must be sufficiently large in order to obtain the required measurement accuracy.

Pick-up BPM designs worldwide

When it comes to the implementation of the pick-up structure, different designs are found in accelerators worldwide. The mechanical design and properties of them can vary depending on several factors. For instance, in the European X-ray Free Electron Laser (XFEL) facilities [76], two different kinds of pick-up buttons are necessary: one type will be installed in the acceleration modules

of the cold linac and the other one in the warm environment, which differ in electrical, mechanical and thermal properties [34]. Another example of the importance of the temperature in the pick-ups is seen in the design of the BPM system for the Brazilian Synchrotron Light Laboratory (LNLS), [70, 5].

The diameter (gap) of the beam chambers is another factor that must be taken into account for the design of the BPMs. For highly relativistic filamentary beams of electrons or positrons, the Lorentz contraction compresses the electromagnetic field of the charged beam into the 2-D transverse plane. This results in the currents induced in the beam chamber wall having the same longitudinal intensity modulation as the charged beam. In this cases, the design of the pick-up's configuration must be optimized for the gap size, as seen in the APS or ELETTRA [63] BPM systems,[31, 35].

The power of the signal measured by different capacitive pick-ups can vary significantly depending on the machine, which is directly related to the cross section of the pick-ups. To illustrate this, the power received by the capacitive sensors of the Electron accelerator ELSA [64] is 10 dB lower compared to the DESY II electrodes [30].

Signal Processing Methods

There are three general methods used in deriving normalized position signal from the raw pickup electrode signals: the amplitude to phase conversion, the log-ratio processing and the difference over sum method.

Amplitude to phase conversion processing carries out an amplitude-modulation-to-phase-modulation (AM/PM), where the measured in-phase RF signals read from the pick-ups are split and re-combined in quadrature. This kind of processing provides a large dynamic range and high real-time bandwidth, but are expensive and difficult to implement [47]. Usually, they involve several analog components such as phase shifters, splitters, limiters and mixers. This method can be found, for example, implemented in the electronics of the e TESLA Test Facility (TTF) [75] linac, [54].

In the log-ratio method, each signal is put into a circuit that produces an output signal proportional to the logarithm of the input signal. A common-mode-rejecting difference amplifier then produces a signal proportional to the difference of the two logarithmic outputs, which is equivalent to the log-ratio of the two input signals [4]. Usually, the log function is obtained by using a forward-biased diode junction in the feedback circuit. This approach has some drawbacks, e.g. the requirement of a strong temperature compensation because the output signal amplitude is proportional to the absolute temperature of the

diode junction. This method is used in several accelerators all over the globe, like in the projected Proton Engineering Frontier Project (PEFP) [1].

The difference-over-sum method (sometimes known as Δ/Σ), is the most straightforward approach to obtain the position of a particle beam (see Equations (2.15) and (2.16)). In its simplest approach, it consists of the detection of the RF signals and the generation of proportional signals to the RF envelope amplitudes [10]. This is the most popular method due to its simplicity to implement, and it has been the approach selected to develop the present work. Another advantage that is worth pointing out is that it does not require a high amount of analog stages. Examples of operating accelerators using the Δ/Σ signal processing methods are DIAMOND Light Source [62] [2] and XFEL [3].

2.4. Low-Level RF control systems

As mentioned above, the energy transfer to a particle beam relies on the RF control system. That is why Low-Level Radio Frequency (LLRF) control systems are essential parts of modern particle accelerators. Their main task is to transfer energy to the beam in a controlled fashion by properly governing the RF accelerating fields and synchronizing them to the particle bunches. They guarantee a proper injection and acceleration of the beam in particle accelerators by providing the required amplitude and phase stability of RF fields in accelerating structures. These systems typically collect measurements of amplitude, phase, and frequency, perform several signal processing and computational processes on that acquired data, and then use the outcome to monitor, control, and regulate RF fields in particle accelerators [57]. A brief scheme of a typical LLRF system (analog setup in this case) is described in Figure2.11

Different LLRF system requirements are demanded depending on the particle accelerator type, taking into account several conditions; mainly: the particle type to be accelerated (electrons, protons., heavy-ions) [45, 29, 32], a higher accuracy in phase and amplitude being required for lighter particles, type of machine (linear or circular), the use of super-conducting or normal RF systems, and operation mode (pulsed or CW). By way of illustration, the Linac Coherent Light Source (LCLS-II) at SLAC requires a maximum tolerance that goes from 0.05 to 0.5 degree in phase and 0.06% to 0.25% in amplitude, depending on the section [23]. The projected ESS, being a proton linac, requires maximum errors in phase and amplitude of 0.5% and 0.5 degree respectively [36]. Heavy-ion accelerators have a not so restrictive constraints; e.g. the FAIR accelerator

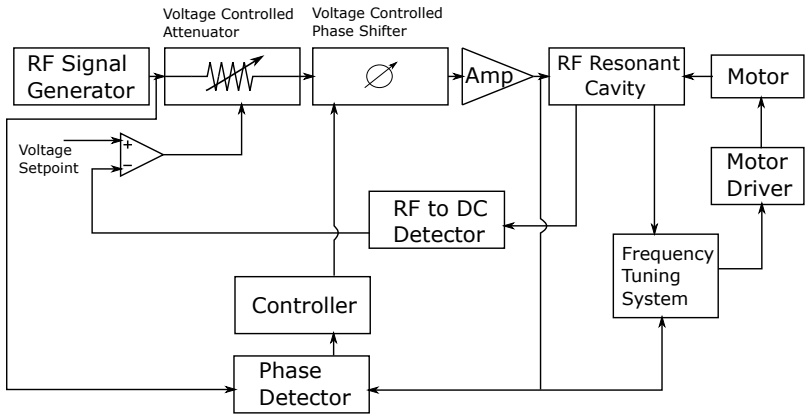

Figure 2.11. – A basic block diagram description of an analog LLRF system.

at the GSI Helmholtz Centre for Heavy Ion Research (GSI) [67] requires an accuracy of 3 degrees in phase and 6% for the amplitude [77].

LLRF systems are typically implemented using analog (as the one found in the ALBA´s [58] booster accelerator [26]) or digital electronics like in the The Low Energy Ion Ring (LEIR) [68], accumulation and acceleration ring in the LHC [8], or a combination of both as found in the RF feedback systems of PEP-II [72] at SLAC [17], Superconducting-DArmstadt-LINear-ACcelerator (S-DALINAC) [73] or [9]. Regardless the implementation type, a typical LLRF control system usually consists of a fast loop to regulate the amplitude and the phase of the accelerating signal as seen by the particles, and one slower loop to tune the resonance frequency of the accelerating cavities. The amplitude and phase loop should have a wide bandwidth, typically in the order of tens of kHz [13], and eventually be able to compensate the ripples of the high voltage power sources (depending on the accelerator type) and other perturbations as well as to have a good time response, particularly when pulsed RF fields are required. The frequency loop, which has a much lower bandwidth (usually in the range of a few hundred Hz) [28], controls the cavity tuners to maintain its nominal resonance frequency in the presence of cavity temperature changes and mechanical perturbations, so that the reflected power is minimized.

These three control loops are briefly described:

Amplitude control loop

The amplitude control loop of an LLRF system keeps stable the amplitude of the cavity gap voltage, within an acceptable range against several perturbations. The main sources of amplitude disturbances include:

- Beam loading effects.
- Voltage gain fluctuations caused by the effects of the amplifier's non linearities.
- Attenuation caused by passive devices.

The amplitude of the accelerating field in the cavities is measured using a pick-up (coupler). It provides a sample of the RF signal inside the cavity. Then, different techniques can be applied to obtain the amplitude of the signal. A typical analog solution consists of a RF to DC detector that performs an amplitude demodulation of the RF signal, a voltage comparator and a voltage controlled attenuator. A different way is to perform the amplitude detection and control actions digitally. This requires the discretization of the RF signal and the development of a suitable program.

Phase control loop

The phase control loop of a LLRF systems is used to maintain stable the phase of the cavity gap voltage. This loop must be able to set the required phase of the RF field in the cavity and keep it stable within the maximum possible range. Among the mayor perturbations affecting the phase, the following can be found:

- Ripples generated by the high voltage power supply of the RF amplifier.
- Phase changes induced by the non linear effects of amplifiers.
- Phase noise from the RF generator.
- Phase variations caused by temperature drifts of different electronic devices.

Two main approaches are used to control the phase of the RF field in the cavity. The first one is the analog procedure, in which a phase detector, a controller and a voltage controlled phase shifter are used. The digital approach discretizes

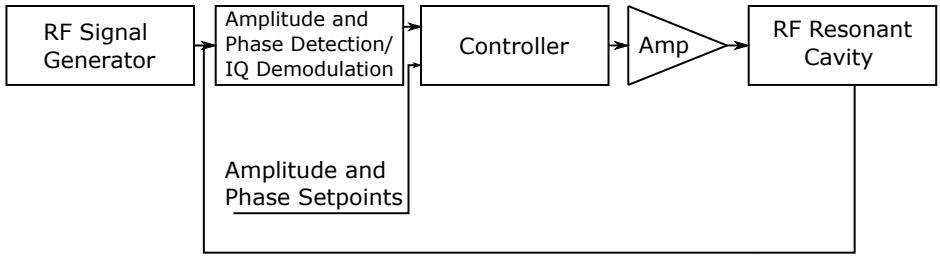

Figure 2.12. – Phase and amplitude control loop diagram.

the RF signal measured from a pick up in the cavity and performs the phase detection and control action.
Figure 2.12 shows a generic amplitude and phase feedback loop, which can represent two parallel loops, one for the amplitude and one for the phase, depending on the implementation type.

Frequency tuning loop

The frequency tuning loop is in charge of maintaining the resonance frequency of the cavity fixed at its nominal value, so the reflected power is minimized. The resonance frequency can vary due to several sources, which are listed below:

- Thermal effects.
- Lorenz force detuning.
- Microphonics.
- Other mechanical perturbations.
- Beam loading effects

Frequency tuning loops are usually implemented using stepper motors controlling pistons that change the cavity geometry and, thus, its resonance frequency. The most common architecture in frequency tuning loops consist in the frequency measurement based on a phase detection method (analog or digital), applied to the cavity voltage. The measured frequencies are compared to the reference input signal frequency to control the motor drivers. This basic concept is represented in Figure 2.13.

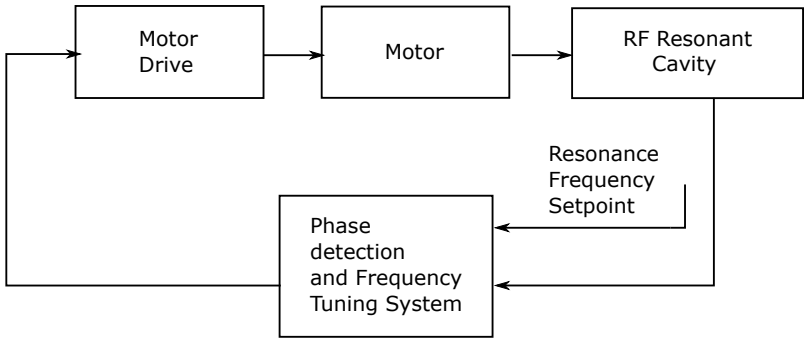

Figure 2.13. – Block diagram description of a typical frequency tuning loop of a LLRF system.

2.4.1. Digital Low-Level RFs (DLLRFs)

The rapid advances in digital technology over the last years, specially since the irruption of FPGAs and the fast development of the throughput offered by them, have opened the door to the use of digital systems in the field of LLRF [8]. The digital solutions have some drawbacks with respect to their analog counterparts, but also many interesting advantages. The main advantage of analog based solutions in the field of closed loop control is their short loop latency, leading to high loop bandwidths. They are also comparatively cost-effective. But digital implementations of LLRF systems provide much more flexibility, reprogrammability and stability of the controlled variables. They also allow to develop more sophisticated algorithms and control structures; e.g., advanced controllers, state machines, exception handling [25]. Repeatability is another important feature in which the digital approach is superior to the analog one. A more detailed comparison between digital and analog solutions is described in Table 2.2. The increasing computational speed of digital systems now allows to meet the bandwidth requirements of many LLRF systems and, therefore, replace analog setups.

The digital LLRF feedback loops typically implement the phase and amplitude controls in a single loop, taking advantage of the parallel execution possibility offered in digital signal processing architectures. A basic scheme of a LLRF control system is described in Figure 2.14.

	Digital	Analog
Latency	-Longer	-Short
Precision	-High	-Lower
Implementation	-Higher development effort -Complex algorithms	-Easier -Simple -Linear functions
Data Acquisition	-Direct Sampling -Subsampling -Digital Down Conversion (DDC) -I/Q sampling	-IF downconversion
Monitorization	-Easy - High traceability	-Extra hardware required
Flexibility/ Reconfigurability	-High	-Limited
Repeatability	-High -No drifts	-Lower -Effect of component tolerance
Radiation tolerance	-Higher	-Smaller
Operation mode	-Remote -Multi-user	-Presential -Single-operator
Diagnostics	-Built-in	-Extra devices required
Automation	-Easier	-Limited

Table 2.2. – Comparison between digital and analog solutions for LLRF applications

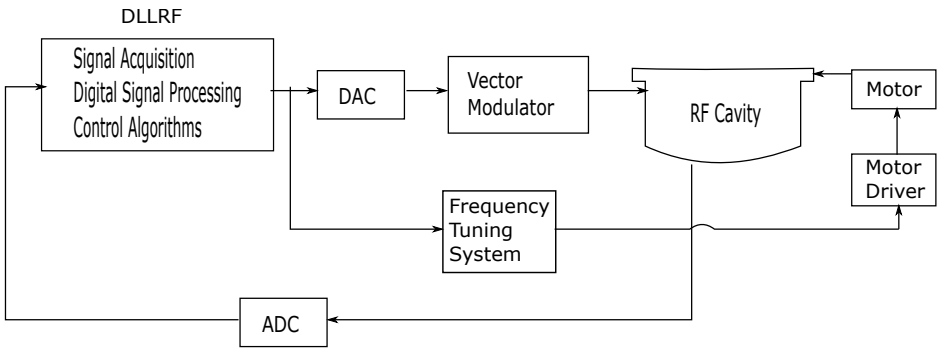

Figure 2.14. – Simplified scheme of a digital LLRF control system.

2.5. Summary and conclusions

Being particle accelerators such complex systems, they require the coexistence of a number of technologies to ensure a proper operation. The continuous improvement of this technologies is essential as the requirements of particle accelerators become more stringent day after day. The deep understanding of them becomes necessary to continue the research around them and thus, enhance their capabilities. This chapter focuses mainly on both of them, the diagnostics and the RF control system. It has made an introduction of the main principles of both of them in order to understand the tools developed and that are described in Chapters 4 and 5.

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CHAPTER 3

Digital Solution Selected and Involved Technologies & Sampling Technique

The selection of a suitable technology is a key factor in the development of any kind of application. It must provide specific features that allow the developer achieve the requirements of the project. The technology must be carefully studied, paying special attention to its limitations. Sometimes this limitations make the goals unreachable, but often they can be solved by tackling the problem from another point of view.

The first part of this chapter introduces the hardware technology selected, mainly digital, to develop two diagnostic and control tools in the field of particle accelerators, as well as justifying this decision. The second one is centered around the description of a digital technique, the subsampling technique, which has been applied to solve some limitations of the hardware employed.

3.1. Introduction

In this chapter, the technology selected in which the presented solutions are based is discussed, as well as an in depth study of the proposed signal sampling technique.

The hardware has been chosen with a clear goal: to develop highly reconfigurable systems for the proposed applications. The design of the diagnostic and control tools presented in the Chapters 4 and 5 has been centered in the attainment of versatile solutions, well suited for prototyping, therefore making very valuable tools for research tasks.

In the planning stage, it was concluded that digital hardware was the best way to develop the required reconfigurable solutions. To meet the aforementioned goals, the solution should also fulfill some enhanced characteristics, such as being highly flexible and modular. This features enhance the concept of reconfigurability, providing the developed prototype the ability to easily adapt to new requirements and the possibility to quickly add new functionalities.

From this premise, the most suitable architecture is selected. The PXIe architecture of National Instruments was chosen to develop the diagnostic and control applications described in Chapters 4 and 5. This platform offers a rugged PC based platform for measurement and automation systems. PXI is both a high-performance and (relatively) low-cost deployment platform for applications and consists of four main components: the chassis, the PC based controller, the modules and the LabVIEW based software environment. The added value of this architecture is the large variety of avaliable modules, includes the FPGA based ones.

The usage of analog components is avoided as much as possible in the projects presented, so the data acquisition PXIe modules selected have to deal with the continuous signals directly, with no analog downconversion stages. This presents quite a challenge considering that RF signals must be sampled, in the range of hundreds of MHz-s. The available DAC (Digita-to-Analog Converters) in data acquistion (DAQ) cards for the PXIe platform do not provide enough speed to carry out classic sampling (oversampling) meeting the Nyquist criterion [13] for all applications, so an advanced sampling technique known as subsampling has been studied and implement so that the cards available can acquire target signals for its subsequent processing with no information loss.

3.2. Digital Technology Selected

As mentioned above, the hardware required must provide a list of features in order to be able to the build the desired systems:

- Digital: the solution architecture must be mainly based on digital hardware, microprocessors and FPGAs, minimizing the usage of analog components.

- Modular: the platform selected must have a modular nature, giving the opportunity to easily exchange independent modules without being the rest of the system being affected.

- Reconfigurable: the solution must allow for quick changes or the addition of new functionalities and adapt to future changes in requirements.

A technology that meets the previous conditions has been sought out in the market. After considering some options, the PXI platform from National Instruments [23] have been chosen. The MicroTCA (or µTCA) standard [29] has also been considered as it provides a similar structure to PXI. On the one hand, MicroTCA has some advantages over the PXI standard, as for example the double width cards (called AMCs or Advanced Mezzanine Cards) [8]. On the other hand, it is a relatively new technology and therefore, the tools available to develop applications for this standard are not as advanced as the PXI related are. This is a big drawback regarding the intention to achieve a system that allows to quickly prototype desired solutions, and has been key in discarding this platform in favor of PXI.

The specific hardware chosen is built based on an 8 slot NI 1082 PXIe chassis. Two different PC based controllers have been selected, each one chosen to develop different approaches: a NI PXIe 8108 RT embedded controller running a real-time operative system and a NI PXIe-8135 embedded controller running Windows 7. For data I/O, the most relevant modules are members of the FlexRIO family, more specifically the NI PXIe-7961R and NI PXIe7966R FPGA cards and the NI 5751R, NI 5761R and AT-1212 adapter modules. In addition, some multifunction cards have also been employed, like the NI PXIe 6259 or the NI PXIe 7852R.

In the following sections, the technology selected and employed in terms of hardware, mainly the PXI and FlexRIO technologies, and software, the LabVIEW environment, is listed and described.

PXIe platform

The basis of the architecture is a PXIe chassis from National Instruments, with 8 slots, allowing the use of diverse control and data acquisition modules. Details of the PXI technology are explained in an auxiliary box and a schematic description of its features is described in Figure 3.2.

PXIe technology. PCI eXtension for Instrumentation is a modular control and data acquisition technology originally developed by National Instruments and arrived to market in 1997. Many industrial partners joined together into the PXI System Alliance (PXISA) [24], with the objective of ensuring interoperability between different vendors for maintaining control over the specifications [28].

It provides a robust and compact chassis, and a wide variety of modules (data acquisition, RF, communication, etc.). Many vendors produce modules and system controllers. In addition, synchronization of modules can be obtained from the backplane, via triggering or clock sharing.

The key elements of the PXI specifications start with the chassis, the element which encloses the system controller and modules. The backplane contains a reference clock running at 10 MHz. It also contains the PXI bus itself for connecting one slot with contiguous slots with the aim of transferring signals. Finally, the PXI trigger bus is divided into the Trigger and Star bus, the first one consisting of eight separate lines [19]. They enable the synchronization and timing signals to be passed from one module to another. The Star trigger bus is devoted to the applications where a high speed trigger is required.

The PXI system controller, or embedded controller, is always located in the first slot of the chassis. Following this approach, a fully controlled and embedded solution is obtained, an interesting feature for remote or compact control systems. A typical configuration of a PXI is shown in Figure 3.1, where a 8 slot chassis, the controller and some modules can be observed.

PXIe or PXI Express is an extension to the PXI platform added in 2005 [17]. This specification integrates PCI Express signals to PXI standard while maintaining backwards compatibility. It increases the blackpane bandwidth from 132 MB/s up to 6GB/s [3], 45 times higher. It also enhances time and synchronization features by incorporating a 100 MHz differential reference clock and differential trigger lines.

It is available for many different operating systems, such as different versions of Windows, Linux, and Real-Time OSes. There is also the possibility for connecting the system slot to a computer, or even to an extra chassis.

Finally, what really gives functionality to a PXI system is the wide variety of

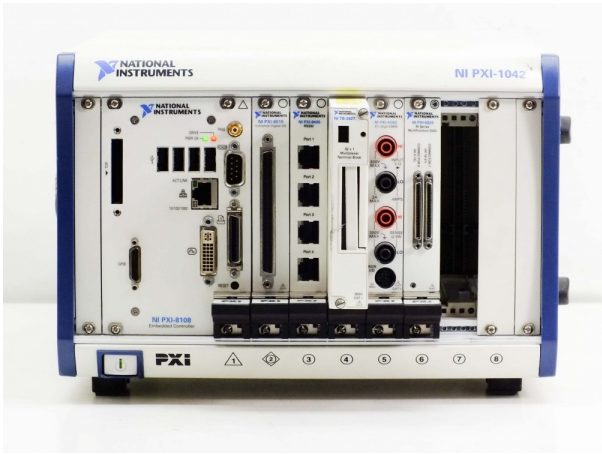

Figure 3.1. – A 18 slot PXI chassis, with a controller in the left side of the picture and 8 modules installed.

modules. PXISA is composed by around 60 companies, some of them are well known and with an important market share, such as National Instruments and Agilent [22]. Therefore, there are thousands of different modules which makes virtually any kind of measurement achievable.

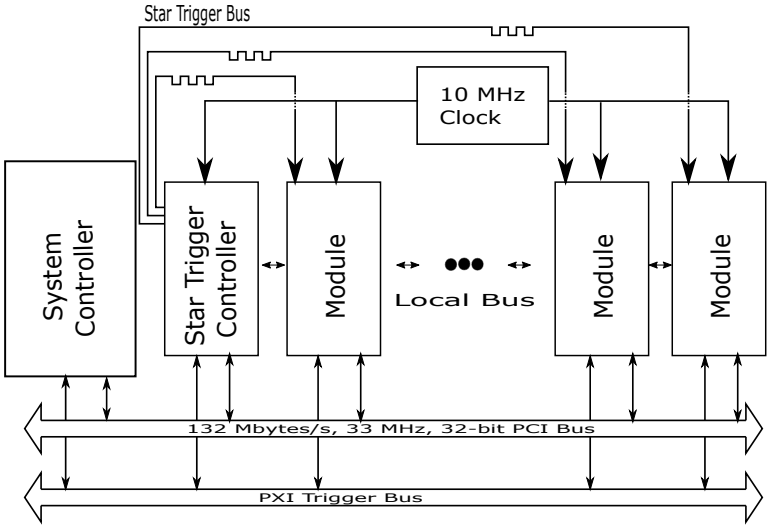

Figure 3.2. – Schematic description of a PXI system showing its main features

Figure 3.3. – A complete FlexRIO card, consisting in the FPGA module (right) and the adapter module (left).

FlexRIO. FlexRIO is a product family from National Instruments that takes advantage of FPGA technology. It provides customizable I/O for LabVIEW to create high-performance, reconfigurable instruments [26]. Specific analog to digital converters, digital buffers, connectors, and even specific channel counts can be designed to work in concert with a LabVIEW programmable FPGA target.

They are composed of two parts: the FPGA module and the adapter module.

- FPGA modules are based on the PXI platform and they are graphically programmed with LabVIEW FPGA. All the onboard processing and custom timing and triggering is performed in this part. They take advantage of the high-speed data streaming and synchronization provided by the PXI platform.

- The adapter modules are where the physical inputs and outputs of a FlexRIO system are defined. These modules are customizable and interchangeable, and they are provided by different vendors.

The Figure 3.3 shows a whole FlexRIO card, consisting in the aforementioned two parts, the FPGA module and the adapter module.

Working with FPGA technology has several benefits. The most relevant are listed in an auxliar box. The FlexRIO modules allow for the use of FPGA technology, with an high level programmation tool integrated in the LabVIEW environment and combined with other PXI modules.

FPGA technology. The most relevant advantages of the FPGA technology are:

- Performance: hardware parallelism allows to overcome the computing power of digital signal processors (DSPs). This is possible by breaking the paradigm of sequential execution and accomplishing more per clock cycle [18].
- Cost: The engineering expense of a custom ASIC design is much higher than the FPGA based hardware solutions [21], specially when small quantities of the systems are needed. This makes FPGA based hardware more suitable for prototyping purposes. It also allows to redesign the solutions if system requirements change over time.
- Reliability: It is worth remembering that FPGA circuitry is truly a hardware implementation of program execution, opposite to software tools that just provide the programming environment. This way, they guarantee true parallel execution and deterministic hardware dedicated to every task. Processor based systems involve several layers of abstraction (e.g. drivers, operative system) that are at risk of time-critical tasks preempting one another.
- Long-Term Maintenance: FPGA based solutions are easily upgradable, keeping up with future modifications that might be necessary. The required functional enhancements do not require the time and cost involved with ASIC redesign.

LabVIEW. National Instruments LabVIEW is a development environment for building data acquisition tools and instrument control systems quickly [27]. It is a graphical programming language with an integrated graphical user interface and it is especially suited for quickly prototyping systems.

LabVIEW allows the integration of different hardware devices such as scientific instruments, data acquisition tools, sensors... into the same test, measurement or control system. It is done by using a consistent programming approach. This translates into a well-known initialize-configure-read/write-close pattern for

most devices and a common compatible data returned from the analysis and reporting functions.

LabVIEW programming is based on G Language. This is coded graphically, and it is designed to be intuitive, based on a flowchart-like dataflow programming model. It was developed with the goal of offering a shorter learning curve than traditional text-based programming. This language naturally represents data-driven applications with timing and parallelism.

The G proggraming language is often called "LabVIEW programming", and defines the LabVIEW programming philosophy. As mentioned before, is a graphical dataflow language in which functions or operations (called nodes) operate on data as soon as it becomes available, rather than in the sequential line-by-line way that most classic programming languages employ. It allows the developer quickly tie together data acquisition, analysis, and logical operations and this way easily understand how data is being modified. The data flow is defined using wires that connect one nodes outputs with the inputs of another.

This helps abstracting from administrative complexity of computer programming such as memory allocation and language syntax, foscusing on data and operations. LabVIEW provides a powerful optimizing compiler to translate the graphically programmed code into efficient machine code [30]. This programming approach is also very friendly in debugging tasks, as dataflow can see flowing through the diagram thus making errors easy to find.

LabVIEW programs are called virtual instruments, or VIs, because originally, their appearance and operation often imitate physical instruments. Each VI is composed of two separate parts, the front panel and the block diagram:

- Front Panel: this window is the user interface for the VI, and is where controls and indicators are placed. Controls (knobs, push buttons, dials, sliders, strings...) define inputs, and indicators (graphs, charts, LEDs...) display outputs. When you interact with the front panel as a user interface, you can modify controls to supply inputs and see the results in indicators.

- Block Diagram: is where subVIs, structures, terminals, functions, constants, and wires, which transfer data among other block diagram objects, reside. The real functionality of the VI program is defined here. To do so, the Functions Palette is used. This contains the VIs, functions and constants you use to create the block diagram.

A sample VI, with its respective front panel and block diagram, can be observed in Figure 3.4.

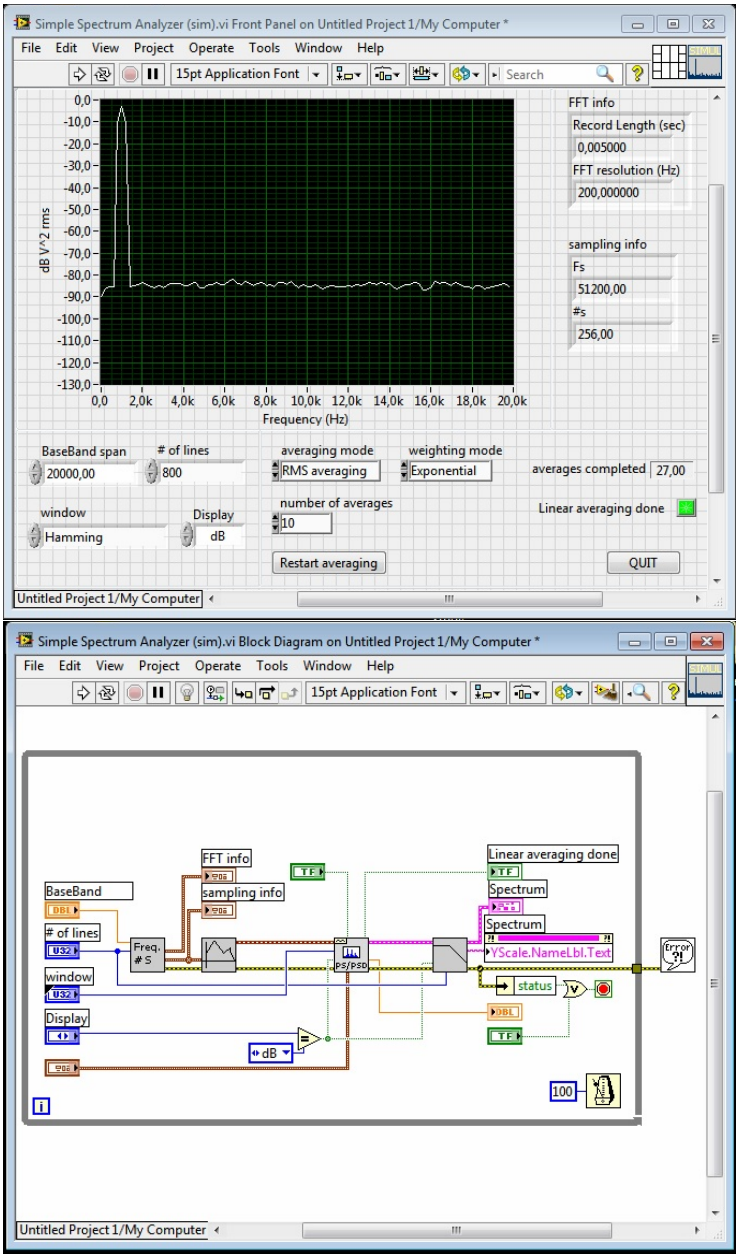

Figure 3.4. – Snapshot of a LabVIEW VI that simulates a spectrum analyzer, with its respective front panel window (up) and block diagram (down).

LabVIEW has drivers for thousands of NI and third-party hardware, thus providing a valuable hardware abstraction to the developer. Thie APIs of the drivers allow the developer to use high-level functions that keep a balance between abstracting the unnecessary administrative tasks such as memory management and format conversion, but keep the flexibility of being able to customize many aspects of the task you need to accomplish. Each API gives you full control of the actual process involved but does not require you to deal with all of the intricacies of implementing the minutia of the protocol. Most of these driver APIs implement a specific technology. For example, the NI VISA (Virtual Instrument Software Architecture) standard is used to communicate (configuring, programming, and troubleshooting) with most instrumentation buses including GPIB, USB, Serial, and Ethernet [31]. It provides a consistent and easy to use command set to communicate with a variety of instruments. VISA was created to through an alliance of several companies including GenRad, Racal Instruments, and Tektronix, formed the VXIplug&play Systems Alliance and National Instruments to ensure multi-vendor interoperability, thus reducing the development time and effort for a fully working system including multi-vendor instrumentation.

The main advantage of VISA is that it uses many of the same operations to communicate with instruments regardless of the interface type, that is, VISA provides interface independence. It provides the most used functionalities in the instrumentation field in a very compact command set, building this way function calls that are easily portable from one platform to another. The communication architecture between a physical device and LabVIEW using the NI-VISA stadard is shown in Figure 3.5.

It is worth pointing out that LabVIEW also offers the same low level access as you would get in traditional programming languages (via Low-Level APIs), in case you need to define every detail of a task.

LabVIEW also provides built-in application frameworks for most of the communication protocols used in science and industry fields, including widely known ones like TCP, serial or CAN, and more specific ones as EPICS.

The cross-platform nature of LabVIEW allows to develop code to many different computing platforms. This includes not only general purpose operative systems like Windows, Mac OSX or Linux, but also different hardware targets like embedded real-time controllers, ARM microprocessors or even FPGAs.

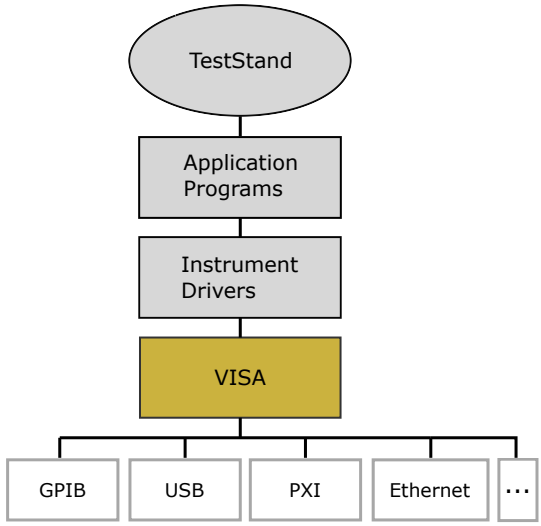

Figure 3.5. – Communication architecture from a wide variety of devices to the final LabVIEW application using VISA standard.

3.3. Subsampling

Almost all the digital signal processing theory is built around the periodic sampling. It consists on the representation of continuous signal with a sequence of discrete values, spaced regularly in time. This is the so called sampling period t_s. Then, the discrete sequence representing a continuous signal $x(t)$ is [4]:

$$x(n) = x(nt_s) \quad n = 0, 1, \ldots$$

Sampling, also known as discretization, is the process of obtaining each $x(n)$ value and is performed using analog-to-digital converters (ADCs), whose output are conformed by series of digital values. One of the most relevant concerns of sampling theory is to determine how fast a given continuous signal must be sampled in order to preserve the original information in the output value string. The next paragraphs study and clarify some key aspects of the sampling theory as well as presenting an advanced technique.

3.3.1. Aliasing

Discrete time signals have an associated intrinsic fequency-domain ambiguity that does not ocur in continuous signal field [5]. This phenomenon is called aliasing. This is defined as an effect that causes different signals to become indistinguishable when sampled. This indistinguishable signals are referred as aliases. That is, a given sequence of values can represent values of an infinite number of continuous signals, being all of them equally valid. In order to prove this, lets assume a f_0 frequency pure sinusoid given in its time domain:

$$x(t) = sin(2\pi f_0 t) \tag{3.1}$$

If this signal is sampled at a rate of $f_s$samples per second, that is, at regular periods of t_s seconds being $f_s = (t_s)^{-1}$, a time dependent successive samples are obtained. This way, the n^{th} sample, which corresponds to the original sinewave value at the time instant nt_s can be expressed as

$$x(n) = sin(2\pi f_0 n t_s) \tag{3.2}$$

Using the well known trigonometric property that states that two values of a sinewave are identical at two points separated exactly by an integer multiple of 2π radians,

$$x(\theta) = sin(\theta + 2\pi k) \tag{3.3}$$

being k any positive or negative integer, Equation 3.2 can be modified as follows,

$$x(n) = sin(2\pi f_0 n t_s) = sin(2\pi f_0 n t_s + 2\pi k) = sin\left(2\pi(f_0 + \frac{k}{nt_s})nt_s\right) \tag{3.4}$$

Defining k as a multiple of n, $k = mn$,

$$x(n) = sin(2\pi(f_0 + \frac{m}{t_s})nt_s) \tag{3.5}$$

Going back to frequency notation,

$$x(n) = sin(2\pi f_0 n t_s) = sin(2\pi(f_0 + mf_s)nt_s) \tag{3.6}$$

The Equation 3.6 implies one of the most important relationships in digital processing theory, which is that a $x(n)$ series of discrete values that represent a f_0 frequency continuous sinewave also represent any other sinewave of frequency

$(f_0 + mf_s)$.

That means that the spectrum of any discrete sequence of sampled values contains periodic replications of the original continuous spectrum. This replications are known as aliases, and they repeat infinitely in both directions of the frequency spectrum, separated by a period of f_s. The replicated spectra are not just mathematical concepts, they physically exist and have effect on the digital signal treatment process.

Despite the fact that aliasing is usually a problem and an undesirable effect, reviewing the mathematical origin of this ambiguity allow to not only avoid when desired, but also use it to our advantage.

3.3.2. Sampling process

In order to understand the sampling process and how the aliasing can be used to develop advanced sampling techniques, the sampling of low pass signals must be carefully studied.

To illustrate this process, lets assume that a signal with the continuous signal spectrum, centered and symmetrical at 0 Hz as seen in the upper schematic of Figure 3.6, is sampled. To make a more realistic scenario, this spectrum is also band-limited, that is, all of its energy is inside the [-B, B] Hz range, which is to say that the signal amplitude outside this range is 0. If this signal is sampled at a f_s rate, spectral replications effect occurs, as described in the lower part of Figure 3.6. Note that the amplitude of the energy distribution of the continuous signal and the discrete one in the frequency spectrum differs in a factor of $f_s(1/t_s)$ [25].

Notice that in the exposed example, the f_s sampling frequency employed is greater than twice the highest frequency component B, that is, $f_s/2 \geq B$. This condition is known as the Nyquist criterion [13].

The $f_s/2$ frequency is an important quantity in sampling theory, and is referred to by different names, such as folding frequency, critical Nyquist or half Nyquist [16]. The frequency range of $\pm f_s/2$ will be the spectral band of speciall interest from now on.

If $f_s$is reduced looking to achieve a slower and therefore cheaper data acquisition system, the location of the replicas shifts, caused by the reduction of the periodic distance between aliases. This can lead to the overlapping of this aliases, as illustrated in pale yellow in Figure 3.7. When this happens, the upper and lower edges of the first order aliases (those centered at $+f_s$ and $-f_s$) lie in the band of interest, combining with the original spectrum. This results in aliasing errors. The consequence is that the information obtained does not

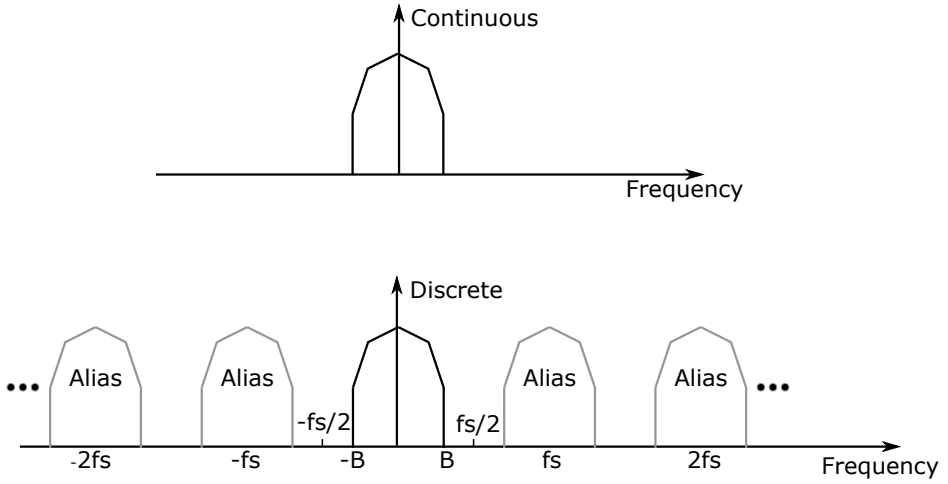

Figure 3.6. – Spectrum of the original continuous signal (up) and spectral replications of the sampled signal (bottom).

contain the same information as the original.

It is worth pointing out that in real applications meeting the Nyquist criterion is usually not enough condition to sample low pass signals. Non-ideal (real) continuous signals are always accompanied by noise, that is located beyond the boundaries of the range [-B,+B], as shown in the upper part of Figure 3.8. When this signal is sampled, the noise components outside the [-B,+B] (where the signal of interest reside) end up in the band of interest, regardless of the sample rate. This is the reason why building a real sampling application requieres analog low-pass filters with a cutoff frequency of B prior to the analog-to-digital (A/D) converters, often referred as anti-aliasing filters, to attenuate as much as possible any energy above +B and bellow -B.

3.3.3. Sampling Bandpass Signals

Another sampling scheme is described in this subsection. Now, the goal is to sample a continuous bandpass signal not centered at 0 Hz. If the original signal allows in terms of bandwidth and center frequency, a sampling technique known as subsampling, also referred in the literature as bandpass sampling [20], harmonic sampling [11], IF sampling [6], subsampling [7] or sub-Nyquist sampling [10], it can be employed in order to reduce the speed requirements of the ADCs necessary for traditional low-pass sampling schemes. In this

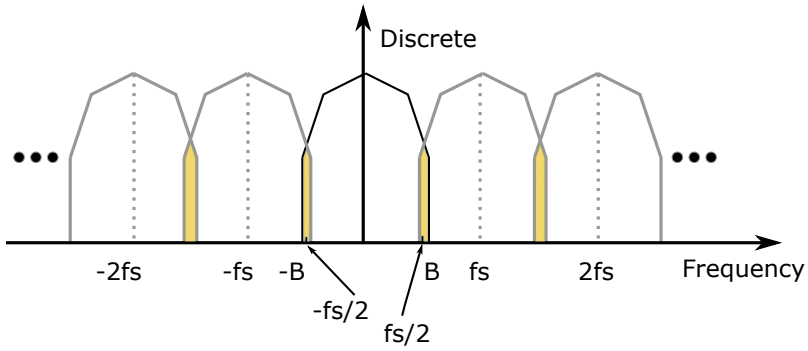

Figure 3.7. – Frequency overlapping when $f_s/2 \geq B$ condition is not satisfied.

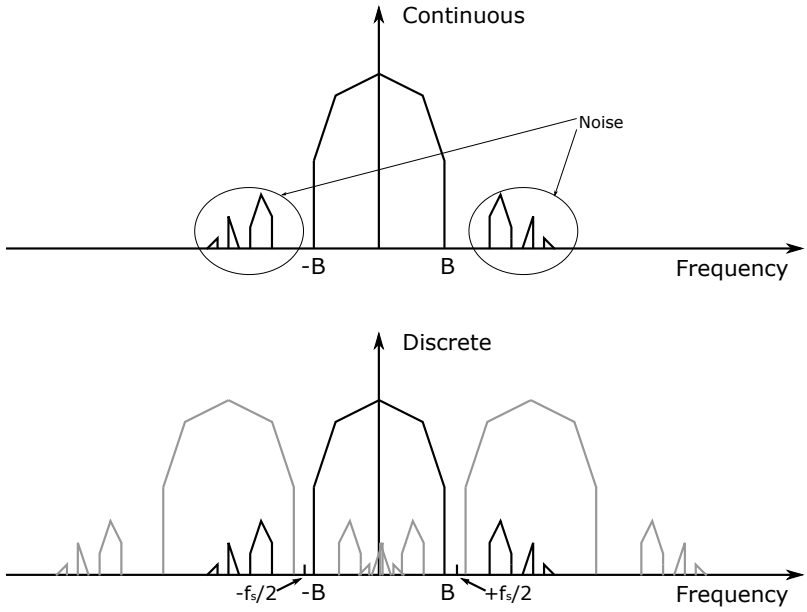

Figure 3.8. – Original continuous spectrum, including noise (up) and the discrete spectrum of the sampled signal, where the noise of the replicas corrupt the information on the band of interest.

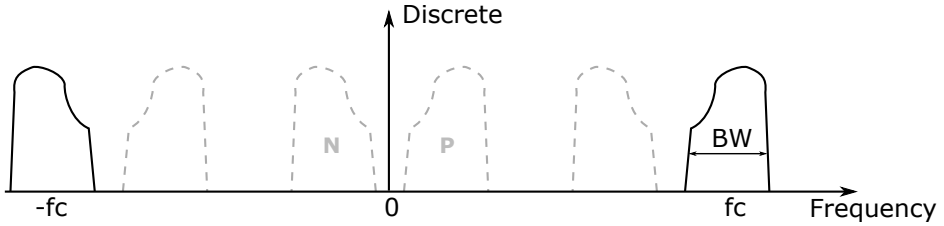

Figure 3.9. – Frequency spectrum of a sampled bandpass signal.

technique, the main concern is the signal's bandwidth and not its highest frequency component, as stated by the Nyquist criterion.

Subsampling relies on the spectral replicating effects to reconstruct the target signal. In this technique, the digitization and the frequency translation is performed in a single process. Figure 3.9 represent a sampled bandpass signal whose bandwidth is BW. It has been discretized at a frequency of f_s, being this lower than the carrier frequency f_c but fulfilling $f_s > 2BW$. Spectral replications of the original positive band are referred as P, while N is used to designate aliases of the negative band.

However, not all the sampling rates are adequate for performing a successful subsampling process without lossing information. In order to find out which the range of suitable sampling rates is, its boundaries must be studied.

If the sampling rate f_s employed in Figure 3.9 is increased to f_{s1}, $f_{s1} > f_s$, the P replicas will shift up to the left and the Ns to the right, while the original negative and positive bands stay fixed. The maximum acceptable f_{s1} is reached when P and N replicas face up against each other (this is represented in the upper picture of Figure 3.10), since increasing sampling rate beyond this point will cause overlapping, leading to aliasing errors. In this limit situation, an arbitrary m number of replications appear in the range of $2f_c - BW$, being m any positive integer (always assuming $f_{s1} > 2BW$)

$$mf_{s1} = 2f_c - BW \text{ or } f_{s1} = \frac{2f_c - BW}{m} \tag{3.7}$$

As mentioned above, this is maximum acceptable sampling range to avoid overlapping, so

$$f_{s1} \leq \frac{2f_c - BW}{m} \tag{3.8}$$

Now, a lower sampling rate is assumed, f_{s2}, that is, $f_{s2} < f_s$. In this case, P

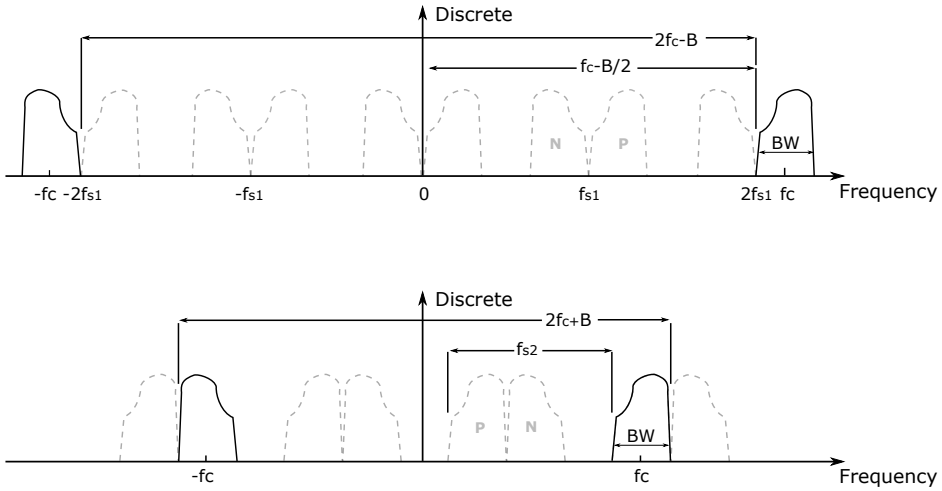

Figure 3.10. – Distribution of spectral replications when sampling rate is increased (top) or decreased (bottom) to the limit before overlapping occurs.

replicas shift to the right and Ns to the left. The lower picture of Figure 3.10 shows the point where P and N butt up against each other. This occurs when the minimum possible sampling rate f_{s2} is used. In this condition,

$$(m+1)f_{s2} = 2f_c + BW \text{ or } f_{s2} = \frac{2f_c + BW}{m} \tag{3.9}$$

so, the minimum sampling rate must fulfill the following,

$$f_{s2} \geq \frac{2f_c + BW}{m+1} \tag{3.10}$$

Combining Equations 3.8 and 3.10, the suitable range for the sampling rate $f_s$is obtained in order to avoid aliasing errors,

$$\frac{2f_c - BW}{m} \geq f_s \geq \frac{2f_c + BW}{m+1} \tag{3.11}$$

where m is any positive integer, and once again, only if $f_s > 2BW$.

Equation 3.11 is key in subsampling and must be studied in detail. In oder to understand its nature, it is usually plotted the normalized minimum sampling rate $(2f_c + BW)/(m+1)$ as function of the highest signal frequency $f_c + BW/2$ component normalized to bandwidth BW [15]. This is shown in Figure 3.11.

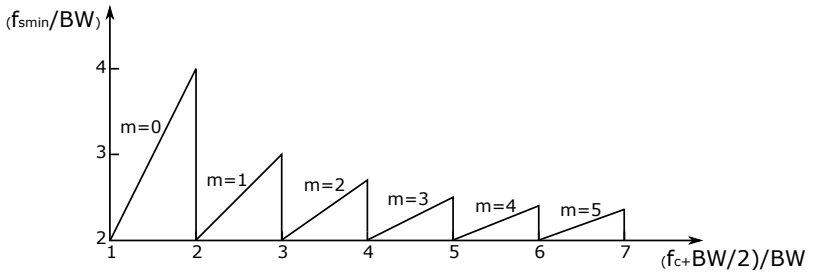

Figure 3.11. – Minimum subsampling sampling rate for various values of m.

Two important conclusions are drawn from here. First, the minimum sampling rate is never greater than 4BW and second, the minimum suitable sampling rate decreases as the center frequency of the target bandpass signal increases.

This feature must be studied carefully. Not every sample rate above the ones shown in Figure 3.11 is acceptable. To find them, the ranges given by Equation 3.11 must be regarded. In Figure 3.12, suitable regions are shown by plotting upper and lower boundaries of valid sampling frequencies for different values of m. Regions of acceptable subsampling sampling rates normalized to the sample rate over the signal bandwidth are shown in pale yellow.

It can be concluded from Equation 3.11 or Figure 3.12 that a sampling rate that lies on the boundaries of non-valid and valid regions can be used, but in practice, these values must be avoided [9]. Is strongly recommended to choose f_s separated from limits, due to unavoidable imperfections of the required setup (bandpass filters, clock generator...), as nonlinearities or instabilities.

At this point, the concept of a guard band is created, which are located at each side if the original signal as shown in Figure 3.13. The filter's bandwidth in this case is $BW' = BW + (\triangle BW_L + \triangle BW_H)$, being $\triangle BW_H$ and $\triangle BW_L$ the upper and lower guard bands widths, respectively. This is an important parameter when it comes to finding which the optimum sampling rate is, that is, the operating point. It is logical to try to set up the sampling rate as close to the corners of colored areas showed in Figure 3.12 as possible, as it means lower rates. However, the closer to the boundary of yellow area is the operation point selected, the more narrow the guard band must be, involving the usage of more expensive setup. The Figure 3.14 represents a practical operation point selection in order to compensate nonideal hardware in a graphical way.

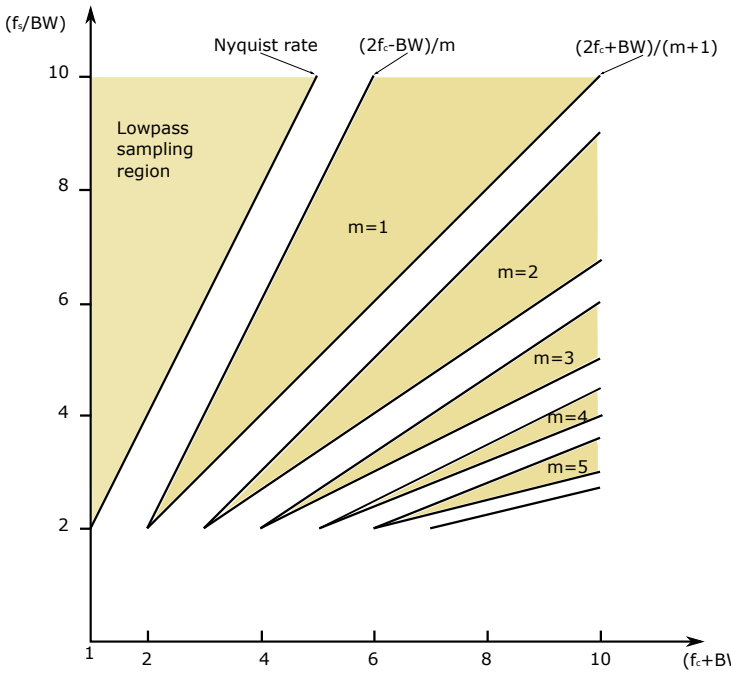

Figure 3.12. – Acceptable regions for the selection of normalized sampling frequency (colored in yellow) for different values of m.

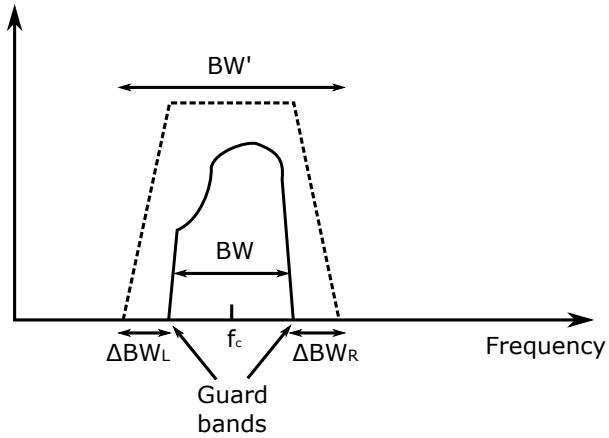

Figure 3.13. – Guard band representation of a bandpass signal.

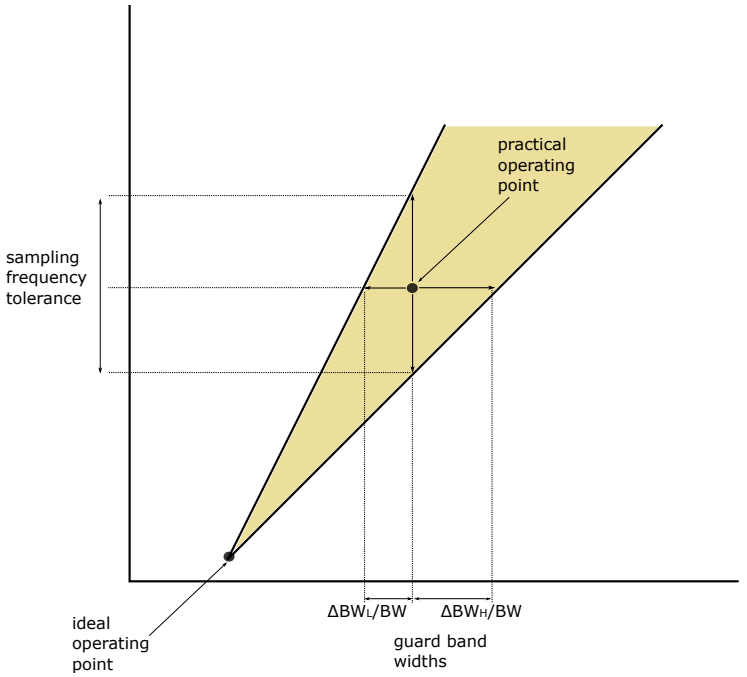

Figure 3.14. – Practical operation point selection description against ideal operating point.

There are two main procedures to select the practical operation point in the literature [20]. The first one suggest to set the sampling rate in the middle of an acceptable (yellow) wedge for a given value of m. This is calculated performing the average of the upper and lower limits defined by Equation 3.11:

$$f_{s-mean} = \frac{1}{2}\left[\frac{2f_c - BW}{m} + \frac{2f_c + B}{m+1}\right] \tag{3.12}$$

The second way is to determine an intermediate operating point defined by:

$$f_{s-inter} = \frac{4f_c}{m_{odd}} \tag{3.13}$$

where m_{odd} is an odd integer.

3.3.4. Spectral inversion

For certain valid sampling rates, it may occur that the replication located in the baseband spectrum (concretely in the positive side of the band of interest, $f_s/2$) correspond to the negative component of the sampled signal, which means that it has the inverted shape of the desired signal. This is called spectral inversion, and happens when m in Equation 3.11 is an odd integer.

When the original bandpass components present a symmetrical distribution about its carrier frequency f_c, spectral inversion does not cause any problem. But when this condition is not met, two solutions may be chosen. The first one is the most obvious, and consists on choosing even m values for Equation 3.11. The second involves some additional digital processing. To reinvert the spectrum back to its original shape, the discrete sample sequence can my multiplied by a sequence of alternating plus ones and minus ones, $(+1, -1, +1, -1, ...)$. This process is equivalent to multiplying the sequence obtained in the sampling process by a cosine whose frequency is $f_s/2$ [9].

3.3.5. Advantages of Subsampling

Besides from the obvious advantage of allowing for the possibility to employ slower ADCs and therefore more cost effective hardware, the use of subsampling in data acquisition processes reports several advantages. The most important are listed bellow:

Reduction of Data Rates tp FPGAs. It is common to use FPGAs to capture the output data from ADCs, and as expected, reducing the ADC sampling rate also decreases the required FPGA rate. This allows a less restrictive design in terms of amount of layouts of the board, signal routing and clock speed, and therefore the usage of more cost effective FPGA devices for a given data acquisition application if subsampling is performed.

Avoiding Downconversion. Many classic system designs perform an additional analog down conversion stage previous to the ADCs. This implies the usage of a mixer, an local oscillator signal and a band filter. If subsampling is carried out, the ADC itself acts as a downconverter.

Setup and Hold Time. The higher the data rates are, the more problematic setup and hold times of the ADCs become. This parameters are critical to ensure

the ADC data capture inside the FPGA or any digital system. Unsersampling allow more relaxed specification compared to the oversampling.

If setup and hold time requirements are not met, marginal capturing may occur. This happens when some of the data bits change its value providing wrong data output.

Power Consumption. Increasing data rates directly increases the power consumption of the ADCs, a feature which may be critical for some applications, such as autonomous devices using powering batteries. Many applications that use pipeline ADCs need to pay special attention to the consumption as these ADCs comparatively consume more power to get the required performance [14] and subsampling can be a solution for this problem.

However, subsampling also presents some disadvantages compared to oversampling. The most trivial is the restriction of the available frequencies to employ to perform the digitalization. This results in less flexible planning in the subsampling case, as oversampling designs can select the sampling frequency location wherever required in the first Nyquist Zone without any other considerations.

Another inherent drawback that must be pointed out is that oversampling can handle higher signal bandwidths [14]. Finally, the last relevant issue of subsampling is related to process gain and obtained noise level. In a real sampling process, a processing gain is achieved in addition to the SNR shown in the ADC datasheets. Processing gain (PG) is defined by [32]:

$$PG = 10log(\frac{f_s}{2BW}) \tag{3.14}$$

Regarding the signal-to-noise ratio (SNR), the total amount can be calculated following [14]:

$$SNR_{total} = SNR_{ds} + PG \tag{3.15}$$

being SNR_{total} the total SNR of the measured signal and SNR_{ds} the value provided in the datasheet. So, the higher the sampling rate f_s, the higher the process gain and therefore, the noise level of the signal obtained from the discretization process.

When looking at the SNR, the clock jitter must be also regarded. Jitter is defined as a low random variation on the sampling period [12]. The contributors to the system jitter are the aperture jitter of the sample-and-hold switch at the input of the ADC and the sampling-clock jitter. Combining these two uncorrelated jitter-noise sources using the root-sum-square formula, or

$t_{jitter} = \sqrt{(t_{jclock})^2 + (t_{jADC})^2}$ in rms picoseconds, where t_{jitter} is the total jitter of the system, t_{jclock} is the jitter from the external ADC clock, and t_{jADC} is the jitter of the ADC-input-sampling switch [1].

The jitter-related factor that limits the SNR of the ADC is given by $SNR_{jitter}(dBc) = -20 \cdot log(2\pi \cdot f_c \cdot t_{jitter})$ [2]. That means that for a fixed amount of clock jitter, the SNR degrades as the input frequency increases, which must be taken into account in subsampling applications.

3.4. Conclusions

This chapter has presented the initial goals of the projects to be developed, focusing in the attainment of flexible, reconfigurable and modular nature solutions in the field of particle accelerator diagnostics and control. Based on this requirements, a suitable hardware architecture has been selected, being this the PXI platform from National Instruments. This offers a robust PC based environment to develop measurement and automation systems, providing a wide variety of interchangeable modules of very different nature such as data acquisition, timing cards, signal generators... Another advantage of this solution is that all the hardware as well as the code writing is carried out under a LabVIEW environment, which eases the development of algorithms and the integration of the different hardware cards without worrying about driver coding.

Although PXI offers a very suitable platform for the intended purposes, some limitations must be taken into account. For the selected hardware, the available data acquisition ADC speed does not allow to oversample all the required RF signals. So, to overcome this problem, an advanced sampling technique called subsampling has been proposed. This technique uses the phenomenon known as aliasing in order to recover the information of the original continuous signal information looking at the spectral replication located at low frequencies. This way, lower sampling frequencies and thus, more cost effective ADCs can be employed in the hardware setup. The main advantages of using this technique, as well as its drawbacks have been also studied in this chapter.

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CHAPTER 4

Design and testing of a compact BPM diagnostic for particle accelerators based on PXIe

Diagnostic devices are vital components of any particle accelerator. The success of the machine as a whole, largely relies on the success of the full range of beam diagnostics. They allow to measure a wide variety of properties of the particle bunches. A large diversity of diagnostic tools are used in every machine. Each one is based on a different physical process, depending on the accelerator type. Among them, the most common is the Beam Position Monitor or BPM, which is used to measure the center of mass of the particle beam under study.

This chapter describes the design and development of a compact BPM test-bench based on the PXIe architecture.

4.1. Introduction

This chapter is devoted to the design and development of a digital and compact BPM diagnostic system and a prototype for testing of such devices. These diagnostics devices are essential parts in every particle accelerator, as they are used to obtain non-intercepting beam position information from the beam-induced signals.

The system presented is conceived as highly modular, flexible and easily reconfigurable system for a 352 MHz signal, which is a typical master signal in many accelerator types like photon and proton acceleration facilities [4, 7]. For this purpose, the PXIe environment of National Instruments has been chosen as the core hardware platform for the system development. It has allowed the integration of all the devices needed for developing the required fast data acquisition task, digital data processing and monitoring tools, in order to build the diagnostics structure.

Along with the digital BPM system, a complete testbench has been built in order to test and validate the developed solution. This includes an aluminum structure containing a copper conductor fed by a RF generator to simulate the particle beam, a vacuum system and a linear two-dimensional translation platform employed in order to simulate the beam deviation. This structure is attached to two stepper motors which are used to automate tests.

The digitalization required for the data acquisition has been carried out using an advanced sampling technique known as undersampling (see Chapter 3), a fact that has allowed the development of a more cost-effective solution.

4.1.1. Area of the project work

This project was born as a collaboration between the Automatic Control Group (GAUDEE) and the RF and Microwave Group of the Department of Electricity and Electronics of the University of the Basque Country UPV/EHU. It was supported by the Provincial Council of Bizkaia to build a prototype for beam diagnostics in the field of particle accelerators.

The goal is the development of a beam position monitor and a complete testbench for testing such device in the laboratory. The design is oriented to obtain a fully functional device for research tasks, but at the same time being a solution that can be directly implemented in a real machine. The presented setup is designed for a 352 MHz frequency signal, but can be easily adapted to a wide range of frequencies.

In addition, all the required mechanical design has been carried out by the aforementioned research groups.

4.2. Proposed solution

This work proposes the development of a compact BPM system based on capacitive or electrostatic pick-ups. The main goal of this project is to build a system specially suitable for fast prototyping and capable of easily adapting to new requirements coming for different testing and research experiments. This idea requires a highly flexible system in order to offer the desired features. To satisfy the proposed objective, a mainly digital solution has been built, focusing on the achievement of a highly modular and reconfigurable system.

Recently and due to the quick growth of the telecommunication technologies, there is the trend to a higher digitalization in data acquisition systems. As ADC speeds are constantly increasing, the digitalization is performed in early stages, and some of the analog signal conditioning is replaced by digital signal processing. Despite of requiring a higher development effort, there are several advantages to the digital processing based solutions over analog based systems; among them it is worth emphasizing the stability of measured and processed variables, the higher repeatability and the ease to monitor. Furthermore, and what is more important for the proposed compact BPM testbench, digital systems are much more flexible, allowing to develop very versatile solutions. They also provide a reconfigurable environment, meaning that new functionality or adjustments can be easy and quickly implemented simply changing the program code, not depending of extra-hardware. This is a very valuable feature for the solution that is proposed in this chapter.

Apart from the aforementioned advantages, digital systems allow to implement complex algorithms and data processing, thus making possible the development of a compact system suitable for laboratory testing and research tasks.

In order to plan the systems settings in terms of hardware, its essential to determine the signal processing that is going to be required in the current BPM. Three general methods are used for deriving a normalized position signal from the raw pickup electrode signals: amplitude-to-phase conversion (AM/PM) processing, log-ratio processing and difference-over-sum processing. Each one has it own advantages and drawbacks over the others as simplicity, cost or dynamic range as studied in Chapter 2. Due to its simplicity of implementation, the difference-over-sum processing, also known as delta-sigma (Δ/Σ), is the most widely used method to perform the position calculation. In the current

project, this method has been selected to carry out the implementation. The relation between the measured signals from each sensor and the beam position in both directions is given by:

$$x = \frac{1}{S_x}\frac{U_{right} - U_{left}}{U_{right} - U_{left}} + \delta_x = \frac{1}{S_x}\frac{\Delta U_x}{\Sigma U_x} + \delta_x \tag{4.1}$$

$$y = \frac{1}{S_y}\frac{U_{up} - U_{down}}{U_{up} - U_{down}} + \delta_y = \frac{1}{S_y}\frac{\Delta U_y}{\Sigma U_y} + \delta_y \tag{4.2}$$

where $S_x$and S_y constants are defined as position sensitivity and represent the difference between the measured normalized voltage difference and the real beam displacement. It is given in [%/mm]. $\delta_x$and δ_y are the offset correction for the deviation of the electrical center, given in [mm].

The data acquisition system must sense the RF signals in order to generate valuable data for the subsequent data processing. Following with the idea of the minimization of analog electronics, the acquisition stage has been designed to perform a direct discretization of RF signals. This implies that the ADC must digitize RF frequency signals. In this particular case, a 352 MHz signal is used as the master oscillator of the system. The sampling of a such high frequency signals under the classic rules of sampling theory based on the Nyquist theorem implies the use of really fast ADCs. In the present application, an ADC with a minimum sampling rate of 704 MHz (twice the original signals fastest frequency component) is required in order to perform the sampling process meeting the Nyquist criteria. The subsequent digital process must be performed considering this rate. This approaches to the state of the art in ADCs and digital processing systems[5], thus implying a high economic cost.

With the intent to obtain a more cost-effective solution, an advanced sampling technique known as undersampling has been used to discretize the RF signals read from BPM pick-ups. This has allowed to use not so high throughput ADCs, improving the cost of the final system.

Considering the proposed requirements and the flexible nature of the system that is desired, the PXIe technology of National Instruments has been chosen as the core platform for the compact BPM development. This provides a powerful solution where a wide variety of hardware modules can be integrated into a compact and robust chassis. In addition, all the device management and programming tasks are performed under a LabVIEW environment, which eases and speeds up the development.

The PXIe architecture supports cards based on FPGA technology, offering a very appropriate platform for the development of digital monitoring and

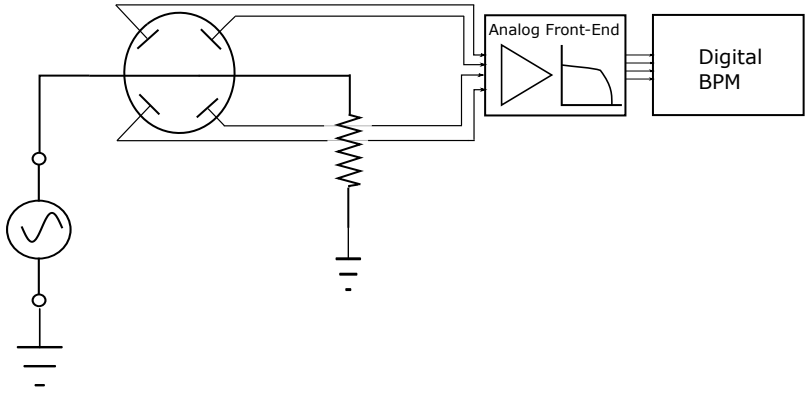

Figure 4.1. – Block diagram describing the developed BPM system.

diagnostic tools.

So, taking advantage of the possibilities of the PXIe systems, a real-time momitoring system has been built following the scheme shown in Figure 4.1.

This work can be divided in two separate parts. The first one corresponds to the design of a digital BPM system for beam diagnostics for monitoring the beam position relative to the pipe. The second part describes the testbench that has been built in order to test the BPM system in the laboratory and used to obtain experimental results.

4.3. Developed BPM

In this section, the design and development of the digital BPM system is described. This includes a list of the technology and hardware employed and the implementation details of digital processing algorithms, based on the undersampling digital discretization technique.

4.3.1. Description of the technology used

In this section, a brief description of the PXIe platform is given. This has been taken as the reference for building the system. The main elements are: a PXIe chassis, FlexRIO modules and multifunction DAQ cards, along with LabVIEW as the development environment.

	FlexRIO card		Adapter module
Model	NI PXIe-7961R	Model	NI 57561R
FPGA	Virtex-5 SX50T	ADC/DAC rate	250 MS/s
DMA channels	16	Nº of channels	16
Embedded RAM	594 KB	Resolution	14 bits
FPGA slices	8160	Bandwidth	500 MHz
DSP slices	288		

Table 4.1. – Specifications of the data acquisition system, conformed by a FlexRIO card and its respective adapter module.

PXIe chassis. The core of the system implementation is an 8 slot NI 1082 PXIe chassis. It offers a robust basis for building flexible solutions, allowing to work with a very wide variety of modules. A NI PXIe 8108 RT embedded controller based on an Intel Core 2 Duo T9400 processor (2.53 GHz dual core) has been used together with the mentioned chassis. This is the core of the system, running a real-time operative system and being a suitable platform to develop deterministic applications for data acquisition.

FlexRIO card and adapter modules. In the development presented, a high throughput FlexRIO FPGA card has been used, more concretely the model NI PXIe 7961R (introduced in Chapter 3. The adapter module employed to carry out the data acquisition tasks has been the NI PXIe 5761R with an ADC up to 250MS/s (also presented in Chapter 3. The main features of the data acquisition system, including the FlexRIO module and adapter module are listed in Table 4.1.

Additional cards. The main inputs of the BPM system are the RF signals sensed by the pick-ups. However, some low speed signals, as temperature, should be also acquired to get valuable information. For this task, a NI PXI 6259 multifunction DAQ card has been selected along with a SCb-68 connector pane.

LabVIEW. All the aforementioned devices are operated in LabVIEW 2012 SP1. The FlexRIO card is programmed taking advantage of the LabVIEW

FPGA module, while the functions of the host program are implemented on the Real-Time Module.

4.3.2. Subsampling technique: implementation details

With the aim of building a cost-effective data acquisition system for the desired BPM, the discretization of the RF signals read from the capacitive pick-ups has been performed based on the advanced sampling technique called subsampling, which is studied in detail in Chapter 3. The typical digital BPM solutions perform an analog processing of the RF signals with the aim of obtaining an IF signal thus handling lower frequency signals in the digitalization process [2]. In the presented work, no such process is applied, directly discretizing the signals at the original frequency of the master signal of the system.

In order to simulate a particle beam, a pure sinusoid obtained from a RF generator is used at 352 MHz, which is a widely used master frequency in particle accelerators [4]. The election of an appropriate sampling rate is essential to obtain a reliable acquisition stage avoiding information loss and errors in the measured data. As previously mentioned, the 250 MS/s DAC of the Ni PXI 5761R card has been in charge of the discretization of the RF signals. This is a suitable undersampling frequency regarding the upper and lower limits stated in Equation 4.3 obtained in Chapter 3 for a given original signal of 352 MHz, considering $m = 2$ and assuming that the original signals have a small bandwidth compared to the carrier frequency:

$$\frac{2f_c - BW}{m} \geq f_s \geq \frac{2f_c + BW}{m+1} \tag{4.3}$$

$$352\,MHz \geq 250\,MHz \geq 234\,MHz$$

Sampling the original signal of $352\,MHz$ at this sampling rate, the alias located at $102\,MHz$ signal is obtained (inside the Nyquist zone) as stated in expression $(f_0 + mf_s)$ from Chapter 3.

4.3.3. BPM diagnostic tool designed

The beam position monitoring application scheme follows the flow described in Figure 4.2.

The application designed basically consists in the acquisition of the four RF signals measured in the electrostatic pick-ups and its processing to get valuable data related to the position of the beam under study. As previously presented,

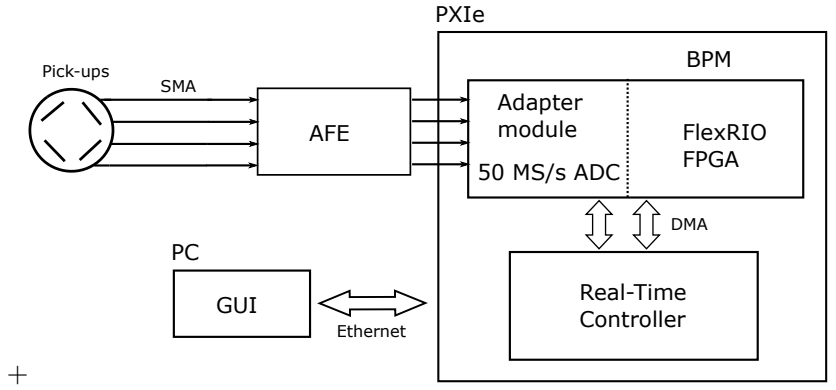

Figure 4.2. – Block diagram view of the BPM diagnostic application, from the capacitive pick-ups to the operator interface.

it its done digitally, although a basic analog treatment is required previous to the sampling of the signals.

Analog front-end (AFE)

The signals obtained from a BPM button usually have a low signal level. So, the voltage levels read from the picks are often slightly above the noise floor level. That is the reason why an analog signal conditioning is included in this work, even when the initial idea was to minimize the analog stages in the solution. It must be pointed out that this kind of subsystems are always required in a real application [6].

The signals produced by the BPM sensors are brought to an analog front-end (AFE) of four channels in which signals are conditioned through two amplification and one filtering stages. For amplification stage, two concatenated LMH6629 OPAMPs have been chosen, a low noise and high speed model from Texas Instruments. The main characteristics of each amplifier are a gain of 14 dB (or 5V/V) and a 900 MHz bandwidth.

In order to improve the signal to noise ratio after the amplification stages, a filtering stage is added. For this purpose four bandpass filters (centered at our work frequency of 352 MHz) from K&L Microwave have been used. A narrow band filter is critical to achieve a significant reduction of thermal noise. These filters have a 10 MHz bandwidth, which is a suitable value for the current system requirements.

The AFE stage is completed with a ECL15UD01-E power supply from XP

Power to feed the mentioned devices. The Figure 4.3 shows the rack box containing the amplification and filtering front-end.

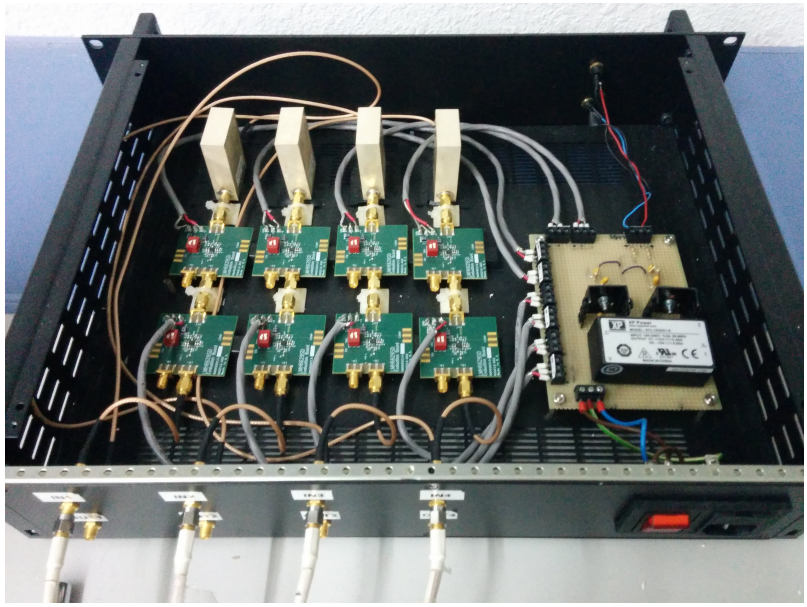

Figure 4.3. – Picture of the built analog front-end to amplify and filter the signals measured by the pick-ups.

Digital solution

The digital part of the developed BPM system, which is the core of the solution presented, begins with the discretization of the four output signals of the AFE and, after a digital treatment, it produces a bunch of essential measurements for the beam diagnostics that are displayed in a LabVIEW based graphic interface. In the next paragraphs, the main steps of this process are listed and explained:

- The four analog signal coming from the BPM pick-ups (and after been amplified and filtered in the AFE stage) are sampled by the FlexRIO 5761R ADCs. It uses two ADCs (ADS62P49 from Texas Instruments) per channel and provides a sampling rate of 250 MS/s with a wide bandwidth of 500MHz. It has a 14 bit precision and a dynamic range of 1.23V, which gives a resolution of 75μV.

- Those samples are acquired by the FlexRIO 7961R module powered by a Xilinx Virtex 5 FPGA. The most time-critical operations are handled in this stage, taking advantage of the true parallel processing of the FPGA technology. So, the code that needs to meet hard real-time constraints is implemented here, such as data packaging, FFT or DMA communication handling. The LabVIEW FPGA module allows to the developer the implementation of all the required code in a graphical LabVIEW environment avoiding the need of HDL, which eases and speeds up the deployment of the application. It also gives the option to configure some of the adapter module ADCs parameters using the SPI protocol. All the program inside the FPGA executes in a timed loop at a rate of 125 MHz, which contains a simple state machine defining the functionality. This way, every 8 ns a processed sample is ready to be sent to the controller side.

- The FPGA (which is referred as target in the PXIe architecture) and the PXIe 8108 controller (host) communicate and transfer data in both directions using DMA protocol. DMA transfers are accomplished using FIFO architecture. The FIFO is composed of two parts that behave as just one FIFO: the first one is on the FPGA side, and uses block RAM on the FPGA device. The second part of the DMA FIFO is on the host machine and uses the RAM memory of the host. The DMA engine automatically transfers data from the FPGA device RAM to the host machine memory.

- The host machine runs a Real Time LabVIEW (Pharlap) operative system. This part of the data acquisition system handles the communication with the operator (GUI) and performs the not so time critical operations. First of all, the host program configures some FPGA and DMA related parameters, corrects the offset seen by the ADCs, defines the length of the frame to acquire (number of samples) and the trigger to be used to control the acquisition in the FPGA. Then, inside a periodic loop, the deployed program sends a software trigger in each iteration (set at a 5ms rate), reads the data from the DMA, unpackages it, scales the values to real voltage values and performs all the desired data analysis: time domain graphs, averaged FFTs, noise parameters, beam position calculation through the signal processing method called detal-sigma (implementing Equations 4.1 and 4.2) and data logging. Besides, the host also handles the temperature acquisition performed by the PXI 6259 DAQ card through DAQMX

interface.

- All the programming tasks are carried out in a regular desktop PC that will behave as the development machine. This PC is connected to the PXIe via Ethernet in a LAN. The GUI created by the host in the PXIe controller is shown in this machine and contains controls that allow the operator to set many parameters as well as indicators that display all the relevant data and measurements of the system, as it is shown in Figure 4.4.

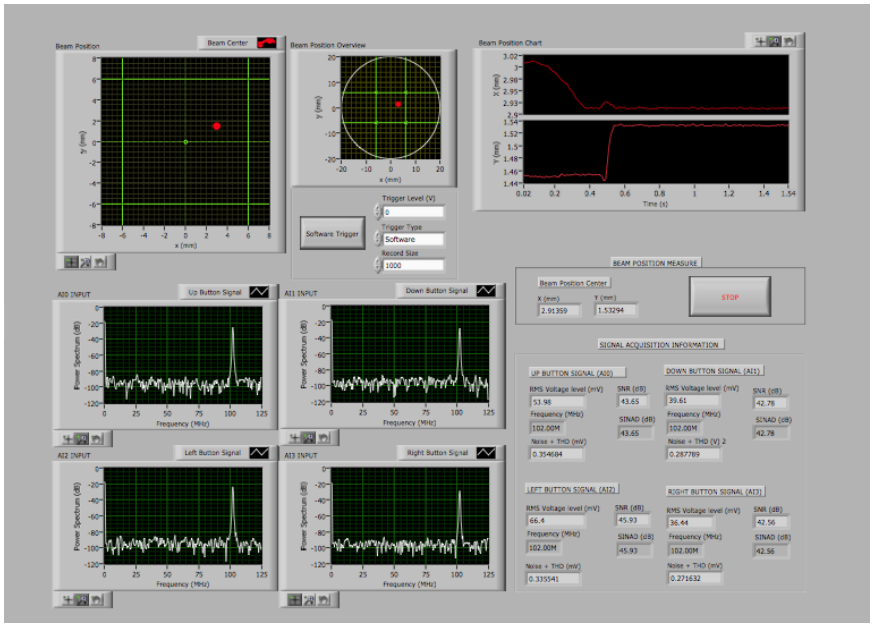

Figure 4.4. – A snapshot of the LabVIEW based graphic user interface show relevant data related to the beam position.

4.4. Test bench description

In order to test in the laboratory the digital BPM developed, a complete testbench has been designed and built by the RF and Microwave and Experimental Control groups of the UPV/EHU. This testbench consists in a main metallic structure built using parts under the CF standard of the UHV (Ultra-High Vacuum) technology (ISO/TS 3669-2:2007). Figure 4.5 shows the basic structure

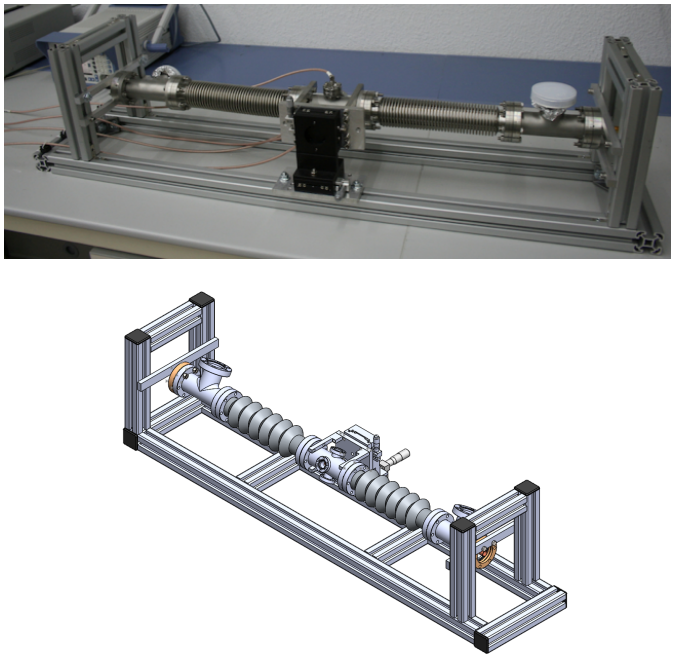

Figure 4.5. – Basic structure of the testbench for the BPM testing.

of the testbench. It consist of two T DN40 parts, two corrugated bellows and a central conductor pipe where the four sensors, the capacitive pick-ups, are placed crosswise.

The main parts of this structure are listed bellow:

- Two T DN40 parts. These are located at the edges of the structure and each one provides a port to connect a vacuum pump or pressure gauge.

- Two corrugated bellows connecting the T DN40 parts and the central element. This components provides the necessary flexibility to the structure when beam displacements are simulated.

- A central piece where the four sensors, the capacitive pick-ups (see Figure 4.6), are placed. This part has been designed by the research group so that the bottom flat surface of the capacitive sensor is tangent to the inside diameter of the vacuum beam pipe. Besides, it satisfies the size

Figure 4.6. – Picture of the used capacitive pick-up sensors. The metallic plate can be observed.

specifications of the CF 40 standard. This is physically the beam diagnostic device and has been designed to allow its use in a real acceleration facility. It can be unmounted and mounted again very easily. The model used in the design stages of of this part of the testbench as well as a lateral view of the built piece can be seen in Figure 4.7. Notice that the metallic plates of the pick-up sensors can be observed in the bottom picture.

- A 14 mm external diameter copper pipe. This acts as the central conductor of the BPM testbench, conducting the reference RF signal that simulates a particle beam. This pipe is placed concentrically to the DN40 pipes, the bellows and the central element. Its diameter has been chosen to get the best approach to a coaxial cable matched to 50 Ω, in relation to the diameter of the CF 40 components. The equivalent coaxial structure is described in Figure 4.8. The impedance of this coaxial cable is obtained from Equation 4.4 [8]. Being D_o the inner diameter of the outer conductor, D_i the diameter of the inner conductor and ε_r the relative permeability of the dielectric. In this particular case, the D_o is fixed to 38 mm, as specifies the CF 40 standard. So, for a $\varepsilon_r = 1$(air), the most suitable length for the copper conductor has been $D_i = 14\,mm$ (taking into account that not every diameter is available from vendors). With this parameters, a $Z_0 = 59\,\Omega$ is obtained.

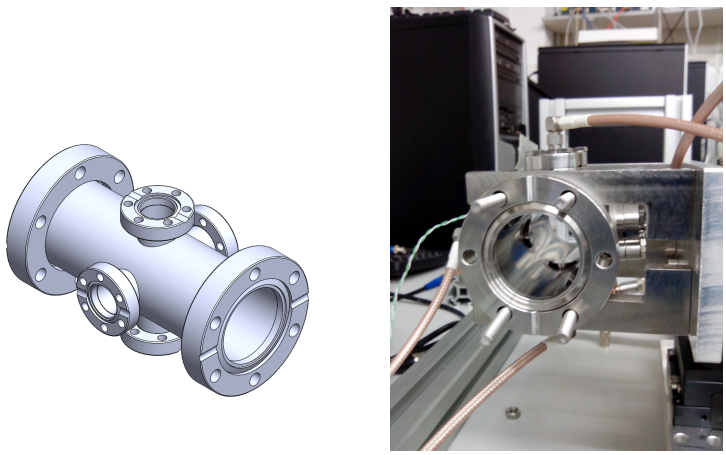

Figure 4.7. – The 3D model of the central element of the testbench (up) and the inner section of the built piece (down). It provides for openings placed crosswise to insert the electrostatic sensors, which can be seen in the bottom picture.

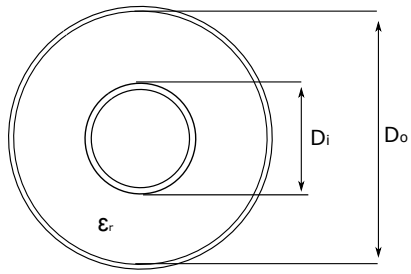

Figure 4.8. – Equivalent coaxial cable of the designed RF signal transmision structure.

$$Z_0 = 138 \cdot log_{10}\left(\left(\frac{D_o}{D_i}\right) \cdot \left(\frac{1}{\sqrt{\varepsilon_r}}\right)\right) \tag{4.4}$$

- A two-dimensional micrometric linear translation structure. This is attached to the central part and allows to transversely displace the pipe relative to the central conductor, which stays fixed. Taking as reference the central element, which supports the sensors, and moving it independently in X and Y axis, the movement of the particle beam is simulated. The linear displacement system uses two high precision manual positioning elements, the micro-platform model 66-436 (see Figure 4.9) from Edmund Optics, with 2µm of straight line accuracy and a linear range (travel) of 13 mm.

- A metallic structure that acts as support for the aforementioned elements.

Figure 4.9. – Micrometric linear translation platform employed to simulate beam deviation.

The input and the output of the conductor are connected using RF feedthroughs. The one in the input is connected to the RF signal that simulates the beam, while the output one is connected to a 50 Ω load. The reference RF signal is provided by a low phase and amplitude noise RF signal generator: the Agilent 8657A.

Besides from the basic structure and components of the BPM testbench that is described above, some improvements has been added. The first of them is

the installation of a high vacuum system. The goal of this is to obtain a more complete testbench, thus allowing tests in more realistic scenarios, including microphonic effects. A HiPace 80 turbopump from Pfeiffer has been used to achieve the required vacuum level. This is attached to the port of the T DN40 pipe in the side of the 50 Ω load. The turbopump is controlled by a HiCube 80 pumping station of the same vendor. The vacuum sensor is attached to the port of the T DN40 component located at the input of the testbench.

Another improvement of the testbench is related with the automation of the measurements. In order to perform the required measurements programmatically, two StepSyn 103H7123-0104 stepper motors have been added to the testbench. These motors are attached to the micrometric translation platform drives through a custom plastic non-rigid motor couplers, that have been designed and created by the research group using a 3D printer.

4.5. Experimental results

Several test and experiments have been carried out to characterize the whole system from the input of the BPM test bench to the digital post-processing. One of the main goals of the experiment was to achieve the maximum possible accuracy in the measurements and to identify each source of errors and its contribution to the results.

The experiments performed and results obtained are described in the next sections.

4.5.1. Input power range testing

For measuring the quality of the signals acquired, the SIgnal to Noise And Distortion ratio (SINAD) measure is used, since it takes into account the noise plus distortion. It is straightforward that better quality of acquired signals leads to better precision of the position measurements. For that reason, the SINAD is a key factor to observe and optimize the signal acquisition subsystem.

On the one hand, if the input power feeding the amplifiers is too low, the position measure are very poor. On the other hand, if the input power is too high an additional nonlinearity is added to the position measure, derived from the anplifier nonlinearities. Consequently, for testing purposes, an input power is chosen in such a way that good levels of SINAD are achieved, working the amplifiers in a linear zone. Regarding this factors, the input power level has been set to -5 dBm (RF signal generator power), leading to above -16 dBm for

the ADC´s inputs.

4.5.2. Gain calibration and correction

Each AFE channel presents a slightly different gain because of different paths and different gains of amplifiers. This will cause an error in the position reading. For this reason, the gain differences of AEF channels are characterized and corrected in software. These gain differences around the working point are shown in Figure 4.10.

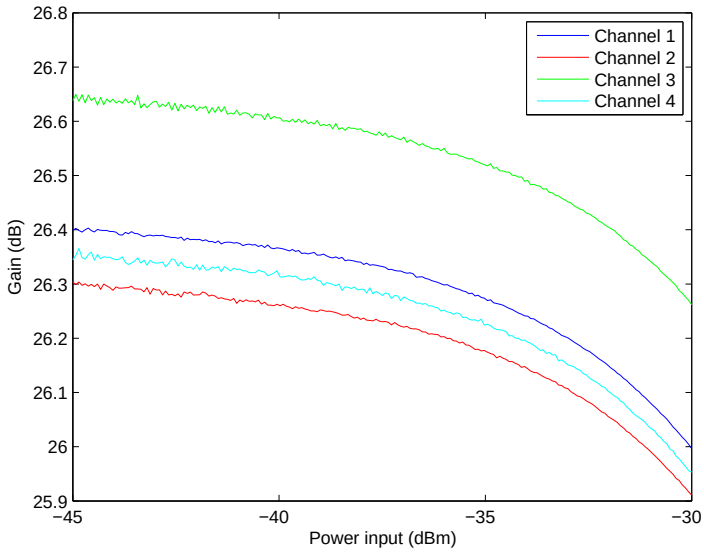

Figure 4.10. – Gain obtained from the amplification stages in a given range of input levels.

4.5.3. Sensitivity coefficient and offset calculation

The sensitivity coefficients and offset parameters of the beam position equations are obtained from a linear regression with the micrometric system positions (mm) as independent variables and the normalized signal difference (%) as dependent variables. For the calculation of S_x and δ_x, several equidistant measurements are made along the horizontal axis, from (x,y)=(-3mm,0) to

(x,y)=(+3mm,0). The same procedure is repeated (changing the moving axis) to obtain S_y and δ_y. The results are:

$$\frac{1}{S_x} = K_x = 10.02 \pm 0.049\, mm/\%$$

$$\frac{1}{S_y} = K_y = 10.07 \pm 0.039\, mm/\%$$

$$\delta_x = -0.46 \pm 0.01\, mm$$

$$\delta_y = -0.45 \pm 0.01\, mm$$

4.5.4. Accuracy in the position measurement

As described in Equations 4.1 and 4.2, the particles center of mass, that is, the beam position, is calculated from the voltage levels read from the BPM sensors. To obtain the voltage level, the root mean square (RMS) value calculation of 2048 signal samples is performed. In order to minimize the statistical error, the RMS values obtained are averaged, because it is a good method to obtain more accurate positions (for white noise).Of course, it takes more time to calculate each position, and an over-averaging could make the time delay between measured positions unacceptable. Typical values for averaged readings are from 10 to 1000 ms [3]. As the data processing real-time loop in the host PXI executes every 5ms, the maximum acceptable number of averages considered is 200.

In this experiment, a near-to-center position is chosen, and several measurements are made. The tests are performed for N=1, 10 and 100 averages in a centered position and a given input power of 0 dBm. The results are shown in Table 4.2 and Figure 4.11.

Number of averages	std dev x(μm)	std dev y(μm)
1	2.02	1.89
10	0.61	0.62
100	0.20	0.19

Table 4.2. – Standard deviation of position calculation in both orthogonal axis depending on amount of averages performed.

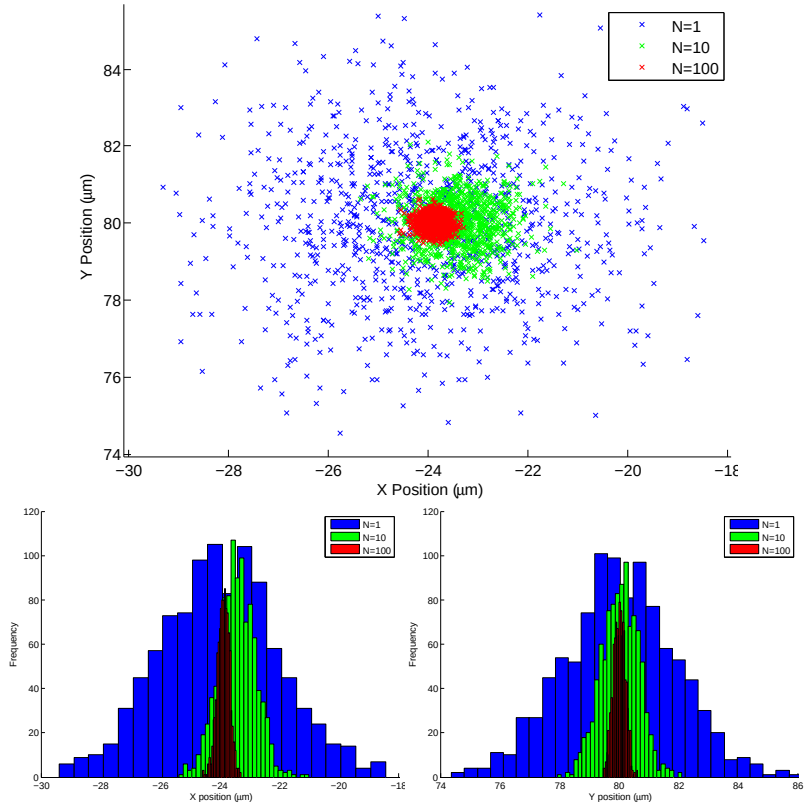

Figure 4.11. – Standard deviation of the position measurements in both axis at the same time (up) and separately (down) in order to calculate the position accuracy.

As expected from the statistical properties of the measured signals, considering white noise, the standard deviation of the measured position decreases by $1/\sqrt{N}$ [10] being N the number of averaged RMS values.

Regarding this results, it was decided to set initially the number of averages to N=10 for being used in the experimental tests, which is a good compromise between accuracy on the position and time lapses between readings.

4.5.5. Linear positioning system accuracy

With the aim of identifying all the contributions to the final measurement's error when simulating the beam movement, the 2D micrometer linear translation system which moves the BPM block is tested. The linear positioning system

has a ±2µm uncertainty from manufacturer's specification. We must obtain the uncertainty added by other elements to our measurements, apart from the value given for the linear positioning system.

The procedure is to check the repeatability of the readings every time a position is set manually. For this experiment, the number of averages is set to a very high value (N=200) to minimize the contribution of the acquisition system to the uncertainty of the measurements. The chosen method is to fix a position and make a single reading at that point. Then, the positioning platform is moved to a new position in one axis and returned again to the starting one to take another sample. This step is repeated 250 times. The results obtained can be seen in Figure 4.12. The errors in both directions given by the standard deviation are shown in Table 4.3 (as well as the maximum errors). Regarding the results obtained, it can be concluded that the maximum distance between points read is no higher than the 2µm uncertainty, for a given set of stable conditions (constant temperature, warmed electronics, ...). So the contribution to the positioning measurement error will be that coming from the linear positioning system setup itself.

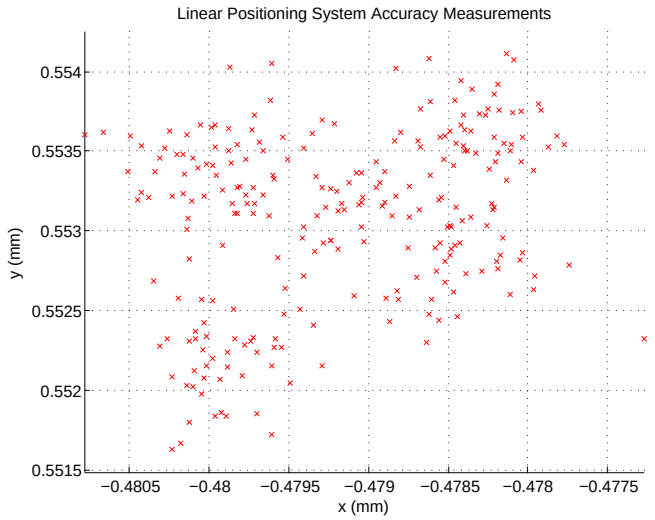

Figure 4.12. – Result of the measurements performed following the methodology described to find the linear positioning system accuracy.

	std_dev (µm)	max_error (µm)
X direction	0.7788	3.5117
Y direction	0.5570	2.4817

Table 4.3. – Error and maximum error in both axis measurements of consecutive measurements of a single point.

4.5.6. Long term position stability (LTPS)

When making regular readings in long time periods, variations in position measurements are expected, mainly related to temperature drifts or material dilatation. To observe this long term stability, periodic measures are taken at regular interval of minutes for a long time (several hours or even days).

A first long experiment measurement in a fixed position is preformed monitoring X and Y beam positions and room temperature (see Figure 4.13) for two days. Significant drifts in beam position and room temperature are observed. Temperature drift is caused by day/night cycles and the consequent temperature change. In order to study if the position drifts are caused by temperature drifts, the rank correlation is calculated, obtaining a coefficient of 0.3618 for the horizontal direction and 0.3325 for the vertical direction. The thermal effect contribution could be corrected through the position temperature coefficient, defined as the slope of the position drift with the temperature [9]. This way, a software numeric correction based on the measured room temperature should improve the LTPS.

4.5.7. Position map

In order to characterise the non-linearities in positions distant from the center, a 13x13 point matrix-shaped sweep is done. A significant deviation from linearity starts at about ¼ of the beam pipe radius [3]. In our case this would be at about 4 mm from the center considering that the travel of the positioning system is 13 mm. This agrees with the experimental results obtained and shown in the left side of Figure 4.14.

It can be observed that for positions further than 4 mm the nonlinearities decrease the accuracy significantly. Although for most applications only the central part is of interest, it is necessary to add numerical corrections, in order to get needed accuracy.

So, a polynomial fit based on Horner's method [1] has been performed in order to linearize the measured positions. Fifth order polynomials have been used to

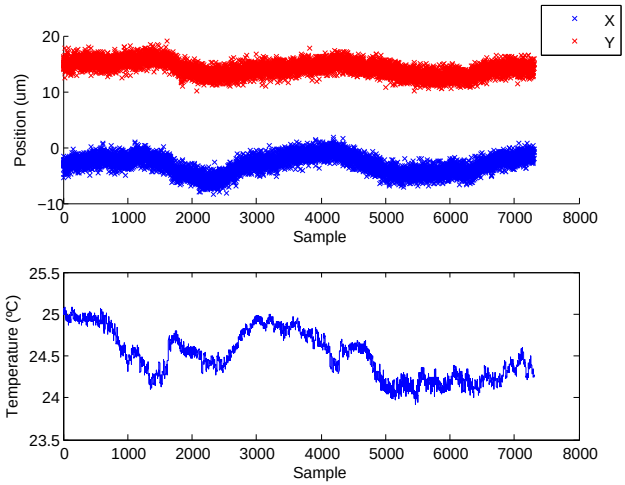

Figure 4.13. – A long term position measurement in X and Y direction versus temperature reading.

fit the measured points to the theoretical positions. Applying this corrections, the position map shown in the right picture of Figure 4.14 is obtained.

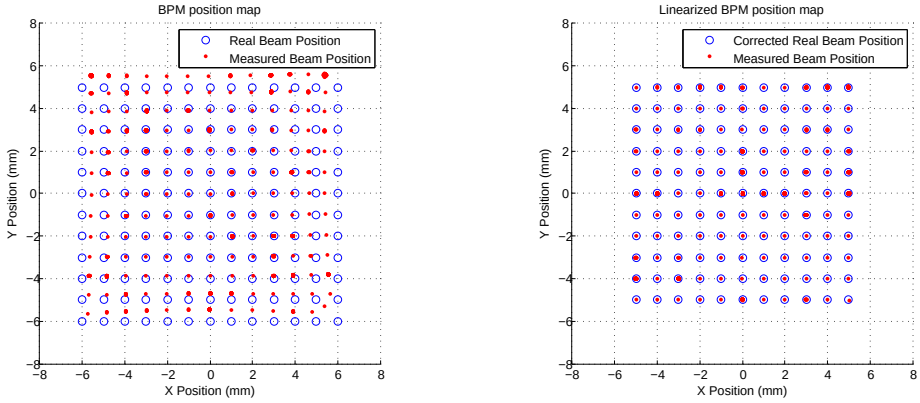

Figure 4.14. – Position map performed in the maximum area allowed by the positioning system and facing the theoretical beam position and the measured position (left) and position map with the measured positions linearized using a polinomial fit (right).

4.6. Summary and conclusions

In the current chapter, a complete and compact BPM diagnostics for particle accelerators is presented. The proposed system has been conceived as a flexible and easily reconfigurable solution, particularly suitable for laboratory testing and research tasks.

The system includes a capacitive effect based pick-up BPM diagnostic, an analog front end for signal conditioning and a fast DAQ system based on PXI architecture and FlexRIO modules. This hardware solution along with undersampling technique allows to efficiently sample the high frequency signals typically used in light ion accelerators, usually in range of hundreds of MHz.

To test the design, a complete testbench has been implemented, allowing a large variety of experiments. From the results obtained after several different experiments, it can be concluded that the presented solution for a compact BPM diagnostics constitutes an accurate solution for beam position monitoring in particle accelerators.

Finally, the next future steps are mainly focused on three directions: first, the correction of measured data affected by temperature drifts and the non-linearities due to far-from-center positions; second, the implementation of a high-vacuum system for the BPM; and third, the use of a more realistic input signal to simulate the beam in a more real particle accelerator environment.

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CHAPTER 5

PXIe-based LLRF architecture and versatile test bench for heavy ion linear acceleration

RF systems are essential parts of particle accelerators. They are responsible for particle acceleration by transforming electrical energy into energy transferred to a beam of particles. Resonant cavities play a central role in this process, since the energy transference is mainly performed in these mechanical structures. These RF systems require a fast and accurate control system in order to keep the phase and amplitude of the gap RF field within the required values. In addition, the control system maintains the resonance frequency of the cavity as stable as possible. This RF control is known as Low-Level RF system.

This chapter deals with the design and implementation of a highly flexible and modular digital LLRF system and its integration to a complete testbench.

5.1. Introduction

The subject matter of this chapter is the description of a digital LLRF system for heavy-ion acceleration developed under the specification of the projected future heavy-ion accelerator facility in Huelva, Spain[1]. A prototype LLRF test bench operating at 79.59 MHz in Continuous Wave (CW) mode has been designed and built. The core LLRF control has been digitally implemented on a PXIe chassis , including an FPGA for digital signal processing and a real time controller. This PXIe platform was purchased from National Instruments. The test bench is completed with a low phase and amplitude noise signal generator used as master frequency reference, an analog front end for reference modulation and signal conditioning, some RF components completing the circuit, and, finally, a tunable resonant cavity at 79.59 MHz, whose RF amplitude, phase and frequency are real-time controlled and monitored.

As mentioned before, the LLRF system presented is mainly digitally implemented, and is based on IQ modulation and demodulation. The system can be configured to use both direct sampling and undersampling techniques, thereby making possible to build a more cost-effective solution, depending on the requirements. All this results in a high performance and versatility RF control system. All the system is programmed using the LabVIEW environment, which makes the prototyping process and its reconfigurability much easier.

Area of the project work

This project was designed to develop a LLRF prototype system for a projected future heavy-ion linear accelerator. The research groups of Automatic Control (GAUDEE) and the RF and Microwave group of the department of Electricity and Electronics of the University of the Basque Country (UPV/EHU) have developed a whole testbench, with the aim of testing all the specifications in a systematic way. The main goal has been to build a fast LLRF control system capable of keeping stable the RF field in the cavity, within 1% in amplitude and 1^{o} in phase for proper operation, as well as building a flexible and reconfigurable digital solution suitable for testing new techniques and ideas for LLRF systems.

The solution proposed has been mainly implemented based on FPGA technology, which provides high throughput in data processing, along with high speed digitizers required to acquire RF signals. The feedback control loop implemented uses a I/Q modulation technique, allowing to control the desired

[1]This project is not active in this moment

variables without dealing with the RF signals directly, thus saving computational resources. Taking advantage of digital implementation, different control architectures and strategies have been carried out and obtained results studied.

5.2. LLRF Control system: Proposed Solution

The LLRF control system developed has been conceived to be a highly scalable, flexible and reconfigurable structure. This idea has lead to the design of a system based mainly on a digital solution, thus allowing to introduce substantial changes in the implemented scheme in order to add or modify functionalities simply changing the program's code. This possibility is a very valuable advantage when prototyping, as it reduces the implementation time and brings the opportunity to meet new project requirements.

This way, one of the main goals of the solution proposed has been to avoid the use of analog electronics as much as possible. This presents a major challenge when working with RF signals in the range of few hundreds of MHz. Many LLRF designs [14] use an analog front end to downconvert the incoming RF signal to an IF signal. This is done by mixing the input RF signal with an adequate frequency local oscillator and by low pass filtering the output. This type of solution has shown its validity and has been applied in different projects like [10, 3, 12, 1].

This work proposes to directly sample the RF signals, without any intermediate stage between the input and the ADCs, similar as proposed in [5]. This allows the use of a simplified analog front-end.

To direct sample high frequency signal meeting the Nyquist criteria would require high throughput ADCs, since the discretizers need to work at a rate at least twice as fast as the original signal frequency. In control applications, the margin is usually larger, being the usual to use speeds ten times higher than the target signal. Working in the range of dozens even hundreds of MHz could require technology close to the present state of the art [2]. In any case, the equipment-cost becomes expensive.

Regarding this and considering that another goal of the current work is to develop a cost-effective solution, the solution proposed is based on the advanced sampling technique presented in Chapter 3, known as undersampling. The discretization of RF signals with the undersampling technique has allowed to use lower sampling rate ADCs and, consequently, to reduce the system budget.

Summarizing, the starting point for the LLRF system design has been the development of a mainly digital modular system, which allows the use of

undersampling techniques. Additionally, high throughput technology is required in order to develop the signal processing, control structures and to be able to close the control loop within the required specifications of typical heavy-ion accelerators. On the other hand, a powerful and flexible development environment is needed to integrate the necessary hardware and to ease the programming tasks.

Considering the requirements, the National Instruments PXIe platform has been chosen as the core to develop the LLRF solution. The hardware environment is described in detail in Chapter 3. It provides a wide variety of modules for signal acquisition, generation, timing, etc., integrating FPGA technology and a chassis to interconnect them. An important advantage of working with this architecture is that the whole system is operated in a LabVIEW environment. This is an important advantage since it allows to easily integrate a wide catalog of hardware devices, reducing the effort of complex tasks like driver development, peer-to-peer streaming or DMA transfers. The use of LabVIEW also facilitates and speeds up the development of monitor and control structures thanks to the provided programming tools.

To obtain the highest troughput and the widest bandwidth in the feedback loops (specially in the phase and amplitude loop), FPGA technology based cards have been used. The PXIe FlexRIO series of National Instruments provides flexible, customizable I/O and FPGA technology oriented to perform onboard proccesing and real-time applications. The possibility of graphically programming FPGAs using LabVIEW code must be highlighted, avoiding the use of long and complex HDL coding which would prevent rapid prototyping.

In order to develop the necessary fast feedback loops, an RF demodulation technique known as In-phase and Quadrature (IQ) demodulation have been performed [18]. The conversion of the RF signal into I/Q baseband components allows to directly manipulate the amplitude and phase without handling the discretized carrier signal directly, reducing the jitter derived computational problems. It is also advantageous because the symmetry of the I/Q signals [16]. A more detailed description of the modulation/demodulation technique implemented is given in the next subsections. This scheme allows to control both phase and amplitude in a single feedback loop but using separate and independent controllers for both I and Q components [7].

Performing a feedback loop of IQ components requires an IQ modulation to re-create the controlled RF signal that is used as the signal input of the cavity. Two different approaches can be followed to do this. The first one is based on performing the IQ modulation digitally in the FPGA card and generating

the RF signal using a generating adapter module. The second one consists of generating the controlled I and Q baseband components and using an analog quadrature modulator to build the RF which feeds the plant.

This works proposes to use the second approach, despite have been said that one of the goals of the project was to minimize the analog stage usage in the LLRF solution. The reason is that quadrature modulators are fed with the reference RF signal of the system, which comes from the master oscillator present in every accelerating line. This means that the modulated RF carrier signal will inherit the quality of the reference signal of the master oscillator in terms of stability, frequency, phase and amplitude noise. Obtaining such high accuracy carrier signal digitally can be complicated.

The schemetic representation of the designed LLRF system, including each required feedback loop and variables, as well as the main experimental setup with every element is described in Figure 5.1.

So, this work is divided in two main parts. On the one hand, the development of a LLRF control system to regulate the amplitude and phase of the accelerating fields as well as the resonance frequency of the tunable cavity. On the other, the design and setup of a complete testbench, basically a resonant cavity, to validate the LLRF control system in the laboratory. This two parts are deeply described in the following sections of this chapter.

5.3. LLRF control system developed

This section is devoted to the design and development of a digital LLRF control system, including the description of the hardware used and digital processing techniques. As seen in Chapter 2, a typical LLRF control system usually consists of a fast loop to regulate the amplitude and the phase of the accelerating signal as seen by the particles, and one slower loop to tune the resonant frequency of the accelerating cavities. Both have been digitally implemented based on the National Instruments PXIe platform.

5.3.1. Description of the technology used

In this section, a brief description of the technology used is given. The main elements are: a PXIe chassis, FlexRIO modules, a Quadrature modulator and the LabVIEW development environment.

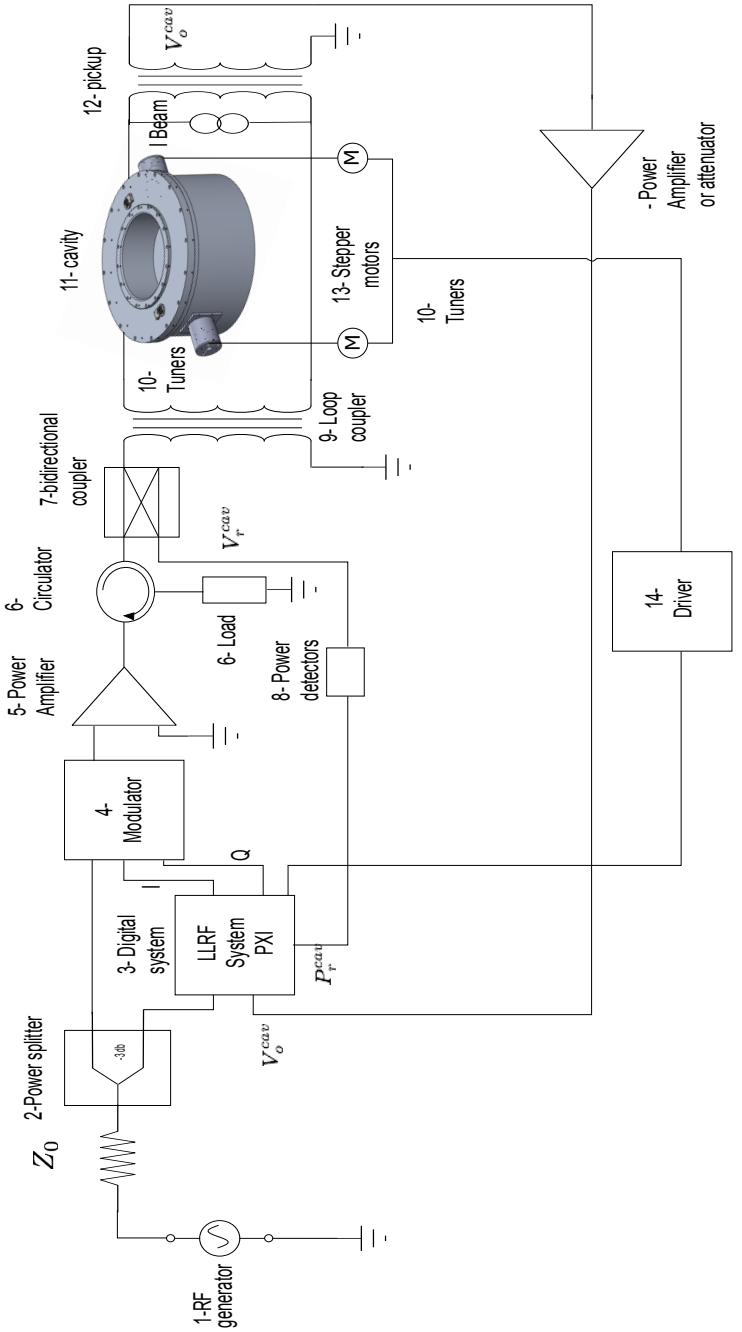

Figure 5.1. – Basic description of the LLRF system and the experimental setup.

	NI PXIe-7961R	NI PXIe-7966R
FPGA	Virtex-5 SX50T	Virtex-5 SX95T
DMA channels	16	16
Embedded RAM	594 KB	512 MB
FPGA slices	8160	14720
DSP slices	288	64

	NI 5751R	NI 5761R	AT-1212
Function	Acquisition	Acquisition	Generation
ADC/DAC rate	50 MS/s	250 MS/s	1.25 GS/s
Nº of channels	16	4 (single-ended)	2 (differential)
Resolution	14 bits	14 bits	14 bits

Table 5.1. – Main features of used FlexRIO modules and adapter modules.

PXIe chassis. The core of the presented implementation is an 8 slot NI 1082 PXIe chassis. It provides a robust structure for building digital solutions. Two different embedded controller modules have been used, each one fitting the requirements of the two approaches that will be discussed later on: a NI PXIe 8108 RT controller, running LabVIEW Real-Time operating system and a NI PXIe-8135 embedded controller running Windows 7.

FlexRIO card and adapter modules. For the current work, two different FlexRIO FPGA cards has been used, corresponding to models NI PXIe 7961R (introduced in Chapter 3) and NI PXIe 7966R. The adapter modules chosen for the acquisition tasks have been the NI PXIe 5751R with an ADC up to 50MS/s and the NI PXIe 5761R (also presented in Chapter 3) with an ADC up to 250MS/s, while the adapter module in charge of signal generation has been the AT-1212 at 1.25 GS/s. The main features of the mentioned modules are listed in Table 5.1.

Additional cards. For not so demanding tasks, lower throughput multifunction cards have been also used. More concretely, a NI PXI 6259 multifunction DAQ card and a NI PXI 7852R multifunction FPGA card. Both are operated along with a NI SCB-68 connector pane.

ADL5385 Quadrature Modulator. The ADL5385 from Analog Devices, Inc. is a silicon based, monolithic, quadrature modulator designed for use from 30 MHz to 2200 MHz. It provides high phase accuracy and amplitude balance.

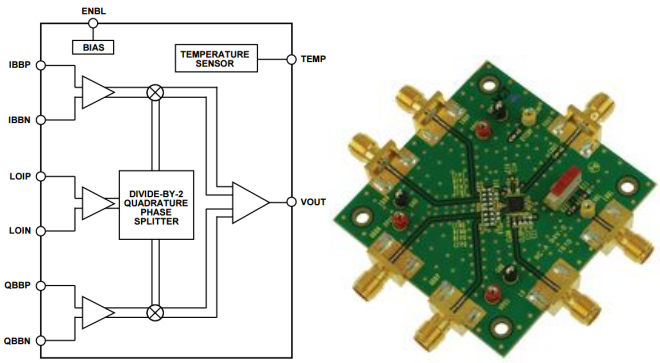

Figure 5.2. – Block diagram of the ADL5385 quadrature modulator and a picture of the physical device

The AD5385 takes the signals from two differential I and Q baseband inputs and modulates them into two carriers in quadrature with each other. The two internal carriers are derived from a single-ended, external local oscillator input signal at twice the frequency of the desired carrier output. The two modulated signals are summed together in a differential-to-single-ended amplifier designed to drive 50 Ω loads. A block diagram of the ADL5385 quadrature modulator and a picture of it can be found in Figure 5.2.

LabVIEW. A detailed description of LabVIEW is presented in Chapter 3. This work has been carried out under version 2012 SP1 of LabVIEW. An intensive use of the FPGA module of LabVIEW must be highlighted, as it has provided the required tools to develop all the necessary FPGA code.

5.3.2. Sampling technique performed: subsampling

In order to sample the required RF signals, the advanced sampling technique studied in Chapter 3 known as undersampling has been performed.

The nominal frequency given in the specifications of the project is around 80 Mhz. However, as the cavity used for testing purposes (described in next section) has a resonance frequency of 79.59 MHz, the LLRF system has been designed to work at this frequency (79.59 MHz), and a suitable sampling frequency must be chosen. On the one hand, the NI PXI 5761R adapter module can perform a digitalization at a maximum rate of 250 MS/s, speed that allows to satisfy the Nyquist criteria. On the other, the NI 5751R has a 50 MS/s ADC, which

forces to perform subsampling. Regarding the upper and lower limits from the Equation 5.1 obatined in Chapter 3 and assuming that the 79.59 MHz signals to be sampled (both reference signal and cavity output) have a small bandwidth compared to the carrier frequency and for a $m = 3$, this rate of 50MS/s proves to be a suitable sampling frequency:

$$\frac{2f_c - BW}{m} \geq f_s \geq \frac{2f_c + BW}{m+1} \tag{5.1}$$

$$53.05\ MHz \geq 50\ MHz \geq 39.80\ MHz$$

Discretizing the original signal of 79.59 MHz at this sampling rate, the alias located at 20.41 MHz signal is obtained as stated in expression $(f_0 + mf_s)$ from Chapter 3. Note that spectral inversion occurs. As described in the mentioned chapter, this occurs when m is an even number (3 in this case). It must be remarked that as a pure sinusoid has been employed, the original positive spectral bandpass components are symetrical about the f_{center} and therefore spectral inversion causes no problem.

5.3.3. Digital processing techniques performed: IQ demodulation

I/Q data is a signal representation alternative to the classic one which consists of a series of samples of the momentary amplitude of the signal. I/Q data shows the changes in magnitude (or amplitude) and phase of a sine wave. If amplitude and phase changes occur in an orderly, predetermined fashion, you can use these amplitude and phase changes to encode information into a sine wave. This process is know as modulation. The demodulation process is just the opposite, to decode the amplitude and phase information of a sine wave in two parameters.

A given sinusoidal signal $x(t)$ with a given amplitude A, frequency ω and phase φ , can be represented into its in-phase (I) and quadrature (Q) components:

$$x(t) = Asin(\omega t + \varphi) = Acos(\varphi)sin(\omega t) + Asin(\varphi)cos(\omega t) \tag{5.2}$$

Defining,

$$I = Acos(\varphi) \tag{5.3}$$
$$Q = Asin(\varphi) \tag{5.4}$$

Equation (5.2) results in

$$x(t) = I \cdot sin(\omega t) + Q \cdot cos(\omega t) \tag{5.5}$$

This way, the amplitude and phase of the signal can be expressed in terms of I and Q :

$$A = \sqrt{I^2 + Q^2} \tag{5.6}$$
$$\varphi = atan(\frac{Q}{I}) \tag{5.7}$$

This notation of the I/Q data sample is known as the polar form. It can be easily represented in the polar coordinate system as shown in Figure 5.3, where the instantaneous sine wave state is presented. Here, the distance from the origin to the black point represents the amplitude (magnitude) of the sine wave, and the angle from the horizontal axis to the line represents the phase. Thus, the distance from the origin to the point remains the same as long as the amplitude of the sine wave is not changing (modulating). The phase of the point changes according to the current state of the sine wave.

I/Q data can be also given in rectangular or Cartesian form. It can be viewed as positions in a coordinate system. I and Q are the x and y axis respectively. This notation can be represented in different ways:

- As two separate variables: I and Q
- As a vector of length two: (I,Q)
- As a complex number I + Qi

The quadrature demodulation process of an RF signal can be illustrated as shown in the Figure 5.4. It consists of mixing the RF signal with a local oscillator of the same frequency. Note that a cosine is just a sine with a phase shift of

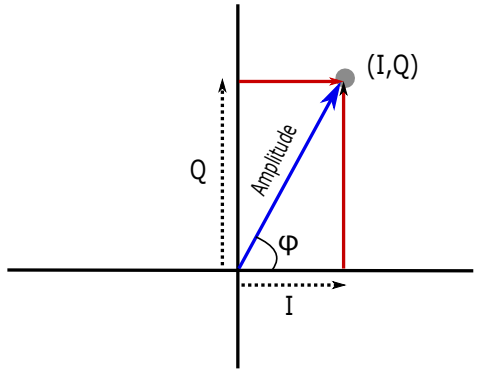

Figure 5.3. – Polar coordinate system representation of I/Q data

90º, that is way the signal carrier of the local oscilator is shifted before the mixing operation in order to get the Q component.When two signals enter an RF mixer and are mixed together, new signals are seen at frequencies that are the sum and difference of the two input signals, i.e. if the two input frequencies are f1 and f2, then new signals are seen at frequencies of $(f_1 + f_2)$ and $(f_1 - f_2)$. Being $f_1 = f_2$ in this case, the produced signal will have a component in $2f_1$ and in DC. Thus, multiplying the Equation (5.5) by cos(ωt)

$$\begin{aligned} x'(t) &= x(t)\cos(\omega t) = I\cos(\omega t)\cos(\omega t) + Q\sin(\omega t)\cos(\omega t) \\ &= \frac{1}{2}I + \frac{1}{2}I\cos(2\omega t) + \frac{1}{2}Q\sin(2\omega t) \end{aligned}$$

At this point, a narrow low pass filter must be applied at the output of the mixers in order to filter the high frequency component 2ω and obtain the baseband components, that is, I and Q.

5.3.4. LLRF control system design

The Figure 5.5 represents a simplified schematic of the feedback loop of the LLRF system proposed. The digital solution for both phase and amplitude and frequency tuning loops consists of three inputs and three outputs. These inputs are:

- The reference signal from a RF generator. A low phase-and-amplitude-noise RF signal generator was used to act as the master oscillator of the

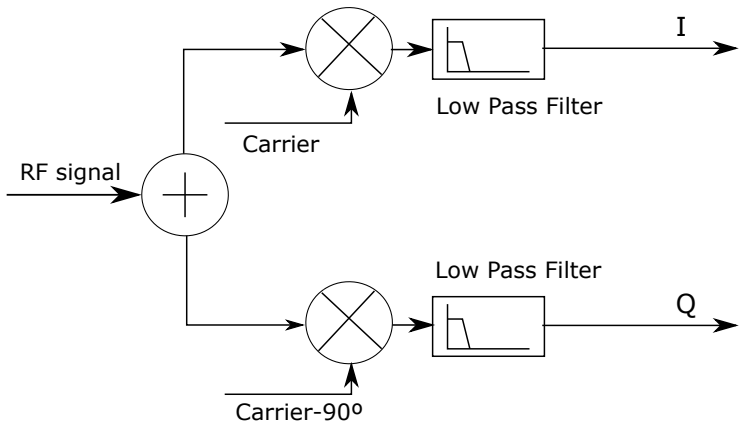

Figure 5.4. – Schematic demodulation process of an RF signal

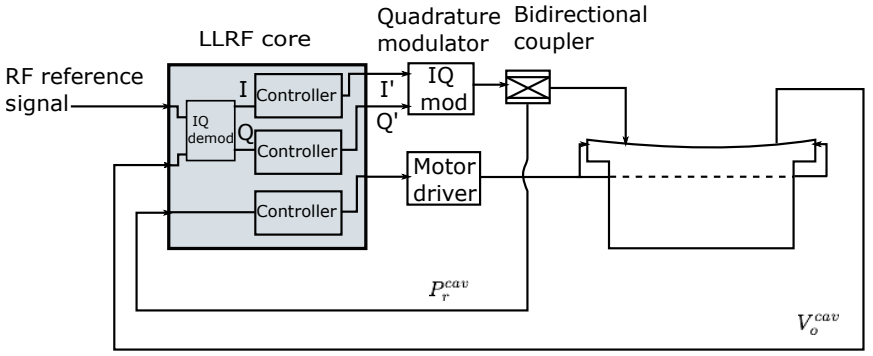

Figure 5.5. – Block description of the feedback loop of the digital LLRF system and its main input and output signals

system. It feeds the system with a pure sinusoid signal at the desired frequency of 79.59 MHz.

- V_o^{cav}, a voltage sample of the RF fields of the resonant cavity. This is extracted from the cavity through a coupled pickup, and acts as the feedback signal for the phase and amplitude loops. In addition, this signal can be used to measure the phase difference introduced by the cavity, and, thus, as feedback signal in the frequency tuning loop.

- P_r^{cav}, the reflected signal's DC voltage of the power level at the cavity input, V_r^{cav}. V_r^{cav} is measured using a bidirectional coupler located at the input port of the cavity. Performing a DC power detection over this signal, P_r^{cav} is obtained and can be used as feedback signal for the frequency tuning loop. If the cavity is operating at its nominal resonance frequency, the transmitted signal power is maximum, and hence, the reflected coupled signal minimum. Following this criteria, a control loop to keep the reflected power minimized is built in order to keep the resonance frequency matched at the desired value.

And outputs:

- I' in-phase baseband component. This value is the output of LLRF control for the phase and amplitude loop.

- Q' quadrature component. In the same way as the I component, Q' is the control value of the Q demodulated component obtained from the acquired V_o^{cav}. Together with I', they encode the control information for the desired amplitude and phase. They both are used as inputs in a quadrature vector modulator that will modulate the local oscillator RF carrier signal with the controlled phase and amplitude values. This modulated signal is injected back to the cavity.

- Motor control. This composed signal consists of two digital lines used to control the driver of a stepper motor. The first one controls the step number to be moved and the second one the rotation direction. The stepper motor moves mechanical tuners which change the geometry and, thus, the resonance frequency of the cavity.

The reference RF signal used is obtained from a RF signal generator, which acts as the Master oscillator in the current implementation. It is around $80\,MHz$

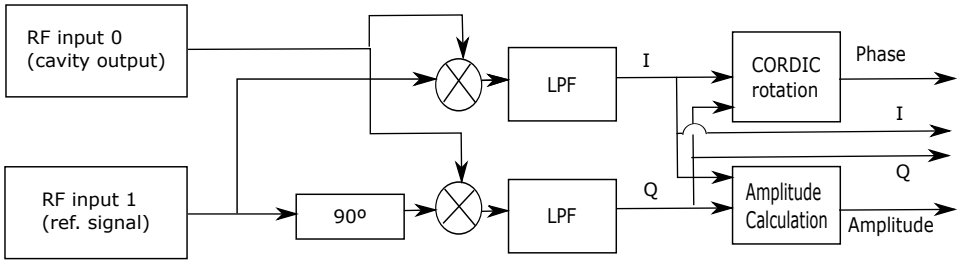

Figure 5.6. – I/Q demodulation and phase and amplitude detection in the FPGA

signal, which is the nominal resonance frequency given in the specifications of the project.

The core of the presented implementation is an 8 slot NI 1082 PXIe chassis. Different configurations have been designed and tested, depending on the pursued goals, each one involving different modules and cards. One again, the flexible and modular nature of the PXIe architecture have provided the opportunity to quickly reconfigure the built solution to add or exchange hardware modules as needs change.

The next sections lists and describes the details of the solutions implemented, first focusing on the amplitude and phase loop and, then, on the cavity's frequency tuning loop.

5.3.5. Phase and Amplitude feedback control loop implementation

Working with the proposed PXIe architecture, the control structures and the signal processing can be implemented in both the real-time controller and the FPGA cards. Implementing all the functionalities purely in the FPGA, faster loop rates can be obtained, leading to higher bandwidths. The disadvantage of this solution is a more complex and slower design and prototyping process.

On the other hand, the use of the real-time controller in combination with the FPGAs, leads to a much more flexible and fast design due to the long compilation times and the limitation of working with fixed-point arithmetic of the FPGA code. But, with this methodology, a significant reduction of the system bandwidth is obtained.

So, at this point, two models are proposed in order to develop the control loops of the LLRF system: the first one closes the loop over the real-time controller, and the second one uses exclusively FlexRIO FPGA cards. With the

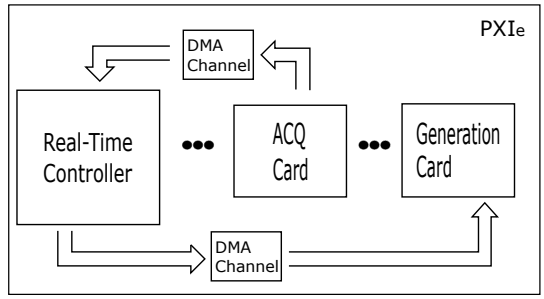

Figure 5.7. – Schematic description of the data communication flow between hardware parts in the real-time controller based approach

first approach, the tests and validation of the studied schemes are performed easily. With the second one, the implementation of the validated algorithms provides a useful control bandwidth, valid for final applications.

From the point of view of the implementation of the control, the greatest challenge of the phase and amplitude loops is to be able to close the control loops in the minimum amount of time possible, thus obtaining the best possible bandwidth. Most of the efforts performed in this solution have been focused around this constraint, as well as the main problems faced.

5.3.5.1. Real-time controller based approach

In order to get the desired agility in the design process, the implementation of the phase and amplitude loop is separated in two parts: the FPGA part and the real-time controller part.

In this approach, three devices are used under the PXIe platform to close the phase and amplitude loop. Two of them are FPGA based cards. One is in charge of the data acquisition tasks and the second one generates the I and Q controlled signals that are used to modulate the RF carrier signal in the vector modulator. The third part is the real-time controller, where the main control structure is implemented. Below, their main characteristics and tasks to perform are listed:

- Acquisition card: A FlexRIO family card which acquires the cavity's output V_o^{cav} and the reference signal from the RF generator. Taking advantage of the computational power and speed provided by the FPGA, time-critical operations such as I/Q demodulation and phase and ampli-

tude detection are performed here.

- A Real-time controller in charge of the not so time-critical signal processing, control actions and monitoring. A more detailed description of the implemented design is given in the following paragraphs.

- Generating card: As the variables to generate are baseband components, no RF signal generator cards are needed. So, a multifunction FPGA is used to generate the corrected I'/Q' values.

To build the scheme described, a PXIe 8108 RT embedded controller has been chosen, running the LabVIEW Real-Time operating system.

For the data acquisition, a high throughput NI FlexRIO 7961R card has been used, along with its respective adapter module. In this case, a NI 5751R adapter module has been mounted, which includes an ADC up to 50 MS/s together with sixteen analog input channels.

Implementation of the data processing and control structure

As mentioned before the NI 7961R FlexRIO card along with the NI 5751R adapter module is in charge of the digitalization of the analog RF signals and the high priority data processing, more specifically, the signal conditioning and the IQ demodulation.

- Signal conditioning: this stage consists of three operations:
  - Word lenght adjustment: the ADC produces a 14 bit word in a 16 bit signed integer. So, a two position bit shift is performed, which is equivalent to multiply by four.
  - Dynamic range adjustment: the 16 bit value is scaled to the dynamic range of the ADC.
  - Offset adjustment: the ADC produces a discretized signal with a slight DC offset. This is corrected in the FPGA.

- IQ demodulation: following the process described in Figure 5.4, the IQ demodulation was implemeted in three steps:
  - Phase shift: In the mixers, the cavity output V_o^{cav} is mixed with the reference RF signal that acts as a master oscillator. In order to get Q, this reference signal must be phase shifted 90^{o}. To do so, the

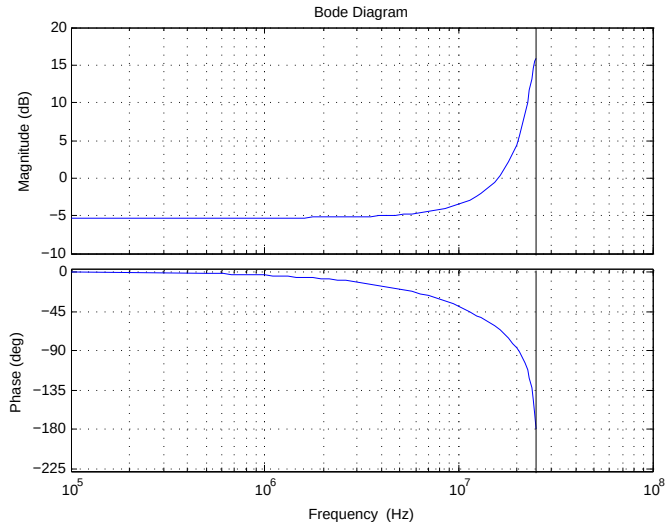

Figure 5.8. – Frequency response of the discrete filter implemneted to shift 90º the phase of the reference signal

following discrete filter has been implemented in the FPGA:

$$U(z) = \frac{1}{z + 0.8402} E(z)$$

Its frequency response shows a -90º phase shift at the working frequency of 20.41 MHz as can be seen in the bode diagram of the filter implemented shown in Figure 5.8. This filter has a gain of 5dB at the working frequency that is compensated.

– Mixing: this consists simply in a high throughput math multiplying block of LabVIEW.

– Low pass filter: in order to dismiss the high frequency components produced in the mixer, a narrow low pass filter is required to get the baseband component. The simplest way is to use a LabVIEW function to calculate the DC value of the mixer product. However, this function needs to accumulate a minimum number of 50 values to produce an output, so the loop delays consequently. That is the reason why a discrete filter has been implemented, with the following

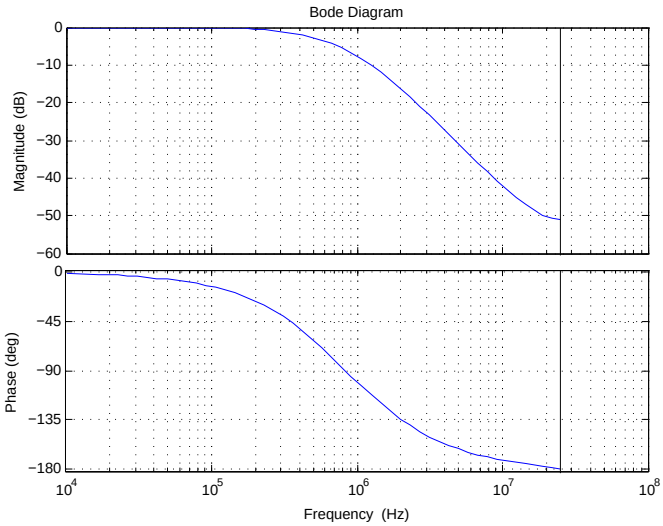

Figure 5.9. – Frequency response of the discrete transfer function implemented to filter the high frequency components of the mixing products

transfer function:

$$U(z) = \frac{0,01z}{(z-0,9)^2}E(z)$$

which completely filters the $40.82MHz$ frequency component (second harmonic), and does not affect the baseband component magnitude or phase (see Figure 5.9) where the I and Q are located.

The next and last step of the acquisition's FPGA card part, after obtaining the I and Q components, is to insert them into a DMA FIFO to transfer them to the real-time controller, where the control actions are performed.

All this functionality is placed inside a Single-Cycle Timed Loop (SCTL). This is a special use of the LabVIEW Timed Loop structure. Timed Loop structures are always SCTLs when used in an FPGA VI. When used with an FPGA target, this loop executes all functions inside within one tick of the FPGA clock you have selected. In this case, the clock used is the clock provided by the adapter module (IOModuleclok) at a 50Mhz rate.

All the algebraic operations performed in the previous processing are implemented using the high throughput math functions for FPGA. These are functions to perform high throughput math and analysis with fixed-point numbers on FPGA targets. They are are similar to the Numeric functions but support higher throughput rates, handshaking terminals inside a single-cycle Timed Loop, input/output registers, and automatic pipelining.

The communication between the FPGA cards and the real-time controller is based on Direct Memory Access (DMA), which allows the FPGAs to access the host's RAM directly. A DMA channel consists of two FIFO buffers: one on the host controller and one on the FPGA target. After creating a DMA FIFO, you write block diagram code to write data to, and read data from, the appropriate buffer. Because DMA communication is based on FIFOs, data transfer occurs one element at a time. The first element in one buffer is the first element transferred to the other buffer.

Regarding to the real-time controller, this is the part that carries out the control of the variables acquired. All the functionalities are coded under a Real-Time LabVIEW environment.:

- The real-time controller code reads the I and Q components sent by the acquisition FPGA from a DMA Host FIFO and performs a phase compensation in order to fix the phase difference induced by the cables present in the experimental setup. Additionally, an amplitude correction is also carried out to compensate the all the known gain losses.

- Then, the values obtained are compared to the desired I and Q values encoding the setpoint phase and amplitudes, thus obtaining the control variables for two parallel PID controllers.

- The baseband inputs QBBP, QBBN, IBBP, and IBBN of the quadrature vector modulator must be driven from a differential source and s biased to a common-mode level of 500 mV DC. As the NI PXI-7852R FPGA card outputs are single-ended, the required conversion is digitally performed at the real-time controller, as well as biasing.

- I' and Q' in differential mode (I'+, I'-, Q'+ and Q'-) are packed and stored for a more efficient transmission and written to a DMA Host FIFO and sent to the FPGA multifunction card that will generate them.

Then, the FPGA card in charge of signal generation reads the four differential values written in the DMA FIFO by the real-time controller and simply sends them to output nodes.

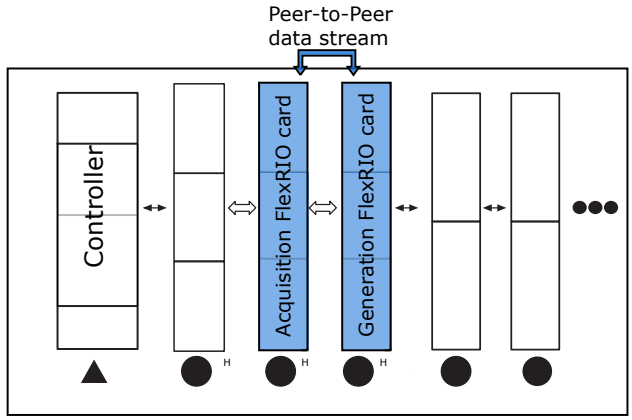

Figure 5.10. – Schematic description of the approach based exclusively in FPGAs

Finally, in order to minimize unnecessary latency sources, all the GUI is moved to a regular PC, which is connected with the PXIe as Host controller via a TCP/IP LAN. All the necessary data to monitor the relevant data of the phase and amplitude loop, as the control and error signals, are sent from the PXIe to the host PC using LabVIEW network shared variables in a parallel low priority task.

This approach has allowed the development of fast solutions to test different control strategies before moving to a pure FPGA based implementation.

5.3.5.2. FPGA approach

The second approach is focused on obtaining the highest possible throughput. This is more oriented to a final implementation of a previously tested configuration based on the solution presented above.

In this case, the control loop is closed over two FlexRIO FPGA cards, where the controller does not take part in the data processing of the closed loop structure, as shown in Figure 5.10. This avoids any data transfer protocols (as DMA) to share data between cards and controller, and consequently, the associated latency is not introduced in the feedback loop.

Using two FlexRIO cards inside a single PXIe chassis allows to use peer-to-peer streaming to communicate between them. NI peer-to-peer (P2P) streaming, similarly to DMA protocol, is a buffer interface. This technology uses PCI Express to enable direct, point-to-point transfers between multiple instruments

without sending data through the host processor or memory. This enables devices in a system to share information without burdening other system resources [17]. That is, the chassis backplane switches provide direct links to the slots occupied by the FlexRIO cards so there is no need to transfer data through the host controller or use system resources such as the CPU or host memory. As a result, high speed transfers are obtained between FPGA cards, in the order of some hundred MHz . So, taking advantage of the P2P streaming, the phase and amplitude loop bandwidth is not limited by the data transfer rates between devices as happens in the previous approach.

This solution requires higher development effort due to several reasons:

- Compilation times: The process of running a user-defined application directly in silicon requires the application to be synthesized to a bitfile following the steps shown in Figure 5.11. This compilation process can last several hours. As all the program is coded in FPGAs, the debugging process becomes much slower, as any minimal change requires the recompilation of the whole FPGA. Although LabVIEW provides the opportunity to simulate the FPGA code on the development computer and resolve any programming errors before going to hardware in order to reduce the amounts of compilations, real I/O can not be properly simulated, thus many problems related to acquisition and/or generation cannot be fixed this way and require a compilation,

- Fixed-point arithmetic: when using SCTLs, High Throughput Math functions must be used to obtain valid value every clock cycle. These require to operate in fixed-point format, which is highly speed and resource-efficient but type has an inferior range and precision compared to floating point. When working with this format, a detailed planning of every operation must be carried out in order to deal with overflows, inconsistent data sizes and sign related issues.

- Resource limitation: Both FlexRIO cards used are based on the Virtex-5 family of Xilinx FPGAs, which provide a fixed number of resources such as slices, DSPs, RAM blocks, onboard memory or clock speed. Two problems must be taken into account. On the one hand, the processing that can be held in a single card is limited by the physical resources of the FPGA. This forces to the developer to optimize the code if a large amount of functions and complex algorithms are required. On the other, there is a loop rate limitation for the FPGA execution. By default, FlexRIO cards use their onboard 40MHz base-clock, that can be derived to compile

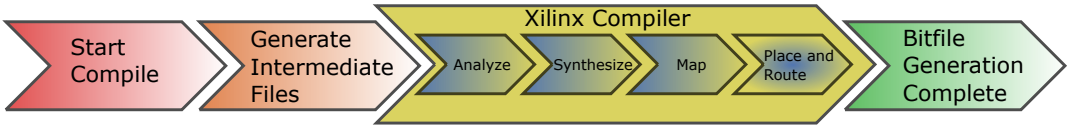

Figure 5.11. – The Compile Process from Run Arrow button of LabVIEW to the final Bitfile.

the code to run at higher clock rates. The maximum rate that can be achieved depends on the length of the longest combinatorial path. This requires an strict management of pipelining between functions executed on the FPGA.

The hardware setup in this approach, consists on a 8 slot NI PXIe-1082 chasis. A NI PXIe-8135 embedded controller running Windows 7 has been used for development, configuration and monitoring purposes only. Two FlexRIO cards with their respective adapter modules are responsible for closing the feedback loop. Two different models have been chosen, the NI FlexRIO 7966R and the NI FlexRIO 7961R. The first one is used along with a NI 5761R adapter module with an ADC up to 250MS/s, while the second one is completed with a AT-1212 signal generator module at 1.25GS/s.

Although a module with a 250 MS/s ADC has been used for the signal digitalization, the sampling rate has been set to 50MS/s, performing a decimation of acquired samples. The reason for not using the Ni 5751R module (50MS/s) used in the real-time controller based solution is the higher bandwidth provided by the NI 5761R module. Different sampling rates could have been used in order to test the designed solution with undersampling discretization, but a rate of 50MS/s has been chosen to get the greatest possible similarity in both approaches.

Implementation of data processing and control structure

All the proccessing and calculations performed by the real-time controller in the previous approach has been moved to FPGAs. One important part of the design has been to decide how to distribute the code between the cards. In the final implementation, all the control part is placed in the acquisition card, the NI 7966R. The reason behind this decision is that this card is based on a more powerful FPGA model, thus providing more resources.

The acquisition card performs two parallel SCTL loops. The first one, governed by the IOModuleClock of the NI 5761 at a 125 Mhz rate, generates two

samples per clock cycle at a clock rate that is half the sample rate. The default sample rate is 250 MHz, which sets the default clock rate for this loop at 125 MHz. In the next stage, the required samples are discarded to obtain the desired sampling rate of 50 MS/s for the required two signals. Finally, it writes the discretized samples into a local FIFO.

The second SCTL loop is executed at 50 MHz. It reads the data sent by the first loop from the local FIFO and performs all the steps in the following list:

- The same signal conditioning and I/Q demodulation described in the real-time controller based approach is carried out.
- Once the I and Q parameters are obtained, a phase compensation is performed in order to compensate the phase shift caused by cables used in the setup. If cables introduce a measured phase deviation of $\varphi^{cables}$to the cavity output signal phase φ, the demoduled I and Q parameters encode a wrong phase information in this way:

$$I_{demoduled} = Acos(\varphi + \varphi^{cables})$$

$$Q_{demoduled} = Asin(\varphi + \varphi^{cables})$$

  In order to compensate this undesired phase value, trigonometric identities are followed to obtain compensated I and Q signals. Being $I_{cables} = cos(\varphi^{cables})$ and $Q_{cables} = sin(\varphi^{cables})$ known parameters as the cables have been characterized, the following calculations are performed:

$$I_{demoduled} \cdot I_{cables} + Q_{demoduled} \cdot Q_{cables} = cos(\varphi) = I$$

$$Q_{demoduled} \cdot I_{cables} - I_{demoduled} \cdot Q_{cables} = sin(\varphi) = Q$$

In addition, an amplitude compensation is also carried out to compensate any losses caused in cables.

- At this point, the I and Q signals are sent to independent and parallel PID controllers. These are implemented in discrete form using High Trougput Math functions (divide, add and multiply) and feedback nodes to implement the unit delay z^{-1}. The form of the controller is:

$$PID(z) = K_p \left[\frac{K_i T_i T_d}{z-1} \left(1 + \frac{z}{K_d} \right) + \frac{K_d}{z} + 1 \right]$$

Being K_p the proportional gain, K_d the derivative gain, K_i the integral gain and T_i the integral time. These controllers are implemented manually since the PID function for FPGA is not supported in SCTL loops.

- At the output of the PID controllers, the regulated $I^{controlled}$ and $Q^{controlled}$ are obtained, which encode the desired setpoint amplitude and phase values. This two parameters are then converted to the format that is used in the generator card, which is +14,14 FXP. Finally, the values are properly packaged and written into a pee-to-peer FIFO.

It must be remarked that a great effort has been put in handshaking. First, to synchronize two loops executing at different rates. For this, an algorithm has been designed in LabVIEW by combinating mathematical functions in order to adequate the write/read rate of the FIFO structure that share both loops. And second, in the 50 MHz loop all the data flow is controlled using the handshaking tool provided by the High Throughput Math functions of the LabVIEW FPGA module. This is necessary to ensure a proper execution flow in the implemented signal processing and controllers. This is particularly important in FPGAs, as the code executes in a true parallel way.

Moving to the second FlexRIO card, it is based in two parallel STCL loops both running at 156.25 MHz, which is the nominal speed of the AT-1212 modules IOModuleClock. The reason for using two loops at the same speed is that the AT-1212 module forces the use of its IOModuleClock for a proper operation of its output nodes. If all the required code is placed inside a single loop, the FPGA is not able to compile due to an excessive combinatorial path. So, the algorithm is divided in two parallel loops.

The first one simply reads from the peer-to-peer FIFO and writes the data into a local FIFO. The second one discards a certain number of samples to adequate its execution rate to the 50 MHz rate of the acquisition and control loop and sends the values to output nodes, thus generating the physical $I^{controlled}$ and $Q^{controlled}$ signals.

In this solution, the PXIe controller is only used in monitoring tasks and for configuration purposes such as peer-to-peer streaming enabling, PID gain parameter and setpoint phase and amplitude setting.

5.3.6. Frequency tuning loop

The second loop present in LLRF systems takes care of the variations in the resonance frequency of the cavity. High-Q cavities having a small bandwidth can be detuned by small perturbations as temperature changes. Fabrication

tolerances and temperature drifts have to be tuned out for most applications to be exactly on resonance. Since the adjustment of an external impedance would also change the coupling, tuning is often done by deformations of the inner cavity surface [9]. As main sources of frequency perturbation in the resonant cavity are much slower than the RF signals, such as thermal effects or Lorentz force detuning, the frequency tuning loop can be considered a slow control loop [7].

The frequency loop has been also designed and implemented. For this loop, time constraints are less restrictive, since the dynamics of the disturbances are much slower than the RF signal [4]. In this case, the feedback loop rate obtained closing the loop over the Labview Real-Time based controller is large enough to keep the resonance frequency fixed against external disturbances, even without adding compensation networks. The signal processing and control architecture of the tuning loop can thus be implemented in the controller.

This feedback loop acts on two stepper motors that move two pistons in the radial direction of the resonant cavity. This pistons change the geometry and volume of the cavity gap, thus changing its resonance frequency. The goal of this loop is to keep the resonance frequency matched to the operating frequency, 79.59 MHz in this case.

The control implemented produces two different signals that are used to drive the stepper motor. The first one is a pulse train that determines the step number to be rotated and the second one the direction of the movement.

Depending on which variable is measured and used as the control signal, two different frequency tuning loops are studied.

5.3.6.1. Phase detection based tuning loop

When the cavity is at resonance, the phase difference between the input and the output has been measured to be -108º in the current experimental setup (see Figure 5.17).This phase difference considers the value due to the resonance and the phase changes introduced by measurement elements. The frequency loop keeps this value stable against perturbations in order to minimize the reflected power in the cavity input. The phase difference is calculated on the FPGA following the scheme described in Figure 5.6. This value is transferred to the controller through DMA and corrected using a PI controller to keep the measured phase matched to the resonance setpoint. The magnitude of the controller output determines the amount of steps to move in each iteration while its sign gives the direction.

In this setup, the same hardware described in the Real-time controller based

Figure 5.12. – Bidirectional coupler and power detector at the coupled reverse port to measure the reflected signal voltage

approach subsection has been used except for the digital signal outputs, that have been generated using a NI PXI 6259 multifunction card along with a SCB-68 connector block. This multifunction card is also placed in the same PXIe chassis in charge of the amplitude and phase loop.

5.3.6.2. Reflected power minimization based tuning loop

An alternative way to control the resonance frequency of the cavity is to study the reflected power at the input of the cavity. In resonance condition, transmission is maximum and reflection, consequently, minimum [8].

In this approach, model *zfbdc20-62hp-s+* bidirectional coupler from Mini-Circuits has been used at the input of the cavity. To measure the reflected power, model *zx47-40ln-s+* power detector is attached to the coupled reverse output port of the coupler. This can be seen in Figure 5.12. This power is measured through an analog input of a NI PXI 6259 multifunction card. This variable is used to design the control algorithm,

The goal is to keep the measured voltage value at its minimum. The proposed methods have been to characterize the reflected power voltage for a certain reference signal power, 9dBm in this case, for all the range of the pistons and use the measured minimum as a fixed setpoint for a PID controller. This control is implemented in the controller of the PXIe the same way as in the aforementioned phase detection based tuning loop. To generate the controller digital outputs, the same multifunction card as for acquisition is used. Alternatively, the set point can be obtained from an optimization algorithm, being the objective the

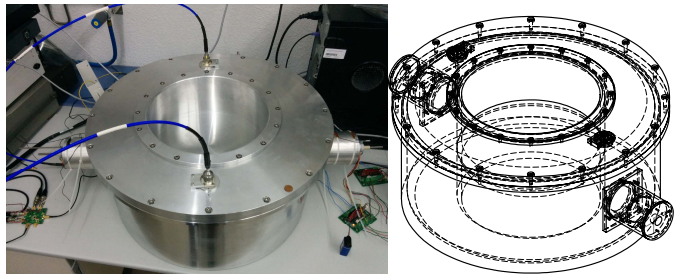

Figure 5.13. – The aluminum resonant cavity designed to test the proposed LLRF system with a 79.59 MHz resonance frequency.

minimization of the reflected signal power.

5.4. Test bench description: 79.59 MHz resonant cavity

A complete testbench has been built in order to test and operate the developed LLRF control system with the goal to simulate real accelerating installation conditions (as much as posible) in a laboratory.The central element of the test bench is the tunable resonant cavity shown in Figure 5.13. It is a reentrant type cavity machined in aluminum, with the electric field concentrated on an accelerating gap near the axis, and the magnetic field mostly located on the outer perimeter. It has been designed by the research group in the UPV/EHU to have a resonance frequency of 79.5 MHz (dominant resonance mode or TM_{010}), a suitable value for heavy-ion acceleration. A 3D model of the cavity is shown in Figure 5.14 along with a dimmensioned drawing of the design. The structure presents two tuners, each one 40mm in diameter. They are displaced in the radial direction (see Figure 5.15) in order to change the geometry of the cavity, and thus, its resonance frequency. For a maximum given depth of 70 mm, a tuning range of 1 MHz is obtained.

Two rotatable loops coupling to the magnetic field are used as RF input (drive) and output (pickup) couplers in the cavity, respectively (see Figure 5.16). Finally, a calculation of the quality factor of the cavity has been carried out considering that the structure is built in Aluminum with a conductivity $\sigma = 3.3 \cdot 10^7 S/m$, obtaining a value of $Q_u = 68000$.

After the process of mechanization and once the real cavity was built, a characterization of the cavity was performed. It showed that the resonance fre-

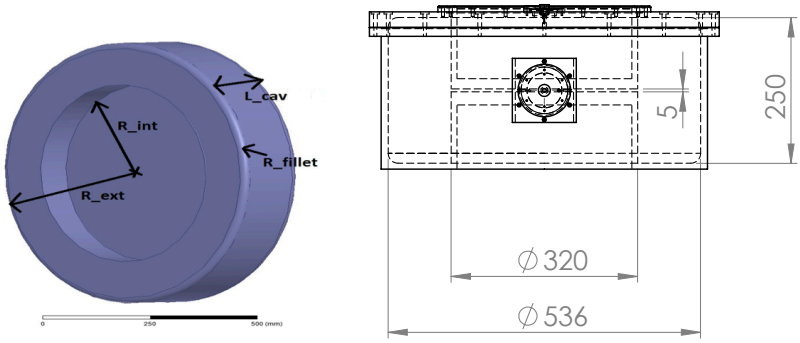

Figure 5.14. – A 3D model of the designed resonant cavity and a dimmensioned drawing.

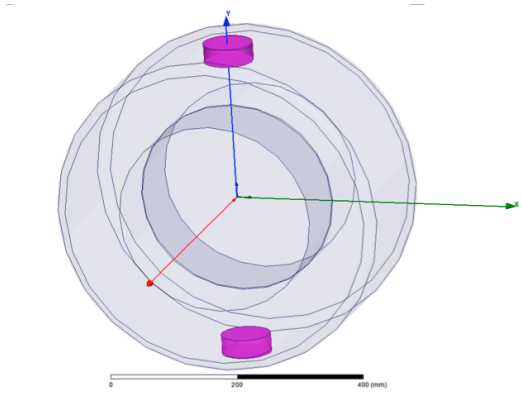

Figure 5.15. – Tuner position in the cavity.

Dimmensions (mm)	Figures of Merit
L_cav=250	Freq. TM_{010}=79.5 MHz
L_plates=5	Q_u=6800
L_max_depth=70	Tuning Range=1 MHz
R_fillet=17	
R_ext=268	
R_int=160	
R_tuner=70	

Table 5.2. – Summary of cavity design dimensions and main figures of merit

Figure 5.16. – One of the two coupled pickups of the resonant cavity.

quency was slightly shifted from the nominal value, being located at 79.59 MHz as shown in Figure 5.17. This deviation does not cause any problem for the LLRF control developed.

When power is applied to an empty resonant cavity, the fields build up in time. The filling time, t_{fill}, is the time for the energy stored in the cavity with loaded Q_u to build to $1/e$ of its saturation point [13]. It is essential to characterize this filling time, as it will determine the dynamics of the process to be controlled and the necessary control bandwidth of the required feedback loop. Measurements from an oscilloscope (Hameg model HMO3524) showing the the filling time for the presented cavity be seen in Figure 5.18.

From this empiric result, the model of the cavity filling is obtained as a first order transfer function:

$$G(s)_{cav} = \frac{K_{cav}}{\tau s + 1} \tag{5.8}$$

Where $K_{cav}$is the DC gain and τ the system time constant. From the Figure 5.18, it can be stated that $\tau = 6\ \mu s$ and the DC gain $K_{cav} = 0.7$ (measurement carried out with an input level of 32 mV). This dynamics represents the I and Q dynamics to control if the mixing dynamics are disregarded, that is, making the assumption that changes in I signal at the input do not affect the Q signal measured at the output of the cavity and vice versa. The control designs were done taking as reference the transfer function in Equation 5.8, obtaining

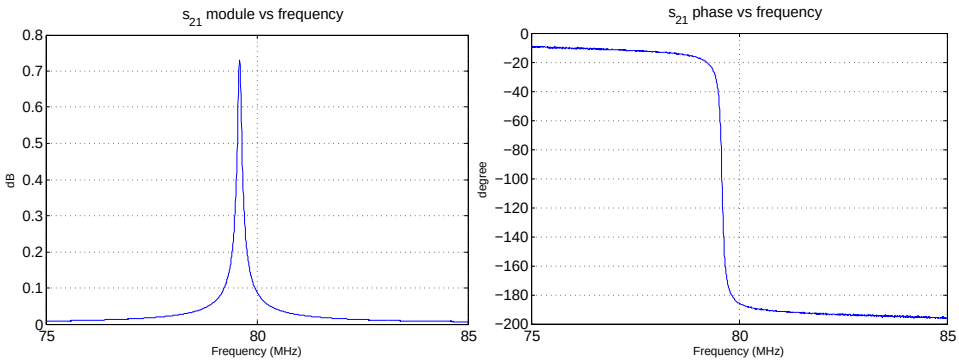

Figure 5.17. – Characterization of the cavity from S-parameter measurements

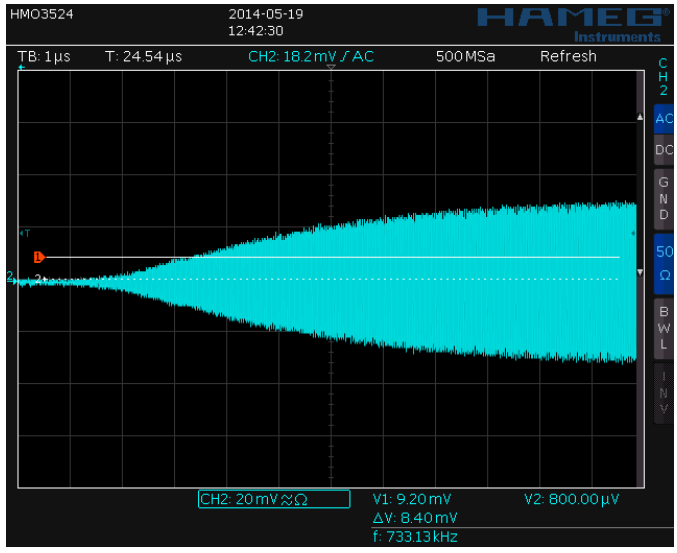

Figure 5.18. – Cavity output measurement showing cavity filling time

satisfactory results as shown in sections below.

The testbench is completed with a low phase and amplitude noise Agilent 8657A RF signal generator, which provides the reference RF signal used to feed the current test bench.

5.5. Experimental results

In this section, the results obtained in the testbench with the proposed LLRF control system are presented. The tests have been performed following the two proposed approaches.

5.5.1. Phase and Amplitude feedback control loop experimental results

As mentioned before, this feedback control loops is implemented in order to maintain the stability of the RF fields. The aim of this fast loop is to set the RF gap voltage of the cavity and its phase as required, as well as keeping both process variables stable within acceptable range. The requirements for the current project are $< 1\%$ in amplitude and $< 1^{\circ}$ in phase error, values which are usual for heavy ion LLRFs [6], as well as being able to close the control loop in an adequate time relative to the cavity's time constant.

5.5.1.1. Real-time controller based approach

The latency caused by the DMA transfer protocol present in this solution limits the bandwidth of the control loop obtained. It results in a $20\,kHz$ bandwidth, that is, it takes a minimum amount of $50\,\mu s$ to close the loop. As the cavity filling time, i.e., the time constant, has been measured to be about $6\,\mu s$, this solution would not be suitable for such application regarding the dynamics of the plant.

As a solution, a compensation network, a lag network more specifically, is proposed. Lag compensators can be used to adjust the frequency response of a system [11]. This compensation network can be used to provide better stability, better performance and a general improvement.

In this particular case, the main goal is to slow down the plant's dynamic in order to make the closed-loop bandwidth suitable. A first order compensator is designed to change the cavity's time constant from its nominal value of 6 μs (see Figure 5.18) up to some hundreds of μs. The compensator in its discrete form is:

$$H_{lag}(z) = \frac{0.002}{z - 0,998} \tag{5.9}$$

This compensation network is applied in the closed loop control, separately for both I' and Q' control signals. Applying this dynamics, the measurement of the cavity output validates the implemented lag compensation as seen in the measurements performed with the oscilloscope shown in Figure5.19, where a 1.5 ms filling time can be observed. Simply adjusting the location of the zero and the pole of the implemented $H_{lag}(z)$ filter, the frequency response of the plant can be modified to change the system's bandwidth and allow to test different control strategies.

Using this implementation, phase and amplitude control tests have been carried out. The phase and amplitude references are externally set and the result is monitored. Figure 5.20 shows the obtained I/Q, while its phase response can be found in Figure 5.21. A more detailed time response of the phase is presented in Figure 5.22. The system response against a reference change shows low overshoot and error in steady condition fulfilling the requirements in phase and amplitude accuracy. The settling time depends on the adjusted bandwidth and, consequently, the perturbation correction bandwidth.

5.5.1.2. FPGA approach

In order to measure the minimum time to close the loop in the pure FPGA implementation, a simple application has been designed. It consists in a periodic arbitrary function, software-generated by the NI PXI-7966R, and sent to the NI PXI-7961R through peer-to-peer streaming. The transferred data is generated by the AT-1212 module, which output ports are wired to the imput ports of the NI 5761 adapter module of the first FlexRIO NI PXI-7966R.

At this point, the acquired function is compared with the previously software-generated one in the same SCTL loop, thus using the same clock rate. The delay is calculated searching for a certain pattern and measuring the sample amount between the two sequences compared. Knowing the clock rate, this number of samples is translated into time. Following this procedure, a value of 6 μs has been obtained, which is similar to the cavity time constant. It suggests that with a proper control design and implementation, the dynamics of the plant can be controlled.

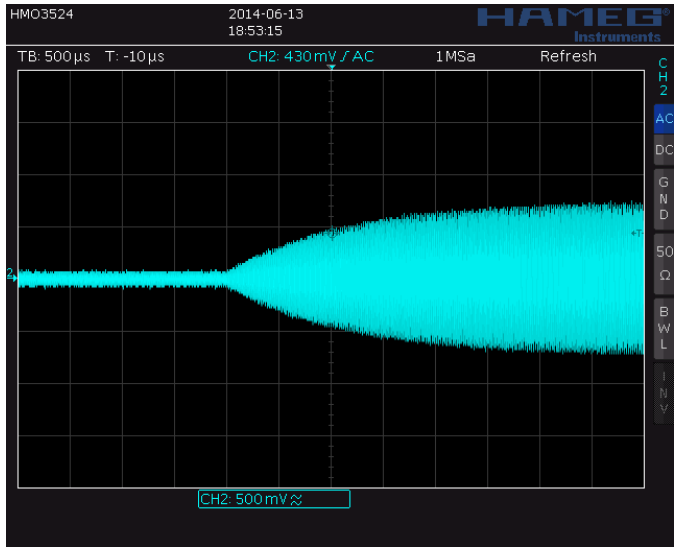

Figure 5.19. – Screenshot of a Hameg HMO3524 oscilloscope of the cavity filling time measurement applying the lag compensation.

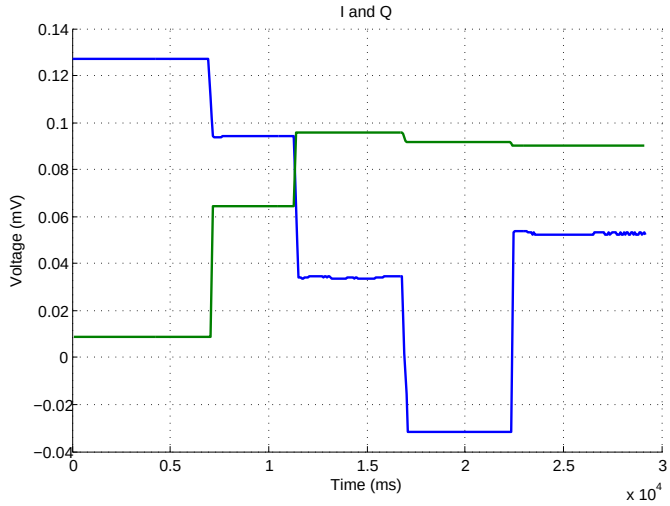

Figure 5.20. – I and Q signals measured at cavity output against arbitrary phase reference changes.

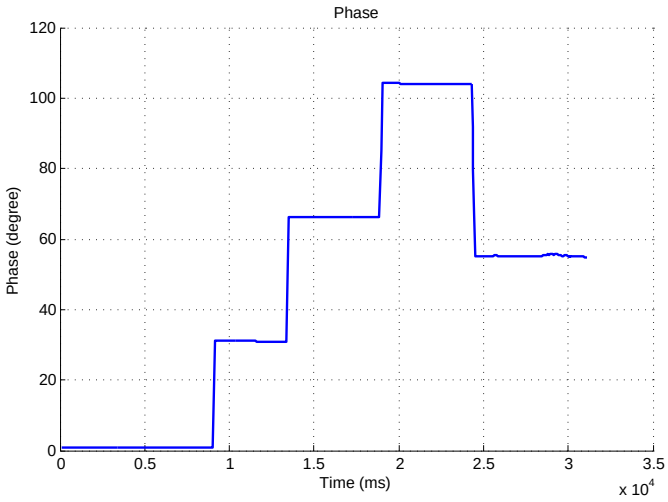

Figure 5.21. – Measured phase response against setpoint changes.

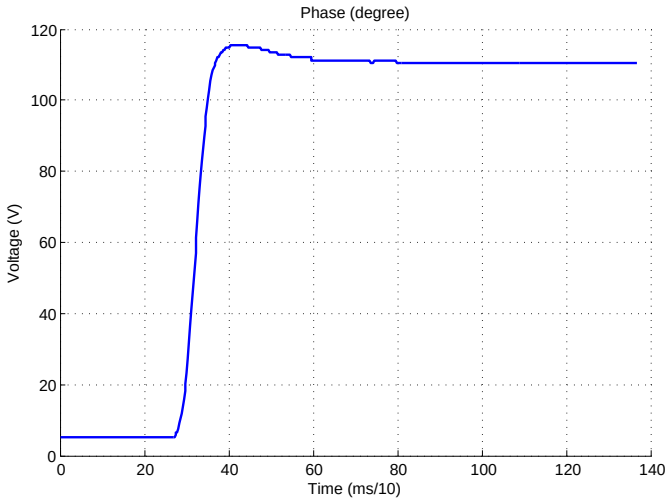

Figure 5.22. – Detailed Step response of the the phase..

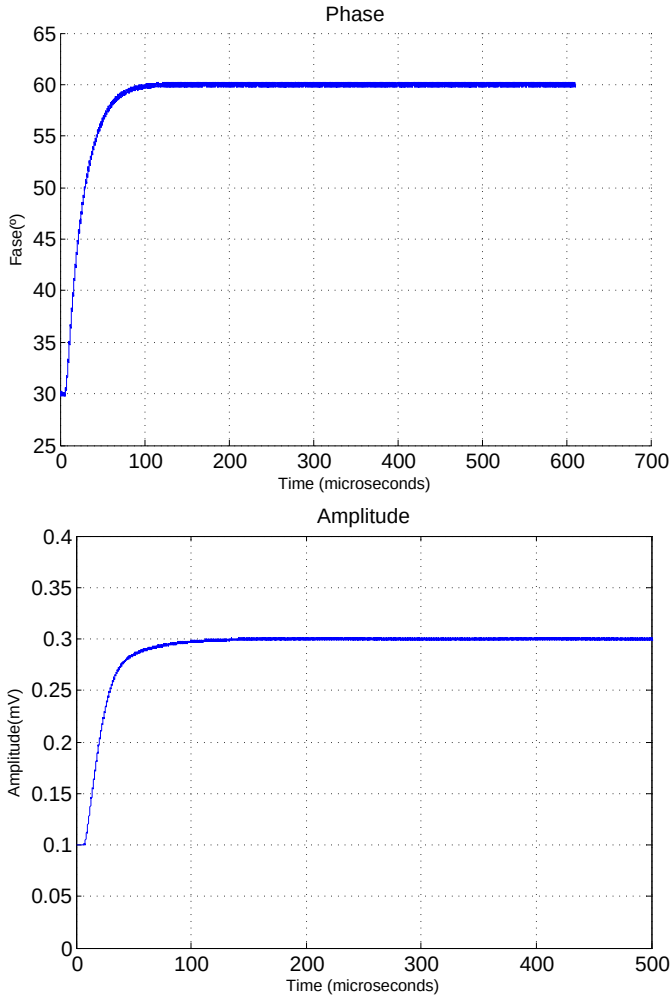

Figure 5.23. – Change in phase reference measured at cavity output (up) and Amplitude reference change response (down)

The results of the pure FPGA based approach also fulfills the requirements of $<1^{o}$ on phase and $<1\%$ on amplitude errors, incrementing the closed-loop bandwidth. The closed control action with a PI controller can be observed in Figure 5.23. The tuning of the control parameters is performed empirically following the Ziegler-Nichols method [15]. The top figure shows the phase response of the system against a step change set in the monitoring system (from 30^{o} to 60^{o}) and the one in the bottom represents the amplitude response against a step from 0.1 to 0.3 mV. In such configuration, higher control gains result in a response with overshoot. More advanced control strategies can be tested in order to get improved results.

Overall noise, including amplitude and phase noise contributions, are shown in Figure 5.24 for the pure FPGA-based approach (as it is considered as the final solution implemented for the proposed LLRF control system). Measurements have been obtained from a high-precision spectrum analyzer Agilent E4440A. The two curves correspond to the RF signal generator used as reference source (Hewlett Packard 8657B) and to the overall loop, respectively. Notice that the overall noise produced by the RF source is fundamentally phase noise, as amplitude noise is much lower than phase noise in this kind of signal sources, On the other hand, the overall noise measures for the loop includes noise introduced by the control system but also from the RF signal source. As it can be observed in Figure 5.24, the noise introduced by the control system is not much higher than the RF phase noise produced by the RF source itself. In addition, just amplitude noise (not including phase noise contribution) measurements have been carried out using a high-precision sampling oscilloscope with signal-statistic analysis capabilities Agilent 58833A DSO. The results show that amplitude noise is five times higher in the loop measurements than in the reference. However, as the overall noise values are quite similar in both curves in Figure 5.24, and knowing that in RF signal generators amplitude noise is negligible compared to phase noise, it can be concluded that the results shown in Figure 5.24 can be considered mainly as phase noise. So, in the frequency range of [100 Hz, 10 MHz], the jitter values obtained for 79.59 MHz are: $\tau_{reference} = (6.090 \pm 0.001)ps$ and $\tau_{in-loop} = (7.033 \pm 0.001)ps$ ($\tau_{in-loop}$ includes noise from reference signal).

This pure FPGA implementation implies a higher resource utilization of the FPGA cards, since all the code (including the PID controller) is placed inside them. The resources consumed by both architectures is shown in Table 5.3.

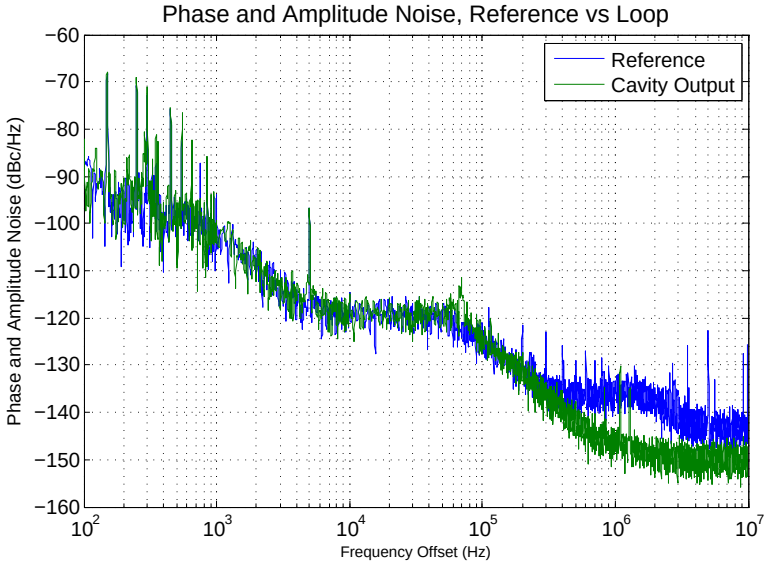

Figure 5.24. – Measured overall noise (phase and amplitude noise) curves in a range of [100Hz, 10MHz] of RF reference signal generator and the feedback loop

Table 5.3. – FPGA device utilization summary given in % of the total capacity of both architectures

RT Controller approach	Slices	Slice Registers	LUTs
7961R	93%	69%	63%
7966R	22%	10%	10%
Pure FPGA approach			
7961R	58%	29%	29%
7852R	11%	5%	4%

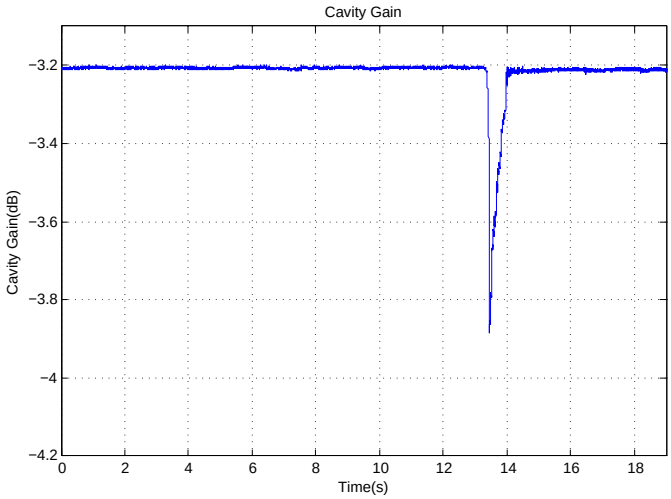

Figure 5.25. – Resonance frequency compensation against perturbation

5.5.2. Frequency tuning loop experimental results

Regarding the results of the tuning loop, the Figure 5.25 presents the power gain between the input and the output of the cavity with the phase detection based approach. It can be observed how the power gain decreases from -3.2 dB (in resonance) to -3.8 db in the instant in which a external deforming mechanical pressure is applied on the top of the cavity and how the stepper motors act to keep the resonance frequency matched to the nominal one. The control is able to recover from the perturbance in the range of under 1s, which is a sufficient value regarding the dynamic of the disturbance sources.

In the Figure 5.26, a similar graph is shown, where the same response is shown, but this time obtained from the reflected power minimization based solution. As seen, a mechanical perturbation shifts the resonance frequency of the cavity and consequently, the reflected power rises. The implemented control keeps this magnitude at the setpoint value, that is, the minimum.

In this case, the response is about 4s. This is slower than in the previous implementation, but still admissible in some applications. This is caused by the compensation of the noise introduced by the power detector, since the measured signal level is low. Future work will be focussed on the improvement of this

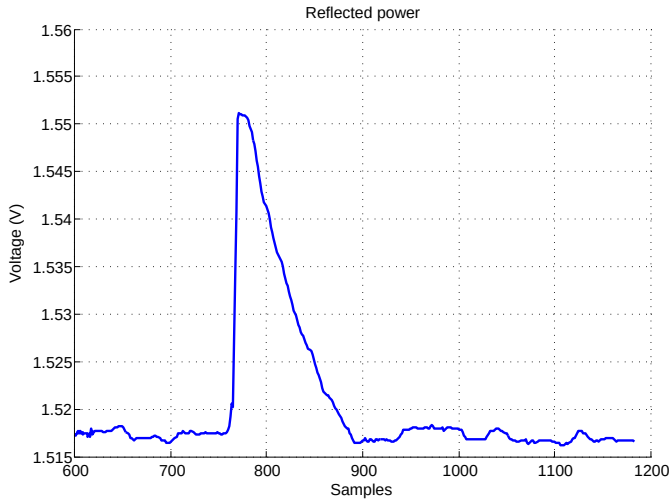

Figure 5.26. – Reflected power correction of the incident RF signal of the resonant cavity against a perturbation.

time response. One way is the selection of an adequate signal power level and power detector. The use of advanced optimization techniques is another way of possible improvement of such time response.

5.6. Summary and conclusions

This work presents a LLRF architecture for heavy ion linear acceleration following the specifications of the future LFR in Huelva, Spain. The LLRF system is based on a PXIe platform and is completed with a test bench for experimental validation of the prototype. The LLRF system is mainly digital, offering several advantages over classic analog systems, such as high flexibility, versatility and reconfigurability. Two different configurations are presented for the fast loop of the LLRF system, which controls the amplitude and phase of the RF fields. The first one combines a real-time controller with two FPGA cards, leading to a very flexible system but reduced bandwidth. The second one is only based on FPGA cards improving the bandwidth but increasing the development cost. The key advantage of the two strategies and the presented testbench is its flexibility to add new functionalities and its ease of testing. In particular, the controllers can be initially designed, implemented and tested in the RT system and, in a second phase, the implementation can be translated as

a whole to the FPGA card, taking advantage of the tools offered by a LabVIEW based environment.

For the frequency tuning loop, in addition to the use, as usual, of a phase detection based method, a second approach is proposed, using the reflected power of the cavity input signal to perform the regulation.

On the other hand, a subsampling discretization technique is proposed in order to develop a fast data acquisition system avoiding excessive equipment costs. The main drawback when using subsampling, the increment of the clock jitter; is not excessive in this case due to the relatively small difference between the original and final frequencies and the particular implementation developed. In any case, the minimization of this effect and the study of the application of this techniques in other LLRF system configurations (for instance, variable bandwidth) are considered for future work.

Focusing on the amplitude and phase loop, the results presented validate the proposed scheme, in both configurations. That is, the initial specifications are fulfilled in both configurations: $<1^{o}$ on phase and $<1\%$ on amplitude errors. It is must be remarked that the use of a lag compensator is the key feature which allows the application of the proposed real-time controller based strategy, since it adjusts the system's bandwidth, reducing it and maintaining the system stability.

Regarding the frequency tuning loop, both configurations performs as expected, maintaining the cavity nominal resonance frequency against perturbations.

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CHAPTER 6

LabVIEW process variable integration in EPICS networks: performance test

Large scientific projects present technological challenges, such as the distributed control over a communication network. In particular, the middleware Experimental Physics and Industrial Control System (EPICS) is the most extended communication standard in particle accelerators nowadays. The integration of modern control architectures like PXI/PXIe in these EPICS networks becomes a very valuable feature, and many efforts and initiatives are being made in this direction.

The current chapter presents an experiment with the aim to validate a non-standard EPICS fast controller (which integrates solutions based in LabVIEW RT into EPICS) as a reliable solution for systems based on PXI/PXIe solutions. This solution opens the option to integrate LabVIEW based designs as those shown in Chapters 4 and 5 into EPICS in a transparent way.

6.1. Introduction

Particle accelerators are built from the integration of very different and complex subsystems that require a high variety of technologies for a correct operation. The scale of this installations ranges from a few of meters for an small linear accelerator, to a circumference of 27 kilometers for the Large Hadron Collider [32]. The physical dimension gives some insights into the complexity of the machine, and as can be expected, controlling tens or hundreds devices spread over a large area is a quite challenging task. The control tasks in a large scientific facility are fundamental for a correct machine operation and for ensuring the safety of the machine and personnel.

The design of those control systems must take into account considerations about the distributed nature of this kind of facilities and the variety of present technologies, what supposes a big challenge. Experimental Physics and Industrial Control System (EPICS) [15] middleware is one of the most relevant solutions developed for the implementation of the control in big physics facilities, and in particular, it is usually used as the main control technology in particle accelerators.

In fact, EPICS is a software framework designed for the development and implementation of distributed control systems for scientific facilities. In particular, it is specially suited for the connection of large number of controllers in a networked environment and gives monitoring, supervision and control utilities, including feedback actions and guaranteeing soft real-time behavior. More details about EPICS are given in the next sections.

Different hardware solutions in terms of architectures, standards and protocols are used under EPICS environment for the development of the control systems and the related diagnostics. In this regard, it is worth pointing out that one of the most relevant characteristics required in those hardware components is the high availability and reliability and long lifecycle of the selected technology, since the accelerators are designed for decades of operation. For this reason, the technology involved in the implementation of any particle accelerator must be well known and, therefore, have been used along decades. Relevant examples of this are hardware components based on the standards CAMAC [35], and VME [17] and its extensions.

However, the technological advances in the fields of instrumentation and control has lead to the irruption of new standards such as PXI/PXIe [34] and the more recent xTCA [8]. A great lot of work is being done through different initiatives to integrate this newer technologies into EPICS, giving support to

these emerging devices.

In the case of PXI/PXIe, the most remarkable initiative to integrate in EPICS comes from the International Thermonuclear Experimental Reactor (ITER) [30]. This project has standardized many of the control solutions using the PXI/PXIe platform. This decision has lead to the development of the CODAC system [9]. This is a modified distribution of the EPICS base which includes added functionalities, including the device and driver support for PXI/PXIe-based hardware, in order to develop EPICS Input/Output Controllers (IOCs) [18]. The deployment of the integration of a standard EPICS IOC for a NI PXI/PXIe-based controller is described in [19].

In particular, there is a strong interest in providing support for the National Instruments devices which include FPGA cards for data acquisition and control applications. This is specially relevant for the developed tools presented in Chapters 4 and 5 which are fully based on a LabVIEW environment. Therefore, being able to publish the information provided by these solutions into an EPICS network in a integrated way is a very valuable feature.

An architecture appropriate for the integration of NI PXI/PXIe platforms in EPICS networks is presented in [7]. This chapter focuses on the design and realization of a performance test of the mentioned architecture, compatible with the systems developed in Chapters 4 and 5. The goal is to test if this nonstandard EPICS fast controller constitutes a suitable solution, in terms of reliability, taking as reference a similar solution based on a standard EPICS IOC from a CODAC distribution. This comparison is based on a test bench which simulates a real control system environment. The environment designed for this experiment emulates real schemes present in scientific facilities and, in particular, a particle accelerator. A large number of process variables are considered, including digital and analog input/outpu (I/O) signals, monitors, and data processing.

6.2. Nonstandard EPICS Fast Controller

The main objective of this chapter is the test of the architecture proposed in [7], valid for the integration of NI PXIe based control systems in EPICS networks. In this section, some details of this architecture and the description of key elements are presented.

EPICS

EPICS is a software environment created for the development and implementation of distributed soft real-time control systems of large scientific and industrial facilities. It is widely used in particle accelerators, big telescopes and other large experiments. The EPICS collaboration started in 1989 in Los Alamos National Laboratory and Argonne National Laboratory, but nowadays, it is being developed by many more scientific facilities than in the beginning, all around the world, e. g. CEBAF [28], LBL [31], SLAC [33] or DESY [27], [29, 20].

This tool is designed for supporting the development of systems with a large number of network controllers. It provides monitoring, feedback and control, data archiving and user access control among other characteristics. EPICS can be considered as an supervisory control and data acquisition (SCADA) system regarding the data gathering functions, as well as a distributed control system (DCS) when the local devices, the so called Input Output Controllers (IOC), are set to control processes.

The evolution of EPICS over the years in different facilities reflects its capabilities in these environments. On the other hand, it has some drawbacks derived from its complex architecture and the lack of comprehensive documentation. The maintaining of full support for obsolete architectures has caused a slower technological evolution in some cases, mainly due to the long machine life cycle required. However, the development of new projects based on EPICS is pushing the support for new architectures as PXI, PXIe, xTCA, among others. In this way, it is necessary to mention the outstanding contribution of the international project ITER. They chose EPICS as the general infrastructure for control, and it being the core of the so called CODAC system [13]. This system is a clear international reference as well as the ESS, which also chose EPICS as the base of the control systems [11]. The international project IFMIF/EVEDA will also use EPICS [5]. Nowadays, the main current facilities using EPICS are SNS in USA [6] and KEKB in Japan, [2].

An important concept of EPICS are the Process Variables (PV), the basic information unit, organized as Records; these are “objects” with an unique name in the whole EPICS system, and its behaviour is determined by its type (analog input/output, PID controller, calculations, etc.). All the data related to a record is stored is several fields, as many as required, corresponding to individual PVs.

A typical EPICS IOC implements different types of records, with several funcionalities, and defines a Database of such records, creating a local control

system, with mutiple PVs which are published along the EPICS network. An EPICS database interconnects local PVs and records with PVs and records which are published in the EPICS network by other IOCS, transparently for the developer. In addition, EPICS gives a large number of tools for data monitoring, archiving or GUI definition, among other funtionalities.

Further information about EPICS can be found in [21, 25, 22].

CODAC

Control Data Access and Communication (CODAC) is the ITER control system which is based on the EPICS base and EPICS client tools [10]. The Plant Control Design Handbook (PCDH) defines the methodology, standards, specifications and interfaces applicable to Instrumentation and Control (I&C) [23]. CODAC Core System shows how the control design principles are applied in practice and provides a means to build plant system controls that are compatible with the ITER central I&C systems. The design and implementation of the CODAC system includes addressing complexity, reliability, transparent access respecting security and high experiment data rate and volume [26].

ITER CODAC system dristibutions include drivers for the use of NI PXI/PXIe hardware as EPICS IOCS, implemented by mean of standard EPICS base code. This solution is used as reference for comparison purposes, since the underlying system is EPICS base, but with the advantage of providing drivers to integrate some PXI/PXIe devices into the EPICS network.

Nonstandard EPICS Fast Controller description

The controller presented in [24] is implemented using LabVIEW-RT, and it is integrated into EPICS networksusing the LabVIEW EPICS server which is provided by the Data logging and Supervisory Control module (DSC) [16], with an additional interface to EPICS by means of a new external IOC. The resulting system is equivalent to a standard EPICS IOC, overcoming the limitations present in the LabVIEW EPICS server, which is not a complete EPICS environment and, in many cases, is not enough for control purposes. The most remarkable drawbacks are related to alarm handling and to a limited EPICS record support.

In this solution, the primary interface between the local fast controller and the EPICS control network is based on the tools provided by National Instruments in the LabVIEW DSC module, and runs on the real-time system in the PXI controller. This module acts as a plug-in to the Shared Variable Engine and

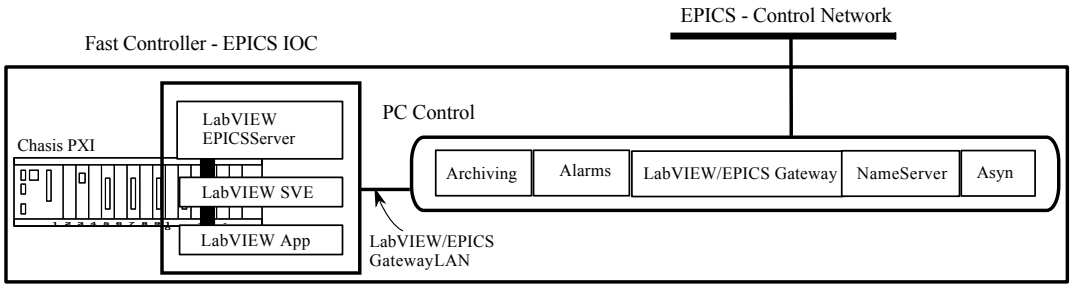

Figure 6.1. – Integration of fast controllers based on LabVIEW RT into an EPICS network.

functions as the link between shared variables and the EPICS network. Shared variables are bound to an EPICS PV while the I/O server handles updates to the PVs. The I/O server then publishes the PVs to the network using the Channel Access Protocol [14]. The arquitecture of the integration of the fast controllers in EPICS networks is shown in Figure 6.1.

6.3. Testbench description

The nonstandard EPICS Fast Controller described is a very versatile and poweful tool. Therefore, this can be a suitable option to be used in a particle accelerator as control element, substituting the standard IOC controller, specially when FPGA computation features are needed. However, the reliability and performance of such a solution must be assured with rigorous and realistics tests. The test of new control elements is hardly possible in a real particle accelerator, since the real environment is not usually accessible for those testing purposes. Besides this fact, the real facilities are not flexible, and the introduction of new devices and equipment into the system becomes a difficult task. For these reasons, a laboratory test bench has been designed and implemented, with the aim of replicating the characteristics of a control system in a particle accelerator, with an appropriate scaling in its dimensions. This strategy has been followed to implement the proposed fast controller and to compare this alternative with another implementation based on the standard EPICS strategy. The latter was implemented using the tools provided by the CODAC system. Anyhow, in both cases similar hardware solutions have been considered, in order to get a realistic comparison. The test bench includes two parallel systems which implement two fast controllers to be tested in a long-term experiment. Both

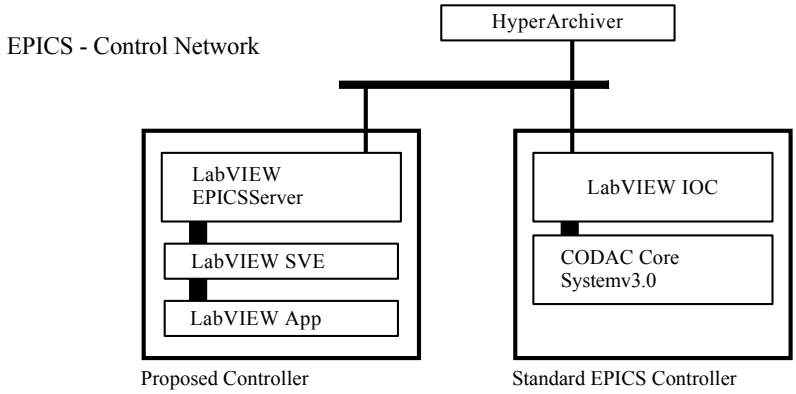

Figure 6.2. – Basic scheme of the networked distributed system for the comparison between the proposed fast controller and the standard EPICS solution.

Architecture	LabVIEW RT based	Standard EPICS based
PXI Chassis	PXIe-1082	PXIe-1031
PXI Controller	PXIe-8108	PXIe-8106
Microprocessor	2.53 Intel Core 2 Duo	2.16 Intel Core 2 Duo
RAM	1 GB RAM	512 MB RAM
Operative system	LabVIEW RT	Scientific Linux 6.1
Software version	LabVIEW 2011	EPICS R3.14.12.2

Table 6.1. – Main characteristics in terms of hardware and software used in both approaches.

systems implement the same functionalities and the typical actions which are habitual in a controller for a subsystem of a particle accelerator. These actions are mainly data acquisition, feedback control actions, and finite-state machines.

Hence, the first implementation is based on an embedded controller under LabVIEW Real Time, publishing PVs into an EPICS network. The second implementation uses an embedded controller under Linux by means of a standard EPICS IOC [3]. This second implementation is equivalent to the solution used in ITER, based on the CODAC system. The basic scheme of the test bench is shown in Figure 6.2, and the main characteristics of both implementations are shown in Table 6.1.

The laboratory testbench includes a simulation of a plant to be controlled. The plant simulates a system with several processes, such as different process-

Figure 6.3. – Picture of the laboratory setup showing both fast controller approaches.

ing of acquired signals (from a signal generator and from the outputs of the system itself) and pseudo-random signal generation which trigger event-trigger processing and alarms, as well as signal generation that act as feedback. This structure has been implemented in both approaches.

The solution based on a standard EPICS IOC is the reference for the experimental comparison, since it is a well-known solution by the community. The IOC runs in a NI PXI-8106 embedded controller enclosed in a PXI-1031 chassis under Scientific Linux 6.1 OS. The I/O actions are performed using a PXI-6259 card. The drivers for this card can be obtained from the public version of the ITER CODAC Core System v3.0.

On the other hand, the proposed novel implementation to be validated is based on a PXIe-8108 embedded controller in a chassis PXIe-1082. In this case, the system runs under LabVIEW Real-Time OS. All of the control actions and the I/O signals are defined in a program developed using LabVIEW. In addition, this program implements a limited EPICS Server, which is used to later create a full IOC and to publish the control variables in the EPICS network. The test bench uses a conventional Ethernet local network, which at the end defines the EPICS network. The overall laboratory test bench is shown in Figure 6.3.

6.4. Performance Test

All of the results obtained with both systems are analyzed exhaustively and archived using a dedicated database. Therefore, the performance of both systems can be studied and compared. In this experiment, a novel archiving system, called HyperArchiver, has been used. This archiving system was developed at ESS Bilbao in collaboration with the Instituto Nazionale di Fisica Nucleare (INFN) research center in Legnaro and the GAUDEE research group from the University of the Basque Country. HyperArchiver allows the use of large data tables with high performance thanks to the usage of Hypertable database [1, 4], and it is considered scalable and reliable.

The main parameters under consideration in order to perform comparison analysis are related to the performance and the repeatability. The tests carried out use 1960 records which have been implemented equally in the both systems to compare, and then, the total number of defined process variables is 9600, similar to the number of PVs presented in [12]. Most of the PVs are processed periodically every 1 or 5 s. On the contrary, a set of 760 records are event processed.

Regarding to the data archiving process, as soon as a PV is processed, it is written in a Hyperarchiver buffer, and the resulting data sets are batch processed each 10 s, storing the data in the database. Figure 6.4 displays the behavior of two process variables of the type of analog input during a time interval of 24 h of continuous operation. Each of the two variables corresponds to one of the solutions implemented in this work: the solution based on the use of LabVIEW and the one based on the standard EPICS system. The timestamps observed are obtained from the server side, the LabVIEW RT system and the CODAC IOC, respectively. The figures show the distribution of the processing period around the theoretical period of 1 s for 24 h. The analysis of the data obtained, which is shown in Figure 6.4 and summarized in Table 6.2, indicates very good performance with similar jitter in both cases. That is, the results show on the one hand that no data was lost during the experiment and on the other, that the time interval was very precise.

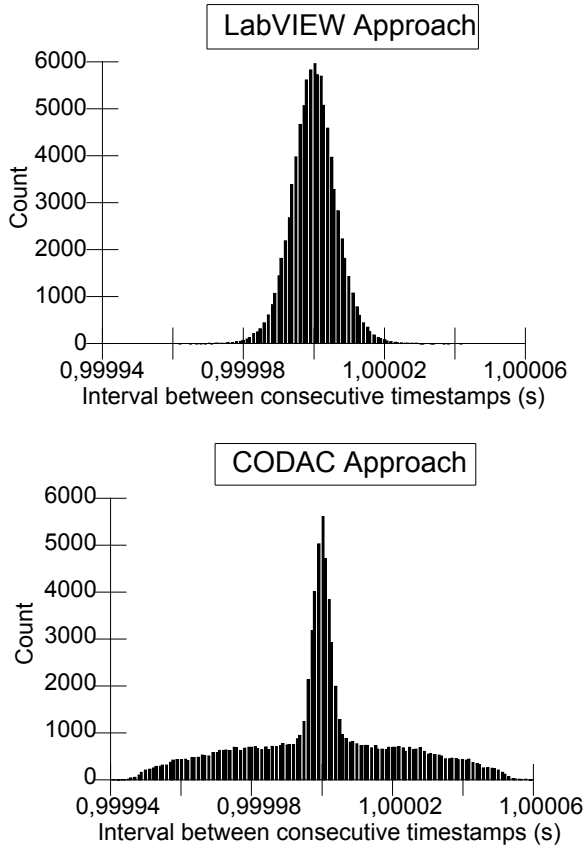

Figure 6.4. – Behavior of one of the variable pairs considered for the comparison, showing the jitter of the processing period running continuously for 24 h.

	Mean error	Std. Deviation
LabVIEW RT	$2.3 \cdot 10^{-11}$	$6.407 \cdot 10^{-6}$
Standard EPICS	$4.5 \cdot 10^{-5}$	$6.74 \cdot 10^{-3}$

Table 6.2. – Main statistics results of both system to be compared.

Moreover, the rest of the signals involved in the comparison experiment behave in a similar way. At the present status of the study the tests have been running continuously for several days. However, a longer time interval (months) is

required to fully ensure the adequate performance of the proposed approach for the fast controller integration and to provide more reliable comparison results.

The present test bench is also used for the validation of the archiving system. By using the Hyperarchiver archiving tool, the time span between consecutive timestamps can be analysed. This data can be later be used to analyse the quality of the archiving process. Thus, the test bench provides an appropriate mechanism for the improvement and adjustment of the parameters of the archiving system, which eventually might help avoid data loss. The proposed test bench can be used for long-term tests, analysing the presence of failures in both solutions, in order to perform a complete reliability test.

Worst Case Test Results

The main objective of the proposed fast controller is oriented to the systems which require a high performance with a high-speed data acquisition and time synchronization. It is not oriented to applications aimed to a high data volume processing. However, in order to test the behavior of the system in different scenarios, the next situations have been also considered:

- An increase in the number of access in the EPICS network. The increment of get petitions does not lead to any problem when packets up to 180 PVs are requested at once.

- An increase in the number of records up to 16 000 in each controller, i.e., the number of PVs is approximately eight times higher. The results are similar in both cases, showing a good behaviour. However, the deployment of the application, that is, the initialization time, is higher using the proposed solution than the standard solution. Considering a large number of PVs, for instance several thousands, this initialization time can be several tens of seconds longer. Anyway, this is not a severe implementation drawback, since operational startup time is generally long and the extra time needed is not excessive in a typical scenario.

- An increase in the number of EPICS monitors. Monitors are a mechanism that provide a user program with data from the database without the user having to constantly poll the database. Through channel access, monitors inform the operator interface, archivers, alarm handlers and other user programs when a database field changes. The standard IOC does not present additional issues. However, when the number of synchronous EPICS monitors exceeds 80 monitors, the LabVIEW-based

system presents robustness problems, can become unstable; and randomly hangs on data requests.

The results obtained show that the standard solution is more robust in applications with a large number of PV monitors. A standard EPICS IOC supports a large number of monitors without a significant performance degradation. Several hundred of simultaneously changing PVs run correctly. However, the LabVIEW RT-based solution running an EPICS server hangs with less than 100 monitors. This fact is not a surprise; the standard configuration is preferable to be used when a large number of PVs is required, including simultaneous monitoring since is specially well suited for working as a data server. In any case, this issue is not an important drawback of the proposed solution, since it is oriented to control applications with high-processing requirements but not with high data volume. That is, the nonstandard solution under study is well suited for applications with high computation needs, performing as a fast controller with a, relatively, low number of PVs.

6.5. Summary and conclusions

In this chapter, a performance test for a nonstandard EPICS fast controller is presented. The motivation is to study the validation of the mentioned fast controller in terms of repeteabilty to see if it can be used as a suitable solution for the integration of systems based on LabVIEW as development tool on EPICS networks, such as the applications presented in Chapters 4 and 5.

With this aim, a laboratory testbench was developed to carry out a comparison between two systems; one based on the nonstandard fast controller and the other following a standard EPICS architecture, both using similar hardware setups. The testbench emulates real schemes present in particle accelerators to be as complete as possible.

The results obtained in the experimental comparison are positive, since the proposed methodology gives similar results comparing to a standard solution while the development process is faster. In any case, the results show a reliable system, comparable with other solutions used nowadays.

However, additional long term tests are needed to full validation of the proposed architecture.

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CHAPTER 7

Conclusions and future work

This thesis is devoted to new technologies for diagnostic and control tools oriented to particle accelerators. The rationale behind this research line was to contribute to the research and development of new technologies in the field of diagnostics and control oriented to particle accelerators. This is one of the main work areas of the *GAUDEE Experimental Control Research Group* and *RF and Microwave Research Group* of the department of Electricity and Electronics of the University of the Basque Country UPV/EHU and its is considered strategic by both the University of the Basque Country and the Basque Government.

The two main contributions of the current work are two applications in the mentioned areas: a BPM on one hand and a LLRF control system on the other. These two tools are present in every particle accelerators, both being essential systems for the proper operation of the machine. Therefore, they need to be continuously improving the features offered to enhance the performance of the overall system, requiring a very dynamic research work around them.

Due to the rapid performance increase in the digital hardware, digital solutions in diagnostic and control oriented to particle accelerators are becoming more usual in recent times. They show several advantages over classic analog based systems and some drawbacks, which must be solved. Building these applications using flexible and modular architecture like National Instruments PXIe provides an added value to the solution. This way, the tools developed can be easily and quickly adapted to new requirements, obtaining tools very well suited for rapid prototyping purposes. In addition, the use of flexible tools allows the testing of new strategies easily, facilitating the solution of the inherent disadvantages of digital implementations.

Real facilities are not easily accessible to test new solutions, making the introduction of new devices and equipment into the system a difficult task. For these reasons, realistic complete testbenches have been designed and implemen-

ted. Using them, the applications developed have been tested simulating real facility conditions, allowing the obtention of measurements and results that have validated the proposed systems.

Finally, this thesis has also dealt with the integration of the presented diagnostic and control tools in an EPICS network, making an experiment related to the performance of a nonstandard EPICS controller that integrates LabVIEW based solutions.

7.1. Conclusions

The general conclusions derived from the chapter structure in the present thesis are presented below.

I. Use of flexible and modular digital hardware. The selection of a modular and easily reconfigurable digital hardware has demonstrated to be a very powerful tool for the rapid development of prototypes and the test of new implementations. In addition, the use of LabVIEW as main design tool has been a key for the rapid development process. In particular, LabVIEW and the FlexRIO technology allows the design of applications in real-time systems and FPGAs using an unified platform.

II. Subsampling technique. The theoretical background provided by the Nyquist-Shannon theorem has resulted very interesting in the field of particles accelerators, due to the characteristics of the RF signals involved in those systems. The main advantage provided by the use of the subsampling techniques is the reduction of the sampling rate, although the subsequent digital processing must be carefully carried out in order to get the necessary accuracy in the measurement. The prototypes presented in this thesis make use of this technique obtaining very satisfactory results.

III. Design and implementation of a digital BPM application. A successful implementation is presented in Chapter 4. This diagnostic tool is based on the PXIe platform from National Instruments and is fully operated using the LabVIEW environment. The system presented is mainly digital, and provides a highly reconfigurable and modular solution. In order to carry out this application, the subsampling sampling technique introduced in Chapter 3 has been used.

The system is completed with a testbench in order to test the tool developed in the laboratory, obtaining satisfactory results. One of the most important characteristics of the BPM presented is that has been tested under realistic conditions and that it can be directly installed in a real installation, without important modifications.

IV. Design and implementation of a digital LLRF control system. This LLRF system is presented in Chapter 5. Following the same philosophy as in the BPM above, a digital solution specially suited for rapid prototyping is designed. It is also based on the PXIe architecture, and uses FPGA technology to develop the required fast feedback loops. The system developed, that consist basically in the regulation of a cavity's RF field's amplitude and phase along with its resonance frequency tuning, also takes advantage of subsampling and is tested using a complete testbench where the central element is a resonant RF cavity.

The results obtained have been satisfactory, developing a successful digital LLRF with the desired features and meeting the specifications required. The system presented has been designed following the specifications of a heavy ion source. However, the proposed solution is able to be easily modified to fulfil the specifications required by other kinds of ion sources.

V. Performance test of a nonstandard EPICS fast controller. A study for the validation of a nonstandard EPICS fast controller in terms of repeteabilty is presented in Chapter 6. The goal is to see if it can be used as a suitable solution for the integration of systems based on LabVIEW as development tool in EPICS networks, one of the most used control standards in large scientific facilities.

The test is designed by facing two systems against each other; one based on the nonstandard fast controller for LabVIEW and the other following a standard EPICS architecture, both using similar hardware setups. The testbench emulates real schemes present in particle accelerators to be as complete as possible.

Results are positive, showing a reliable system. The proposed methodology gives similar, or even better, results compared to a standard solution in the case of fast control necessities, with the advantage of having a faster development process. On the contrary, the analysis shows that the proposed solution is not well suited for use as an EPICS server, where a large number of monitors are involved.

To summarize, the following points describe the most relevant contributions

of the present thesis.

- The study of advanced digital and sampling techniques with the aim of implementing them later on in the applications developed.
- The design and development of a digital BPM and LLRF control system, both centered around obtaining the most flexible, reconfigurable and modular solution posible.
- The tests of the aforementioned applications through complete testbenchs suited for laboratory testing.
- The realization of a performance test for a nonstandard EPICS fast controller in order to validate its usage along with the diagnostic and control applications developed.

7.2. Future work

The research work done in this thesis leaves the door open to new research and development lines, in short and longer term. The most relevant are listed below:

BPM linearization techniques. Measurements obtained with button based BPMs suffer from nonlinear effects that must be compensated for obtaining the necessary accuracy. The initial linearization methods has been applied with good results. However, other linearization techniques can be useful in order to improve the measurement accuracy. The study of this techniques is very interesting to improve the results obtained.

Microphonics. Microphonics are a inherent phenomenon in beam position monitors and LLRF control systems. Their influence can cause unwanted distortions in the measurements. As an example, the study of the effect of the vacuum system is planed to be performed in the presented BPM testbench. In this case, the microphonic effects are caused by the vacuum system pumps vibrations. Therefore, a study of this effect becomes relevant in order to optimize the presented tools.

New control architectures. In the feedback loops of the LLRF systems, PID controllers are implemented. It is proposed to test new control strategies, such as more robust controllers, Smith predictors or improved minimum-detection

algorithms in the case of the frequency tuning loop. In addition, the study of improved implementation techniques based on the subsampling technique for different control algorithms is also an interesting research line.

Tests in a real facility. All the measurements performed and test of both applications have been carried out in the laboratory, taking advantage of the respective testbenchs developed. Shortly, the LLRF system is going to be tested in a real accelerator facility, more concretely in a RF cavity at the ISIS pulsed neutron and muon source [2] at the Rutherford Appleton Laboratory [1]. The characteristics of this facility are very different from the reference specifications used in this thesis. However, the flexibility of the proposed solution allows the employment of the system for the achievement of the ISIS source specifications.

Long term tests. Regarding the test of the nonstandard EPICS fast controller performed, a longer term experiment would be interesting as these applications are designed to be running in a non-stop mode for periods of months.

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CHAPTER 8

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APPENDIX A

Implementation technical details

The present appendix gives additional information about the technical implementation of the digital signal processing in LabVIEW, in particular centered around the solutions that are based in the FPGA module features. First, the employed synchronization methods between parallel processing loops are described. Next, how has been dealt with the input and output module clocks is introduced. It is also described the use of the high throughput math functions. Finally, some of the applied specific solutions are detailed.

A.1. High speed processing

In this thesis work, the main implementation difficulties when developing the diagnostic and control tools presented in Chapters and , come from the time constraints, specially in the LLRF control system. The feedback loop must be closed in the order of few microseconds to be able to regulate the amplitude and phase of the RF fields. This is specially challenging in digital LLRF, since latencies are usually higher compared to their analog counterparts (as seen in Chapter).

In order to achieve such fast digital signal processing, FlexRIO cards based in FPGA technology have been employed, which are introduced in Chapter . These cards, along with the mechanisms provided by LabVIEW FPGA module, offer the needed throughput to develop high performance applications. In the next sections, the key characteristics of the implementation related to the high speed processing are listed, describing the used solutions and mechanisms.

Synchronization

In the presented solutions, loops executing at different rates are employed, running in parallel. These loops share variables, so the management of the structures used to share data becomes critical. Two main types can be identified:

- Local FIFOS: used to pass data between loops in the same FPGA.
- Peer-to-Peer FIFOs: used for data communication between FPGAs, the data acquisition card and the generation card in this case.

Handshaking is a vital tool to ensure a proper operation in FPGA cards. This refers to the communication between two nodes that establishes the parameters for continued communication. For a given block diagram node in a single-cycle Timed-Loop (SCTL), handshaking determines when the following actions occur. SCTLs are specific timed loops for FPGAs, in which their timing corresponds exactly to the clock rate of the FPGA clock you specify. In this kind of cycles, handshaking is necessary because multi-cycle nodes need more than one cycle to compute valid data, but the SCTL forces these nodes to return data every clock cycle. Therefore, multi-cycle nodes do not return valid data every clock cycle. To ensure the numerical accuracy of an algorithm, nodes that depend on this data must know whether the data is invalid or valid.

The management of the local FIFOs is based on the *Timed Out?* handshaking terminal of the LabVIEW function. In the READ mode of the FIFOs, This

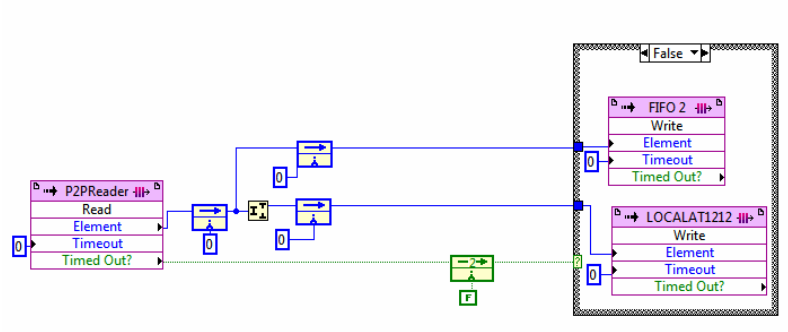

Figure A.1. – Example of the use of the *Timed out?* terminal of the FPGA FIFOs in LabVIEW in order to perform the synchronization of the data communication between different loops.

terminal returns TRUE if an element is not available in the FIFO before the function completes execution. If *Timed Out?* is TRUE, Element is undefined. In the WRITE mode, *Timed Out?* returns TRUE if space in the FIFO is not available before the function completes execution. This way, the synchronization between FIFOs located in loops running at different rates can be carried out. Figure A.1 shows an example of a Peer-to-Peer FIFO in READ mode, whose terminal *Timed Out?* is employed to control the writing to subsequent FIFOs, applying a delay of two samples to compensate the latency of the peer-to-peer streaming.

Clock rate management

In order to achieve the maximum possible bandwidth in the feedback loop, the execution of the code must be performed as fastest as possible. The hardware limitations when setting the clock rate at which the code will run comes from the longest combinational path implemented. The longer the biggest path, the lower the execution clock is set.

To illustrate, in the case of the LLRF system, the main data processing (where the IQ demodulation and the PID controllers are implemented) has been set to 50 MHz. However, the data acquisition is performed with a clock (IOModuleClock) at 250 MS/s, which means that all the acquires data can not be processed. To solve this, an algorithm that discards the unnecessary samples has been implemented. As shown in Figure A.2, this implements a handshaking method to guarantee a proper execution.

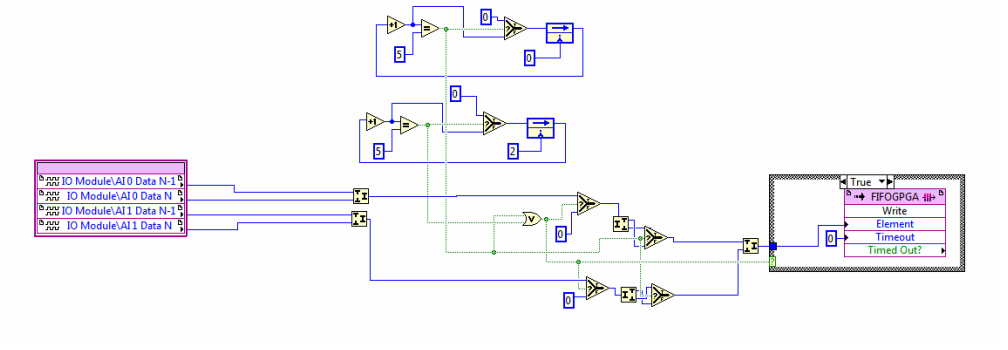

Figure A.2. – Algorithm to adapt the acquired data volume to the data that can be processed.

The generation cards produces samples at 1.25 GS/s (governed by its own clock, IOModuleclock), but the data read from the peer-to-peer correspond to data processed at 50 MHz. So, similarly to the previous case, an algorithm has been designed and implemented to hold the data in the output ports at 1.25 GS/s until a new value is available. A snapshot of the aforementioned process is shown in Figure A.3.

High Troughput Math

LabVIEW provides High Throughput Math functions to perform high throughput math and analysis with FPGAs. These functions are similar to the Numeric functions but support higher throughput rates, handshaking terminals, input/output registers, and automatic pipelining. They can be placed inside a SCTL, ensuring that they will be performed in a single clock tick.

High Troughput Math functions use a fixed-point data type. In the solutions presented, an exhaustive work has been done to adapt the word-length of the data used in every operation in order to optimized the resource consumption. Figure A.4 shows the implementation of two parallel PID controllers using fixed-point data types and High Troughput Math functions and taking advantage of the features provided by them: handshaking and input/output registers to name a few.

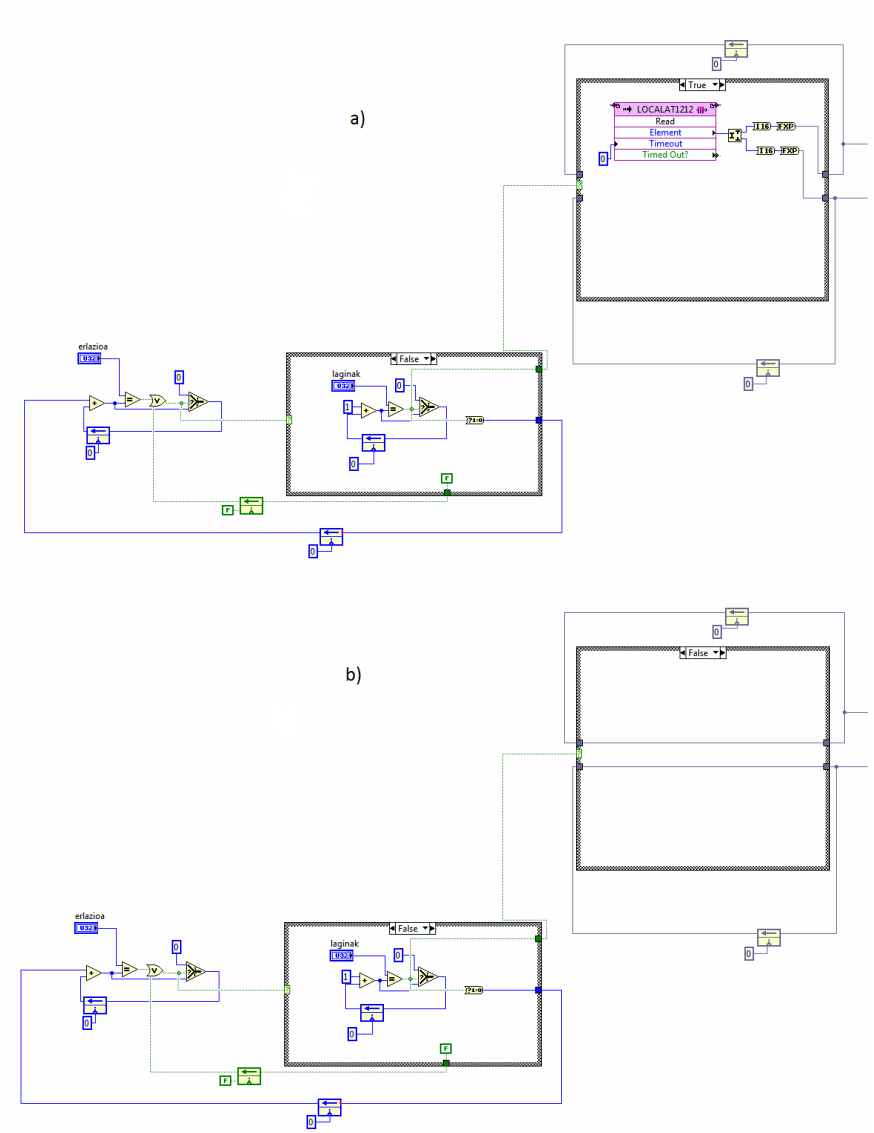

Figure A.3. – Algorithm to adapt the generated data rate to the data that is processed. The upper a) corresponds to the generation of a new value, while the b) holds the value until a new one is processed.

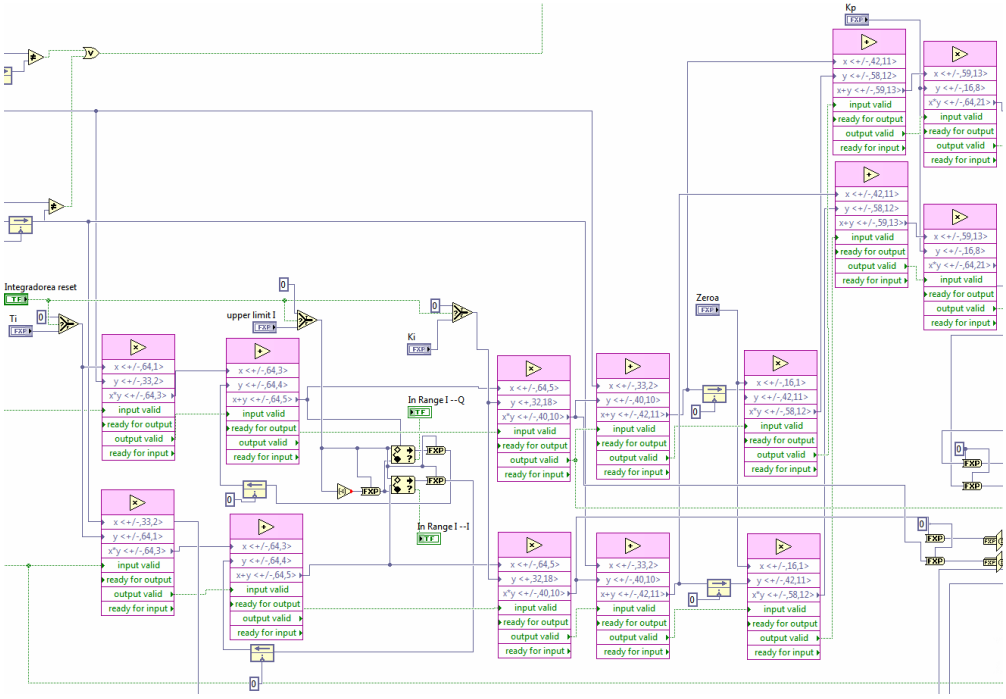

Figure A.4. – Implementation of two parallel PID controllers in a FPGA card using High Troughput Math functions.

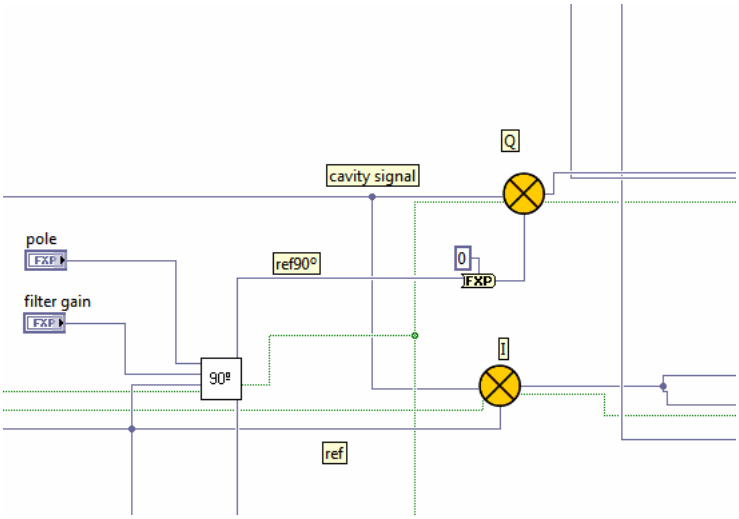

Figure A.5. – Snapshot of the mixing stage required for the I/Q modulation, where the cavity output signal it mixed with the reference signal and with the same signal shifted in phase.

Implementation details

With the aim of optimizing the throughput of the digital signal processing and having a closer control over it, the required functions in the I/Q demodulation have been implemented using low level mathematical functions, avoiding specific functions (filters...) provided by LabVIEW. The main examples are:

- The signal mixing. At this point, the acquired cavity signal is mixed with the reference signal on the one hand, and with the same reference signal shifted 90 degrees in phase on the other, thus obtaining I and Q signals respectively. This is shown in Figure A.5.

- The 90 degree phase-shift of the reference is shown in Figure A.6.

- The low-pass filter to obtain the I and Q signals at DC can bee seen in Figure A.7.

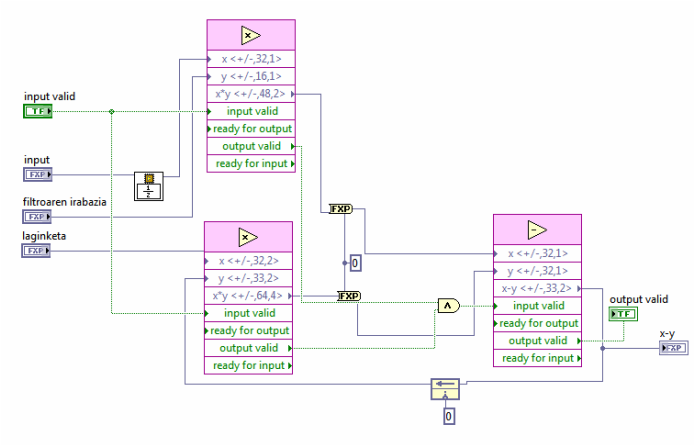

Figure A.6. – Implementation of the 90 degree phase shift of the reference signal by means of a discrete filter.

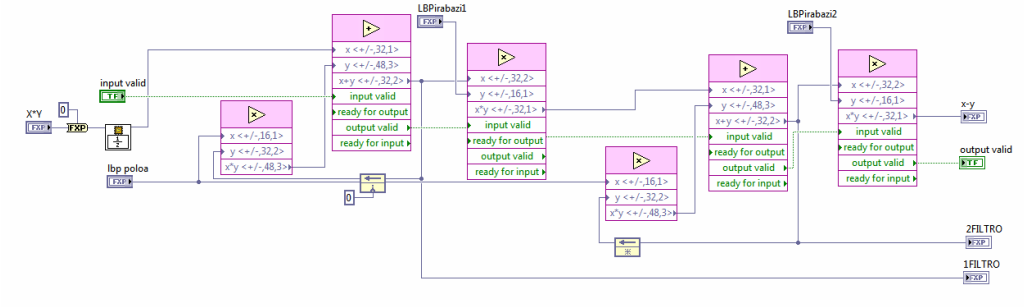

Figure A.7. – Snapshot of the developed low-pass filter for the mixing products using a discrete filter.