eman ta zabal zazu

# Bilboko Ingeniaritza Eskola

**Industria Elektronikaren eta Automatikaren Ingeniaritzako Gradua**

## Gradu Amaierako Lana

2015 / 2016

**(IBILGAILU AUTONOMO ERROBOTIZATUAREN KONTROLA)**

# 3.DOKUMENTUA: ERABILERA ESKULIBURUAK


| **IKASLEAREN DATUAK** | **ZUZENDARIAREN DATUAK** |
|---|---|
| IZENA: ENEKO | IZENA: KOLDO |
| ABIZENAK: PUMAREJO FRADUA | ABIZENAK: BASTERRETXEA OYARZABAL |
| | SAILA: TEKNOLOGIA ELEKTRONIKOA |
| SIN.: | SIN.: |
| DATA: | DATA: |


MODUA:

- ❑ JATORRIZKOA
- ❑ KOPIA

# AURKIBIDEA

# 1 DC Motorra

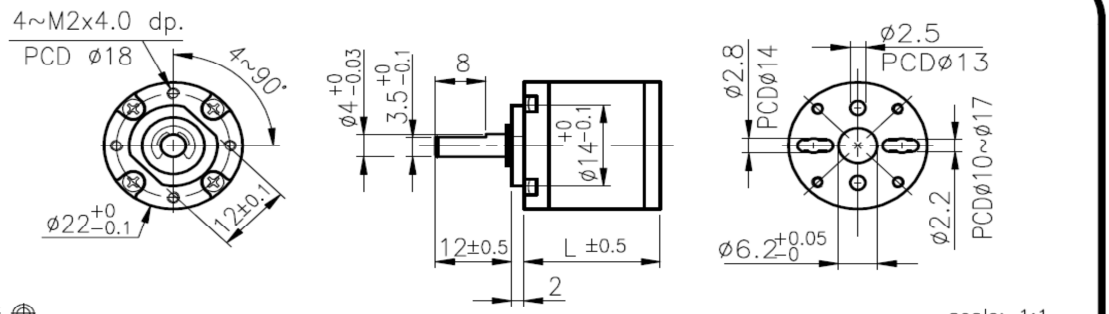
行星齒輪 (Planetary gear)

IG-22 GEARHEAD SERIES

# IG-22

| | | | |
|---|---|---|---|
| 外殼材質 Housing material | 金屬 metal | 背隙(無負荷時) Backlash,at no-load | ≦ 3° |
| 輸出軸承型式 Bearing at output | | 含油軸承 Sleeve bearings | 滾珠軸承 Ball bearings |
| 徑向負荷 Radial load ( 10mm from flange ) | | ≦ 0.8 kgf | ≦ 1 kgf |
| 軸向負荷 Shaft axial load | | ≦ 0.6 kgf | ≦ 0.6 kgf |
| 主軸最大承受壓入力 Shaft press fit force,max. | | ≦ 5 kgf | ≦ 5 kgf |
| 徑向間隙 Radial play of shaft | | ≦ 0.05 mm | ≦ 0.04 mm |
| 軸向間隙 Thrust play of shaft | | ≦ 0.2 mm | ≦ 0.2 mm |

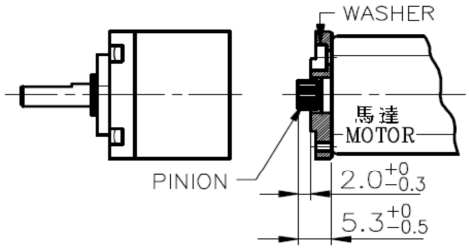
外形尺寸 APPEARANCE SIZE




馬達齒輪型式 /PINION SPECIFICATIONS

| | | |
|---|---|---|
| 模數 Module | 0.3 | |
| 齒數 No. of teeth | 13 | 16 |
| 壓力角 Pressure angle | 20° | |
| 孔徑 Hole diameter | ø1.98 | |
| 減速比 Reduction ratio | 1/4 ,1/16 ,1/19 ,1/62<br>1/72 ,1/84 ,1/104 ,1/231<br>1/270 ,1/316 ,1/370 ,1/455<br>1/1014 ,1/1249 ,1/1621 ,1/1996 | 1/14<br>1/53<br>1/198<br>1/742 |

馬達裝卸方法 /MOTOR INSTALLATION




★ 使用相對溼度: 20%~85%RH Operating relative humidity

★ 使用溫度範圍: −10℃~+60℃ Operating temperature range

標準減速比型式 /GEARBOXES SPECIFICATIONS

| 減速比 Reduction ratio | 精確減速比 Exact reduction ratio | 定格容許扭力 Rated tolerance torque | 瞬間容許扭力 Max momentary tolerance torque | 效率 Efficiency | L | 重量(含油軸承) Weight ( g ) Sleeve bearings | 重量(滾珠軸承) Weight ( g ) Ball bearings |
|---|---|---|---|---|---|---|---|
| 1/4 | 4 5/13 | 1.0 kgf-cm Max. | 3.0 kgf-cm | 80% | 14.40 | 27.0 | 26.0 |
| 1/14 | 14 1/16 | 1.5 kgf-cm Max. | 4.5 kgf-cm | 70% | 18.05 | 31.0 | 30.0 |
| 1/16,1/19 | 16 23/52,19 38/169 | 1.5 kgf-cm Max. | 4.5 kgf-cm | 70% | 18.05 | 31.0 | 30.0 |
| 1/62,1/84 | 61 137/208,84 645/2197 | 2.0 kgf-cm Max. | 6.0 kgf-cm | 60% | 21.70 | 35.0 | 34.0 |
| 1/104 | 103 688/845 | 2.0 kgf-cm Max. | 6.0 kgf-cm | 60% | 21.70 | 35.0 | 34.0 |
| 1/231 | 231 183/832 | 2.5 kgf-cm Max. | 7.5 kgf-cm | 50% | 25.35 | 40.0 | 39.0 |
| 1/316 | 316 887/8788 | 2.5 kgf-cm Max. | 7.5 kgf-cm | 50% | 25.35 | 40.0 | 39.0 |
| 1/370 | 369 16992/28561 | 2.5 kgf-cm Max. | 7.5 kgf-cm | 50% | 25.35 | 40.0 | 39.0 |
| 1/455 | 455 2036/10985 | 2.5 kgf-cm Max. | 7.5 kgf-cm | 50% | 25.35 | 40.0 | 39.0 |
| 1/1014 | 1013 8767/10816 | 3.0 kgf-cm Max. | 9.0 kgf-cm | 40% | 29.00 | 44.0 | 43.0 |
| 1/1621 | 1620 197397/371293 | 3.0 kgf-cm Max. | 9.0 kgf-cm | 40% | 29.00 | 44.0 | 43.0 |
| 1/1996 | 1995 116052/142805 | 3.0 kgf-cm Max. | 9.0 kgf-cm | 40% | 29.00 | 44.0 | 43.0 |



April 2010

# 2 Kodetzailea

譯碼器 (Encoders)

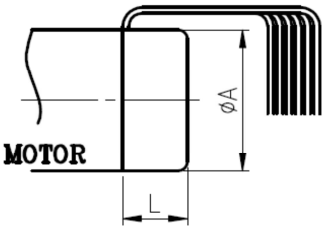
ENCODERS
MAGNETIC
SERIES

# Magnetic Encoders

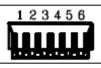
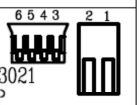
- 雙向霍爾作用譯碼器
  Two Channel Hall Effect Encoder
- 單向霍爾作用譯碼器
  One Channel Hall Effect Encoder

★ 使用相對溼度: 20%~85%RH Operating relative humidity
★ 使用溫度範圍: −10°C~+60°C Operating temperature range

外形尺寸 APPEARANCE SIZE



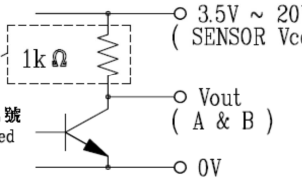

☆ WITHOUT CAP

| Motor øA | CAP L | COUNTS POLES OF PER TURN(PPR) current | limit. | Wire Type Length | Connector Type |
|---|---|---|---|---|---|
| ø12 | ☆6.5 | 2, 6 (1, 3) | 6 (3) | UL1061 AWG26 100mm | JST ZHR-6 P=1.5-6P  |
| ø15.4 | ☆6.5 | 2, 6 (1, 3) | 6 (3) | | |
| ø20.3 | ☆8.5 | 2, 6 (1, 3) | 6 (3) | UL1007 AWG24 100mm | JST PHR-6 P=2.0-6P  |
| ø30.0 | 12.6 | 2, 6, 14 (1, 3, 7) | 14 (7) | | |
| ø32 | 14.3 | 14 (7) | 14 (7) | | |
| ø36 | 13.5 | 14 (7) | 14 (7) | | |
| ø42.5 | 15.5 | 2, 10 (1, 5) | 10 (5) | UL1007 AWG24 UL1007 AWG18 100mm | JST PHR-4 P=2.0-4P  Molex 09-50-3021 P=3.96-2P |
| ø52 ø54 | 18.0 | 2, 10 (1, 5) | 10 (5) | | |

電氣特性
ELECTRICAL CHARACTERISTICS

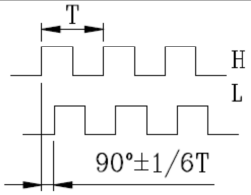
| 規格特性 CHARACTERISTICS | 代號 SYMBOL | 測試條件 TEST CONDITIONS | 極小 MIN. | 基準 REF. | 最大 MAX. | 單位 UNITS |
|---|---|---|---|---|---|---|
| 輸入電壓 Supply Voltage | Vcc | --- | 3.5 | – | 20 | V |
| 輸出飽和電壓 Output Saturation Voltage | Vce(sat) | Vcc=14V ; Ic=20mA | – | 300 | 700 | mV |
| 輸出漏電電流 Output Leakage Current | Icex | Vce=14V ; Vcc=14V | – | < 0.1 | 10 | μV |
| 輸入電流 Supply Current | Ice | Vcc=20V Output open | – | 5 | 10 | mA |
| 輸出上升時間 Output Rise Time | $t_r$ | Vcc=14V ; $R_L$=820Ω; $C_L$=20pF | – | 0.3 | 1.5 | μS |
| 輸出下降時間 Output Fall Time | $t_f$ | Vcc=14V ; $R_L$=820Ω; $C_L$=20pF | – | 0.3 | 1.5 | μS |

輸出電路
Output Circuit :




需外加電阻才能產生訊號
Extra Varistor(1KΩ) needed

輸出波形
Output Wave :




Two Channel Encoder
Connections :

1. Black : −MOTOR
2. Red : +MOTOR
3. Brown : HALL SENSOR Vcc
4. Green : HALL SENSOR GND
5. Blue : HALL SENSOR A Vout
6. Purple : HALL SENSOR B Vout

One Channel Encoder
Connections :

1. Black : −MOTOR
2. Red : +MOTOR
3. Brown : HALL SENSOR Vcc
4. Green : HALL SENSOR GND
5. Blue : HALL SENSOR A Vout
6. Purple : EMPTY



April 2010

# 3 H-zubia

## Digilent PmodHB5™
## 2A H-Bridge Reference Manual

Revision: February 26, 2007
Note: This document applies to REV D of the board.

DIGILENT®
www.digilentinc.com
215 E Main Suite D | Pullman, WA 99163
(509) 334 6306 Voice and Fax

### Overview

The Digilent PmodHB5™ 2A H-Bridge Module (the HB5) is an ideal solution for robotics and other applications where logic signals are used to drive small to medium-sized DC motors, such as the Digilent motor-gearbox.

Features include:

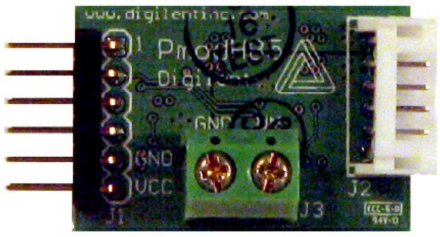
- a 2A H-bridge circuit for voltages up to 12V
- a JST 6-pin connector for direct connection of Digilent motor-gearboxes
- a 2-channel quadrature encoder with Hall-effect sensors to detect motor speed
- small form factor (0.8" x 1.30")

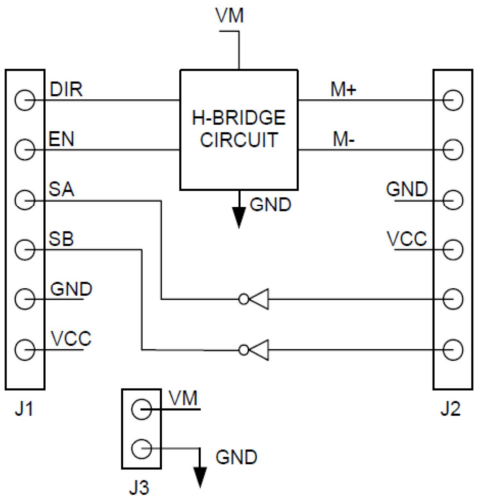
### Functional Description

The HB5 works with power supply voltages from 2.5V to 5V, but is normally operated at 3.3V as this is the supply voltage on most Digilent system boards.

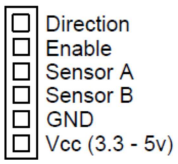
The HB5 is designed to work with either Digilent programmable logic system boards or embedded control system boards. Most Digilent system boards, such as the Nexys, Basys, or Cerebot, have 6-pin connectors that allow the HB5 to plug directly into the system board or to connect via a Digilent 6-pin cable.

Some older Digilent boards may need a Digilent Module Interface Board (MIB) and a 6-pin cable to connect to the HB5. The MIB plugs into the system board and the cable connects the MIB to the HB5.




Motor power is provided via a two-pin terminal block (J3) that can accommodate up to 18-gauge wire. The HB5 circuits can handle motor voltages up to 12V.




**HB5 6-Pin Header, J1**

The HB5 is controlled by a system board connected to J1. The motor rotation direction is determined by the logic level on the Direction pin. Current will flow through the bridge when the Enable pin is brought low. Motor speed is controlled by pulse width modulating the Enable pin. See below for a description of pulse width modulation. The direction of the motor should not be reversed while the Enable pin is active. If the direction is reversed while the bridge is enabled it is possible to create brief short circuits across the bridge as one leg will be turning on while the other leg is turning off. This could damage the bridge transistors.

Two Schmitt trigger buffered inputs are provided on connector J2 to facilitate bringing motor speed feedback signals to the controlling system board. The Digilent motor/gearboxes have Hall-effect sensors arranged as a quadrature encoder. These buffers have 5V tolerant inputs when operated at 3.3V.

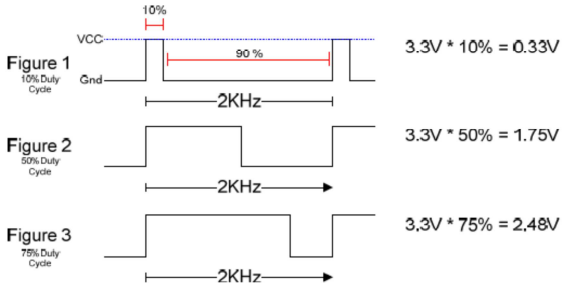
The quadrature encoder signals are a pair of square waves whose frequency is proportional to motor rotation speed and which are 90° out of phase. Motor speed can be determined by the frequency and motor rotation direction can be determined by the phase relationship of the two signals.

## Pulse Width Modulation and Motor Speed Control

In an analog circuit, motor speed is controlled by varying the input voltage to a circuit. In a digital circuit, however, only a logic high or logic low signal can be applied to the motor. Therefore, there are only two ways to control a motor digitally: use a variable resistance circuit to control the motor voltage, or, pulse the power to the motor. Since variable resistance circuitry is expensive, complicated, and wastes much energy in the form of heat, the better solution is pulse width modulation (PWM).

Pulse width modulation is a digital method of transmitting an analog signal, and while it is not a clean source of DC output voltage, PWM suits motors relatively well.

The figures below illustrate a PWM system with an input frequency of 2KHz. The motor speed is controlled by adjusting the time each wave is at peak output power. Figure 1 shows a 10% "duty cycle" where the signal is logic high for only 1/10 of a wavelength. This 10% positive peak is equal to 10% of the total 3.3V input, or 0.33V (shown in Figure 2). Figures 2 and 3 show duty cycles of 50% and 75%, respectively.




An H-bridge is a voltage amplification and direction control circuit that is used to format the signal to the appropriate motor voltage and polarity to spin the motor.

While voltage is being applied, the motor is driven by the changing magnetic forces. When voltage is stopped, momentum causes the motor to continue spinning a while. At a high enough frequency, this process of powering and coasting enables the motor to achieve a smooth rotation that can easily be controlled through digital logic.

PWM has two important effects on DC motors. Inertial resistance is overcome more easily at startup because short bursts of maximum voltage achieve a greater degree of torque than the equivalent DC voltage. Another effect is a higher level of heat generation inside the

motor. If a pulsed motor is used for an extended time, heat dissipation systems may be needed to prevent damage to the motor. Because of these effects, PWM is best used in high-torque infrequent-use applications such as airplane flap servos and robotics.

PWM circuits can also create radio frequency interference (RFI) that can be minimized by locating motors near the controller and by using short wires. Line noise created by continually powering up the motor may also need to be filtered to prevent interference with the rest of the circuits. Placing small ceramic capacitors directly across the motor terminals and between the motor terminals and the motor case can be used to filter RFI emissions from the motor.

For more information see www.digilentinc.com.

# 4 Serbomotorea

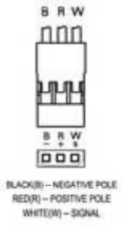
**SM-S2309S MOTOR**

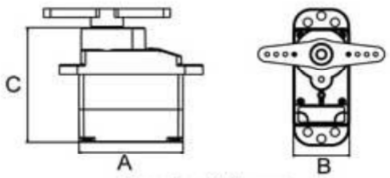

**No. :** SM-S2309S

**Size:** 22.9x12.3x22.2mm / 0.9x0.49x0.87in

**Weight:** 0.35oz

**Specifications:** Micro analog servo,4 plastic gears + 1 metal gear




*Dimension（Unit：mm）*

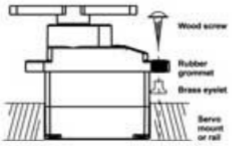



*Diagram of installation*

| Products specification | | | | | | | | Technical parameters | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Size(mm) | | | | | Weight | | Wire | 4.8V | | | 6V | | | Rotation angle |
| | | | | | | | | Speed | Torque | | Speed | Torque | | |
| A | B | C | D | E | g | oz | cm | sec/60° | kg•cm | oz•in | sec/60° | kg•cm | oz•in | |
| 22.9 | 12.3 | 22.2 | - | - | 9.9 | 0.35 | 20.0 | 0.11 | 1.1 | 15.3 | 0.09 | 1.3 | 18.1 | ±60° |

(Specifications are subjected to change without notice.)

**Product brochure**

Micro analog servo,4 plastic gear+ 1 metal gear.

**Products packing**

◦Packing with elevators (Elevators+PE bag)

Packaging content:Servo×1PCS、Servo arm×1bag、Manual×1PCS

Packaging specifications：Size-120×85mm、PE bag：120×85×0.07mm、Net weight-9.9g、Gross weight-11.5g

◦General packing (PE bag)

Packaging content：Packing with PE bag

Packaging specifications：PE bag size-90×85×0.07mm、Net weight-9.9g、Gross weight-11.5g

# 5 Ultrasoinu Sentsorea

Tech Support: services@elecfreaks.com

## Ultrasonic Ranging Module HC - SR04

### Product features:

Ultrasonic ranging module HC - SR04 provides 2cm - 400cm non-contact measurement function, the ranging accuracy can reach to 3mm. The modules includes ultrasonic transmitters, receiver and control circuit. The basic principle of work:
(1) Using IO trigger for at least 10us high level signal,
(2) The Module automatically sends eight 40 kHz and detect whether there is a pulse signal back.
(3) IF the signal back, through high level , time of high output IO duration is the time from sending ultrasonic to returning.
Test distance = (high level time×velocity of sound (340M/S) / 2,

### Wire connecting direct as following:

- 5V Supply
- Trigger Pulse Input
- Echo Pulse Output
- 0V Ground

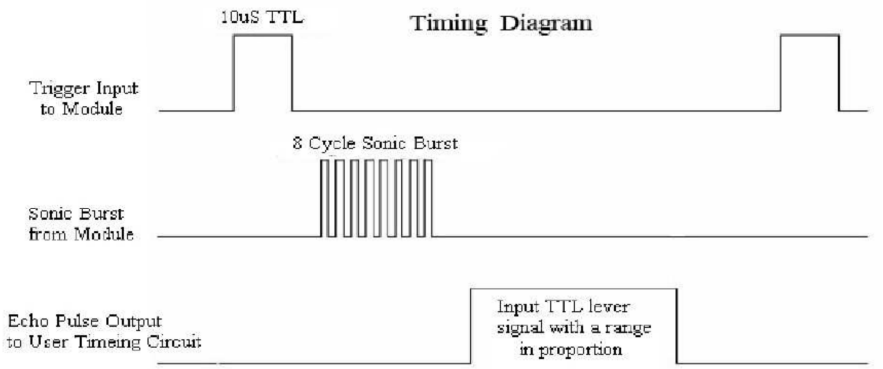
### Electric Parameter

| | |
|---|---|
| **Working Voltage** | **DC 5 V** |
| **Working Current** | **15mA** |
| **Working Frequency** | **40Hz** |
| **Max Range** | **4m** |
| **Min Range** | **2cm** |
| **MeasuringAngle** | **15 degree** |
| **Trigger Input Signal** | **10uS TTL pulse** |
| **Echo Output Signal** | **Input TTL lever signal and the range in proportion** |
| **Dimension** | **45*20*15mm** |


**Vcc Trig Echo GND**

## Timing diagram

The Timing diagram is shown below. You only need to supply a short 10uS pulse to the trigger input to start the ranging, and then the module will send out an 8 cycle burst of ultrasound at 40 kHz and raise its echo. The Echo is a distance object that is pulse width and the range in proportion .You can calculate the range through the time interval between sending trigger signal and receiving echo signal. Formula: uS / 58 = centimeters or uS / 148 =inch; or: the range = high level time * velocity (340M/S) / 2; we suggest to use over 60ms measurement cycle, in order to prevent trigger signal to the echo signal.



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## Attention:

- The module is not suggested to connect directly to electric, if connected electric, the GND terminal should be connected the module first, otherwise, it will affect the normal work of the module.
- When tested objects, the range of area is not less than 0.5 square meters and the plane requests as smooth as possible, otherwise ,it will affect the results of measuring.

**www.Elecfreaks.com**

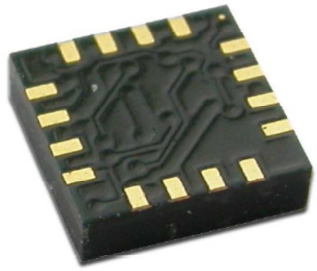
# 6 Konpas Digitala

## 3-Axis Digital Compass IC HMC5883L

Honeywell

*Advanced Information*

The Honeywell HMC5883L is a surface-mount, multi-chip module designed for low-field magnetic sensing with a digital interface for applications such as low-cost compassing and magnetometry. The HMC5883L includes our state-of-the-art, high-resolution HMC118X series magneto-resistive sensors plus an ASIC containing amplification, automatic degaussing strap drivers, offset cancellation, and a 12-bit ADC that enables 1° to 2° compass heading accuracy. The $I^2C$ serial bus allows for easy interface. The HMC5883L is a 3.0x3.0x0.9mm surface mount 16-pin leadless chip carrier (LCC). Applications for the HMC5883L include Mobile Phones, Netbooks, Consumer Electronics, Auto Navigation Systems, and Personal Navigation Devices.



The HMC5883L utilizes Honeywell's Anisotropic Magnetoresistive (AMR) technology that provides advantages over other magnetic sensor technologies. These anisotropic, directional sensors feature precision in-axis sensitivity and linearity. These sensors' solid-state construction with very low cross-axis sensitivity is designed to measure both the direction and the magnitude of Earth's magnetic fields, from milli-gauss to 8 gauss. Honeywell's Magnetic Sensors are among the most sensitive and reliable low-field sensors in the industry.

| FEATURES | BENEFITS |
|---|---|
| 3-Axis Magnetoresistive Sensors and ASIC in a 3.0x3.0x0.9mm LCC Surface Mount Package | Small Size for Highly Integrated Products. Just Add a Micro-Controller Interface, Plus Two External SMT Capacitors Designed for High Volume, Cost Sensitive OEM Designs Easy to Assemble & Compatible with High Speed SMT Assembly |
| 12-Bit ADC Coupled with Low Noise AMR Sensors Achieves 5 milli-gauss Resolution in ±8 Gauss Fields | Enables 1° to 2° Degree Compass Heading Accuracy |
| Built-In Self Test | Enables Low-Cost Functionality Test after Assembly in Production |
| Low Voltage Operations (2.16 to 3.6V) and Low Power Consumption (100 µA) | Compatible for Battery Powered Applications |
| Built-In Strap Drive Circuits | Set/Reset and Offset Strap Drivers for Degaussing, Self Test, and Offset Compensation |
| $I^2C$ Digital Interface | Popular Two-Wire Serial Data Interface for Consumer Electronics |
| Lead Free Package Construction | RoHS Compliance |
| Wide Magnetic Field Range (+/-8 Oe) | Sensors Can Be Used in Strong Magnetic Field Environments with a 1° to 2° Degree Compass Heading Accuracy |
| Software and Algorithm Support Available | Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available |
| Fast 160 Hz Maximum Output Rate | Enables Pedestrian Navigation and LBS Applications |

## HMC5883L

### SPECIFICATIONS (* Tested at 25°C except stated otherwise.)

| Characteristics | Conditions* | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Power Supply*** | | | | | |
| Supply Voltage | VDD Referenced to AGND | 2.16 | | 3.6 | Volts |
| | VDDIO Referenced to DGND | 1.71 | 1.8 | VDD+0.1 | Volts |
| Average Current Draw | Idle Mode | - | 2 | - | µA |
| | Measurement Mode (7.5 Hz ODR; No measurement average, MA1:MA0 = 00) VDD = 2.5V, VDDIO = 1.8V | - | 100 | - | µA |
| ***Performance*** | | | | | |
| Field Range | Full scale (FS) – total applied field (Typical) | -8 | | +8 | gauss |
| Mag Dynamic Range | 3-bit gain control | ±1 | | ±8 | gauss |
| Resolution | VDD=3.0V, GN=2 | | 5 | | milli-gauss |
| Linearity | ±2.0 gauss input range | | | 0.1 | ±% FS |
| Hysteresis | ±2.0 gauss input range | | ±25 | | ppm |
| Cross-Axis Sensitivity | Test Conditions: Cross field = 0.5 gauss, Happlied = ±3 gauss | | ±0.2% | | %FS/gauss |
| Output Rate (ODR) | Continuous Measurment Mode | 0.75 | | 75 | Hz |
| | Single Measurement Mode | | | 160 | Hz |
| Measurement Period | From receiving command to data ready | | 6 | | msec |
| Turn-on Time | Ready for I2C commands | | 200 | | µs |
| Gain Tolerance | All gain/dynamic range settings | | ±5 | | % |
| $I^2C$ Address | 7-bit address | | 0x1E | | hex |
| | 8-bit read address | | 0x3D | | hex |
| | 8-bit write address | | 0x3C | | hex |
| $I^2C$ Rate | Controlled by $I^2C$ Master | | | 400 | kHz |
| $I^2C$ Hysteresis | Hysteresis of Schmitt trigger inputs on SCL and SDA - Fall (VDDIO=1.8V) | | 0.2*VDDIO | | Volts |
| | Rise (VDDIO=1.8V) | | 0.8*VDDIO | | Volts |
| Self Test | X & Y Axes | | ±1.16 | | gauss |
| | Z Axis | | ±1.08 | | |
| | X & Y Axes (GN=100) | | 510 | | LSb |
| | Z Axis (GN=100) | | | | |
| ***General*** | | | | | |
| ESD Voltage | Human Body Model (all pins) | | | TBD | Volts |
| | Machine Model (all pins) | | | TBD | |
| Operating Temperature | Ambient | -30 | | 85 | °C |
| Storage Temperature | Ambient, unbiased | -40 | | 125 | °C |
| Reflow Classification | MSL 3, 260 °C Peak Temperature | | | | |
| Package Size | Length and Width | 2.85 | 3.00 | 3.15 | mm |
| Package Height | | 0.8 | 0.9 | 1.0 | mm |

## HMC5883L

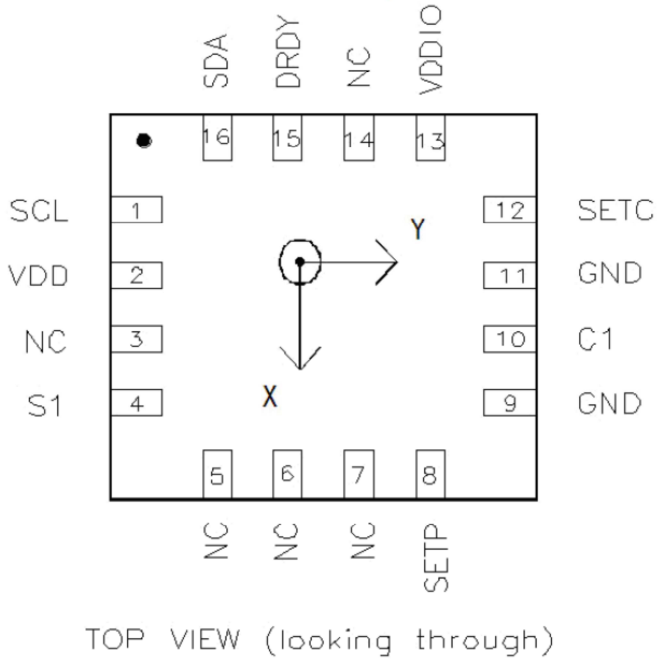
### Absolute Maximum Ratings (* Tested at 25°C except stated otherwise.)

| Characteristics | Min | Max | Units |
|---|---|---|---|
| Supply Voltage VDD | -0.3 | 4.8 | Volts |
| Supply Voltage VDDIO | -0.3 | 4.8 | Volts |

### PIN CONFIGURATIONS

| Pin | Name | Description |
|---|---|---|
| 1 | SCL | Serial Clock – $I^2C$ Master/Slave Clock |
| 2 | VDD | Power Supply (2.16V to 3.6V) |
| 3 | NC | Not to be Connected |
| 4 | S1 | Tie to VDDIO |
| 5 | NC | Not to be Connected |
| 6 | NC | Not to be Connected |
| 7 | NC | Not to be Connected |
| 8 | SETP | Set/Reset Strap Positive – S/R Capacitor (C2) Connection |
| 9 | GND | Supply Ground |
| 10 | C1 | Reservoir Capacitor (C1) Connection |
| 11 | GND | Supply Ground |
| 12 | SETC | S/R Capacitor (C2) Connection – Driver Side |
| 13 | VDDIO | IO Power Supply (1.71V to VDD) |
| 14 | NC | Not to be Connected |
| 15 | DRDY | Data Ready, Interrupt Pin. Internally pulled high. Optional connection. Low for 250 µsec when data is placed in the data output registers. |
| 16 | SDA | Serial Data – $I^2C$ Master/Slave Data |

Table 1: Pin Configurations




TOP VIEW (looking through)

Arrow indicates direction of magnetic field that generates a positive output reading in Normal Measurement configuration.

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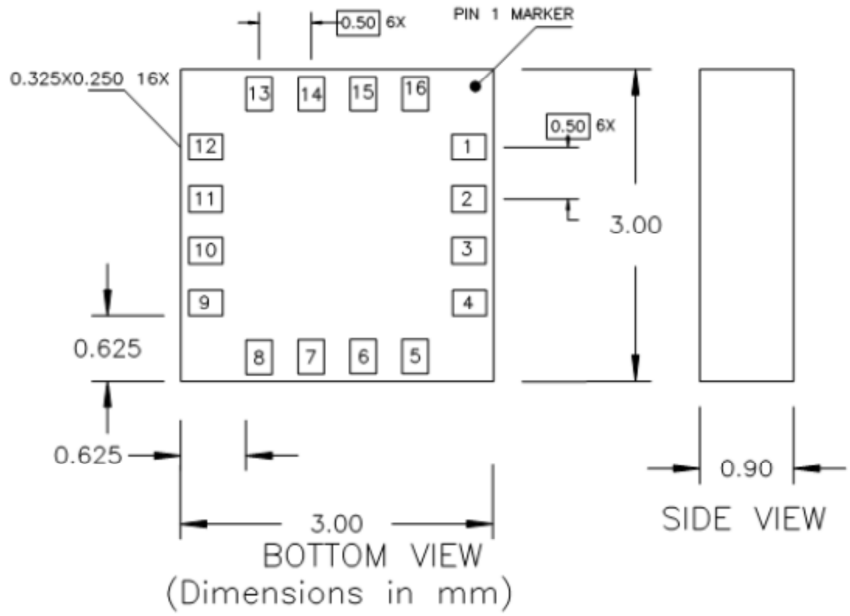
## HMC5883L

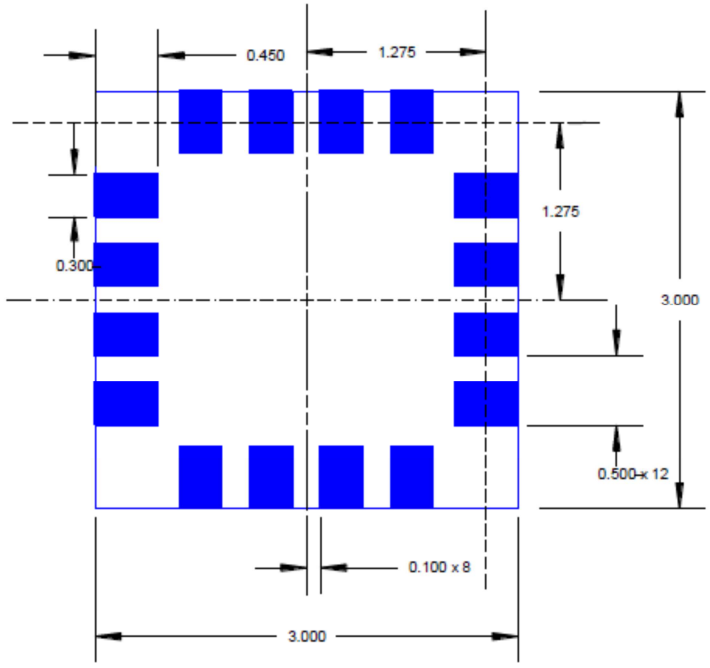
### PACKAGE OUTLINES

**PACKAGE DRAWING HMC5883L (16-PIN LPCC, dimensions in millimeters)**




### MOUNTING CONSIDERATIONS

The following is the recommend printed circuit board (PCB) footprint for the HMC5883L.




HMC5883 Land Pad Pattern
(All dimensions are in mm)

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## HMC5883L

### PCB Pad Definition and Traces

The HMC5883L is a fine pitch LCC package. Refer to previous figure for recommended PCB footprint for proper package centering. Size the traces between the HMC5883L and the external capacitors (C1 and C2) to handle the 1 ampere peak current pulses with low voltage drop on the traces.

### Stencil Design and Solder Paste

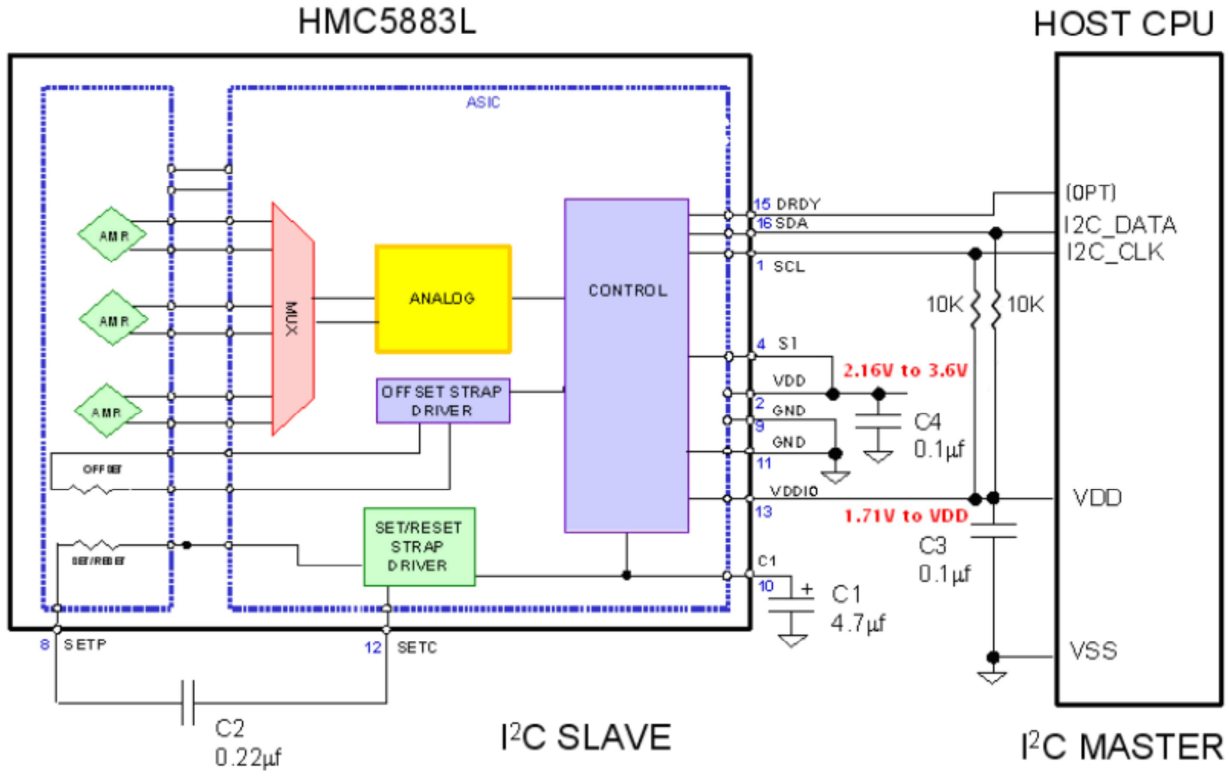
A 4 mil stencil and 100% paste coverage is recommended for the electrical contact pads.

### Reflow Assembly

This device is classified as MSL 3 with 260°C peak reflow temperature. A baking process (125°C, 24 hrs) is required if device is not kept continuously in a dry (< 10% RH) environment before assembly. No special reflow profile is required for HMC5883L, which is compatible with lead eutectic and lead-free solder paste reflow profiles. Honeywell recommends adherence to solder paste manufacturer's guidelines.

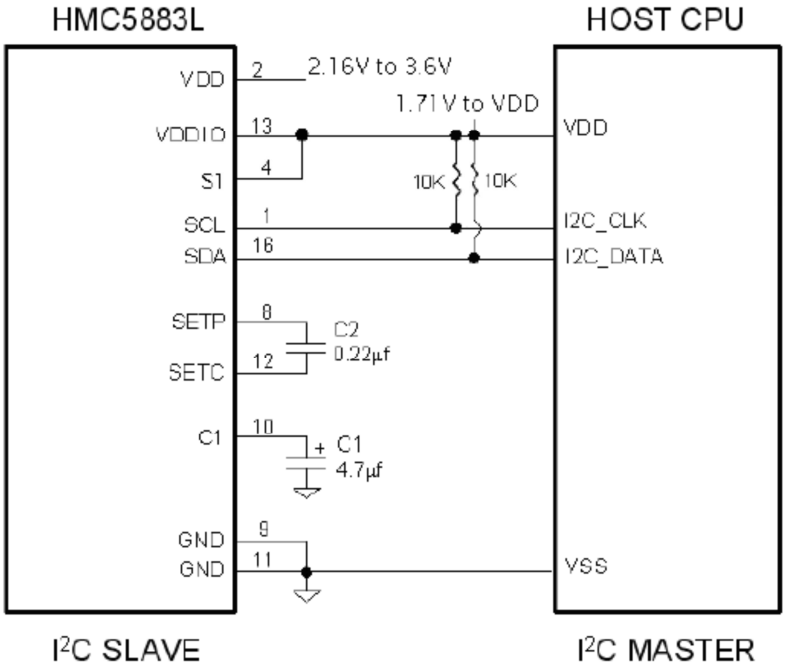
## INTERNAL SCHEMATIC DIAGRAM

***HMC5883L***

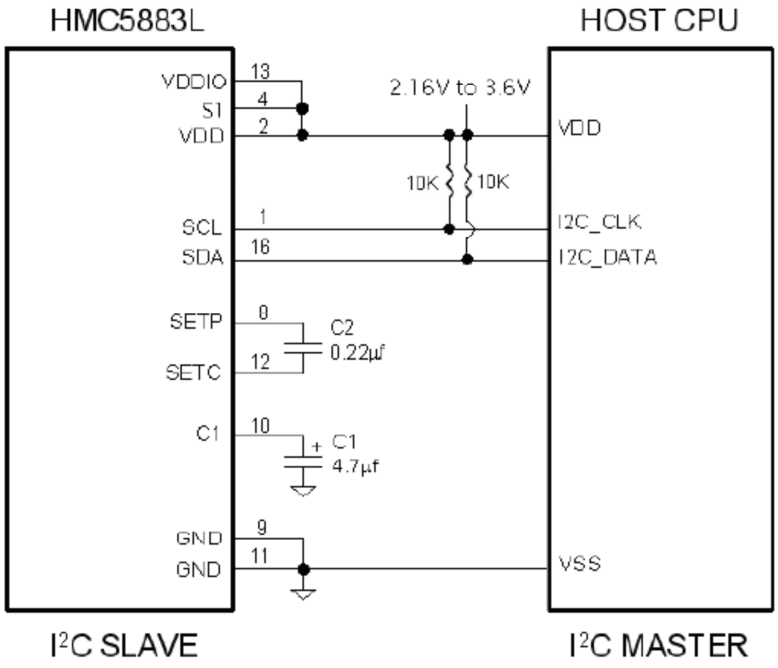


## HMC5883L

### DUAL SUPPLY REFERENCE DESIGN




### SINGLE SUPPLY REFERENCE DESIGN

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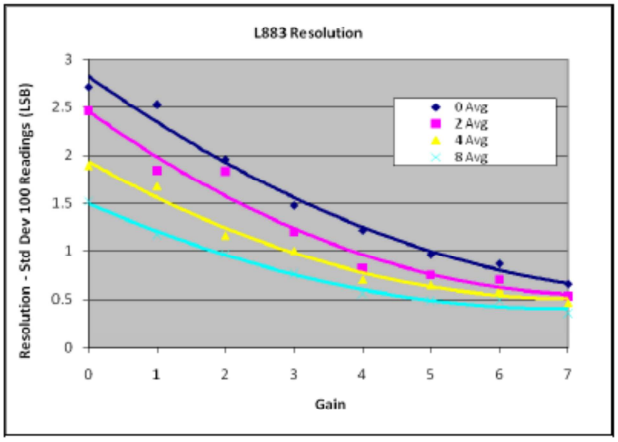
## HMC5883L

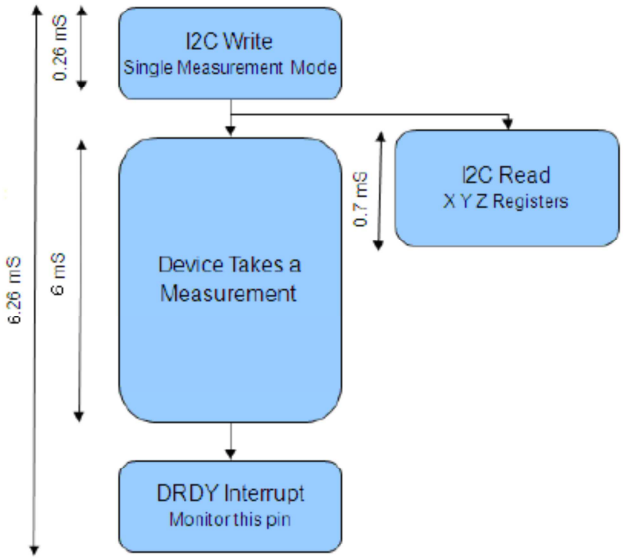
### PERFORMANCE

The following graph(s) highlight HMC5883L's performance.

**Typical Resolution**




**Typical Measurement Period in Single-Measurement Mode**




** Monitoring of the DRDY Interrupt pin is only required if maximum output rate is desired.*

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# HMC5883L

## BASIC DEVICE OPERATION

### Anisotropic Magneto-Resistive Sensors

The Honeywell HMC5883L magnetoresistive sensor circuit is a trio of sensors and application specific support circuits to measure magnetic fields. With power supply applied, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output. The magnetoresistive sensors are made of a nickel-iron (Permalloy) thin-film and patterned as a resistive strip element. In the presence of a magnetic field, a change in the bridge resistive elements causes a corresponding change in voltage across the bridge outputs.

These resistive elements are aligned together to have a common sensitive axis (indicated by arrows in the pinout diagram) that will provide positive voltage change with magnetic fields increasing in the sensitive direction. Because the output is only proportional to the magnetic field component along its axis, additional sensor bridges are placed at orthogonal directions to permit accurate measurement of magnetic field in any orientation.

### Self Test

To check the HMC5883L for proper operation, a self test feature in incorporated in which the sensor is internally excited with a nominal magnetic field (in either positive or negative bias configuration). This field is then measured and reported. This function is enabled and the polarity is set by bits MS[n] in the configuration register A. An internal current source generates DC current (about 10 mA) from the VDD supply. This DC current is applied to the offset straps of the magneto-resistive sensor, which creates an artificial magnetic field bias on the sensor.

See SELF TEST OPERATION section later in this datasheet for additional details.

### Power Management

This device has two different domains of power supply. The first one is VDD that is the power supply for internal operations and the second one is VDDIO that is dedicated to IO interface. It is possible to work with VDDIO equal to VDD; Single Supply mode, or with VDDIO lower than VDD allowing HMC5883L to be compatible with other devices on board.

### $I^2C$ Interface

Control of this device is carried out via the $I^2C$ bus. This device will be connected to this bus as a slave device under the control of a master device, such as the processor.

This device is compliant with *$I^2C$-Bus Specification*, document number: 9398 393 40011. As an $I^2C$ compatible device, this device has a 7-bit serial address and supports $I^2C$ protocols. This device supports standard and fast modes, 100kHz and 400kHz, respectively, but does not support the high speed mode (Hs). External pull-up resistors are required to support these standard and fast speed modes.

Activities required by the master (register read and write) have priority over internal activities, such as the measurement. The purpose of this priority is to not keep the master waiting and the $I^2C$ bus engaged for longer than necessary.

### Internal Clock

The device has an internal clock for internal digital logic functions and timing management.

### H-Bridge for Set/Reset Strap Drive

The ASIC contains large switching FETs capable of delivering a large but brief pulse to the Set / Reset strap of the sensor. This strap is largely a resistive load. There is no need for an external Set/Reset circuit. The controlling of the Set/Reset function is done automatically by the ASIC for each measurement. One half of the difference from the measurements taken after a set pulse and after a reset pulse will be put in the data output register for each of the three axes. By doing so, the sensor's internal offset and its temperature dependence is removed/cancelled for all measurements.

### Charge Current Limit

The current that reservoir capacitor (C1) can draw when charging is limited for both single supply and dual supply

configurations. This prevents drawing down the supply voltage (VDD).

## MODES OF OPERATION

This device has several operating modes whose primary purpose is power management and is controlled by the Mode Register. This section describes these modes.

### Continuous-Measurement Mode

During continuous-measurement mode, the device continuously makes measurements, at user selectable rate, and places measured data in data output registers. Data can be re-read from the data output registers if necessary; however, if the master does not ensure that the data register is accessed before the completion of the next measurement, the data output registers are updated with the new measurement. To conserve current between measurements, the device is placed in a state similar to idle mode, but the Mode Register is not changed to Idle Mode. That is, MD[n] bits are unchanged. Settings in the Configuration Register A affect the data output rate (bits DO[n]), the measurement configuration (bits MS[n]), when in continuous-measurement mode. All registers maintain values while in continuous-measurement mode. The $I^2C$ bus is enabled for use by other devices on the network in while continuous-measurement mode.

### Single-Measurement Mode

This is the default power-up mode. During single-measurement mode, the device makes a single measurement and places the measured data in data output registers. After the measurement is complete and output data registers are updated, the device is placed in idle mode, and the Mode Register *is* changed to idle mode by setting MD[n] bits. Settings in the configuration register affect the measurement configuration (bits MS[n])when in single-measurement mode. All registers maintain values while in single-measurement mode. The $I^2C$ bus is enabled for use by other devices on the network while in single-measurement mode.

### Idle Mode

During this mode the device is accessible through the $I^2C$ bus, but major sources of power consumption are disabled, such as, but not limited to, the ADC, the amplifier, and the sensor bias current. All registers maintain values while in idle mode. The $I^2C$ bus is enabled for use by other devices on the network while in idle mode.

## HMC5883L

## REGISTERS

This device is controlled and configured via a number of on-chip registers, which are described in this section. In the following descriptions, *set* implies a logic 1, and *reset* or *clear* implies a logic 0, unless stated otherwise.

**Register List**
The table below lists the registers and their access. All address locations are 8 bits.

| Address Location | Name | Access |
|---|---|---|
| 00 | Configuration Register A | Read/Write |
| 01 | Configuration Register B | Read/Write |
| 02 | Mode Register | Read/Write |
| 03 | Data Output X MSB Register | Read |
| 04 | Data Output X LSB Register | Read |
| 05 | Data Output Z MSB Register | Read |
| 06 | Data Output Z LSB Register | Read |
| 07 | Data Output Y MSB Register | Read |
| 08 | Data Output Y LSB Register | Read |
| 09 | Status Register | Read |
| 10 | Identification Register A | Read |
| 11 | Identification Register B | Read |
| 12 | Identification Register C | Read |

Table2: Register List

**Register Access**

This section describes the process of reading from and writing to this device. The devices uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address plus 1 bit read/write identifier.

To minimize the communication between the master and this device, the address pointer updated automatically without master intervention. This automatic address pointer update has two additional features. First when address 12 or higher is accessed the pointer updates to address 00 and secondly when address 08 is reached, the pointer rolls back to address 03. Logically, the address pointer operation functions as shown below.

*If (address pointer = 08) then address pointer = 03*
*Else if (address pointer >= 12) then address pointer = 0*
*Else (address pointer) = (address pointer) + 1*

The address pointer value itself cannot be read via the $I^2C$ bus.
Any attempt to read an invalid address location returns 0's, and any write to an invalid address location or an undefined bit within a valid address location is ignored by this device.

To move the address pointer to a random register location, first issue a "write" to that register location with no data byte following the commend. For example, to move the address pointer to register 10, send 0x3C 0x0A.

## HMC5883L

### Configuration Register A

The configuration register is used to configure the device for setting the data output rate and measurement configuration. CRA0 through CRA7 indicate bit locations, with *CRA* denoting the bits that are in the configuration register. CRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

| CRA7 | CRA6 | CRA5 | CRA4 | CRA3 | CRA2 | CRA1 | CRA0 |
|---|---|---|---|---|---|---|---|
| (1) | MA1(1) | MA0(1) | DO2 (1) | DO1 (0) | DO0 (0) | MS1 (0) | MS0 (0) |

Table 3: Configuration Register A

| Location | Name | Description |
|---|---|---|
| CRA7 | CRA7 | This bit must be cleared for correct operation. |
| CRA6 to CRA5 | MA1 to MA0 | Select number of samples averaged (1 to 8) per measurement output.<br>00 = 1; 01 = 2; 10 = 4; 11 = 8 (Default) |
| CRA4 to CRA2 | DO2 to DO0 | Data Output Rate Bits. These bits set the rate at which data is written to all three data output registers. |
| CRA1 to CRA0 | MS1 to MS0 | Measurement Configuration Bits. These bits define the measurement flow of the device, specifically whether or not to incorporate an applied bias into the measurement. |

Table 4: Configuration Register A Bit Designations

The Table below shows all selectable output rates in continuous measurement mode. All three channels shall be measured within a given output rate. Other output rates with maximum rate of 160 Hz can be achieved by monitoring DRDY interrupt pin in single measurement mode.

| DO2 | DO1 | DO0 | Typical Data Output Rate (Hz) |
|---|---|---|---|
| 0 | 0 | 0 | 0.75 |
| 0 | 0 | 1 | 1.5 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 7.5 |
| 1 | 0 | 0 | 15 (Default) |
| 1 | 0 | 1 | 30 |
| 1 | 1 | 0 | 75 |
| 1 | 1 | 1 | Not used |

Table 5: Data Output Rates

| MS1 | MS0 | Measurement Mode |
|---|---|---|
| 0 | 0 | Normal measurement configuration (Default). In normal measurement configuration the device follows normal measurement flow. The positive and negative pins of the resistive load are left floating and high impedance. |
| 0 | 1 | Positive bias configuration for X, Y, and Z axes. In this configuration, a positive current is forced across the resistive load for all three axes. |
| 1 | 0 | Negative bias configuration for X, Y and Z axes. In this configuration, a negative current is forced across the resistive load for all three axes.. |
| 1 | 1 | This configuration is reserved. |

Table 6: Measurement Modes

## HMC5883L

### Configuration Register B

The configuration register B for setting the device gain. CRB0 through CRB7 indicate bit locations, with *CRB* denoting the bits that are in the configuration register. CRB7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

| CRB7 | CRB6 | CRB5 | CRB4 | CRB3 | CRB2 | CRB1 | CRB0 |
|---|---|---|---|---|---|---|---|
| GN2 (0) | GN1 (0) | GN0 (1) | (0) | (0) | (0) | (0) | (0) |

Table 7: Configuration B Register

| Location | Name | Description |
|---|---|---|
| CRB7 to CRB5 | GN2 to GN0 | Gain Configuration Bits. These bits configure the gain for the device. The gain configuration is common for all channels. |
| CRB4 to CRB0 | 0 | These bits must be cleared for correct operation. |

Table 8: Configuration Register B Bit Designations

The table below shows nominal gain settings. Use the "Gain" column to convert counts to Gauss. Choose a lower gain value (higher GN#) when total field strength causes overflow in one of the data output registers (saturation).

| GN2 | GN1 | GN0 | Recommended Sensor Field Range | Gain (LSB/ Gauss) | Output Range |
|---|---|---|---|---|---|
| 0 | 0 | 0 | ± 0.88 Ga | 1370 | 0xF800–0x07FF (-2048–2047 ) |
| 0 | 0 | 1 | ± 1.3 Ga | 1090 (default) | 0xF800–0x07FF (-2048–2047 ) |
| 0 | 1 | 0 | ± 1.9 Ga | 820 | 0xF800–0x07FF (-2048–2047 ) |
| 0 | 1 | 1 | ± 2.5 Ga | 660 | 0xF800–0x07FF (-2048–2047 ) |
| 1 | 0 | 0 | ± 4.0 Ga | 440 | 0xF800–0x07FF (-2048–2047 ) |
| 1 | 0 | 1 | ± 4.7 Ga | 390 | 0xF800–0x07FF (-2048–2047 ) |
| 1 | 1 | 0 | ± 5.6 Ga | 330 | 0xF800–0x07FF (-2048–2047 ) |
| 1 | 1 | 1 | ± 8.1 Ga | 230 | 0xF800–0x07FF (-2048–2047 ) |

Table 9: Gain Settings

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## HMC5883L

### Mode Register

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to select the operating mode of the device. MR0 through MR7 indicate bit locations, with *MR* denoting the bits that are in the mode register. MR7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

| MR7 | MR6 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |
|---|---|---|---|---|---|---|---|
| (1) | (0) | (0) | (0) | (0) | (0) | MD1 (0) | MD0 (1) |

Table 10: Mode Register

| Location | Name | Description |
|---|---|---|
| MR7 to MR2 | 0 | These bits must be cleared for correct operation. Bit MR7 bit is set internally after each single-measurement operation. |
| MR1 to MR0 | MD1 to MD0 | Mode Select Bits. These bits select the operation mode of this device. |

Table 11: Mode Register Bit Designations

| MD1 | MD0 | Operating Mode |
|---|---|---|
| 0 | 0 | Continuous-Measurement Mode. In continuous-measurement mode, the device continuously performs measurements and places the result in the data register. RDY goes high when new data is placed in all three registers. After a power-on or a write to the mode or configuration register, the first measurement set is available from all three data output registers after a period of $2/f_{DO}$ and subsequent measurements are available at a frequency of $f_{DO}$, where $f_{DO}$ is the frequency of data output. |
| 0 | 1 | Single-Measurement Mode (Default). When single-measurement mode is selected, device performs a single measurement, sets RDY high and returned to idle mode. Mode register returns to idle mode bit values. The measurement remains in the data output register and RDY remains high until the data output register is read or another measurement is performed. |
| 1 | 0 | Idle Mode. Device is placed in idle mode. |
| 1 | 1 | Idle Mode. Device is placed in idle mode. |

Table 12: Operating Modes

## HMC5883L

### Data Output X Registers A and B

The data output X registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel X. Data output X register A contains the MSB from the measurement result, and data output X register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DXRA0 through DXRA7 and DXRB0 through DXRB7 indicate bit locations, with *DXRA* and *DXRB* denoting the bits that are in the data output X registers. DXRA7 and DXRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096. This register value will clear when after the next valid measurement is made.

| **DXRA7** | **DXRA6** | **DXRA5** | **DXRA4** | **DXRA3** | **DXRA2** | **DXRA1** | **DXRA0** |
|---|---|---|---|---|---|---|---|
| (0) | (0) | (0) | (0) | (0) | (0) | (0) | (0) |
| **DXRB7** | **DXRB6** | **DXRB5** | **DXRB4** | **DXRB3** | **DXRB2** | **DXRB1** | **DXRB0** |
| (0) | (0) | (0) | (0) | (0) | (0) | (0) | (0) |

Table 13: Data Output X Registers A and B

### Data Output Y Registers A and B

The data output Y registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Y. Data output Y register A contains the MSB from the measurement result, and data output Y register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DYRA0 through DYRA7 and DYRB0 through DYRB7 indicate bit locations, with *DYRA* and *DYRB* denoting the bits that are in the data output Y registers. DYRA7 and DYRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096. This register value will clear when after the next valid measurement is made.

| **DYRA7** | **DYRA6** | **DYRA5** | **DYRA4** | **DYRA3** | **DYRA2** | **DYRA1** | **DYRA0** |
|---|---|---|---|---|---|---|---|
| (0) | (0) | (0) | (0) | (0) | (0) | (0) | (0) |
| **DYRB7** | **DYRB6** | **DYRB5** | **DYRB4** | **DYRB3** | **DYRB2** | **DYRB1** | **DYRB0** |
| (0) | (0) | (0) | (0) | (0) | (0) | (0) | (0) |

Table 14: Data Output Y Registers A and B

### Data Output Z Registers A and B

The data output Z registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Z. Data output Z register A contains the MSB from the measurement result, and data output Z register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DZRA0 through DZRA7 and DZRB0 through DZRB7 indicate bit locations, with *DZRA* and *DZRB* denoting the bits that are in the data output Z registers. DZRA7 and DZRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096. This register value will clear when after the next valid measurement is made.

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| DZRA7 | DZRA6 | DZRA5 | DZRA4 | DZRA3 | DZRA2 | DZRA1 | DZRA0 |
|---|---|---|---|---|---|---|---|
| (0) | (0) | (0) | (0) | (0) | (0) | (0) | (0) |
| **DZRB7** | **DZRB6** | **DZRB5** | **DZRB4** | **DZRB3** | **DZRB2** | **DZRB1** | **DZRB0** |
| (0) | (0) | (0) | (0) | (0) | (0) | (0) | (0) |

Table 15: Data Output Z Registers A and B

**Data Output Register Operation**

When one or more of the output registers are read, new data cannot be placed in any of the output data registers until all six data output registers are read. This requirement also impacts DRDY and RDY, which cannot be cleared until new data is placed in all the output registers.

**Status Register**

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with *SR* denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|---|---|---|---|---|---|---|---|
| (0) | (0) | (0) | (0) | (0) | (0) | LOCK (0) | RDY(0) |

Table 16: Status Register

| Location | Name | Description |
|---|---|---|
| SR7 to SR2 | 0 | These bits are reserved. |
| SR1 | LOCK | Data output register lock. This bit is set when this some but not all for of the six data output registers have been read. When this bit is set, the six data output registers are locked and any new data will not be placed in these register until one of three conditions are met: one, all six bytes have been read or the mode changed, two, the mode is changed, or three, the measurement configuration is changed. |
| SR0 | RDY | Ready Bit. Set when data is written to all six data registers. Cleared when device initiates a write to the data output registers and after one or more of the data output registers are written to. When RDY bit is clear it shall remain cleared for a 250 µs. DRDY pin can be used as an alternative to the status register for monitoring the device for measurement data. |

Table 17: Status Register Bit Designations

## HMC5883L

### Identification Register A

The identification register A is used to identify the device. IRA0 through IRA7 indicate bit locations, with *IRA* denoting the bits that are in the identification register A. IRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

The identification value for this device is stored in this register. This is a read-only register.
Register values. ASCII value *H*

| IRA7 | IRA6 | IRA5 | IRA4 | IRA3 | IRA2 | IRA1 | IRA0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

Table 18: Identification Register A Default Values

### Identification Register B

The identification register B is used to identify the device. IRB0 through IRB7 indicate bit locations, with *IRB* denoting the bits that are in the identification register A. IRB7 denotes the first bit of the data stream.

Register values. ASCII value *4*

| IRB7 | IRB6 | IRB5 | IRB4 | IRB3 | IRB2 | IRB1 | IRB0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

Table 19: Identification Register B Default Values

### Identification Register C

The identification register C is used to identify the device. IRC0 through IRC7 indicate bit locations, with *IRC* denoting the bits that are in the identification register A. IRC7 denotes the first bit of the data stream.

Register values. ASCII value *3*

| IRC7 | IRC6 | IRC5 | IRC4 | IRC3 | IRC2 | IRC1 | IRC0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

Table 20: Identification Register C Default Values

## HMC5883L

### I²C COMMUNICATION PROTOCOL

The HMC5883L communicates via a two-wire I²C bus system as a slave device. The HMC5883L uses a simple protocol with the interface protocol defined by the I²C bus specification, and by this document. The data rate is at the standard-mode 100kbps or 400kbps rates as defined in the I²C Bus Specifications. The bus bit format is an 8-bit Data/Address send and a 1-bit acknowledge bit. The format of the data bytes (payload) shall be case sensitive ASCII characters or binary data to the HMC5883L slave, and binary data returned. Negative binary values will be in two's complement form. The default (factory) HMC5883L 7-bit slave address is 0x3C for write operations, or 0x3D for read operations.

The HMC5883L Serial Clock (SCL) and Serial Data (SDA) lines require resistive pull-ups (Rp) between the master device (usually a host microprocessor) and the HMC5883L. Pull-up resistance values of about 10k ohms are recommended with a nominal VDDIO voltage. Other resistor values may be used as defined in the I²C Bus Specifications that can be tied to VDDIO.

The SCL and SDA lines in this bus specification may be connected to multiple devices. The bus can be a single master to multiple slaves, or it can be a multiple master configuration. All data transfers are initiated by the master device, which is responsible for generating the clock signal, and the data transfers are 8 bit long. All devices are addressed by I²C's unique 7-bit address. After each 8-bit transfer, the master device generates a 9th clock pulse, and releases the SDA line. The receiving device (addressed slave) will pull the SDA line low to acknowledge (ACK) the successful transfer or leave the SDA high to negative acknowledge (NACK).

Per the I²C spec, all transitions in the SDA line must occur when SCL is low. This requirement leads to two unique conditions on the bus associated with the SDA transitions when SCL is high. Master device pulling the SDA line low while the SCL line is high indicates the Start (S) condition, and the Stop (P) condition is when the SDA line is pulled high while the SCL line is high. The I²C protocol also allows for the Restart condition in which the master device issues a second start condition without issuing a stop.

All bus transactions begin with the master device issuing the start sequence followed by the slave address byte. The address byte contains the slave address; the upper 7 bits (bits7-1), and the Least Significant bit (LSb). The LSb of the address byte designates if the operation is a read (LSb=1) or a write (LSb=0). At the 9th clock pulse, the receiving slave device will issue the ACK (or NACK). Following these bus events, the master will send data bytes for a write operation, or the slave will clock out data with a read operation. All bus transactions are terminated with the master issuing a stop sequence.

I²C bus control can be implemented with either hardware logic or in software. Typical hardware designs will release the SDA and SCL lines as appropriate to allow the slave device to manipulate these lines. In a software implementation, care must be taken to perform these tasks in code.

### OPERATIONAL EXAMPLES

The HMC5883L has a fairly quick stabilization time from no voltage to stable and ready for data retrieval. The nominal 6 milli-seconds with the factory default single measurement mode means that the six bytes of magnetic data registers (DXRA, DXRB, DZRA, DZRB, DYRA, and DYRB) are filled with a valid first measurement.

To change the measurement mode to continuous measurement mode, after the power-up time send the three bytes:

0x3C 0x02 0x00

This writes the 00 into the second register or mode register to switch from single to continuous measurement mode setting. With the data rate at the factory default of 15Hz updates, a 67 milli-second typical delay should be allowed by the I²C master before querying the HMC5883L data registers for new measurements. To clock out the new data, send:

0x3D, and clock out DXRA, DXRB, DZRA, DZRB, DYRA, and DYRB located in registers 3 through 8. The HMC5883L will automatically re-point back to register 3 for the next 0x3D query. All six data registers must be read properly before new data can be placed in any of these data registers.

## HMC5883L

### SELF TEST OPERATION

To check the HMC5883L for proper operation, a self test feature in incorporated in which the sensor offset straps are excited to create a nominal field strength (bias field) to be measured. To implement this self test, the least significant bits (MS1 and MS0) of configuration register A are changed from 00 to 01.

Then, by placing the mode register into single-measurement mode (0x01), two data acquisition cycles will be made on each magnetic vector. The first acquisition will be a set pulse followed shortly by measurement data of the external field. The second acquisition will have the offset strap excited (about 10 mA) in the positive bias mode for X, Y, and Z axes to create about a ±1.1 gauss self test field plus the external field. The first acquisition values will be subtracted from the second acquisition, and the net measurement will be placed into the data output registers.

If the configuration register B is left at the factory default value of 0x40, values around +951 ADC LSB (1.16 Ga * 820 LSB/Ga) will be placed in the X and Y data output registers and around +886 (1.08 Ga * 1820 LSB/Ga) in Z data output register. To leave the self test mode, change MS1 and MS0 bit of the configuration register A back to 00. Also change the mode register if single-measurement mode is not the intended mode of operation.

### SCALE FACTOR CALIBRATION

Using the method described above in section SELF TEST OPERATION, user can scale sensors' sensitivity to match each other. Since placing device in positive bias mode (or alternatively negative bias mode) applies a known artificial field on all three axes, the resulting ADC measurement in data output registers can be used to scale the sensors.

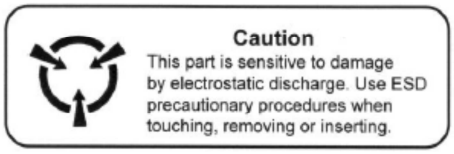
Alternatively, the built-in self test can be used to periodically compensate the scaling errors due to temperature variations. A compensation factor can be found by comparing the self test outputs with the ones obtained at a known temperature. For example, if the self test output is 1130 at room temperature and 1150 at the current temperature then a scale factor of (1130/1150) should be applied to all current magnetic readings. A temperature sensor is not required using this method.

### EXTERNAL CAPACITORS

The two external capacitors should be ceramic type construction with low ESR characteristics. The exact ESR values are not critical but values less than 200 milli-ohms are recommended. Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors to gain Low ESR characteristics.

### ORDERING INFORMATION

| Ordering Number | Product |
|---|---|
| HMC5883L | 3-Axis Digital Compass IC |
| HMC5883L-TR | Tape and Reel 4k pieces/reel |




**CAUTION: ESDS CAT. 1B**

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