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Improvements in P/Al High Efficiency Technology, AlSi

(Mejoras en tecnología fósforo-aluminio de alta eficiencia)

Doctoral thesis

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DEDICATED

TO
My Parents (late)
WHO SET A MODEL ROLE FOR MY LIFE

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All praises for **Almighty ALLAH**, Who is most Omnificent, Omniscient, Omnipotent and Omnipresent for giving me the will and strength to accomplish this job. I am showing my humble submission to the heart and soul of the world and the world here after The **Holy Prophet Muhammad** (Peace be upon him), whose life is an ideal pattern for me.

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Resumen

La tecnología de alta eficiencia P/Al fue desarrollada a mediados de los años 80 mediante estudios teóricos y experimentales de A. Cuevas y M. Balbuena en el IES-UPM. Ellos concluyeron que es posible obtener alta eficiencia con emisores de fosforo profundos poco dopados y contacto de aluminio en la superficie posterior (aluminum back surface field). El objetivo principal de este trabajo fue mejorar la tecnología P/Al de alta eficiencia en el caso de obleas finas de silicio de bajo grado para células solares industriales.

Aplicando la tecnología P/Al, se han realizado diferentes lotes de células solares y su caracterización se llevó a cabo mediante medidas de Soles-Voc, tiempo de vida y curvas IV. Hemos observado alta densidad de corriente de saturación del emisor en la fabricación de emisores, que limita el voltaje de circuito abierto, estando en el rango de 1E-11A/cm^2 para los peores emisores y 5E-13 A/cm^2 para los emisores buenos. La máxima eficiencia que hemos obtenido se situaba en torno a 16.5%. El voltaje de circuito abierto de las células estaban en el rango de 600mV a 610mV y la corriente de cortocircuito estaba en el rango de 36mA/cm^2 a 39.2mA/cm^2. Hemos medido el tiempo de vida de las células P/Al después de cada paso térmico y después de la deposición de SiNx por PECVD, el máximo tiempo de vida que estaba en torno a 20µs por la técnica PCD y 40 µs por la técnica QSSPC después de la deposición de SiNx.

Debido a la poca eficiencia y la pobre calidad de la pasivación del emisor, hemos planeado investigar la difusión de fosforo en profundidad con el objetivo de lograr emisores profundos, ligeramente dopados y pasivados. Hemos llevado a cabo varias experimentos en de difusiones de fosforo a cuatro temperaturas en el rango de 800 a 875 ºC con el fin de lograr emisores n+ profundos y ligeramente dopados y sus perfiles. La densidad de corriente de saturación que limita el voltaje de circuito abierto depende de la concentración de fosforo activo y la profundidad de la unión. Debido a la alta temperatura, la difusión de fosforo forma una capa muerta que aumenta la recombinación y disminuye la eficiencia de la célula. Se introduce un paso de oxidación húmeda y/o seca para minimizar el efecto de la capa muerta. El porcentaje de fosforo eléctricamente activo se calcula por el modelo Tsai. Nuestros resultados muestran que con el aumento de temperatura, la concentración de Fosforo eléctricamente activo disminuye y viceversa. El objetivo de este estudio era realizar un proceso de difusión en un solo paso en el horno para la fabricación industrial de células solares.

La fiabilidad de los emisores fue evaluada por la influencia de la pasivacion. Para las condiciones de superficie de cada emisor, las velocidades de recombinación superficiales han sido simuladas en el PC1D para emisores convencionales con una profundidad de unión de unión de 0.2 µm y para los emisores actuales con una profundidad de union de 0.7 µm, mostrandose que los emisores con una union profunda dan bajos valores de densidad de corriente de saturacion de emisor (Joe) en compraracion con una profundidad de union convencional. Los emisores obtenidos en un unico paso termico estan en torno a 7-8 x10^{19} cm^{-3} con una resistencia de capa de ~60 Ω/□ y una profundidad de union de 0.71 µm y una densidad de corriente de saturacion de emisor de 130 fA/cm^2. En el proceso de difusión de una sola etapa, el gettering es mucho mayor que el obtenido con el proceso convencional y la carga térmica es también baja. En el caso de sustratos de tipo-p

y alta resistividad de 5.4Ω.cm, hemos medido tiempos de vida de en torno a 200 µs y en las obleas de tipo –n de baja resistividad (0.8 Ω.cm) en torno a 505 µs por la técnica PCD. La mejora en tiempo de vida es mucho mayor que en los procesos de gettering convencionales.

Utizandose una receta de SiNx optimizada, el tiempo de vida máximo que se midio en una estructura SiO2/SiNx para un emisor pasivado fue 334 µs por la tecnica PCD y 780 µs por la técnica QSSPC que se corresponde con una velocidad de recombinación superficial (SRV) de 10 cm/s para la técnica QSSPC y 24 cm/s por la técnica PCD para obleas de tipo p y en obleas de tipo n, el tiempo de vida máximo fue 1263 µs por la técnica PCD y 2209 µs por la técnica QSSPC que se corresponde con una veloscidad de recombinación superficial efectiva de 3.8 cm/s pr la técnica QSSPC y 15cm/s por la técnica PCD. La densidad de corriente de saturación del emisor (Joe) disminuye aun más debido al efecto de SiNX que pasa a estar en el rango de 5E-14 a 2.5E-14A/cm^2 (25-25fA/cm^2) para obleas de tipo p.

Para emisores suavemente dopados (resistencia de capa 100-200 Ω/□), es difícil hacer contacto entre el metal frontal y los emisores suavemenete dopados. Este tema puede superarsepor la fabricación de emisores selectivos. Los emisores selectivos tienen alta concentración de dopado bajo la red de contactos metalicos y baja concentración de dopaje en la zona iluminada. La segunda difusión de fosoforo (parte posterior- parte posterior) se realizó a 875 ºC durante 30 minutos en la area de surcos creadas con el láser, protegiendo la superficie posterior y el resto del area frontal con una capa SiNx para crear emisores selectivos. Una capa gruesa de Aluminio se depositó en la parte posterior de las células por medio de serigrafía con el fin de crear back surface field (BSF) asi como contacto posterior. La temperatura óptima para el contacto de Aluminio es 925 ºC a 60 pulgadas/min de veloicidad de cadena para tener un buen quemado y contacto. En este paso, la superficie posterior Al-BSF con oxido de Silicio (SiO_2) muestra alto voltaje de circuito abierto y bajo valor de Joe.

Tras la formación de contactos posteriores, hemos medido los Soles-V_{OC} de las células para obtener los parámetros eléctricos de las células solares, hemos encontrado que la densidad de corriente de saturación (Joe) de las células aumentó, las cuales estaban en el rango de 6.45E-13 a 3.1E-12A/cm^2 y shunt conductance estaban en el rango de 2E-4 a 3.5E-3 ohm.cm^2. Esta Joe es debida a los emisores posteriores (Al-BSF), debemos optimizar algunos parámetros para una apropiada metalización, tales como la pasta de metalización con el fin de medir los valores reales (bajo) de la Joe de las células. La calidad de los emisores selectivos está afectada por el tratamiento químico, este fenómeno se observo tras las medidas de tiempo de vida de los emisores selectivos, hemos encontrado reducción en el tiempo de vida, lo que habíamos medido tras la deposición de la capa SiN_x pero el tiempo de vida se mantiene homogénea en la zona de dopaje suave. La destrucción del tiempo de vida se reduce cuando se ha utilizado baño de teflón para el tratamiento químico en vez del baño metálico. El NaOH o el KOH se utiliza para eliminar los daños del láser previo a la segunda difusión de P. Utilizándose KOH, la reducción en tiempo de vida es menor que en el caso de la NaOH.

Hemos medido valores de Soles-V_{oc} en torno a 624 mV para obleas de tipo-p de alta resistividad y 626mV para las obleas de tipo n de baja resistividad. El comportamiento final de la célula P/Al es debido al Al-BSF, puede ser mejorada más y teóricamente se espera que sea en torno a 650 mV. El proceso que se ha utilizado para fabricar los emisores selectivos es factible para aplicarse en la fabricación industrial de células solares P/Al con emisores selectivos en los que se espera una eficiencia en torno al 20 %.

Laburpena

Efizientzia altuko P/Al teknologia 1980ko erdialdean garatu zen A. Cuevasek eta M. Balbuenak IES-UPMn aurrera eramandako ikerketa teorikoak eta esperimentalak zirela medio. Haiek ondorioztatu bezala, arinki dopatutako fosforozko igorle sakonak eta aluminiozko BSFak erabilita (P/Al teknologia) efizientzia altuak lor zitezkeen. Lan honen helburu nagusia honako hau da: P/Al teknologia hobetzea, maila baxuko siliziozko olata finak erabilita, industriako eskakizunetara begira.

P/Al teknologiaren bitartez gabrikatu dira eguzki-zelula sortak eta Suns-Voc kurbak, bizialdia eta IV kurbak neurtu izan zaizkie horiek karakterizatzeko. Neurketen arabera, asetasuneko korronte-dentsitate altuak ikusi dira igorleen fabrikazioan, zirkuitu irekiko tentsioa mugatzen dutenak. Asetasuneko korronte dentsitatearen tartea $3{\cdot}10^{-11}$ cm^2-tik (txarrena) $5{\cdot}10^{-13}$ A/cm^2-ra (hoberena) artekoa da. Lortutako efizientzia maximoak 16.5 % ingurukoak dira; eguzki-zelulen zirkuitu irekiko tentsioa 600-610 mV tartekoa eta zirkuitu laburreko korronte-dentsitatea 36-39.2 mA/cm^2-koa. P/Al eguzki-zelulen bizialdia neurtu da urrats termiko guztien ostean bai eta PECVDz SiNx geruzak ezarri ostean; SiNx geruza ezarri ostean neurtutako bizialdi maximoa, 20 µs ingurukoa da PCD bidez neurtuta eta 40 µs-koa QSSPC bidez neurtuta.

Igorleen pasibaketaren kalitate txikia eta efizientzia baxua dela eta, fosforozko dopaketak sakon aztertu dira, arinki dopatutako eta sakon pasibatutako igorleak lortu nahian. Horretarako, hainbat saiakera egin dira, fosforo-dopaketak 800-875 ºC tartean lau tenperatura aukeratuta: jomuga arinki baina dopatutako n+ igorleak lortzea izan da, eta bide batez, haien profila. Igorlearen asetasuneko korrontea, zirkuitu irekiko tentsioa mugatzen duena, fosforo-kontzentrazioaren eta junturaren sakoneraren menpekoa da. Tenperatura altuak direla eta, fosforo-dopaketak geruza ahitu bat sortzen du, birkonbinazioa handitzen eta zelularen efizientzia txikitzen duena. Oxidazio lehor/heze bat gaineratzen zaio geruza ahituaren efektua txikitzeko. Elektrikoki aktiboa den fosforo portzentajea Tsai ereduaren bitartez kalkulatzen da. Emaitzen arabera, tenperaturak igo ahala elektrikoki aktiboak diren Pen kopurua txikitzen da eta alderantziz. Ikerketa honek labean gauzatutako urrats bakarreko dopaketa egitea zuen helburu, industrian fabrikatzen diren eguzki.zelulei-begira.

Igorleen fidagarritasuna pasibaketaren eraginaren bitartez aztertu da: igorleen gainazaleko baldintzaren arabera gainazaleko birkonbinazio-abiadurak simulatu dira PC1D bitartez: igorleek 0.7 µm-ko sakonera izanez gero, igorleen asetasuneko korronte-dentsitatea txikia da (J_{0e}) 0.2 µm-ko sakonera duten ohiko igorleekin alderatuta. Urrats termiko bakarrean gauzatutako igorleen kontzentrazioa 7-8 $x10^{19}$ cm^{-3} –ko tartean dago, geruza-erresistentzia ~60 Ω/□-koa, junturaren sakonera 0.71 µm-koa eta igorlearen asetasuneko korronte-dentsitatea 130 fA/cm2. Pauso bakarreko dopatze-prozesuan *getterinq*a handiagoa da, ohiko prozesuarekin alderatuta, gainera, gastu termikoa txikia da. Materiala p-motakoa bada 200 µs-ko bizialdiak neurtu dira erresistibitate altuko olatetan (5.4Ω.cm) eta n-motako erresistibitate baxuko olatetan (0.8 Ω.cm) 505 µs-koak inguru (PCD teknika). Bizialdian hobekuntza ohiko gettering prozesuetan baino handiagoa da.

SiNx ezarketarako errezeta berria erabilita, optimizatutakoa, pasibatutako igorleetarako SiO2/SiNx egituran neurtutako bizialdi maximoa 334 µs-koa da, PCD bitartez

neurtutakoa eta 780 µs QSSPC teknikaren bitartez, hau da, 10 cm/s-ko SRV efektiboa QSSPCren bitartez eta 24 cm/s-ko SRV efektiboa QSSPCren bitartez p-motako olaten kasurako; n-motako olaten kasurako aldiz, neurtutako bizialdi maximoa 1263 µs-koa (PCD) eta 2209 µs-koa (QSSPC), hau da, 3.8 cm/s-ko SRV efektiboa (QSSPC) eta 15 cm/s-koa (PCD). Igorlearen asetasuneko korronte-dentsitatea hare gehiago jaitsi da, SiNx-ren pasibaketaren eraginez, p-motako olaten kasurako eta $5{\cdot}10^{-14}$-$2.5{\cdot}10^{-14}$ tartekoa izatera iristen da.

Arinki dopatutako igorleen kasuan (geruza-erresistentzia 100-200 Ω/sq), ez da erraza aurrealdeko metala eta igorlea kontaktatzea. Arazo horri nagusitu dakioke igorle selektiboak gauzatuz gero: aurrealdeko metalaren kontaktatze-eskualdeetan igorle selektiboak, kontzentrazio handikoak, ezarriko dira eta argiztapeneko eskualdeetan dopaketa baxuko igorleak gauzatuko dira. Igorle selektibo horiek gauzatzeko 2. dopaketa bat gauzatu da, olatak bizkarrez bizkar kokatuta (en *back to back*), 30 minutuz 875 ºC-era laser bidez urratutako eskualdeetan; horretarako, olatak SiNx geruza batez babestuko dira lehenik eta behin, gero laser bidez urratu eta egitura horiek labean sartu. Aluminiozko geruza lodi bat ezarri zaie eguzki-zelulei atzealdean serigrafia bidez BSFa eta atzealdeko kontaktua gauzatzeko. Aluminiozko atzealdeko kontaktuen sinterizazioa zinta-labean egiteko tenperatura eta abiadura optimoak 925 ºC eta 60 in/min dira; urrats horretan atzealdeko Al-BSF gainazala, siliziozko dioxidoa (SiO_2) gainazalean duena, da zirkuitu irekiko tentsiorik altuena ematen duena, bai eta eta J_{0e}-eko baliorik baxuena ere.

Atzealdeko kontaktuak gauzatu ostean eguzki-zelulen karakterizazio elektrikoa egin da, Suns-V_{OC} kurba ezaugarriak neurtuta. Gauzak horrela, $6.45{\cdot}10^{-13}$–$3.1{\cdot}10^{-12}$ A/cm^2 tarteko J_{0e}-ak eta $2{\cdot}10^{-4}$–$3.5{\cdot}10^{-3}$ Ω·cm^2-ko shunt-konduktantziak neurtu dira. J_{0e}-a atzealdeko igorlearen ondoriozkoa da (Al-BSF): metalizazioa egokia izan dadin parametro batzuen optimizazioa beharrezkoa da, metalizazio-oreen optimizazioa, besteak beste, J_{0e}-ko balio errealak (baxuagoak) neurtzeko. Igorle selektiboen kalitatea tratamendu kimikoaren menpekoa da; igorle selektiboen bizialdia murriztu da (SiN_x geruzaren ezarketaren ostean neurtutakoa); bestalde, bizialdia berdintsu mantendu da oro har igorle nagusiaren eskualdeetan. Bizialdiaren degradazioa, baina, txikiagoa izan da tefloizko bainua metalezkoaren ordez erabili denean. NaOH-zko edo KOH-zko soluzioak laser-kaltea txikiagotzeko erabili dira, bigarren fosforo-dopatzearen aurretik. Bizialdia gutxiago txikiagotzen da KOH-zko soluzioarekin NaOH-zko soluzioarekin baino.

Zirkuitu irekiko tentsioa 624 mV ingurukoak neurtu dira p-motako erresistibitate altuko olatetan, n-motako erresistibitate baxuko olatetan 626 mV ingurukoak. P/Al eguzki-zelulen bukaerako bilakaera Al-BSFaren ondoriozkoa da: hobetu daiteke, teorikoki 650 mV-era arte. Igorle selektiboak gauzatzeko erabili den prozesua bideragarria da industria-fabrikazioan txertatzeko, eta horrela, 20 %-ko efizientzia duten igorle selektiboak dituzten P/Al eguzki-zelulak gauzatu daitezke.

Summary

High efficiency P/Al technology was developed in the mid of 1980s by theoretical and experimental studies of A. Cuevas and M. Balbuena at IES-UPM. They have concluded that it is possible to obtain high efficiency with lightly doped deep phosphorus emitters and aluminum back surface field, P/Al (P emitters/Al BSF). The main objective of this work was to improve high efficiency P/Al technology by using low grade silicon thin wafers for solar cells for industrial application.

By applying P/Al technology, we have fabricated different batches of $n^+p\,p^+$ (P/Al) solar cells and their characterization were carried out by Sun-Voc, lifetime and IV curves measurements. We have observed high emitter saturation current density in fabrication of emitters which limits the open circuit voltage were in range of 1E-11A/cm^2 for worse emitters and 5E-13 A/cm^2 for good emitters. Maximum efficiency which we have obtained was around 16.5%. Open circuit voltage of cells were in range of 600mV to 610mV and short circuit current was in range of 36mA/cm^2 to 39.2mA/cm^2. We have measured lifetime of P/Al solar cells after each thermal step and each after SiNx deposited by plasma enhanced chemical vapor deposition, the maximum lifetime which was around 20µs by PCD (transient photo-conductance decay) and 40 µs By QSSPC technique (quasi steady state photo-conductance decay) after SiNx deposition.

Due to low efficiency and poor quality of emitter's passivation, we have planned to investigate P diffusion deeply in order to get softly doped and passivated deep emitters. We have performed several phosphorus diffusion experiments at four temperatures ranging from 800 ºC to 875 ºC in order to get softly doped and deep n^+emitters and their profiles. The emitter saturation current density which limits the open circuit voltage depends on active phosphorus concentration and junction depth. Due to high temperature, P diffusion form dead layer which increased recombination and decrease overall cell efficiency. Dry or/and wet oxidation step with drive-in is introduced to minimize the effect of dead layer. The percentage of electrically active P is calculated by Tsai Model. Our results show that with increase of temperature, concentration of electrically active P decrease and vice versa. Our goal of this investigation was to make a single step diffusion process in a furnace for idustrial fabrication of solar cells.

Reliability of emitters were evaluated by the influence of passivation. For each emitter surface conditions, surface recombination velocities have been simulated by PC1D for conventional emitters with 0.2 µm junction depth and current emitters with 0.7 µm depth which show that deep emitters junction depth give low values of emitter saturation current density (Joe) as compare to conventional junction depth. Emitters obtained by single thermal step are in range of 7-8 x10^{19} cm^{-3} with sheet resistance ~60 Ω/□ and junction depth 0.71 µm and emitter saturation current density was 130 fA/cm^2. In single step diffusion process the gettering is higher than conventional process and thermal budget is also low. In case of P-type material, we have measured lifetime around 200 µs at high resistivity (5.4Ω.cm) wafers and on N-type low resistivity (0.8 Ω.cm) wafers around 505 µs by PCD technique. Improvement in lifetime is much higher than conventional gettering processes.

By using optimized new SiNx recipe, the maximum lifetime which we measured on stack structure SiO_2/SiNx for passivated emitter was 334 µs by PCD technique (transient photo-conductance decay) and 780 µs by QSSPC technique (quasi steady state photo-conductance decay) which corresponds to an effective surface recombination velocity (SRV) 10cm/s by QSSPC technique and 24cm/s by PCD technique for p-type wafers and on n-type wafers, the maximum lifetime which we measured was 1263µs by PCD technique and 2209 µs by QSSPC technique which corresponds to an effective SRV 3.8 cm/s for QSSPC technique and 15cm/s by PCD technique. Emitter's saturation current density (Joe) further decreased due to passivation effect of SiNx, which were in range of 5E-14 to 2.5E-14 A/cm^2 (25-50fA/cm^2) for p-types wafers.

For softly doped emitters (sheet resistance 100-200 Ω/sq), it is difficult to make a contacts between front metal and softly doped emitters. This issue can be overcome by fabrication of selective emitters. Selective emitter have high doping concentration under metal contacts grid and low doping concentration under illumination area. Second P diffusion (back to back) was carried out at 875 ºC for 30 minutes in laser scribed grooves area by protecting back surface and rest of front surface area with SiNx layer to create selective emitters. A thick layer of aluminum was deposited on backside of cells by screen printing technique in order create back surface field (BSF) as well as back contact. Optimal temperature for Al-deposition is 925 ºC at 60inches/min belt furnace speed for good firing and contacts. In this step, rear surface Al-BSF with silicon oxide (SiO_2) surface give highest open circuit voltage and lower Joe value.

After back contacts formation, we have measured *Sun-Voc* of cells to get electrical parameters of solar cells, we have found that emitter saturation current density (Joe) of cells increased which were in range from 6.45E-13 to 3.1E-12A/cm^2 and shunt conductance was in range from 2E-4 to 3.5E-3 ohm.cm^2. This Joe is due to rear emitters (Al-BSF), we have to optimize some parameters for appropriate metallization such as metallization paste in order to measure the real values (low) Joe of the cells. Quality of selective emitters is affected by chemical treatment, this phenomena was observed after lifetime measurements of selective emitters, we have found reduction in lifetime, what we had measured after SiNx layer deposition but lifetime is maintained under homogenous softly doped area. Destruction of lifetime is reduced when we have used teflon bath for chemical treatment instead of metallic bath. NaOH or KOH is used to remove laser damages prior to second P diffusion. By using KOH, reduction in lifetime is minor than NaOH.

We have measured *Sun-Voc* around 624 mV for p-type high resistivity wafers and 626mV for n-type low resistivity wafers. Final behavior of P/Al solar cell is due to Al-BSF, it can be further improved and theoretically expected is around 650 mV. Process which is used to fabricate selective emitter is feasible to apply for industrial fabrication of P/Al silicon solar cells with selective emitters with expected efficiency around 20%.

Contents

Chapter 1

1 Improvements in P/Al high efficiency technology, AlSi

1.1 Introduction

With the increase of human population, energy demand is also increasing steadily and rapidly. The conventional energy resources such as fossil and nuclear fuels are limited and associated with negative effect on environment, such as greenhouse gases effect, holes in ozone layer, acid rain and pollution cannot be neglected. Therefore new means of energy is necessary which should be renewable and environmental friendly.

Today conversion of sunlight into electricity by using photovoltaics is attractive, environmental friendly way to produce renewable energy. Photovoltaics systems especially in case of silicon solar cell raw material is available in abundant in nature, can be used everywhere in world and almost maintenance free flexible scale from milli-watt to megawatt. Due to these advantages, PV competes with conventional energy production but cost of PV electricity is still higher as compared to conventional resource of electricity. The aim of this research work is increase competitiveness of photovoltaics by improving the technology for high efficiency process and decreasing cost. The cost of solar cell modules is at this time is around 0.6$/Wp, this cost can be reduced to below 0.3$/Wp. Major tasks in solar cell research are;

- Reduce material and fabrication costs
- Improve technology
- Improved efficiencies
- Industrial application for high volume of production (≥ 500 MWp/year) [1].

Photovoltaic cell or photoelectric cell is a solid state electrical device that converts the sun light energy directly into electrical energy by the photoelectric effect. Photovoltaic is the field of technology and research related to the practical application of photovoltaic cells in producing electricity from light. After petrol crisis and the emissions problems deriving from the use of petrol derivatives, solar cells and other alternative sources of energy gained important place in the application of alternative energy. It has been under intensive investigation for cost-effective photovoltaics, since the development of the first solar cells in the 1950s [2–4]. The materials currently used for the fabrication of photovoltaic solar cells included crystalline materials are in the form of mono and polycrystalline silicon, amorphous silicon, cadmium telluride, and copper indium selenide/sulfide. Recently available solar cells are fabricated from bulk materials, in which wafers are cut into 150-300 µm thickness, and processed to fabricate solar cells like other semiconductors. Second group of solar cells, which are used as thin film layers are organic dyes and organic polymers that are deposited on substrate. A third group of cells are fabricated from nanocrystals, which is also called quantum dots or nanoparticles. Silicon remains the only material which is deeply investigated in both bulk and thin film forms of solar cell. Among all alternative technologies to silicon-based PN-junction solar cells, could lead the most significant cost reduction. [5]

1.2 Objective of thesis:

The main objective of this work is to develop high efficiency technology for solar cells which are industrializable exceed the efficiency and thickness estimation provided by industry. High efficiency technology, P/Al technology has shown efficiency 19% on float-zone wafer [6]. This technology consists of lightly doped phosphorus emitters of 100-150Ω/square, Aluminum evaporated by electron beam machine, diffused in quartz furnace and contacts are defined by metals evaporation by using photolithographic technique and lift-off. In this work, this technology is applied on monocrystalline silicon wafers, obtained by Czochralski growth (CZ), a low quality wafers than float-zone wafers. This technology will be compatible with 150 µm thickness and it is based on phosphorus and aluminum diffusion on p-type silicon wafers (Cz) with expected efficiencies over 18% [7-8].

The proposed work not only contributes to sustainable development but also direct impact on effective solution of environmental protection. In addition to this, the work aim is to improve P/Al solar cell technology for high efficiency, which can be implemented in industry. It is well recognized that the efficiency of photovoltaic systems is the key and to shorten the time is fully competitive. The proposed work not only contributes to sustainable development but also direct impact on effective solution of environmental protection.

Although the efficiencies achievement is remarkable and next step will be to transfer this technology from laboratory to industry in the future. Optimization analysis of phosphorus emitters is key step of this technology in order to maintain high efficiency. Phosphorus emitters are necessarily to be a selective, for this purpose P diffusion is investigated deeply to get lightly doped emitters under illumination area and highly doped under the metallization grid. Passivation can be achieved through layers of silicon nitride with silicon oxide, which also act as antireflection layers. For optimization of aluminum diffusion, some parameters are taken into account such as the amount of deposition of metal, temperature, process time, and composition of environment in the furnace to improve the lifetime and passivation. Techniques developed during this work under specific tasks (selective phosphorus emitter, aluminum BSF (back surface field), and metallization with photolithography by using electron beam (laboratory technique) and screen-printing or ink-jet (industrial technique), edge insolation of devices (solar cell) through laser), applied in fabrication of P/Al cells on Cz silicon wafers and expected efficiency is close to 18%.

1.2.1 Description of Work:

Photovoltaic solar energy is one kind of renewable energy source, it is started to develop from 1970 as an alternative resource of electricity. It is providing electricity but its efficiency and cost has not yet met the expectations what we have now a days. Solar energy has great advantages associated with its unlimited and widely distributed as fuel in the form of sun light. With respect to cost solar energy is still expensive. According to current estimation as shown in figure 1.1, average cost of solar energy for is ranging from 0.08-0.14€/kWh in European Union while in European Union average cost of electricity for end user is 0.05-0.10€/kWh. However we can see the cost reduction in recent years. By the using advance technology and improved technology, it could be cheaper [2].

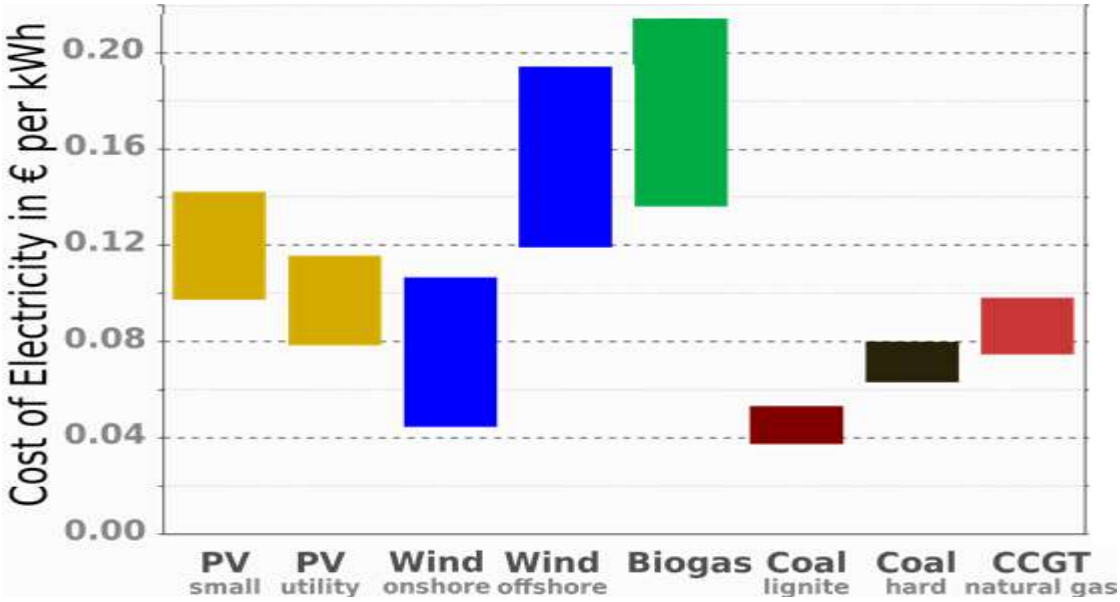

Figure 1.1 Cost of electricity from different resources in € Per KWh (source: Fraunhofer ISE)

Today investigation in solar energy is an area of undeniable interest. On one hand, it is necessary to find new alternative energy resource and other hand we are interested to find clean energy pollution free energy.

- There are many opinions about production of petroleum products and fossil fuel. It is thought that energy resources will be gradually decreased in near future. In 2008 price of petroleum reached as high as 148$/barrel and followed by a fluctuation in the following months. Currently prices of petroleum are very unstable. Natural gas is also evolved in similar way. The European Union is mainly depending on fossil fuel, it is necessary for diversification of energy sources in order to avoid the worsening the economic crisis.
- Second is the uneven distribution of energy resources, which are currently concentrated in small area of Middle East, whose political situation is uncertain. In contrary solar energy is abundant and cannot be monopolized by any country.
- In the mid of June 2009 EU directive force on “Promoting the use of energy from renewable resources” which aims was to reduces emissions of greenhouse gases by 20% in 2020 (Pollution free energy).

In order to solve above mentioned problems, renewable energies are the best candidate to overcome the major problem of energy supply and climate changes. The renewable energy resources which come from external resources usually from sun do not run out, in contrast to conventional energy resources based on fossil fuel in form of carbon, petrol and gas. There are many energy resources such as wind, geothermal biomass, hydrodynamic and solar energy. All of these form of energy resources capable of producing huge quantity of electricity for present and future use. There are strong reasons to use renewable energy which are as follow:

- These resources are environmental friendly in nature; do not contribute to produce carbon dioxide or other greenhouses gases.
- These energy resources are everlasting abundance and widely distributed.

- Renewable energy resources can supply energetically to poor areas/countries, avoiding energy dependence on other countries.

Among them, photovoltaic solar energy is the best positioned to face for long term.

From 2003, global PV productions have increased ten times with annual growth 40-80%. This cumulative capacity will be reached 233 GW in 2015. Their increasing trend and projection is shown in the graph, figure 1.2.

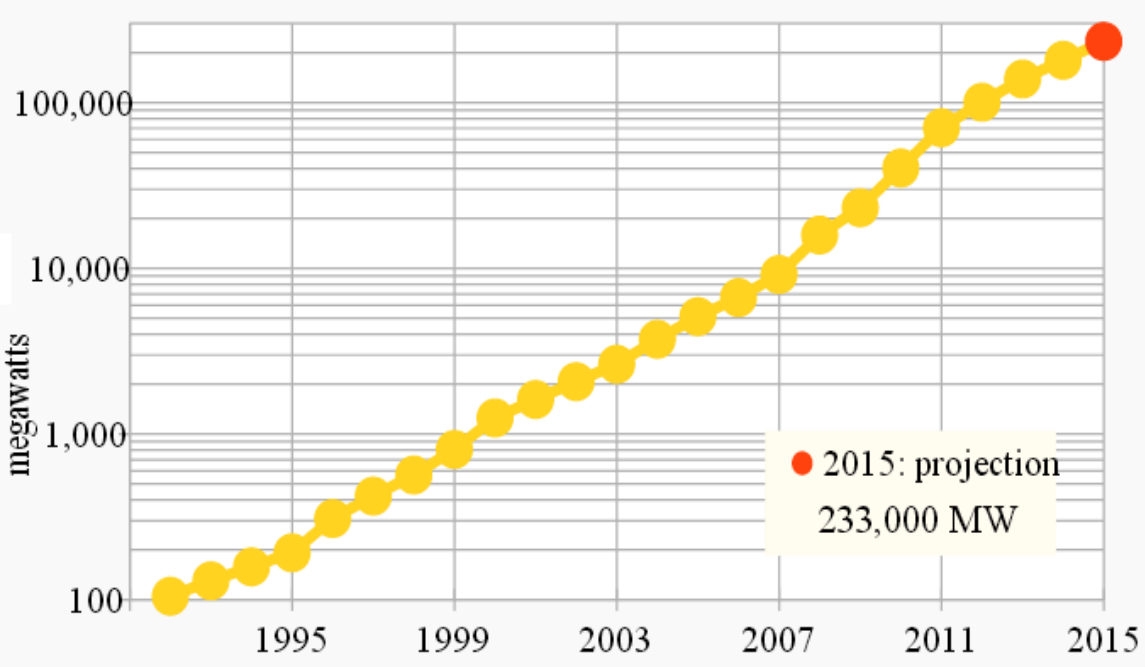

Figure1.2 Global cumulative PV Capacity in MW since 1990

In Spain, coverage of electricity demand from solar energy has experimented in the beginning of 2004 (first decay of twenty-first century), up to 3-5% energy accumulated from solar resources [9]. In 2009-10, the many PV power plants were installed in Spain, the most common PV power plants are Olmedilla Photovoltaic Park (60 MW), Puertollano Photovoltaic Park (47.6 MW), Solar Plant La Magascona and Magasquila (34.5 MW), Arnedo Solar Plant (34 MW), and Dulcinea Solar Plant (31.8 MW). The Spanish situation were very significant in manufacturing worldwide from 90 and thanks to the existence of strong industrial groups, those are leader in manufacturing photovoltaic cells/panels in Spain, emerged as a spin-off of university research groups and in all the cases providing good support in R & D (research and development).

In 2009 due to political restriction on renewable energy, photovoltaic industry collapse in Spain. Module fabrication decreased more than 30%. BP solar in Madrid and some other Photovoltaic's companies from Spain even from Europe moved to Asia, especially in China and India due low fabrication and labor cost. But still some companies have endured without closing their setup and come with better prospects and have plans to expand the module fabrication (Photon January 2010 issue).

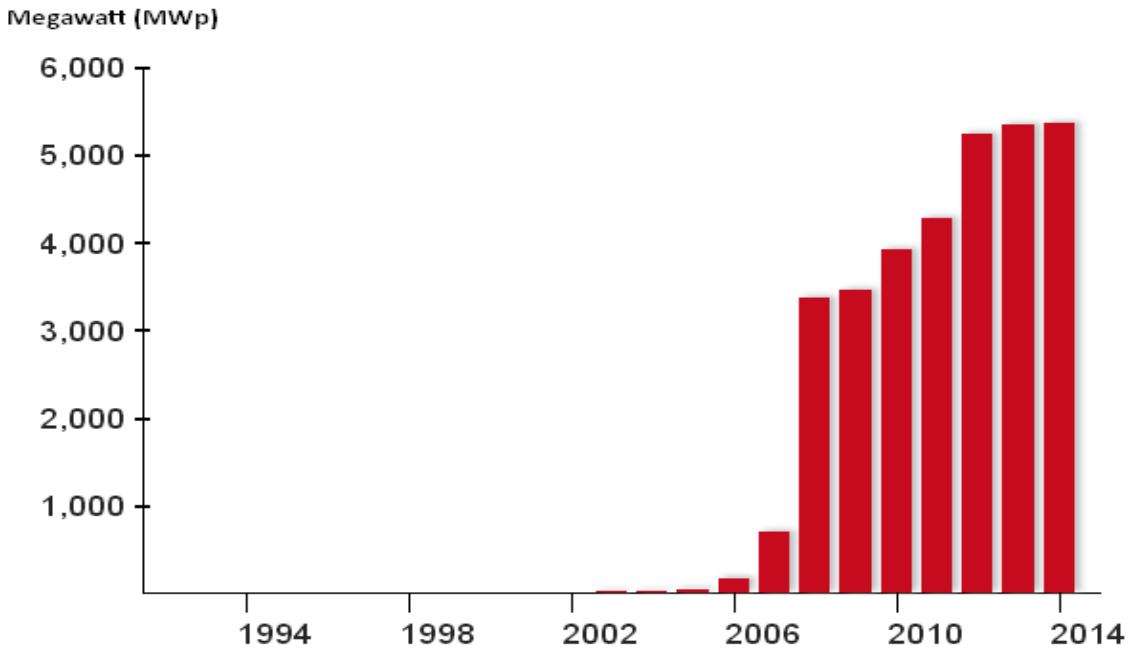

Figure1.3 Photovoltaic solar energy in Spain since 1992, in megawatts (MWp)

As photovoltaic industry is rapidly growing industry in last 2 decade also known as high technology corresponding electronics sector as well as microelectronic and nanotechnology sector.

The global growth of photovoltaics (PV) has been fitted by an exponential curve for more than 2 decades. During this period, PV solar progressed from small scale application toward to become main source of electricity. By the end of 2014, global cumulative photovoltaics capacity researched at 178 gigawatts (GW). This is sufficient to supply 1% of overall electricity demand. For 2015, global deployment of being about 55GW is forecasted and installed capacity is projected to be more than double beyond 500GW between now and 2020. In 2050 solar energy is expected to become the world`s largest source of electricity with PV solar cell and concentrated solar power. It will be necessary to grow PV capacity up to 4600GW, of which more than half is forecasted to be deployed in China and India. [10]. Regional wise global cumulative capacity is given in the graph figure 1.4.

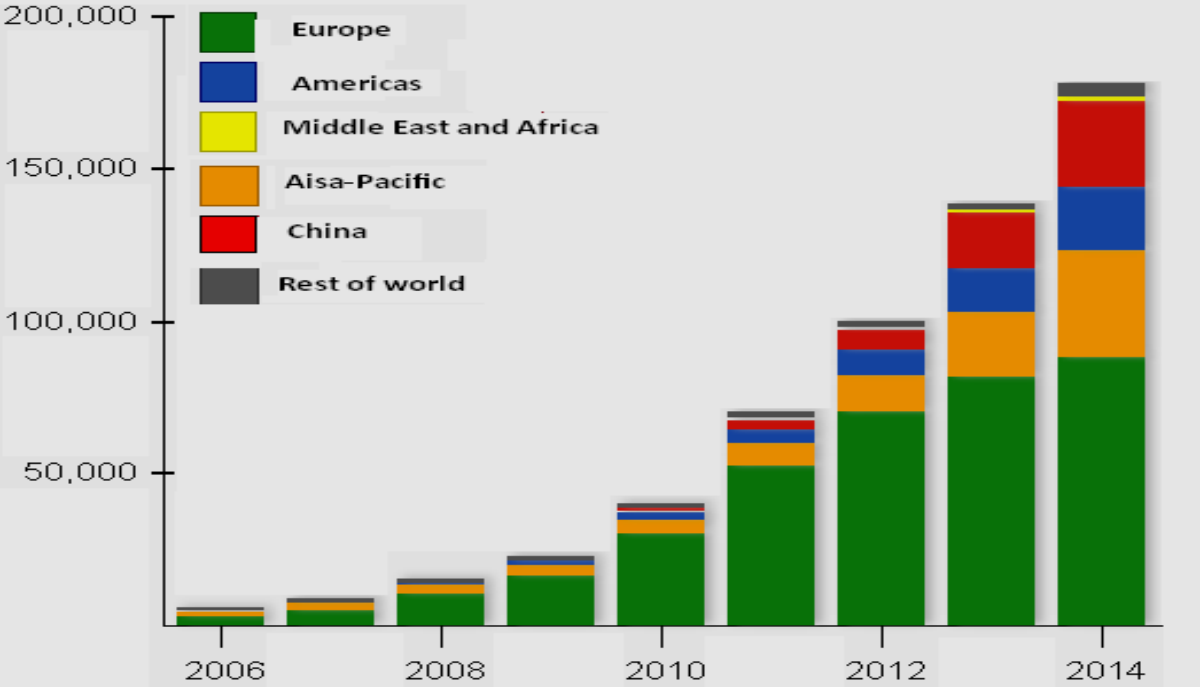

Figure 1.4 Cumulative Capacity in Megawatts [MWp] Grouped by Region

1.2.2 Summary; Analysis of state of Art

The generations for electricity by using photovoltaic solar module have the highest growth rate which is more than 40% annually over last six years. This growth rate is mainly support by crystalline silicon technology, which is currently contributing more than 90% of the world PV market. More than 90% of solar modules/panels are fabricated by using either monocrystalline or polycrystalline silicon globally. See the figure 1.5 for more detail.

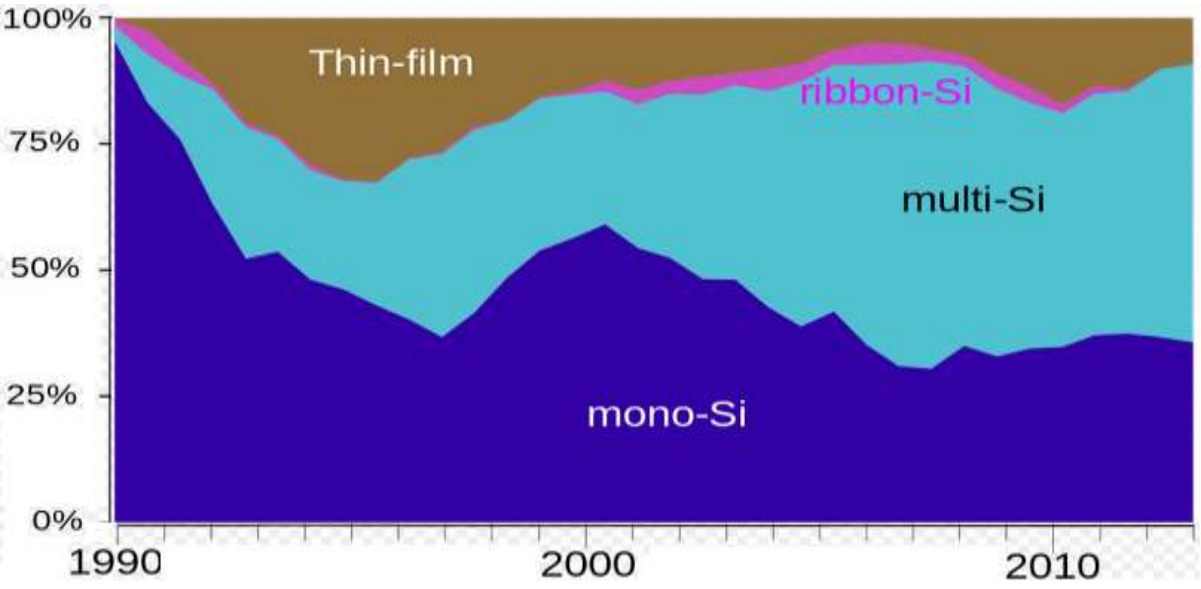

Figure 1.5 Global market-share in terms of annual production by PV technology since 1990

In the recent past, the barrier which exists to massive deployment of photovoltaic solar energy is only its relative high cost as compared to other power/energy generation

technology. It is also true that the calculations which assess the benefits of sustainability of the resources and its environmental impacts, impacts of photovoltaic power resource will be greatly benefits as compared to other power resources.

Now a days these barrier are not well established in distribution of generation, new energetic modules. In our opinion cost reduction does not only depend on the economical scale but also effect of R&D will be significant. Short and medium term technologies support the market that will be an evolution of what will be finding today in line of fabrication/production. While in long terms, we will need of new technologies, perhaps which will be based on better utilization of solar spectrum.

Today more than 90% of photovoltaic solar panels for generation of electricity are based on crystalline silicon wafers which are usually doped with boron and obtaining by casting in the form of monocrystalline and polycrystalline silicon, grown by Czochralski methods. There are many reasons to favor this technology (p-type wafer). On one hand, use of p-type wafers doped with boron, is quite simple to get phosphorus emitters by diffusion which is relatively simple technique, surface is transparent to light, recombination is low enough to give good photocurrent and high open circuit voltage. Moreover phosphorus is more soluble in silicon as compare to silicon oxide. Wafer surface rich in phosphorus could be used for making ohmic contacts even using screen-printing silver paste, in which silver is functional element.

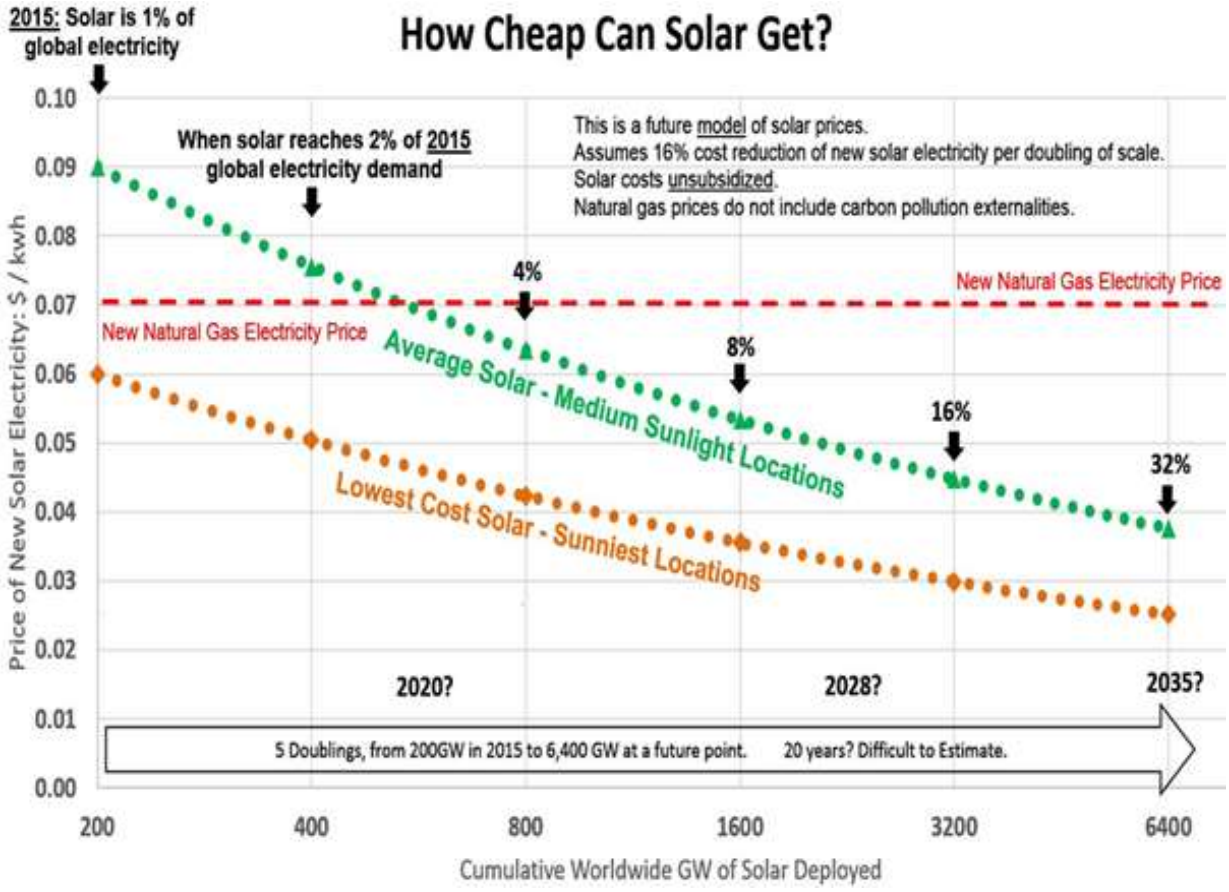

Figure 1.6 Curves of the solar electricity cost and forecasts

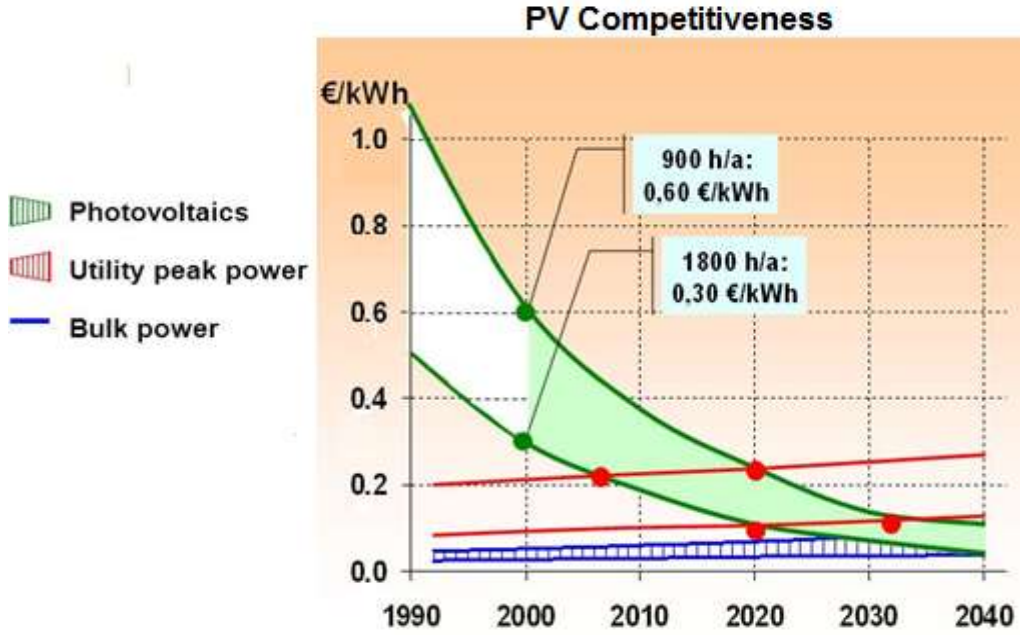

Figure 1.7 Electricity generating cost for PV and utility prices

One of most common way to reduce the cost of photovoltaic is to use thin silicon wafers without loss of conversion efficiency of solar cells. Thin silicon wafers create new challenges, in term of their electrical, optical and mechanical characteristics which are different from conventional silicon wafers even handing is more complicated than conventional wafers. First thing which appear in reducing the thickness is back surface of cell, which are little important in conventional cells. It becomes electrically active.

The carriers which are generated by the absorption of light within the cell, electrons which are minority carriers in case of p-type bases, have major possibility to travel till back surface. Instead of being collected by front contacts. If the back surface do not have any kind of electron repelling property like p+BSF, electrons end their journey at this point and recombine at back surface. In addition to this many photons can pass through entire thickness of wafer without being absorbed in semiconductor material. Overcome these 2 problems we have to design the back surface of solar cell which not only reflect the electrons backward but also reflect the photons back toward the base of material to increase the probability of collection/absorption of photons. A structure that combines the existence of a reflector of electrons and photons is BSF layer with aluminum back reflector layer (in case of thin wafers).

The fragility of thin wafers has resulted in significant breaking rates when they are introduced in line of production or when treated at high temperature [11]. On contrary to thick wafers, thin wafers are more flexible behavior and difficult to handle, Due to this reason, thin wafers must be handled in special way in order to avoid breakage and damages. We have found that thin wafers can be bent to a minimum bend radius and exceeded radius may break the wafers. [12]. Fraunhofer ISE Institute also concluded the existence of minimum radius [14].

The industrial fabrications of silicon solar cells which are based on thin wafers require a better understanding of their mechanical properties. Our institution TIM-EHU also

participated and collaborated with other research groups in different research projects (Cesidel Bimude 2007 thin cells, christhin, and Tobaco) were working on resistances, strength and mechanical properties of material, concluded that there is no relationship between the radius of curvature and thickness of wafers. Wafers are broken due to surface cracks which appear during cutting and processing of wafers by wire saw. It may be deeper than 30 µm [15].

Measurement and analysis of surface of wafers which are removed by chemical etching support the wafers for greater stresses without breaking and consequently smaller radii. [15]. Due to this reason, it seems that thin wafers, which are obtained by thinning of thick wafers by chemical etching, have very low bending radii and high maximum voltages.

At industrial scale, the efficiency that can be obtained by silicon solar cell is range from 16-19% depending on the process and material used. The first industrial technology have presented higher efficiencies than 15% are LGBC (Laser grooved buried contacts) by BP-solar or PCSC (point contacts solar cells) employed by SunPower with efficiency 20%. [16]. In case of SunPower (solar cell fabricating company), the solar cells fabricated by using silicon grown by FZ (float-zone) technology, in order to ensure the necessary high lifetimes. Sanyo solar, commercializing solar module panels with HIT technology (Heterojunction with Intrinsic Thin-layer) new technology, announces modules with cells of 18.5 % [17].

The objective of this thesis is to achieve (P/Al) AlSi industrial technology with cell efficiencies around 18% and thickness of 150 µm. This objective will strongly improve the high efficiency cell fabrication for future. In our opinion there are many technologies which exist in production line, which can be use carefully for mechanical handling of wafers up to 150 µm thick. In addition to this, all our knowledge about mechanical behavior of thin wafer, one part of our work strategy is to optimize the amount of aluminum deposited on backside by using electron beam machine and thermal processing parameters such temperature and diffusion time. These paste which are based on composite of boron and aluminum, it will allow using technology aluminum alloy on backside of wafer of 150 µm thick [18]. As we know, from experimental results, screen printing paste of silver can produce deformation at front surface of the cell. For proper handling of geometry of front electrical contacts, the composition of the glass-frit of the paste and proper condition of firing (time and temperature) allows partially to compensate the tension/problem caused by the alloy of Al-Si of backside.

The efficiency of solar cell either can be increased by using high quality substrates (FZ-silicon) as it was the case of SunPower or by using low temperature processes and excellent passivation of surface as in case of Sanyo HIT cells. In both cases, high quality of base of material must be assured. However, these technology are expensive and we do not believe that high cost of FZ silicon allow these technologies to be competitive with other technologies. With respect to low temperature process, those involve a large number of variations on conventional process. Process such as HIT, it includes a large number of steps in plasma equipment for deposition of amorphous silicon layers. From there, it is necessary to look exquisitely entire thermal process, in order to avoid amorphous silicon not to crystallize. Crystallization may destroy the passivation properties of cells. It is necessary to synthesize screen printing paste for new metallization at commercial scale availability for low temperature fire 750 ^{0}C. In short, it looks a very complex and uncertain competitive process.

The option is selected to implement a process which is based on AlSi, in which phosphorus is supersaturated at front surface and aluminum alloy on back surface. These processes ensure high lifetime of electrons in material and important source of gettering of metallic impurities. This process will be compatible with monocrystalline or polycrystalline silicon wafers, while wafer will be based on monocrystalline Cz industrial wafers.

Increase of efficiency of these solar cells will be based on formation of lightly doped deep phosphorus emitters, which is usually formed by using phosphorus diffusion in saturated conditions. However in case of phosphorus gettering is compromised and high diffusion time is required which severely limit productivity of the process.

There are two technical problems which must be solved for utilization of deep emitters. First is surface passivation for lightly doped deep emitters, passivation will be done by applying SixNy layer in plasma equipment by PECVD. Second is the electrical contact of emitters, which is complex due to specific contact resistance of silver pastes. It dramatically increases with decreasing surface concentration of impurities. For this process which we proposed the use of selective emitters incorporating phosphorus dopant, with this technology we expect to obtain an efficiency of 16.5%.

Selective emitters are already used in some industrial technologies, as SunPower cells and LGBC (Laser grooved buried contact) in case of BP-Solar. Recently two German groups have shown that is possible to form emitters in case of aluminum and phosphorus through laser.

1.3 Description of P/Al technology

In the mid of 80´s, theoretical and experimental studies of A. Cuevas and M. Balbuena have given a conclusion that it is possible to obtain high efficiency with lightly doped deep phosphorus emitters and aluminum back surface field, P/Al (P emitters- Al BSF). They have obtained efficiency around 19% by using high quality FZ (float zone) monocrystalline silicon wafers [6]. In fact when the process was described in mid of 80´s, efficiency achieved was remarkable and among the best silicon solar efficiency reported in the world. The structure of P/Al solar cell is shown in figure below.

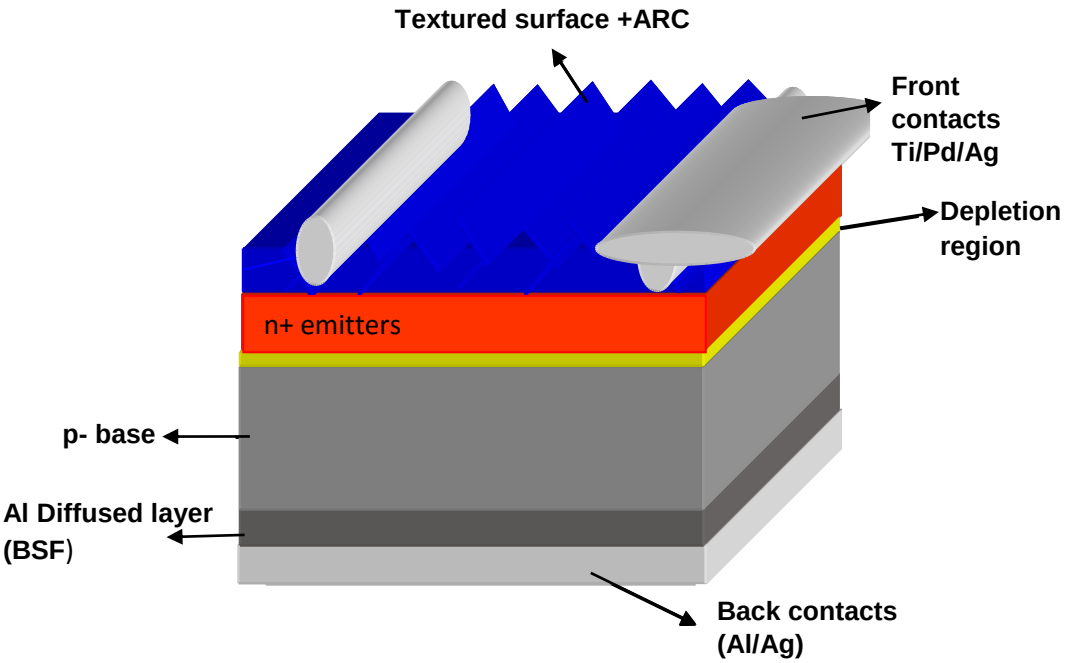

Figure 1.8 Structure of standard P/Al solar cell

The P/Al structure mentioned above of high efficiency can apply to other materials with simplicity; it can be considered useful tool to evaluate the, solar grade potential of materials for photovoltaic application both for monocrystalline and polycrystalline silicon.

The main features of this fabricating process, which we can call as standard process, is consist of simultaneous diffusion for formation of front phosphorus emitters and back surface region as a highly doped aluminum as back surface field.

1.3.1 Research objective:

In this work, we have focused on the fabrication of P/Al solar cells with high efficiency process around 18% by using Cz wafers (other than FZ wafers). The research objective is divided into the following specific tasks:

1.3.2 Task1: Lightly doped phosphorus emitters

One of objective of this work is get lightly doped homogeneous P emitters with moderate surface concentration. Conventional phosphorus emitters doped by using screen printing technique are in range of 40-60 Ω/□ and different characteristic of expected cells are studied by analyzing PCD (Photo conductance decay) and Sun-Voc (irradiance versus open circuit voltage) techniques. For homogeneous emitters, P doping is carried out by diffusion in a quartz tube by passing nitrogen gas through a $POCl_3$ source understand different temperature and quartz furnace conditions. Addition to this we have evaluated sheet resistance, surface concentration and junction depth. Deep emitters which are around 100Ω/□, provide high efficiency.

1.3.3 Selective phosphorus emitter

Conventional homogeneous emitters are formed over full area of silicon wafer by using $POCl_3$ as a source of phosphorus at 800-875 ºC and nitrogen as a carrier gas in tube furnace under standard conditions. Selective emitters are doped selectively with P either by using a tube furnace or other means such as laser, inkjet are called selective emitters. For selectivity of emitters, these are lightly doped under passivated area, open for illumination and heavily doped under metallic contacts. These emitters allow to be metalized by industrial techniques such as screen printing and ink-jet.

1.3.4 Task2: Surface passivation

Front surface passivation we focused on silicon nitride and tandem silicon oxide. Silicon nitride not only passivates the surface but also acts as antireflection layer which is important for high efficiency process. While in case of back surface passivation, Aluminum has been deposited on backside of wafer by electron beam machine and disseminated in quartz furnace (diffuse deeper inside silicon). The extraction of impurities or gettering as well as effect of BSF layer (Back surface field) has been assessed through lifetime and sun-Voc measurements.

P/Al process for solar cells fabrication is shown in figure 1.9 which also represents the minor tasks with little modifications. Process used in this work is modified as compare to standard process described by A. Cuevas and M. Balbuena. [6]

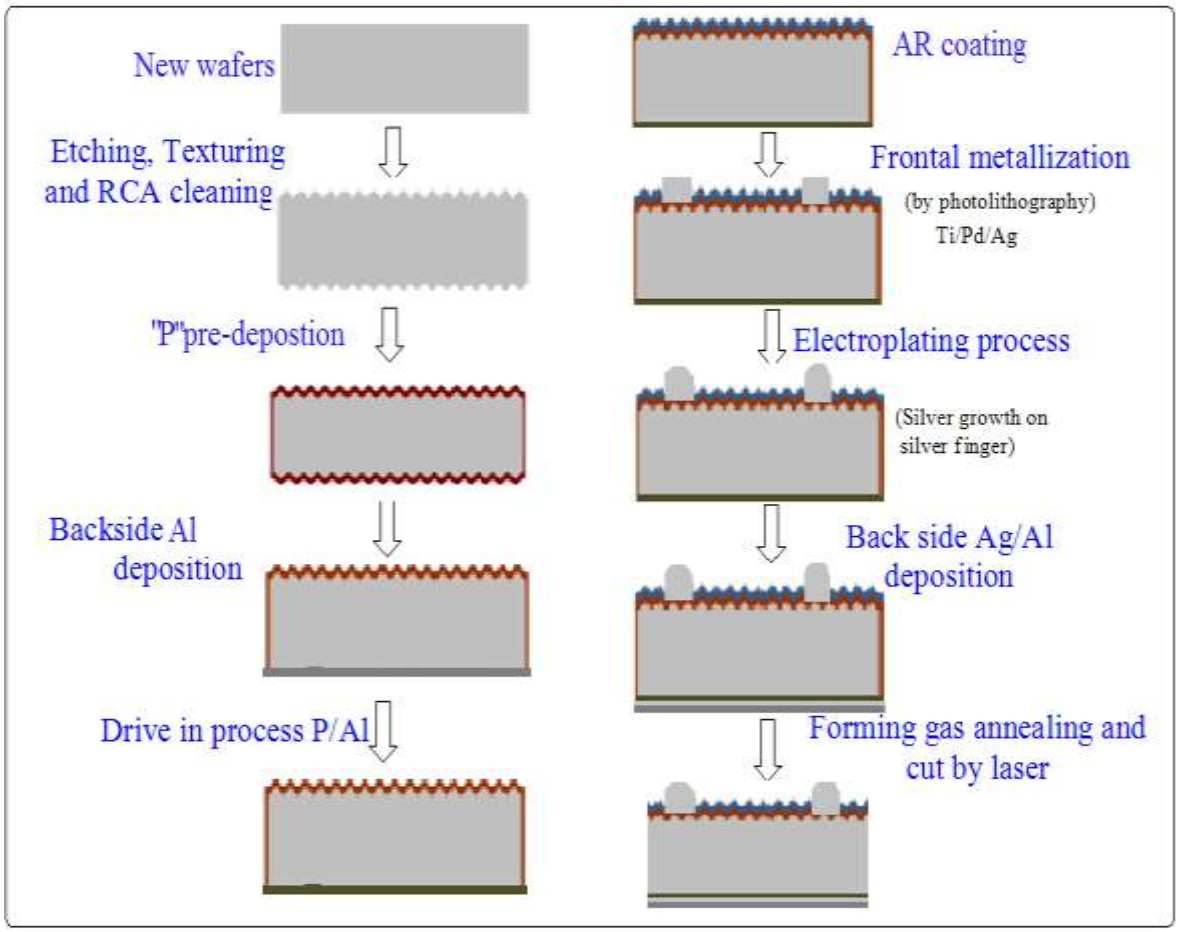

Figure 1.9 Typical silicon solar cell fabrication steps by using P/Al standard process

Lot of work has been done to improve this standard P/Al process and to reduce the fabrication cost by modifying the technological steps. Our main objective is similar, to improve this P/Al standard process for high efficiency and to reduce the cost. In future this standard process will be apply for industrial silicon solar cells fabrication.

Standard P/Al process was design and developed in Institute of Solar Energy, Polytechnic university of Madrid (IES-UPM). This process was first time investigated by J. Alonso on Float-zone wafers of different resistivity. The results are given in doctoral thesis [19]. Subsequently Rosa Lago performed various process of P/Al on Cz wafers supplied by Bayer. She used Cz p-type wafers with resistivity 1.4 Ω.cm and 130-170 µm in thickness, the best result are given in the table 1.1 [7] . Later A. Mousaousi optimized this process to apply on multicrystalline materials with resistivity 0.5 Ω.cm. During this investigation, A. Mousaousi made some modification in standard process. In this new process, he had introduced novelty in initial step of extracting the impurities by phosphorus that is called pre-gettering. In addition to this, new process reduced the thermal budget by uniting step P predisposition and P and Al drive in (redistribution) in one step. Detail of process is given below;

1. “P” pre-gettering step at 850 ^{0}C for 30 minutes, Thus it improves the lifetime of wafers, over all solar cell characteristics will be improved. Etching process removes the diffused area from both sides.
2. Thermal oxidation of wafers in both dry and wet conditions at 950 ^{0}C for 4 hours.
3. Defining the active area on front surface by photolithography and removal of oxides from window, where solar cell to be placed and whole back surface.
4. Alkaline texturing of surface.
5. Evaporation of Aluminum 1µm thick on backside of wafer.
6. For P pre-depostion and redistribution of impurities, optimum temperature was chosen, was 900 ^{0}C for 12 hours. During this step, emitters with depth junction 0.5 µm and surface concentration of $5x10^{19}/cm^3$ was achieved with passivated surface.
7. Metallization of front contacts was carried by electron beam machine by using photolithographic technique. Metallization of back contacts was carried out by evaporation by EBM.
8. Forming gas annealing at 450 ^{0}C for 20 minutes (90% nitrogen and 10% hydrogen).
9. Finally deposition of double antireflection layer (ZnS + MgF2).

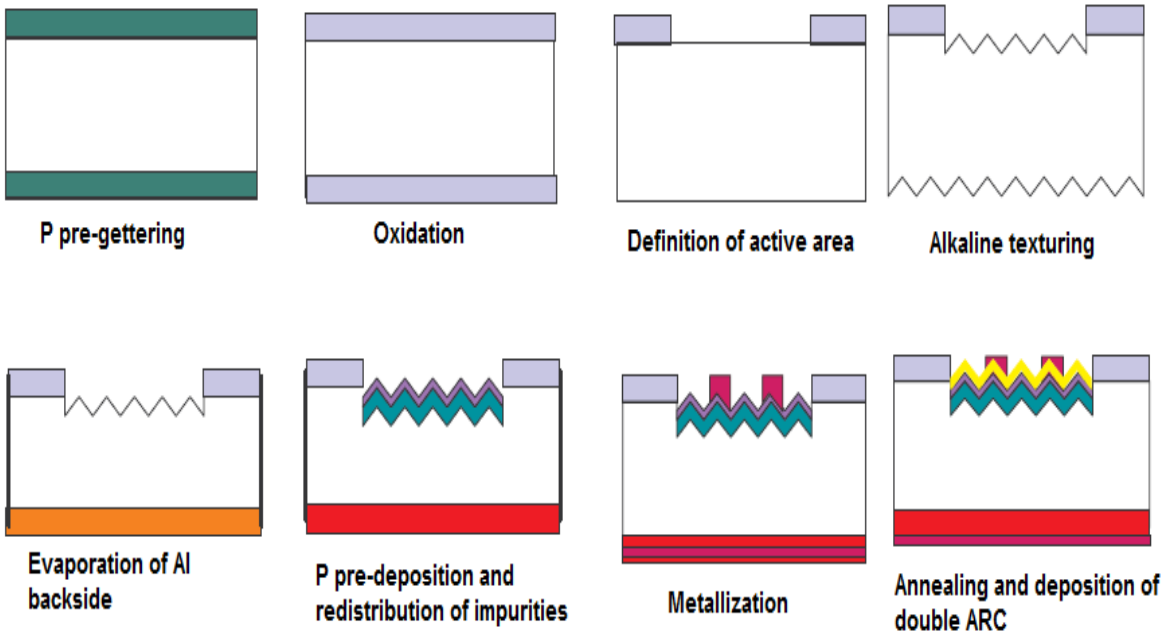

Figure 1.10 Solar cell fabrication processes at moderate temperature by simultaneous diffusion of P and Al [12]

Table1.1 shows typical results of standard P/Al process obtained during solar cell fabrication by using Float zone substrate (high quality wafers), Cz substrate (low quality wafers) and multicrystalline substrate.

Table 1.1

Type of wafers (Resistivity in Ω.cm)	Voc (mV)	Jsc (A/cm^2)	FF (%)	Efficiency (%)	References
Monocrystaline FZ (0.3)	645-650	35	75-83	17.5-19	(6)
Monocrystaline FZ (0.3)	645-650	35	81-83	18.5	(19)
Monocrystaline FZ (1)	628-632	37-38	81	18.5-19.5	(19)
Monocrystaline FZ (20)	612-618	38-39.5	79-81	18.5-19	(19)
Monocrystaline CZ (1.4)	603	33.5	79	15.9	(7)
Monocrystaline CZ (0.5-1.5)	602	35.4	82	17.5	(7)
Monocrystaline CZ (0.5-1.5)	601	36	83	17.8	(7)
multicrystalline (0.5)	635	34.1	79.7	17.3	(20)
Multicrystalline (1.5)	611	33.5	74	15.3	(21)

In A. Mousaousi P/Al fabrication process, high lifetime was measured along with high efficiency on multcrystalline wafers. Although this process has advantage of high efficiency with high lifetime but this process has disadvantage of long duration of P pre-deposition step and redistribution of impurities (step 6 as mentioned above). Its high thermal load made this process unsuitable for other substrate. In addition to this process has low reproducibility [20].

Initial lifetime (µs)	After P pre-gettering (µs)	Final lifetime (µs)
30	100	105

After A. Mousaousi, S. P. Alcántara investigated fabrication of multicrystalline silicon solar cells by using P/Al process with high resistivity. In this process the innovation was simultaneous extraction of impurities by phosphorus and aluminum which is called co-gettering process. But due to high temperature, lifetime was affected, S.P. Alcántara more focused on improvement of lifetime by using passivation technique. The best of results of his research are given in table 1.1 [21]. Later M. C. Delgado was working on fabrication of silicon solar cell under concentrated light by using P/Al technology, with minor modification in concept of cost reduction and industrialization at UPM and UPV/EHU. Flow sheet of fabrication process is shown in figure 1.11. During her investigation and fabricating process of solar cells, she has obtained average efficiency around 18.5% and maximum efficiency 20.2% under 100sun on p-type FZ wafers. More detail of her work is given in reference. [22]

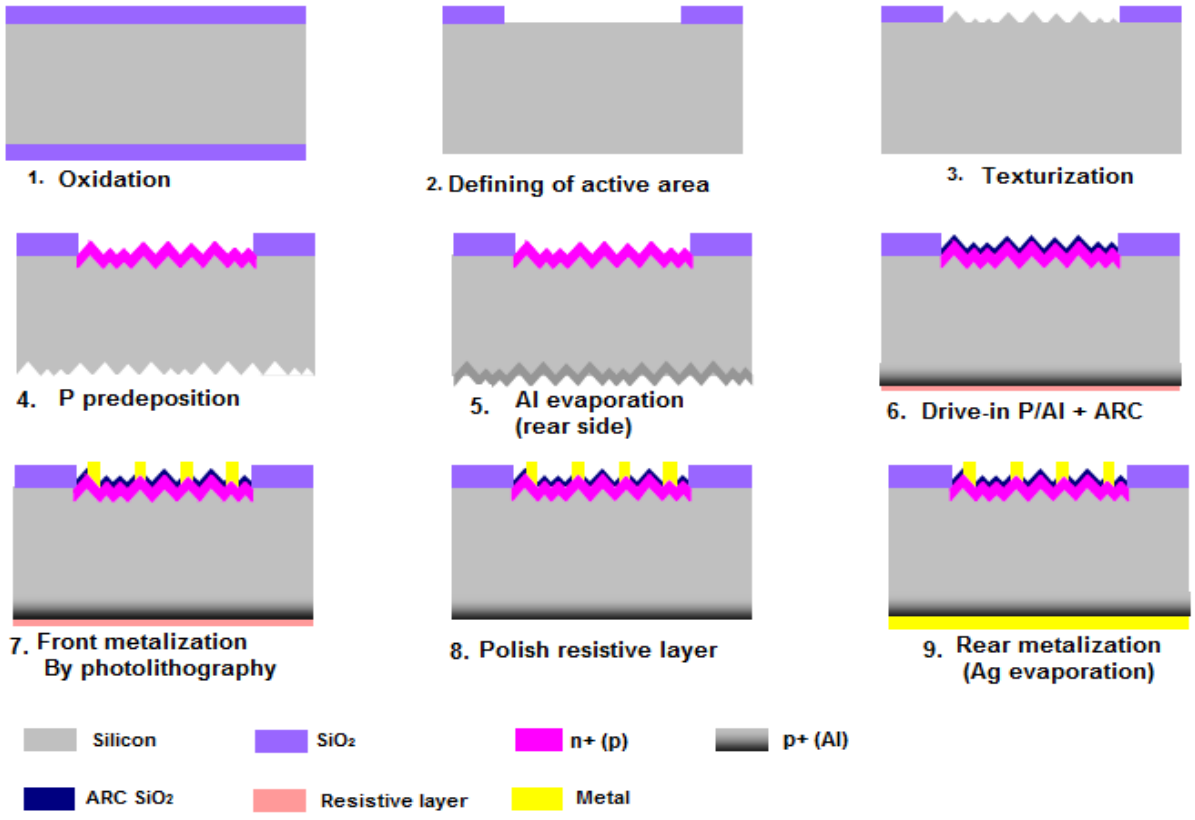

Figure1.11 Fabrication process of solar cell at UPM-PPV

1.4 References:

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Chapter 2

2 Basic of Solar Cell Physics

2.1 Current Voltage characterization

A solar cell is a PN junction diode which is used to create electricity under illumination. The electric current is due to formation of electrons and holes by the absorption of sun light. Before absorption of light (photon) electrons are tightly bound in covalent bonds between neighboring atoms and are unable to move freely in the lattice. By the absorption of light these bounded electrons get free and excite them into conduction band, while covalent bond with missing electron behaves as hole. This hole with missing electron allows the neighboring bonded electrons to convert into hole, leaving behind another hole and in this way holes can move through the lattice. In this way, by the absorption of sun light (photon) holes electrons pairs are created in semiconductor. It is important that photons must have greater energy than band gap energy in order to excite electrons from valence band to conduction.

The solar frequency spectrum is an approximate a black body spectrum at 5800K. Solar radiations which are reaching at the earth surface have higher energy than band gap energy. Some part of photon energy is used to excite the electrons and rest of energy is converted into heat by via lattice vibrations, this phenomenon is called phonon. These electrons and holes pairs move randomly through the lattice and net current flow is zero. To get non-zero net current flow, it is necessary to control the flow of electrons and holes in preferred direction. It is obtained by creating a PN junction or diode by diffusion process. During junction formation, electrons diffuse from the region of high concentration of N-type side of junction into the region of lower concentration that is P-type side of junction while holes moves from P-type side of junction into N-type. Due to diffusion of carriers (electrons and holes), on either side of junction creates charges separation on both side of junction which creates an electric field. This PN junction creates an electric field and electric field creates a diode which promotes charges or carriers flow knows as drift current. This drift current is driven by an electric field [1-5].

As we know that in N-type of semiconductor electrons are majority carries while in P-type of semiconductor electrons are minority carriers. In PN junction electrons start moving from high concentration to low concentration from N-type to P-type by diffusion. This diffusion of electrons constitutes current which is called diffusion current. Similarly holes diffuse from P-type semiconductor to N-type semiconductor, as a result of this diffusion or flow of holes create immobile ions near the junction as shown in the figure 2.1. The immobile negative charges of P-type material and positive charges of N-type material create a depletion of free mobile carriers which is called depletion region. This is region by which electrons and holes diffused across the junction and it does not contain any mobile carriers. It is also known as space charge region [1-5].

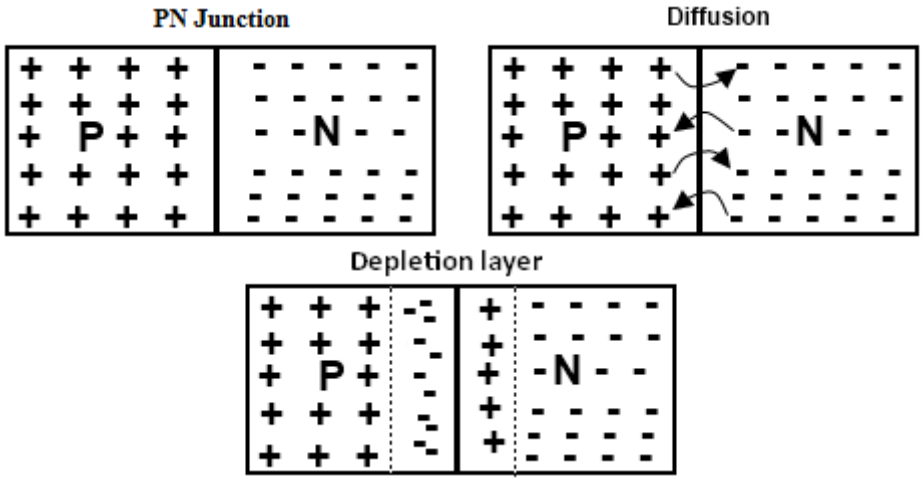

Figure 2.1 Diffusion of electrons and holes to form a depletion layer

Since electrons are negative charged and holes are positive charged, these charged particles or carriers respond to electric field and electrons (negative charged particles) swept to N-type region while holes (positive charged particles) are swept to P-type regions. This flow of charged carriers across the PN junction creates photocurrent (I_L). The separation of charged particles or carriers also creates potential difference or voltage (V) across solar cell diode which is called photo voltage. This potential difference or voltage allows the photocurrent to flow in external circuit connected to cell. Electrons flow from N-type region to external circuit and return to P-type where they are reinjected in low energy status.

During generation process, generated minority carriers are lost due to recombination in the different region of Si solar cell. Recombination may be in the base or depletion region/space charge region, that is called bulk recombination region or in the p+ BSF region or rear surface. Due to this recombination process carriers are being lost and overall reduce the photo-generated current. Recombination also occurs in emitter and at front surface and minority carriers are being lost before their transfer to external load. Recombination regions are shown in the figure 2.2 [1-5].

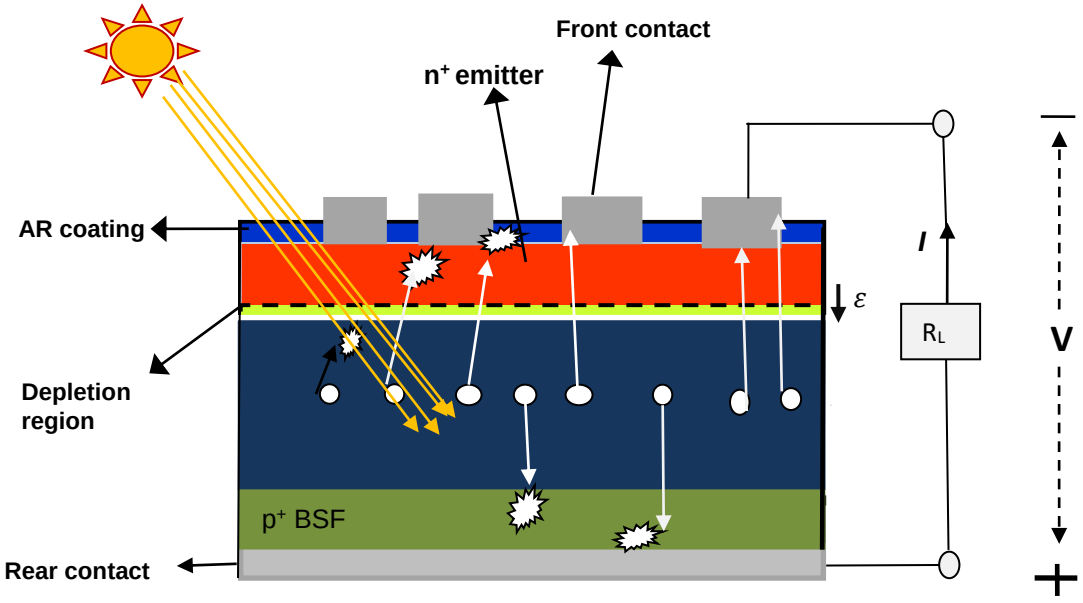

Figure2.2 Representation of $n+pp+$ solar cell with recombination regions

White spots represent electrons (minority carriers) in Si solar cell after generation, representing recombination processes in possible recombination regions while rest of them extracted to metal contacts (external load) in the direction of electric field across the PN junction. The resulted current is less than current generated from light photons.

Mathematically net current I is given by equation 2.2. Whereas I_0 is saturation current density and n is ideal factor. Equation 2.1-2.2 is simple diode equation which described the behavior of IV curve in forward biased diode. Dark current in reality is diffusion current produced by diffusion of electrons n+ emitter to electron deficient P-type base. Drift current which is produced by photo generation, carriers flow in opposite direction to dark diffusion current. According to superposition principle photo generated drift current is subtracted from dark current. In graph IV curve of solar cell which is a diode IV curve shifted downward by light generated current (I_L) as shown in figure 2.3.

$$I = I_0\left[e^{\frac{qV}{nkT}} - 1\right] - I_L \tag{2.1}$$

$$I = I_L - I_0\left[e^{\frac{qV}{nkT}} - 1\right] \tag{2.2}$$

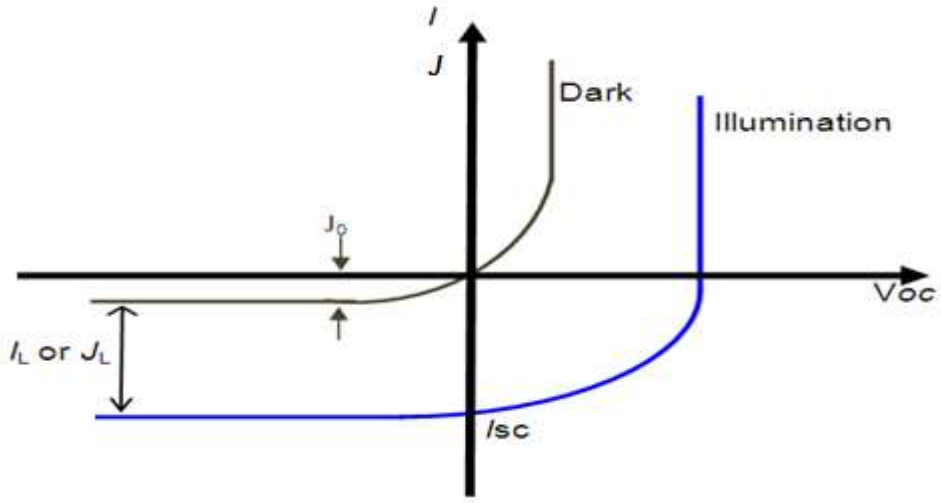

Figure 2.3, I-V characteristics of a solar cell under illumination and dark

It is noted that photo-generated current is negative due to its direction of flow, which is opposite to flow to electrons (as shown in diode model). However, conventionally photocurrent in solar cell is written as positive current. Equation 2.2 can also be written in the form of current density. J (A/cm^2).

$$J = J_L - J_0\left[e^{\frac{qV}{nkT}} - 1\right] \tag{2.3}$$

There are two important operational modes for solar cell, one is open circuit, when there is not current flow to external load, *I*=0. Second is short circuit when current flows to external load (short circuit condition). In short circuit condition there is no potential drop or voltage difference across the solar device, V=0. When voltage is zero, second part of equation 2.3 is cancelled due to zero voltage. $J_{SC} \approx J_L$ which is the maximum output current of solar cell.

When current is not flowing to external load, under open circuit conditions *I*=0 or (*J*=0), we can write equation 2.3 as follow:

$$V_{OC} = \frac{nkT}{q}\ln\left(\frac{I_L}{I_0} + 1\right)$$
$$V_{OC} = \frac{nkT}{q}\ln\left(\frac{J_{SC}}{J_0} + 1\right) \tag{2.4}$$

Detail of Open circuit voltage and short circuit current is given next session

2.2 Equivalent circuit diode model of solar cell

It is useful to create a model of solar cell which is electrically equivalent circuit model in order to understand the electronic behavior. It is based on discrete electrical components whose functions are fully known. An ideal solar cell is modeled by current source in parallel

with rectifying diode. In Practice no solar cell is an ideal solar cell due to shunt and series resistance components. These components are added to equivalent model circuit and resulted model is shown in circuit diagram (figure 2.4). Due to these components, solar cell deviates from ideal behavior.

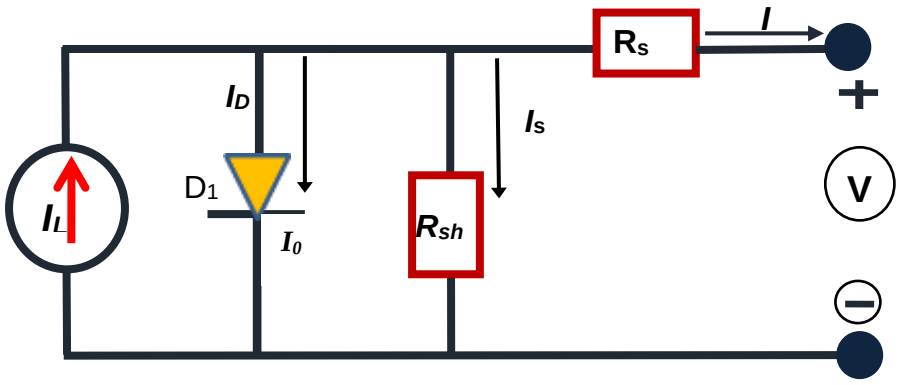

Figure 2.4 Equivalent circuit model of solar cell

From equivalent circuit model, it is evident that current produced by solar cell is equal to current produced from the sun light (photons) minus current flows through diode, minus current flow to shunt resistor.

Mathematically;

$$I = I_L - I_D - I_{SH} \tag{2.5}$$

I is output current, I_{SH} is shunt current while I_L is light generated current and I_D diode current which flows through diode.

The current through these elements of circuit is governed by voltage across them

$$V_j = V + IR_S \tag{2.6}$$

While *Vj is* voltage across the diode as well as resistor R_{SH} and V is voltage across output terminals (in volts). ***I*** is output current terminals and Rs is series resistance. Current passing through diode is given by Shockley diode equation:

$$I_D = I_o \left\{ exp\left[\frac{qV_j}{nkT}\right] - 1 \right\} \tag{2.7}$$

By definition of ohm´s law, current diverted through shunt resistor is given by:

$$I_{SH} = \frac{V_j}{R_{SH}} \tag{2.8}$$

R_{SH} is shunt resistance (Ω).

By substituting these three equations (2.6, 2.7 and 2.8) into equation 2.5 gives us a basic solar cell equation which is related to solar cell parameters to the output current and voltage.

$$I = I_L - I_0 \left\{ exp^{\left\lfloor \frac{q(V+IR_s)}{nkT} \right\rfloor} - 1 \right\} - \frac{V + IR_s}{R_{SH}} \quad (2.9)$$

The significant parameters of solar cells which are extracted from IV curves are the equivalent series resistance and shunt resistance, which is also called parallel resistance as in shown in figure 2.4. The value of series resistance is much lower than shunt resistance. For ideal solar cell *Rs* would be zero and R_{SH} would be infinite. Since the parameters I_0, R_S, R_{SH} and n (ideality factor) cannot be measured directly; the most common application of the characteristics equation is nonlinear regression to extract above mentioned parameters on the basis of their combined effect on solar cell behavior.

Values of I_0, Rs and R_{SH} also depend upon the real size of solar cell, when the area of solar cell increases, values of I_0 also increases while R_S and R_{SH} start decreasing. If area of solar cell will be double, values of I_0 will be double and R_S and R_{SH} will be half. Above equation 2.9 can be written in term of current density or current produces per unit cell are:

$$J = J_L - J_0 \left\{ exp^{\left\lfloor \frac{q(V+Jr_s)}{nkT} \right\rfloor} - 1 \right\} - \frac{V + Jr_s}{r_{SH}} \quad (2.10)$$

J is current density (Ampere/cm^2)
$\mathbf{J_0}$ is reverse current density (Ampere/cm^2)
$\mathbf{J_L}$ is light generated current density (Ampere/cm^2)
$\boldsymbol{r_S}$ is normalized series resistance (Ω-cm^2)
$\boldsymbol{r_{SH}}$ is normalized shunt resistance (Ω-cm^2)

In Solar cell recombination of electron hole pairs do not contribute to any current, mathematically recombination can be treated in same way as dark diffusion current. As we know recombination process is opposite of photo-generation, so photocurrent is opposed by recombination process. In simple or one diode model of solar cell which is represented in equation 2.9 or 2.10 both effects dark diffusion current and recombination is united into single dark current term. Either increase of dark diffusion current or recombination current increases J_0, which reduced J_{SC} and V_{OC}. For ideal solar cell n=1 but in real solar cell, ideality factor can be greater than 1. The ideal and non-ideal behavior real solar cell is often split up using two-diode model.

2.2.1 Two Diode circuit model of solar cell

In one diode model equation, ideality factor, it is considered a constant value. But in reality ideality factor is function of voltage across the device. At high voltage, when recombination process is dominated by surface and bulk regions then ideality factor is approaching to one. At low voltage recombination in the junction region dominates over bulk and surface region and ideality factor approach to two. The junction recombination is modeled by adding a second diode in parallel to first diode and setting the ideality factor to two.

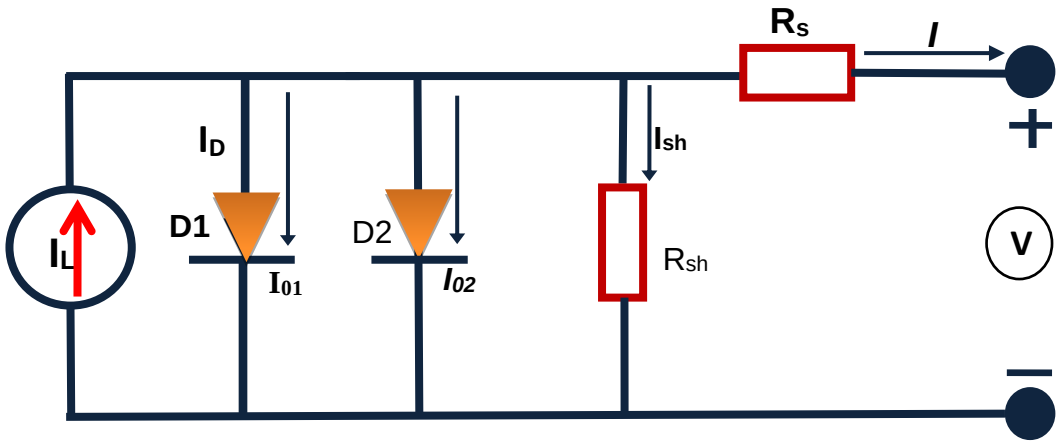

Figure 2.5 Two diode circuit model of solar cell

Under illumination

$$J = J_L - J_{01}\left\{exp\left[\frac{q(V+JR_s)}{kT}\right] - 1\right\} - J_{02}\left\{exp\left[\frac{q(V+JR_s)}{2kT}\right] - 1\right\} - \frac{V+JR_s}{R_{SH}} \qquad (2.11)$$

Above equations are two diode model equations I_{01}, I_{02} (J_{01}, J_{02}) represent saturation current (densities). First term of above equation represent recombination process in the base and in emitters of solar cell, while second term represents the recombination process in the space charge region (depletion region) of the solar cell. In two diode equation, n_1=1 and J_{01} represent ideality factor and saturation current density of ideal diode while J_{02} and n_2 represent the non-ideal diode. The second diode represent the recombination in the depletion region with $n2$=2. In real solar cell $n2$ is often higher than 2 due to various recombination phenomenon. [1-4, 6-7]. It is clear that recombination results in the loss of voltage and current which reduces the efficiency of solar cell [4, 7].

In non-ideal solar cell (real device) may have series resistance (*Rs*) and shunt resistance (R_{SH}). Series resistance is due to bulk resistance of silicon wafers and contact resistance at front and back surface of solar cells. Circuit resistance from connections and terminals also contributes to series resistance. Shunt resistance is mainly due to leakage current at PN junction due to non-ideality factor and impurities near the junction which cause the partial shorting of the junction. All these parameters are shown in the circuit diagram in figure 2.5.

2.2.2 Measurement of IV curve under illumination

For measurement of IV characteristics, it is important to control the standard conditions. It is measured under AM1.5 spectrum and at 25 ^{0}C for terrestrial solar cells. Intensity of radiation power for one meter square area its value is 1kW/m^{2}under one sun illumination. Intensity of radiation is calibrated by using already calibrated cell before real sample cells measurements. Not only the intensity of radiation but also its spectrum must be match with standard spectrum [8-9]. Its short circuit values must be adjusted with radiation output as measures at external laboratory. The current voltage characteristic of solar cell is measured by monitoring current from solar cell point by point from zero to short circuit current by external

electrical load regulator. From IV data measurement, by using computer program or manually we can calculate:

- Open circuit voltage (V_{OC})
- Short circuit current (I_{SC})
- Maximum power (P*max*)
- Fill factor (FF)
- Efficiency (η)

Detail of above mentioned parameters are given at the end of this chapter. All the parameters are important for assessment of quality of solar cell for construction of modules.

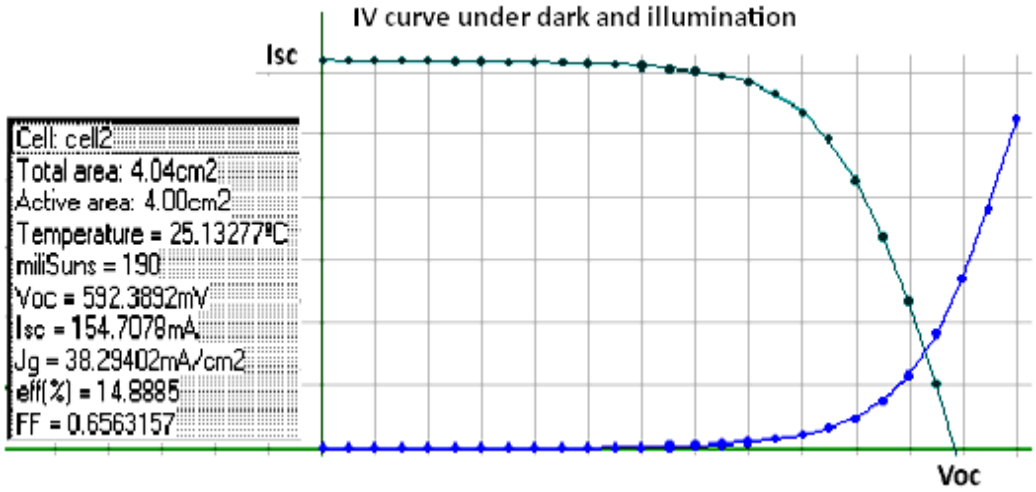

Figure2.6: Computer based information of IV curve under illumination

2.2.3 Measurement of IV under dark and characteristics

The typical graphical form of dark IV curve is shown in figure 2.7 and 2.8. Individual range of dark current characteristics can be assigned different variable in two diode model. Diode equation (2.12) for two diode model is given below.

Under dark

$$J = J_{01}\left\{exp^{\left\lfloor\frac{q(V-JR_S)}{kT}\right\rfloor} - 1\right\} + J_{02}\left\{exp^{\left\lfloor\frac{q(V-JR_S)}{2kT}\right\rfloor} - 1\right\} + \frac{V - JR_s}{R_{SH}} \qquad (2.12)$$

The linear graph of current versus voltage reveals less information about the diode but much more information can be revealed by plotting current on the logarithmic scale. Logarithmic scale plot of same IV curve reveals more information about diode. Different region are dominated by different loss mechanism.

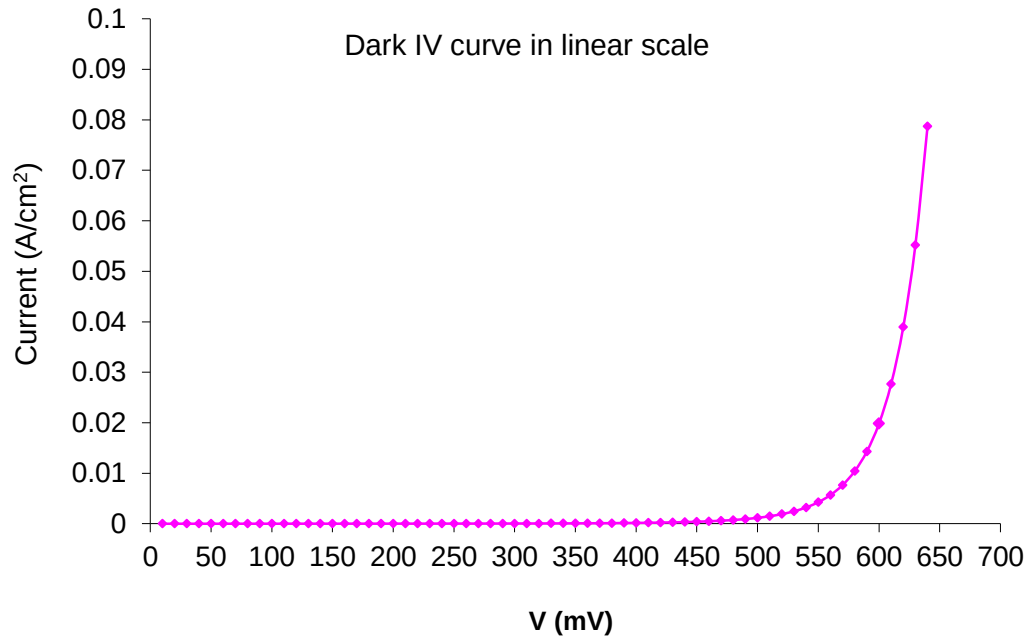

Figure 2.7 Dark IV curve in linear scale

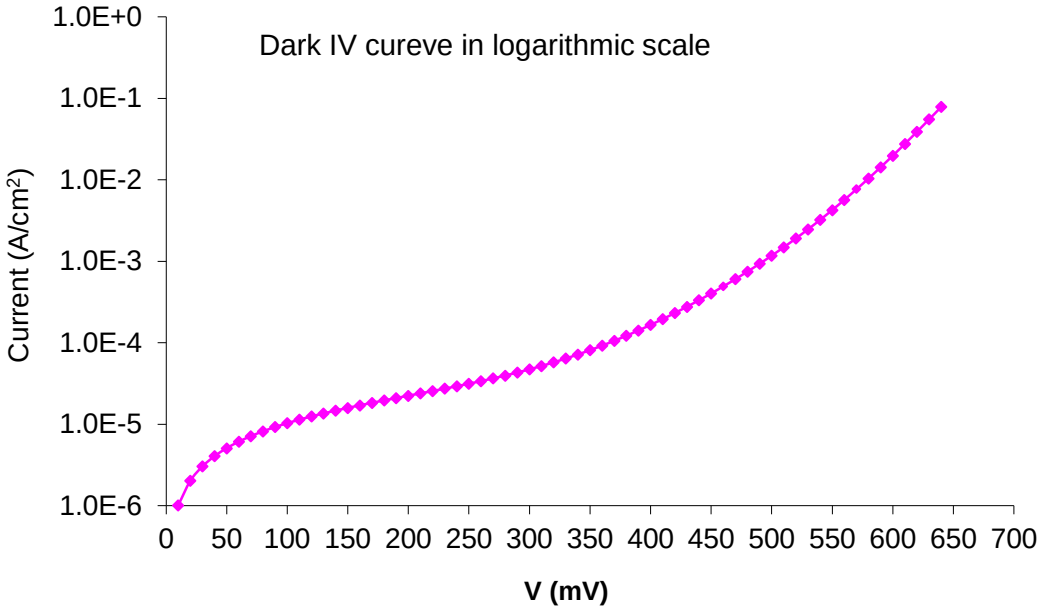

Figure 2.8 Dark IV Curve in logarithmic scale

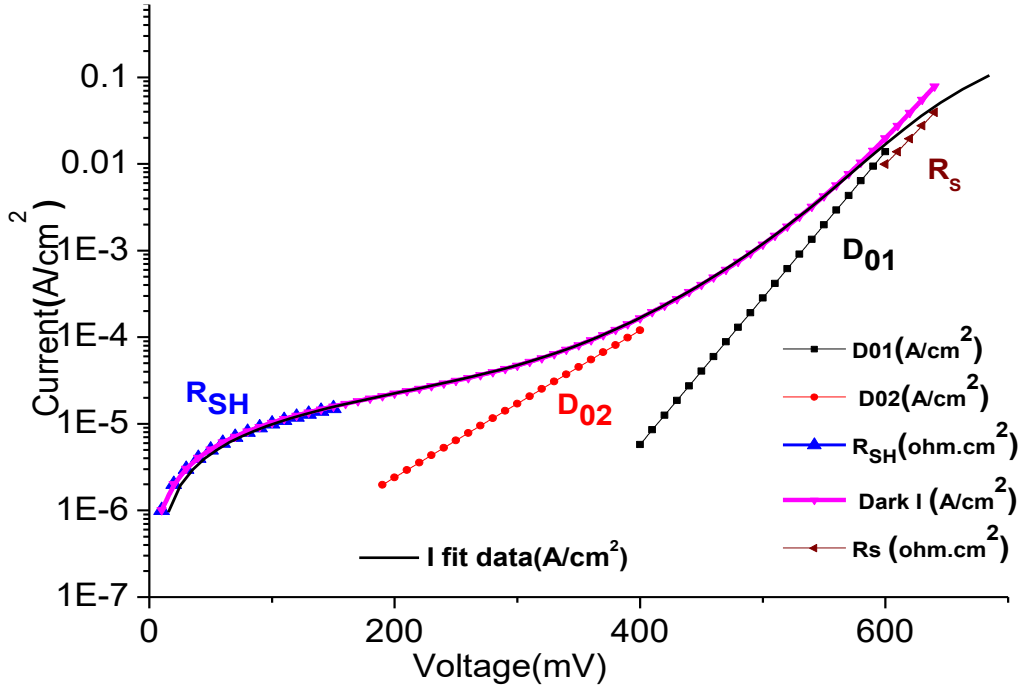

Figure 2.9 Extraction of parameters by fitting of dark IV curve

The dark current in the region of 0 to 150mV, first two terms in equation 2.12 are negligible and dark current is mainly determined by shunt resistance R_{SH} which is also called parallel resistance R_P.

Area in the graph from 200-400mV dark current is assigned to second term of equation 2.13 of two diode model. It is rare relationship with n_2=2. Voltage from 400-600mV. It depends on first term of equation which is dominant. If the dependency is $n1$=1 then saturation current from I_{01} can be determined from it which is responsible for open circuit voltage. Voltage near 600mV to onward, in this region series resistance has influence on IV characteristics.

Based on above assignment as shown in the graph, figure 2.9, different parameters to various regions of dark current characteristics we can determine for all type of solar cell parameters by using different fit program for the measured dark current characteristics. For IV curve adjustment and to fitting the curve we used Multiv fit program, designed by our department (TIM). [10-11].

Series resistance can be more precisely determined by IV curve under illumination as well dark. For Dark current measurement, high voltage is required than open circuit voltage to obtain a current similar values as short circuit current, because additional voltage drop at series resistance must be overcome. From difference between two voltages we can determine series resistance values by using following equation (2.13).

$$V_a - V_{OC} = R_S I_{SC}$$
$$R_S = \frac{V_a - V_{OC}}{I_{SC}} \qquad (2.13)$$

2.2.4 Limitation in two diodes Model

In real solar cell recombination process is a complex function of carrier concentration. In high efficiency solar cell, carrier concentration increase with applied voltage and recombination process change extremely with voltage. In such case analysis is performed by single diode model but allowing both ideality factor and saturation current to vary with voltage. In this case double diode fit model give erroneous values.

2.3 Parasitic Resistance

2.3.1 Series resistance and shunt resistance

During IV curve measurement, efficiency of solar cell is reduced due to parasitic series and shunt resistance. These parasitic resistances can be modeled as parallel resistance which is called shunt resistance (R_{SH}) and series resistance as shown in one diode and two diodes model. This affect is also represented in diodes equation (2.11). For ideal solar cell, shunt resistance should be infinite (No alternate way for current flow) and series resistance should be zero (No voltage drop before load).

Light generated current is usually equal to short circuit current when there are no parasitic resistances. Effect of parasitic resistances is shown in figures 2.11 (a and b). From the equation 2.9, it is concluded that shunt resistances has no effect on short circuit current but reduce the open circuit voltage while series resistance has no effect on open circuit voltage but reduces short circuit current. However their effect mainly reduced values of the fill factor, as a result maximum power output (efficiency) decreased. [1-3].

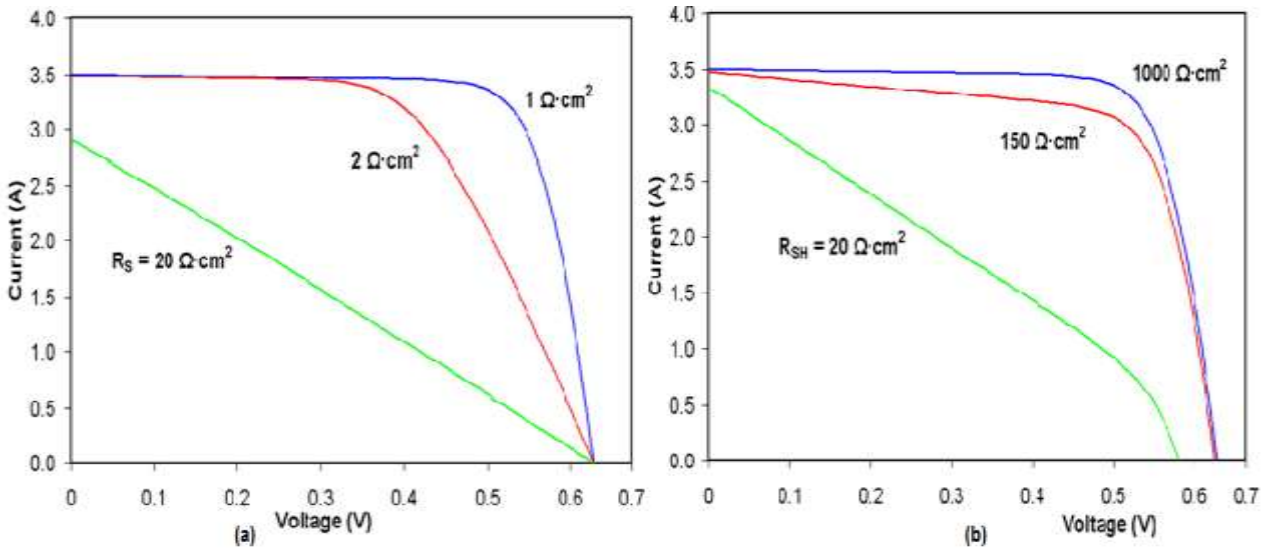

Figure 2.11 IV curves graphs representing effect of series resistance (Rs) in (a) and in graph (b) shunt resistance (R_{SH})

Front and back metal contact particularly front grid also contributes to series resistance. Above equation 2.12 can also written in modified way.

$$I = I_L - I_0 \left\{ exp^{\left[\frac{q(V+IR_s)}{A_0 kT}\right]} - 1 \right\} - \frac{V + IR_s}{R_{SH}} \qquad (2.14)$$

Where A_0 is the ideality of diode (quality) factor, its typical values lies between 1 and 2. A_0=1 for diode dominated by recombination in the quasi neutral region and A_0=2 when recombination dominates in the depletion region.

From IV Curve, it is possible to calculate series and shunt resistance, Rs and R_{SH} from the slope of IV curve at Voc and Isc respectively. The resistance at Voc, however it is at the best proportional to the series resistance but it is larger than the series resistance. R_{SH} is represented by the slope at I_{SC}. Typically the parasitic resistances at I_{SC} and Voc will be measured and noted as shown in the figure.

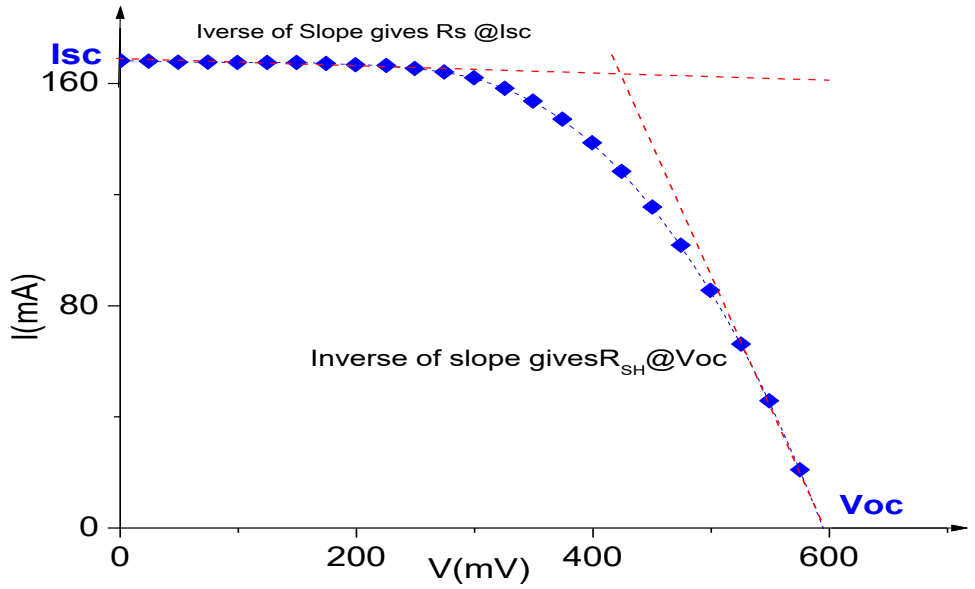

Figure2.13 IV curves for Resistances calculation

2.3.2 Effect of temperature

Temperature affects the characteristic equation directly via T in the exponential term and indirectly via its effect on I_0. With the increase of T reduces the magnitude of exponent in characteristic equation. And I_0 values increases exponentially with T and net effect is to reduce the Voc linear with increase of temperature.

It must be taken into consideration, other parameters such as radiation intensity and temperature; it has also effects on the efficiency of solar cell. All semiconductor crystals are sensitive to temperature, therefore temperature also effect on IV curve. When solar cell is exposed to higher temperature, short circuit current (I_{SC}) increased, while V_{OC} decreased more significantly. Under specific conditions, higher temperature results in decrease in the maximum power output P_{MAX} due to decrease of I_{SC} and V_{oc}. As a result efficiency also decreases.

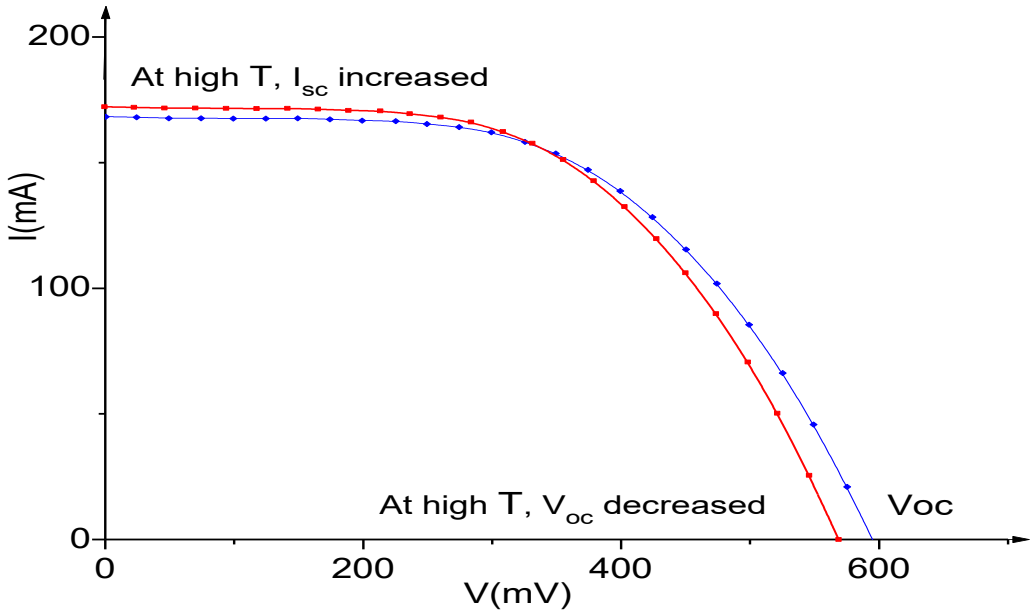

Figure2.14: IV curve Measurement at 25 ^{0}C and 30 ^{0}C of same cell

2.3.3 Short circuit current (*I_{sc}*)

The short circuit current (I_{sc}) corresponds to the short circuit conditions when the impedance is low and is measured when the voltage is zero. In other word the current through solar cell when the voltage across the solar cell is equal to zero.

I (at V=0) =I_{SC}

Short circuit current (*Isc)* occurs at the beginning of the forward bias sweep. It has maximum values of current in power quadrant. For ideal solar cell, short circuit current (*Isc)* is the total values of current produced in solar cell by solar radiation (incident photons) when there is no loss of current due to resistances. Short circuit current (*Isc)* is shown in IV curve in figure (2.15).

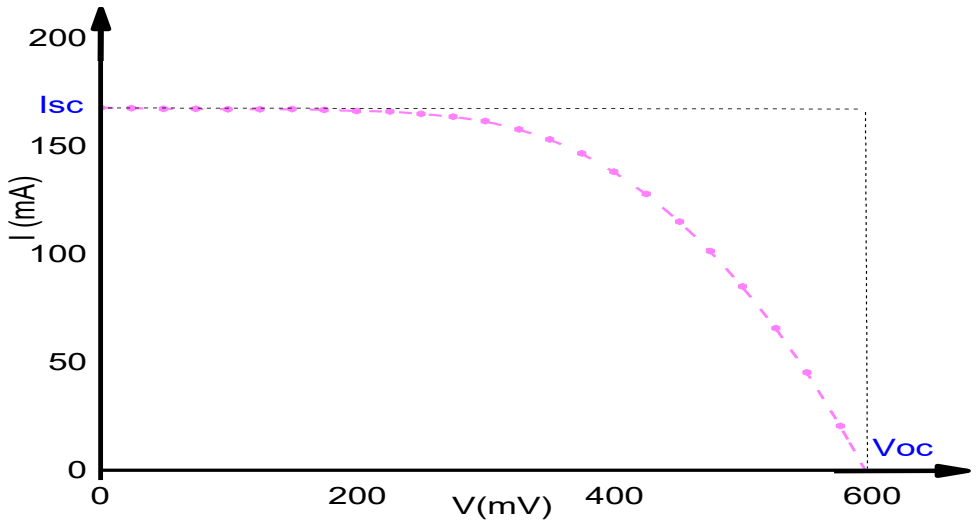

Figure2.15 IV curve under illumination

Isc=I max= I_{ph} for forward bias power quadrant

Short circuit current (*Isc)* depends on the area of solar cell, to remove the dependence of area of solar cell, short circuit current (*I*sc) is usually expressed in short circuit current density (J_{SC} in mA/cm^2)

Generation of current depends on many factors; it is directly related to the intensity of light, spectrum of incident light and optical properties of solar cell as well as collection probabilities, it depends mainly on surface passivation and minority carriers in the base. Short circuit current can be approximated by using equation (2.15) if we have cell with perfect passivation and uniform generation, Equation is given below.

$$J_{SC} = qG(L_n + L_p) \tag{2.15}$$

While
G= Generation rate
Ln and *Lp* = electron and hole diffusion length
q = charge of electron or hole

Although above equation have several assumptions which do not fit completely for conditions encountered in many solar cells. However this equation (2.15) indicates that short circuit current depends mainly on the generation rate and diffusion length. In case of silicon solar cell under AM1.5 spectrum upper maximum limit of short circuit current is 46mA/cm^2. In laboratories short circuit current up to 42mA/cm^2 has been obtained. Short circuit current also depends on the band gap of the material used in fabrication e.g. Short circuit current start decreasing with increase of band gap. While open circuit voltage increases with increase of band gap.

2.3.4 Open circuit voltage (*Voc)*

Open circuit voltage is the maximum voltage available from solar cell when current is not flowing in solar cell. Voltage available from cell when the amount of current is zero (No current flow) is called open circuit voltage (*Voc).* It is corresponded to the forward bias of solar cell due to bias of junction of solar cell with photo-generated current.

V (at *I*=0) = V_{oc}

Open circuit voltage (*Voc) is* graphically represented in IV curve in figure (2.15).

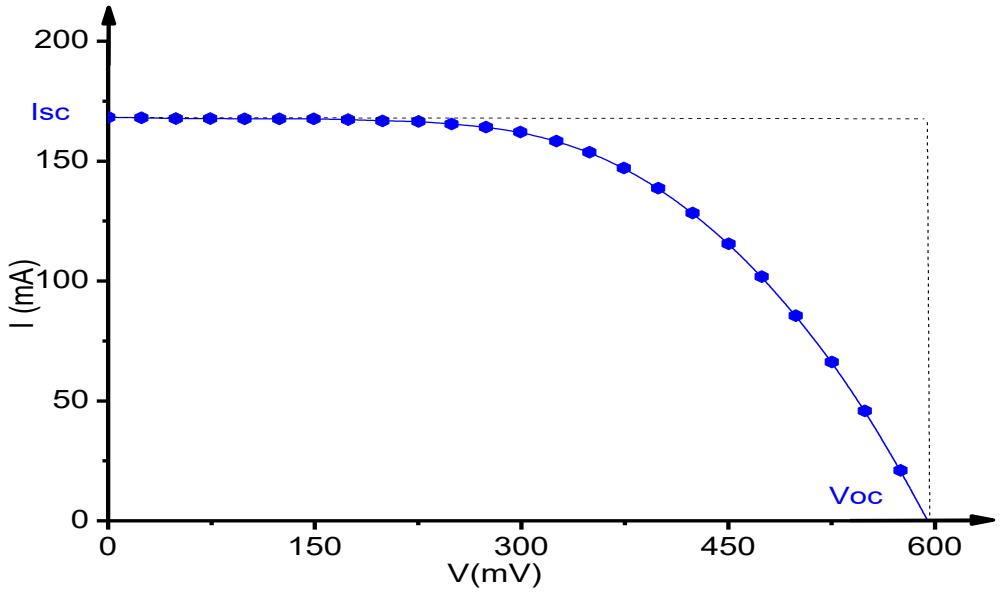

Figure 2.15 IV curve under illumination

We can calculate open circuit voltage by adjusting overall current equal to zero and by considering ideal factor equal to one and shunt resistance is very high enough to neglect it.

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_0} + 1\right) \tag{2.16}$$

While

I_0= Dark saturation current
I_L= photon generated current
n= Ideal factor
T= Temperature
K = Boltzmann constant
q = electronic charge

Open circuit voltage (*Voc)* depends on the dark saturation current that depends on the recombination in the solar cell and photon generated current. Open circuit voltage is a measure of the recombination in the device. Single crystalline silicon solar cells have open circuit voltage (*Voc)* up to 730mV under one sun and AM1.5 conditions at laboratory scale while at commercial scale on multicrystalline silicon solar cells have Open circuit voltage 640mV. Open circuit voltage can be calculated from carrier concentration by using equation (2.17) which is given below. [12].

$$V_{OC} = \frac{kT}{q} \ln \left[\frac{(N_A + \Delta n)\Delta n}{n_i^2} \right] \quad (2.17)$$

While

Δn = is excess carrier concentration
N_A= doping concentration
n_i= intrinsic carrier concentration
T= Temperature
kT/q = Thermal voltage

Open circuit voltage (*Voc)* determined by above equation is called implied *Voc.*

2.3.5 Maximum power (P*max*)

Maximum power (P*max*) is product of I_{MP} and V_{MP}, part of voltage and current participating to get maximum power (Values of current and voltage at P*max* point as shown

$$P = IV \quad (2.18)$$

in graph in figure 2.16. Power can calculate by following equation (2.18).

At short circuit current point or open circuit voltage point, net power is zero but maximum power can be obtained in between these two points as shown in the graphs. The value of power start increasing with the increase of current and voltage and at certain point we get maximum power and this point is maximum power point. After this point value of maximum power starts decreasing till zero values.

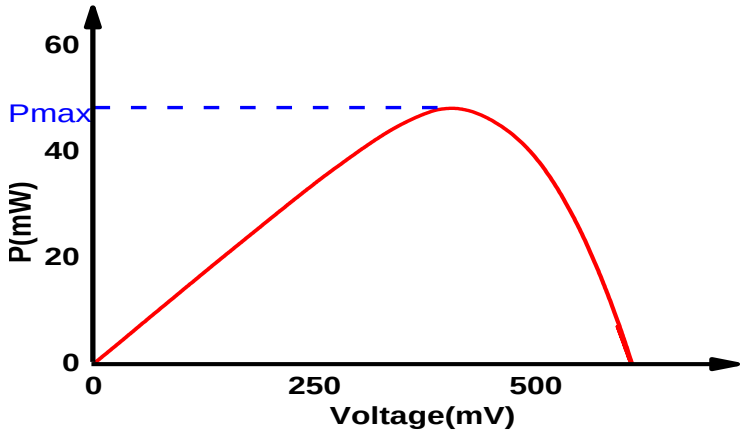

Figure 2.16 (a) (b) Maximum Power for an I-V sweep

2.3.6 Fill Factor (FF)

Fill factor is essential parameter for solar cell characterization which is defined as ratio of maximum power (P*max)* to the area of rectangle formed by open circuit voltage (*Voc)* and short circuit current (*Isc)* as shown in figure 2.17. Maximum power (P*max*) is product of I_{MP} and V_{MP}, part of voltage and current participating to get maximum power (Values of current and voltage at P*max* point as shown in graph in figure 2.17). FF is calculated by dividing the maximum power to the theoretical power (P_T), theoretical power is output of both open circuit voltage and short circuit current [13]

$$FF = \frac{P_{max}}{} \text{ or } \frac{P_{max}}{} \qquad (2.19)$$

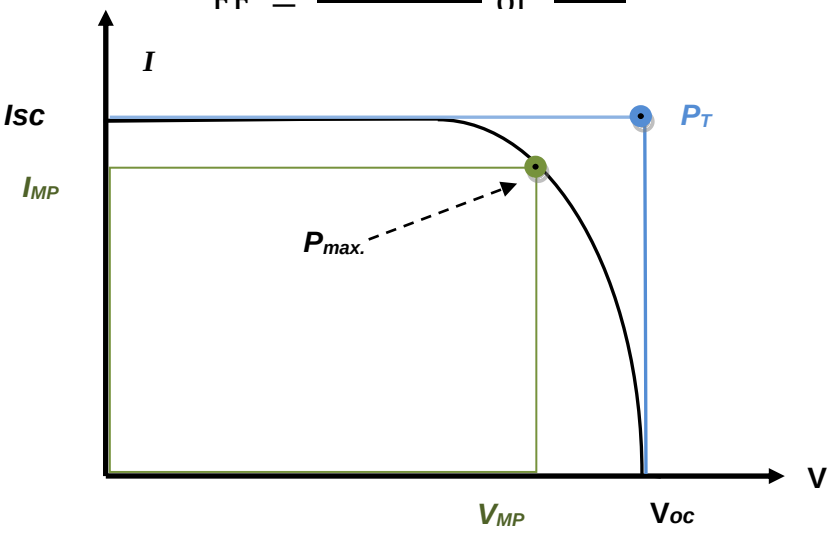

Figure 2.17 Fill factor from I-V Curve.

For good solar cell, larger fill factor is desirable and correspond to I-V sweep that is more square-like. Typical values of fill factors range from 0.5 to 0.85 in case of silicon solar cells, usually fill factors is represented in percentage [14].

2.3.7 Efficiency

Efficiency is the ratio of electrical power output (P_{out}) compares solar power input (P_{in}). It is ratio of energy output from solar cell to input energy from sun light. Efficiency is one of the most common parameter used to describe performance of solar cell and to compare with other cells.

$$\eta = \frac{P_{out}}{P_{in}} \qquad (2.20)$$

$$\eta_{max} = \frac{P_{max}}{P_{in}} = \frac{(V_{OC})(I_{SC})(FF)}{P_{in}} \quad (2.21)$$

Efficiency of solar cell is related to overall performance of solar cell, Reflection has great influences on short circuit current and efficiency. Other common parameters are spectrum and intensity of incident sunlight and temperature. During IV curve measurement, temperature must be controlled. It is usually measured under AM1.5 condition and at 25 ^{0}C for terrestrial solar cells. For efficiency calculation, power input (P_{in}) is taken as product of irradiance of incident light; it is measured in W/m^{2}or mW/cm^2. For 1m^2 area its value is 1000W/m^2 under one-sun illumination. For 1cm^{2}area, its value is 100mW/cm^2. Power input is calculated with respect to surface area of solar cells [1, 14].

2.3.8 Efficiency losses in Solar cell

The conversion efficiency of real solar is always lower than ideal solar cell due to various loss factors. Some of these losses are controllable, we can save efficiency loss but some are intrinsic to the system. Basic principle of solar cell explains physical process by which sun light is converted into electricity, by semiconductor materials. Theoretical study helps us to understand fundamental limits of solar cell and give guidance on the phenomena that contribute to losses and solar cell efficiency.

In general, solar cell operation consists of two steps; one is absorption of sunlight (photon) creates electrons hole pairs and second is transfer of photo excited electrons to external load. Any process which causes loss of photo excited energy of electron before it's captured by external load is known as recombination. This recombination takes place before the completion of step 2. Absorption of sun light results in generation of electrons hole pair, the process by which photo excited electrons loss its energy and being a captured by the lattice which is called recombination of electron with hole.

Efficiency loss mechanism of solar cell is mainly divided in two parts. One is electrical (or electronic) losses and second is optical losses. All electrical losses mechanism in solar cell involves a recombination process i.e. recombination of electron hole pair. It will be discuss in detail in recombination mechanisms (Radiative, Auger and SRH recombination). Optical loss is mainly due to reflection of sun light and low energy photons which are unable to create electron hole pair. Schematic representation of efficiency loss parameters of silicon solar cell is represented in figure 2.18.

When a photon which has energy equal to band gap energy, It excited an electron from valence band to conduction band by the absorption of photon energy (E). If energy of photon is greater than band gap energy (Eg), excessive energy of photon (*E-Eg*) dissipated into lattice vibrations within picoseconds. This loss is known as thermalization loss.

Not all generated electron hole pairs contribute to electric current (efficiency) due to recombination. Due to carriers recombination process efficiency is affected and decreased. The optical and electrical losses mentioned in the figure 2.18 should be minimized in order to get high efficiency solar cell [4].

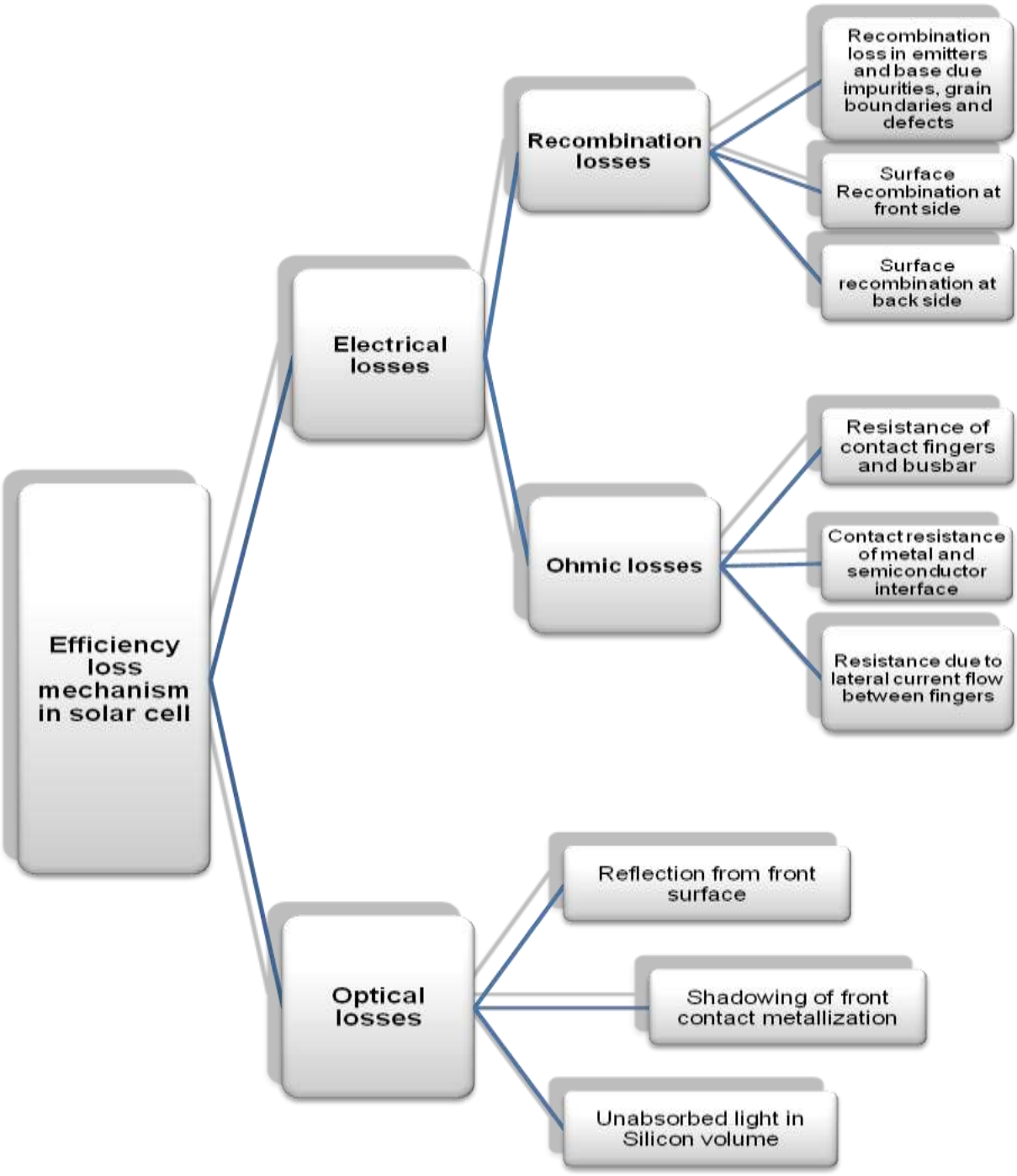

Figure 2.18 Efficiency loss mechanism in silicon solar cell

In silicon solar cell recombination process occurs in various regions such as;

- Bulk region (base region)
- Front emitter regions
- Front surface.
- Rear BSF region
- Rear surface

Recombination regions of solar cell are represented in the figure 2.19

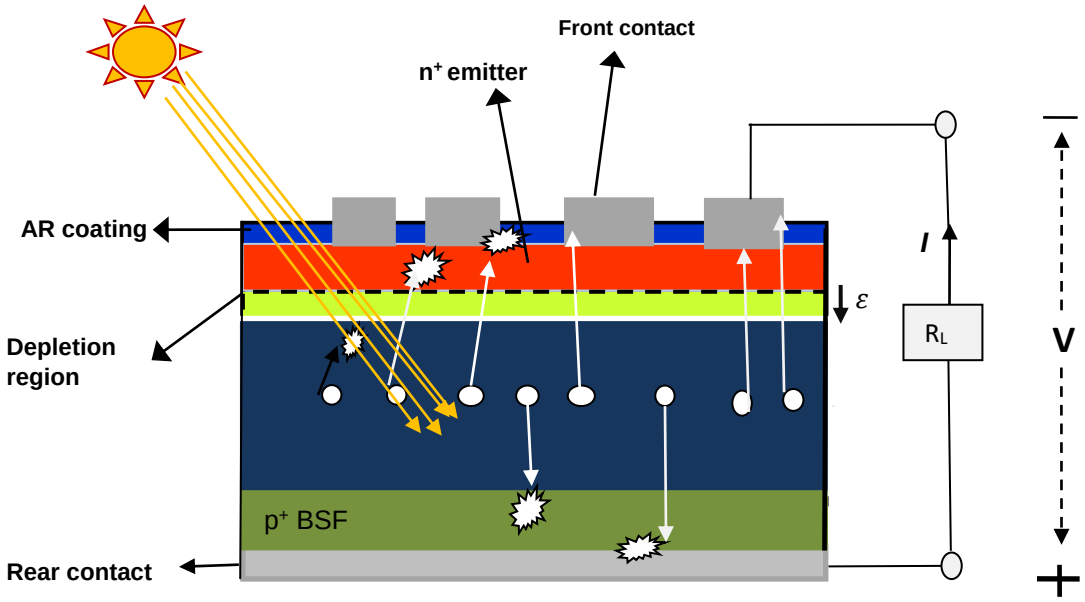

Figure2.19 Representation of $n+pp+$ solar cell with recombination regions

White dots represent electrons (minority carriers) in Si solar cell after generation, representing recombination in possible recombination regions while rest of them are extracted to metal contacts (external load) in the direction of electric field across the PN junction. The resulted current is less than current generated from light photons. Although recombination also occurs in depletion region but in good fabricated solar cell recombination is relatively low. For high efficiency solar cell, reducing recombination losses is very important. It is also one of the objectives of this thesis.

Any electron which exists in conduction band from high energy level will return to into valence band to stabilize in low energy level, where it effectively recombines with hole. This is called recombination. Experimentally recombination loss is quantified as minority carriers' lifetime τ. Lifetime a measure of how long a photo generated electron like to stay around before recombining. It is one of most important parameters for characterization of wafers for power electronic devices and solar cell. Wafers with long lifetime means minority carriers generated in the bulk will persist for a long time before recombining. Usually recombination (R) is expressed in volume recombination rate (U) and lifetime related to recombination rate is given by (2.22):

$$\tau = \frac{\Delta n}{R} = \frac{\Delta n}{U} \qquad (2.22)$$

Where U is expressed cm^{-3}/s, Δn excessive carriers' concentration is in cm^{-3} and lifetime in second (s).

There are three basic types of recombination in silicon semiconductor material.

1. Radiative recombination
2. Auger recombination

3. Shockley Read Hall recombination SRH (Recombination via defects states in semiconductor band gap)

Surface recombination which is due to dangling bonds at the wafer surface; it is considered a special case of bulk SRH recombination applied to the two dimension surface. As recombination occurs in all parts of the solar cell simultaneously, measurements therefore reflect an effective recombination rate and an effective lifetime τ_{eff} by using equation 2.22.

$$U_{eff} = U_{bulk} + U_{emitter} + U_{front} + U_{BSF} + U_{rear\ surface} \quad (2.23)$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{emitter}} + \frac{1}{\tau_{front\ sur.}} + \frac{1}{\tau_{BSF}} + \frac{1}{\tau_{rear\ sur.}} \quad (2.24)$$

Recombination in each region is effected by radiative, Auger and SRH recombination mechanism, Detail of each mechanism is given below.

2.3.9 Radiative Recombination (band to band recombination)

Radiative recombination or band to band recombination correspond to recombination process of electron hole, where an electron in conduction band directly move to valence band to recombine with hole and excess energy is released in the form of photon. The radiative volume recombination is proportional to the electrons concentration in the conduction band and holes concentration in valence band. It is reverse process of photo-generation and energy is release in the form of photon as shown in the figure 2.20.

Mathematically, radiative recombination rate is given by:

$$U_{rad} = Bnp = B(n_0 + \Delta n)(p_0 + \Delta \mathrm{p}) \quad (2.25)$$

Where B is radioactive coefficient, n is the free electrons and p is free holes concentration. While n0 and p0 concentrations in the dark (due to doping) and Δn and Δp are excessive concentration due to light generation in case of solar cell. From detail balance calculation value of B for silicon material is given $2 \times 10^{-15} cm^3 s^{-1}$ [15].

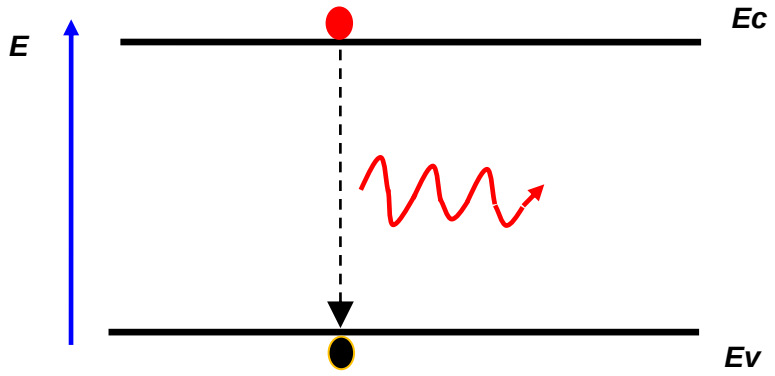

Figure 2.20 Energy band diagram representing relative recombination

By using equation 2.22 and 2.25, the lifetime due to radiative recombination is

$$\tau_{rad} = \frac{\Delta n}{B(n_0 + \Delta n)(p_0 + \Delta p)} \quad (2.26)$$

Under low level injection (LLI) conditions, where ($\Delta n, \Delta p \ll n_0, p_0$) and high level injection conditions, where ($\Delta n, \Delta p \gg n_0, p_0$) equation 2.20 can be simplified as

$$\tau_{rad}LLI = \frac{1}{BN_{Doped}} \qquad \tau_{rad}HLI = \frac{1}{B\Delta n} \quad (2.27)$$

Where N_{Doped} is electrons/holes doping concentration usually represented as N_D for donor and N_A for accepter dopant respectively for n or p-type semiconductor.

It is noted that radiative recombination lifetime is stay constant at low injection but at intermediate or high injection recombination lifetime decrease. The radiative recombination in case of silicon is very low as compared to types of recombination and it has not significant due to that fact that silicon is indirect band gap semiconductor. It means that bottom line of conduction band and valence band do not line up in K-space (momentum).In this process a fourth particle is involved (apart from electron, hole and photon) to the conserve the energy and momentum. See the figure (2.21) [1, 4, and 16].

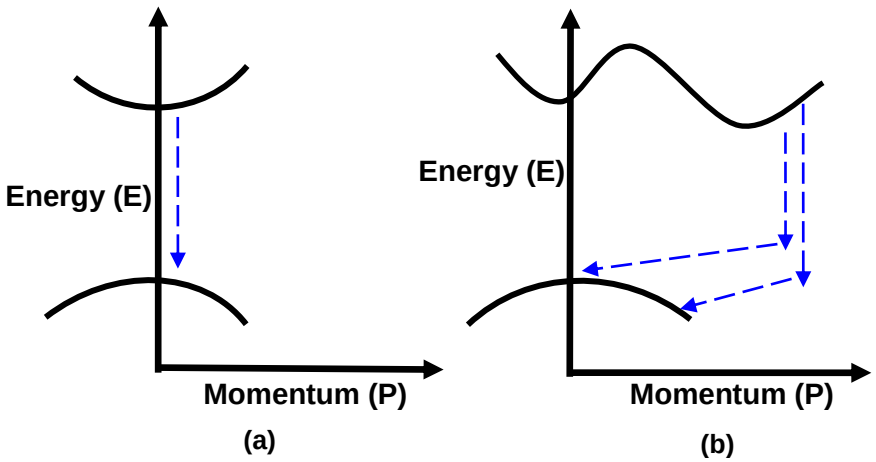

Figure 2.21 Schematic representation of Radiative Recombination (a) direct band gap recombination in GaAs semiconductors (b) indirect band gap in Silicon semiconductor

2.3.10 Auger Recombination

Auger recombination is three particles interaction where an electron in conduction band recombines with hole in valence band by giving extra to energy to third particle which maybe an electron or hole. Mechanism of Auger recombination is shown in figure 2.22.

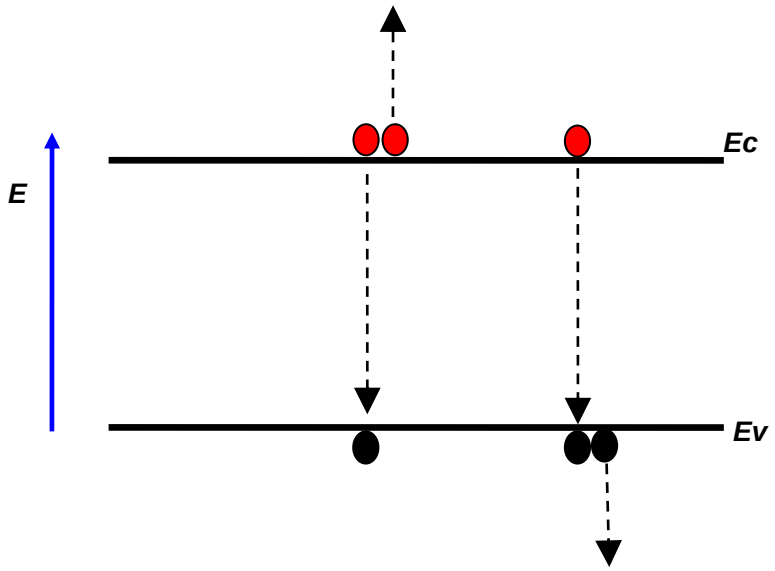

Figure 2.22: Energy band diagram representing Auger recombination process

The 'eeh' and 'ehh' represents the cases where excess energy is transferred to an electron and hole respectively. The total Auger recombination process is sum of two processes two holes and one electron or two electrons and one hole particle *Uehh* or Ueeh respectively. The Auger recombination rate U_{Auger} is given by:

$$U_{Auger} = U_{ehh} + U_{eeh} = C_n n^2 p + C_p n p^2 \quad (2.28)$$

Where Cn and Cp are Auger coefficients, for electrons and holes respectively

Consequently the expression (equation) for Auger recombination lifetime under low and high injection for n-type and p-type silicon are as follows:

N-type Si $\quad \tau_{Auger,LLI} = \dfrac{1}{C_n N_D^2} \qquad \tau_{Auger,HLI} = \dfrac{1}{(C_n + C_p)\Delta n^2}$ (2.29)

P-type Si $\quad \tau_{Auger,LLI} = \dfrac{1}{C_p N_A^2} \qquad \tau_{Auger,HLI} = \dfrac{1}{(C_n + C_p)\Delta p^2}$ (2.30)

The most common used values for Auger coefficient were determined by Dziewior and Schmid: $C_n = 2.8 \times 10^{-31}\,cm^6/s$ and for $C_p = 9.9 \times 10^{-32}\,cm^6/s$ for silicon with dopant concentration greater than $5 \times 10^{18}\,cm^{-3}$ [17 -18].

By the comparison of equations 2.22, 2.23 and 2.24, it shows clearly that Auger recombination is much stronger in heavily doped silicon than radiative recombination. Auger lifetime decreases as the square of doping concentration. While radiative lifetime decreases linearly with doping concentration. Therefore Auger recombination is dominant in emitter region and back surface field. The two values of Auger recombination Cn and Cp show that

Auger recombination in heavily doped n-type silicon is roughly 3 times stronger than p-type silicon. P-type silicon solar cells with n-type emitters are more affected by Auger recombination.

Experimentally many authors have been reported higher Auger recombination rate higher than that calculated by Dzeiwior and Schmid [19].Those higher values of Auger recombination were considered due to coulombic interactions between the charged particles. Recently Kerr and Cuevas [20] have provided some different expression for Auger recombination lifetime but conclusion is same that Auger recombination process is dominant over radiative process in heavily doped silicon and it is three times more effective n heavily doped n-type silicon than p-type silicon.

Revised expression by Kerr and A. Cuevas [20] are valid for doping concentration greater than $5 \times 10^{15}\, cm^{-3}$.

N-type Si
$$\tau_{Auger,LLI} = \frac{1}{1.18\, x10^{-24} N_D^{1.65}} \quad (2.31)$$

P-type Si
$$\tau_{Auger,LLI} = \frac{1}{6x10^{-25} N_A^{1.65}} \quad (2.32)$$

2.3.11 Shockley Read Hall recombination SRH (Recombination via defects states in semiconductor band gap)

Defects in semiconductor can create different energy level within the band gap that can enhance the probability of recombination process. These defect levels also called trap level. In SRH recombination, an excited electron lose its energy in small increment (level traps) in between conduction band and valence band instead of single large step as in case radiative and Auger recombination. SRH recombination mechanism is shown in figure 2.23. Defects in semiconductors are created by doping process or by crystal defects in semiconductor lattice [21-22].

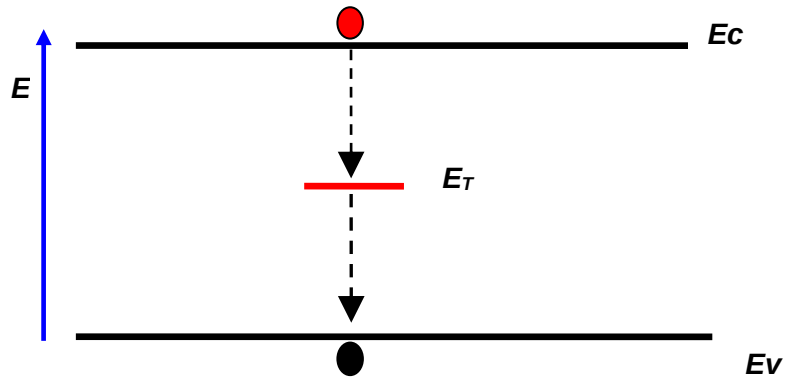

Figure 2.23 Energy band diagram representing SRH recombination process (Recombination through defects level in band gap)

Under 1-sun illumination, SRH recombination is dominant

Mechanism in the bulk region of multicrystalline silicon solar cell. Multicrystalline silicon mostly has defects in lattice or impurities and SRH recombination is dominant mechanism in multicrystalline solar cell. These defects or impurities limits the SRH recombination lifetime of silicon substrate to a few hundred microseconds or even less. While Auger lifetime of silicon wafer with resistivities ($\geq 0.6\Omega.cm$)is over 1 ms using Dziewior and Schmid model or Kerr model [17, 20]. SRH recombination often dominant in bulk region of high quality wafers e.g. float-zone wafers, due to introduction of defect or impurities during solar cell fabrication process.

Recombination rate due to defect levels (level trap) in the band gap was first time analyzed by Shockley, Read and Hall for single defect level [21-22].

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{2.33}$$

Where τ_{n0} and τ_{p0} are electron and hole lifetime which is related to the thermal velocity (v_{th}) and trap density (N_T) and the capture cross section for electrons (σ_n) and holes (σ_p) are:

$$\tau_{n0} = \frac{1}{\sigma_n N_T v_{th}} \qquad \tau_{p0} = \frac{1}{\sigma_p N_T v_{th}} \tag{2.34}$$

The capture cross sections are related to the probability of the defects states capturing an electron or hole. $n1$ and $p1$ are related free electron and holes concentration in case in which Fermi level (EF) lies at the trap energy level, to the fill the trap level with carriers (electrons or holes), which is given by:

$$n_1 = n_i \exp\left(\frac{E_T - E_i}{kT}\right) \qquad p_1 = n_i \exp\left(\frac{E_i - E_T}{kT}\right) \tag{2.35}$$

Where n_i and E_i are the intrinsic carriers concentration and intrinsic energy level respectively. T is the temperature and k is Boltzmann constant. By using equation 2.22, The SRH recombination lifetimes can be obtained as follows:

$$\tau_{SRH} = \frac{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)}{n_0 + p_0 + \Delta n} \tag{2.36}$$

From equation 2.36 it can be seen that SRH recombination lifetime depends on dopant concentration, injection level and defects, specific properties like capture of cross-section and defects energy level. The expression for SRH recombination lifetimes under low and high injection conditions are as follows.

For N-type Si

$$\tau_{SRH,LLI} = \tau_{p0} + \frac{\tau_{n0}(p_1 + \Delta n)}{N_D} \qquad \tau_{SRH,HLI} = \tau_{n0} + \tau_{p0} \tag{2.37}$$

P-type Si

$$\tau_{SRH,LLI} = \tau_{n0} + \frac{\tau_{p0}(n_1 + \Delta n)}{N_A} \qquad \tau_{SRH,HLI} = \tau_{n0} + \tau_{p0} \tag{2.38}$$

From above equations 2.37 and 2.38, it is concluded that SRH lifetime at LLI can be approximately constant (first term in equation) or increase with injection level (second term of equation) depending on capture cross section ratio and energy levels of defects state.

It is also concluded that defects close to middle of band gap, which are also known as recombination centers, are most effective recombination sites. For this kind of defects (deep defects) n_1 and p_1 become very small and second term in LLI equations drops out. The mid-gap traps are considered to be most damaging traps that can greatly enhance the overall recombination in the solar cell.

For N-type Si $\tau_{SRH,LLI} = \tau_{p0}$ for mid gap trap (2.39)

For P-type Si $\tau_{SRH,LLI} = \tau_{n0}$ for mid gap trap (2.40)

For high level injection, Equation remains unchanged which means that SRH recombination lifetime also increases with injection level for deep defects.

2.4 Surface recombination

Surface recombination is a phenomenon, where excited electrons in conduction band recombine with holes in the valence band via defects level at the surface of wafer, in silicon solar cell. Surface of silicon wafer represents a severe disruption of crystal lattice, which promotes the recombination and sites for high recombination. This surface recombination can be treated as an extension of SRH recombination, with two dimension surface. Mechanism is shown in figure 2.24.

Surface recombination rate is limited by the rate at which minority carriers moves toward the surface. Another parameter which is called surface recombination velocity (SRV) is introduced to explain the phenomenon of surface recombination. Surface with no recombination, movement of carriers toward the surface is zero, so SRV is zero. Surface with fast recombination, movement of carriers toward the surface is limited by the maximum velocity which they can attain, is$1 \times 10^7 cm/sec$. [23].

Figure 2.24 Energy band diagram representing SRH recombination through surface defects in the band gap

There are two quantities, which are used to qualify the surface recombination activity.

1. Surface recombination rate (U_S in cm^2/sec) a recombination rate of the carriers per unit area per unit time.
2. Surface recombination velocity (*S* or SRV in cm/s) a velocity of carries by which they travel toward the surface.

These two quantities which are related to surface recombination rate can be express as follow:

$$S = \frac{U_S}{\Delta n} \tag{2.41}$$

Whereas Δn is the excess carrier concentration at the surface. For single surface state equation 2.27 can by modified as in term of surface recombination rate U_S, as

$$U_S = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2.42}$$

Where n_S and p_S are surface carriers concentrations, Sn^0 *and* Sp^0 are the characteristic surface recombination velocities for electrons and holes, which are related to the surface state density $N_{ST,}$ are given by

$$S_{n0} = \sigma_n N_{ST} v_{th} \tag{2.43}$$
$$S_{p0} = \sigma_p N_{ST} v_{th}$$

N_{ST} is density of surface states and v_{th} is thermal velocity, so from definition of surface recombination velocity (equation 2.41) SRH recombination velocity can be written as:

$$S = \frac{n_0 p_0 - \Delta n_S}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2.44}$$

In reality surface states are not localized in a single energy level but these are distributed across the band gap of a semiconductor. Total surface recombination rate is calculated by integrating over the entire band gap:

$$U_S = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{n_s + n_1(E)}{\sigma_p(E)} + \frac{p_s + p_1(E)}{\sigma_n(E)}} v_t D_{it}(E) dE \qquad (2.45)$$

Where D_{it} is surface trap density per unit energy cm-2/eV (1/eV.cm^2). *Ec* is conduction band and *Ev* is valence band. Equations 2.44 and 2.45 shows that for recombination at the surface require the presence carriers (electrons and holes) and defects states which mediate the recombination process. Reduction in carriers, electrons/hole or defects states reduces the surface recombination. Experimentally it is achieved by passivation which maybe field effect passivation or interface passivation (also called chemical passivation).

2.4.1 Minimization of Recombination

Recombination process of generated carriers (electron and hole) is possible at the surface, in the depletion region and in the bulk region of solar cell. In order to get high photocurrent and conversion efficiency, it is necessary to minimize the recombination problems and it is achieved by passivation.

2.4.2 Surface passivation techniques

High number of defects at the surface of semiconductor makes surface recombination dominant mechanism in silicon and other semiconductors. Reduction of surface recombination is called passivation. Passivation techniques maintain the minority carriers' density high to achieve high efficiency solar cells. Passivation can be achieved by two ways.

a) By deposition of dielectric film (interface passivation)
b) By creating surface electric field (BSF)

Deposition of dielectric film, at the surface of crystalline silicon to eliminate dangling bonds is called interface passivation. Chemical deposition of dielectric film such as silicon dioxide or silicon nitride can be used for passivation. Silicon nitride not only passivates the surface but also acts as an antireflection layer. The best passivation is reported until now is that of plasma enhanced chemical vapor deposition (PECVP), tripe layer stack of amorphous silicon, silicon dioxide and silicon nitride (a-Si/SiO_2/Si_3N_4) [24]. By using additional field effect passivation provided by corona charge, Herasimenka *et al.* [24] has reported effective surface recombination velocities (S_{eff}) below 1cm/sec on 1.7Ω.cm on n-type silicon. Similar results have been reported with addition of annealing step [25] and by atomic layer deposition (ALD) of aluminum oxide (Al_2O_3) [26]. These films have reached S_{eff} as low as 2.4cm/sec and 1.2 cm/sec on similar type of material. The values of S_{eff} 20-30cm/s have been commonly observed at industrial level [27].

And second is by creating a surface electric field that (field effect passivation) that repels one type of carriers electrons or holes back and therefore limits the amount of recombination and possible at the interface due to field effect. Field effect can set up either by charging the dielectric film or by doping the surface. Field effect passivation on rear surface of p-type

silicon solar cell is achieved by deposition of p+ doped surface layer which is called back surface field (BSF).

2.4.3 Front surface passivation

As I have mentioned early, unwanted recombination of the photo generated carriers is the major limiting factor in conversion efficiency of solar cell. In crystalline silicon material surface represents discontinuity of the crystal arrangement due dangling bonds. These dangling bonds act as good recombination centers for carriers. In band gap figure (figure 2.24) these dangling bonds give rise to energy state in middle of band gap which acts as recombination centers. In order to avoid this recombination, surface must be passivated. At front surface it is achieved by deposition of an electric layer to passivate the dangling bonds which remove energy states from middle of band gap. SiO_2 and Si_3N_4 or combination of both layers is usually used for front passivation. Both layers have high band gap which prevent carriers to reach them at the surface.

2.4.4 Back surface passivation

Back surface is usually achieved by field effect passivation. In this method high level of doping in low doped semiconductor of similar impurities (for example Al in p-type silicon and P in n-type silicon) is used. It is typically done on rear side (back surface) of silicon solar cell. A layer of heavy doped is deposited on back surface (p+ represents doping concentration above $10^{18}cm^{-3}$ or higher) to obtain pp+ junction. It gives rise an electric field at the junction in the direction from p to p+ side. This junction creates a potential barrier to the minority electrons. The electric field repels electrons back toward PN junction and reduces the recombination at back surface. This is known as back surface field (BSF) or back surface layer. See the figure 2.25.

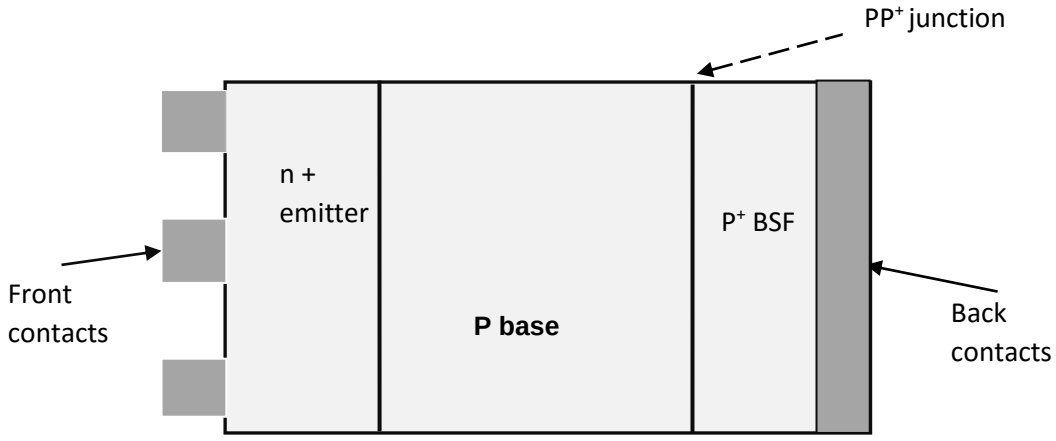

Figure 2.25 n+ p p+ back surface field junction solar cell

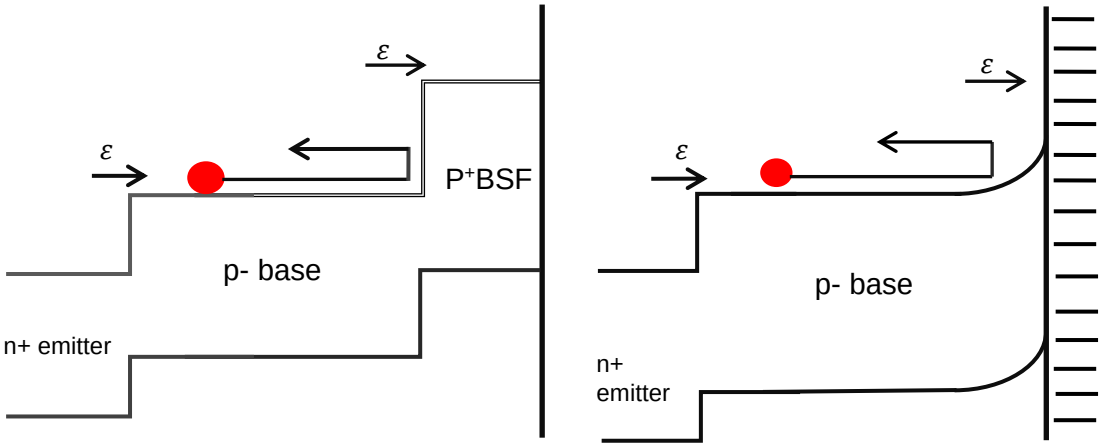

Figure 2.26; Band diagrams representing electric field and band bending caused by a) p+ BSF layer b) a negatively charged dielectric layer with its effect on electron flow

Field effect passivation in case of p base solar cell is achieved with p+ doping surface layer (BSF) or negatively charged dielectric layer as shown in figure 2.26. Both doped layer and negatively charge dielectric layer result in stronger surface electric field and steeper band-bending which enhance field effect passivation. [28].

In high efficiency solar cell, used both passivated methods. E.g. in PERL (passivated emitter rear locally contacted) solar cell with efficiency 25%, solar cell structure which has both high quality rear Passivation and localized B- BSF region under rear point contacts. [29].

Effectiveness of the surface recombination is given in term of surface recombination velocity (SRV or S). It is defined as the rate of recombination at the surface divided by the excess of carrier concentration at the surface.

$$S_{eff} = \frac{U_S}{\Delta n} = \frac{J_{rec}}{q\Delta n} \tag{2.46}$$

For p-type cell, it simplified to

$$S_{eff} = \frac{J_{OE}(N_A + \Delta n)}{qn_i^2}$$

It is common to measure effective recombination velocity which include combined effect of all processes such SRH recombination, Auger recombination in non-uniform emitter (band gap narrowing which increases n_i with in emitters and recombination at emitter surface. The lower is the surface recombination velocity (SRV), better is the surface passivation and vice versa. 10cm/s SRV value is considered to a well passivated surface while value of SRV higher than 10^4 cm/s represented a poor passivated surface.

2.4.5 Bulk passivation

In general multicrystalline silicon and other materials which have low degree of crystallization can contain crystallographic defects, grain boundaries, metallic impurities etc. These defects effect on minority carrier lifetime of the bulk material and degrade solar cell performance. The defects provide recombination centers and decrease to lifetime. To overcome the recombination problems in the bulk, special treatment have been developed either by passivation of bulk crystallographic defects using hydrogen (Hydrogenation) and by gettering process which is used to remove metallic impurities from bulk.

2.4.6 Bulk passivation: The Gettering

Commercial solar cells fabrications on low cost substrates have high concentration of metallic impurities (iron, nick and copper particles) and defects. Silicon technology has harmful effect of metallic impurities on the performance of solar cell. Multicrystalline silicon wafers have high concentration of metallic impurities even it is difficult to avoid in case of single crystalline silicon wafers. These impurities create leakage current in pn junctions. In order to avoid the harmful effects of metallic impurities, gettering technique is used. Gettering is a technique used to eliminate or reduced impurities by relocating and blocking them from active region/bulk of the device. As silicon solar cell comprised the whole wafer thickness, it is important to clear the bulk of solar cell from impurities. In commercial solar cells fabrication, gettering of impurities is obtained by aluminum and phosphorus diffusion. Aluminum is used to create back surface field (BSF) and back contacts. Aluminum not only used to create a BSF and back contacts but also passivate defects in the back. SiAl alloy works very well for gettering of metallic impurities. [30]. In case of p-type solar cells fabrication process which is dominant type of solar cell, the emitter formation by P diffusion, simultaneously getters iron from bulk from p-type silicon to diffuse into phosphorus layer. SiP particles in emitters region acts as gettering sites, [31].

2.4.7 Bulk passivation: Hydrogenation

Hydrogenation has gain attention in low cost solar cell fabrication process by using amorphous silicon. Incorporation of hydrogen strongly improves the properties of amorphous silicon (*a-Si: H*). [32]. Hydrogenation of amorphous a-Si saturate silicon dangling bonds and makes it a semiconductor suitable for solar cell and device fabrication. Dangling band otherwise form band gap defects of a-Si and acts as recombination centers [33-35]. A similar beneficial effect has also noted for grain boundary passivation by hydrogenation in polycrystalline silicon.

2.5 Optical losses in solar cell

Optical losses mainly affect on power loss by decreasing the short circuit current. (I_{SC}).Optical loss is the amount of light which is reflected back or not absorbed in solar cell to generate electron hole pairs. For silicon solar cell, visible spectrum (350-800nm) has enough energy to generate electron hole pair.

Major optical losses in typical silicon solar cell are summarized in figure 2.27, which are given below:

1. Reflection at front surface
2. Parasitic absorption in ARC layer
3. Parasitic absorption in emitter

4. Parasitic absorption in BSF layer and rear contacts
5. Reflection or escape from cell interior

From figure 2.27, it is clear that light absorbed in ARC layer, emitter and BSF layers did not contribute any current or energy. Only light absorbed in p-base region contribute current and power generation.

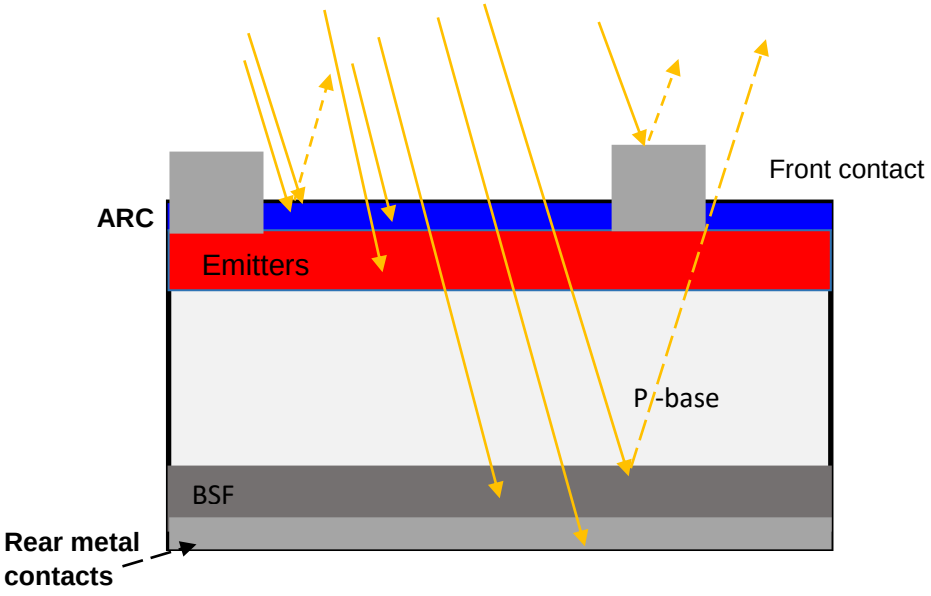

Figure 2.27: Schematic representation of optical losses in silicon solar cell (Arrows represent light rays)

At the front surface, there are metal contacts, which decrease the surface area for light absorption. There are number of ways to decrease optical losses in silicon solar cell.

- Front contact surface coverage can be minimized in order to increase surface area for light absorption (although it can increase series resistance but it can be optimized).
- Anti-reflection coating can be used on front surface of cell (to decrease reflection).
- Reflection can be minimized by surface texturing.
- Thickness of solar cell can be increase to absorb maximum amount of light. (Although light absorption more than diffusion length from junction will have low collection probability, it will not contribute to short circuit current. It will also increase cost of solar cell).
- Optical path length can be increase by the combination of texturing and light trapping.

2.5.1 Front surface Reflection

One of main source of optical loss is front surface reflection. Etched silicon wafers have higher surface reflection than 30%. Reduction of surface reflection is very important, Antireflection effect achieved by using two different ways.

- Anti-reflection coatings

- Surface texturing

2.5.2 Antireflection coatings

A reduction in reflection can be achieved by optical quarter wavelength principle. Penetrating beam of light is reflected at barrier layer between silicon and antireflection layer as shown in figure 2.28.

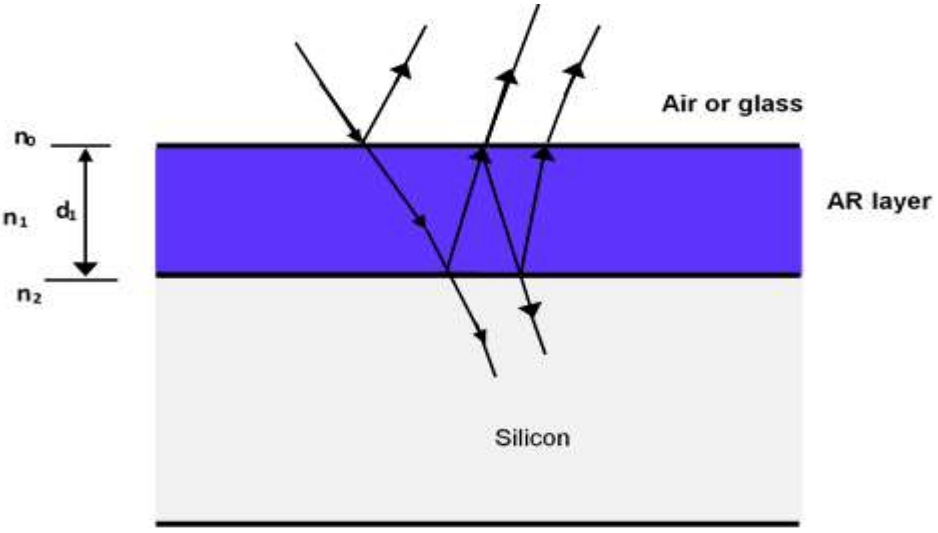

Figure 2.28 Antireflection behavior of thin layer

For planar silicon wafer in air, reflectance at surface for incident light is given by Fresnel equation [4, 36].

$$R = \frac{(n_2 - n_1)^2 + k^2}{(n_2 + n_1)^2 + k^2} \tag{2.47}$$

Where $n1$ and $n2$ are reflective indices of air and silicon and k is extinction coefficient for silicon. Bare silicon has high reflective index ($n \geq 3.5$) over wavelength range of interest typically ranging from 300-1200nm. Reflectance of bare silicon is higher than 30% as shown in graph (figure 2.29). This high reflection can be reduced by using antireflection coatings (ARC).

For bare silicon wafer in air, coating with single layer of antireflection coatings (ARC) having extinction coefficient (k=0).

$$R = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos 2\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos 2\theta} \tag{2.48}$$

With $r_1 = \frac{n_0 - n_1}{n_0 + n_1}$

$r_2 = \frac{n_1 - n_2}{n_1 + n_2}$

$\theta = \frac{2\pi n_1 d_1}{\lambda}$

Where n_0 is reflective index of upper layer (air or glass)

n_1 is reflective index of ARC layer
n_2 is reflective index of bare silicon
d1 is thickness of ARC layer, λ is wavelength θ is phase difference of reflected rays.

If the thickness of ARC is known, product of reflective index and thickness is equal to quarter of the wavelength. At the interface of substrate and ARC, interface is destructively in that way reducing the reflection (destructive interference). It is written as [4, 36].

$$n_1 d_1 = \frac{\lambda}{4} \tag{2.49}$$

Minimum reflection R is calculated as:

$$R_{mini} = \left[\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2}\right]^2$$

For given wavelength, reflectance becomes zero if the ARC meets this condition.

$$n_1^2 = n_0 n_2 \tag{2.50}$$

ARCs that fellow this condition is also called quarter wave coatings. In general, silicon solar cells have minimum reflectance at λ=600nm as shown in the figure 2.29 Silicon nitride (Si_3N_4) n ≅ 2 and silicon dioxide SiO_2 n=1.46 at λ=600nm are most common ARC dielectric which passivate the silicon surface. Si_3N_4 reduce surface reflection averagely from 35 % 10-15%.

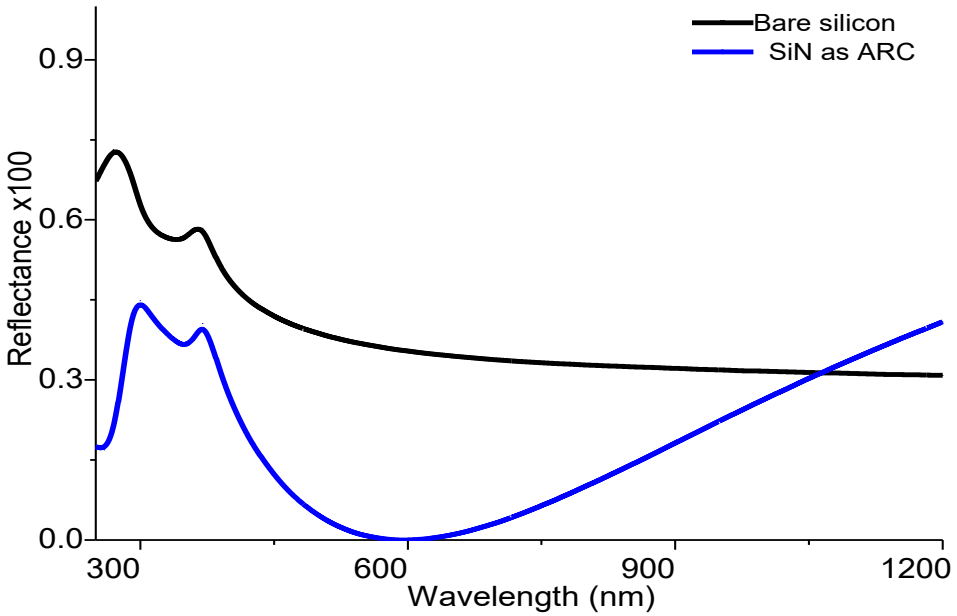

Figure 2.29 Reflection of bare silicon and silicon with antireflection coatings

There are many candidates for ARC, such as ZnO, SiOxNy, ITO (indium tin oxide, silicon nanowire, perovskite [1]. The function of ARC is to reduce the reflection of incoming light, passivate the surface and provide insulation allowing selective plating of top contacts. Si_3N_4 is considered the best layer due to its unique above three functions.

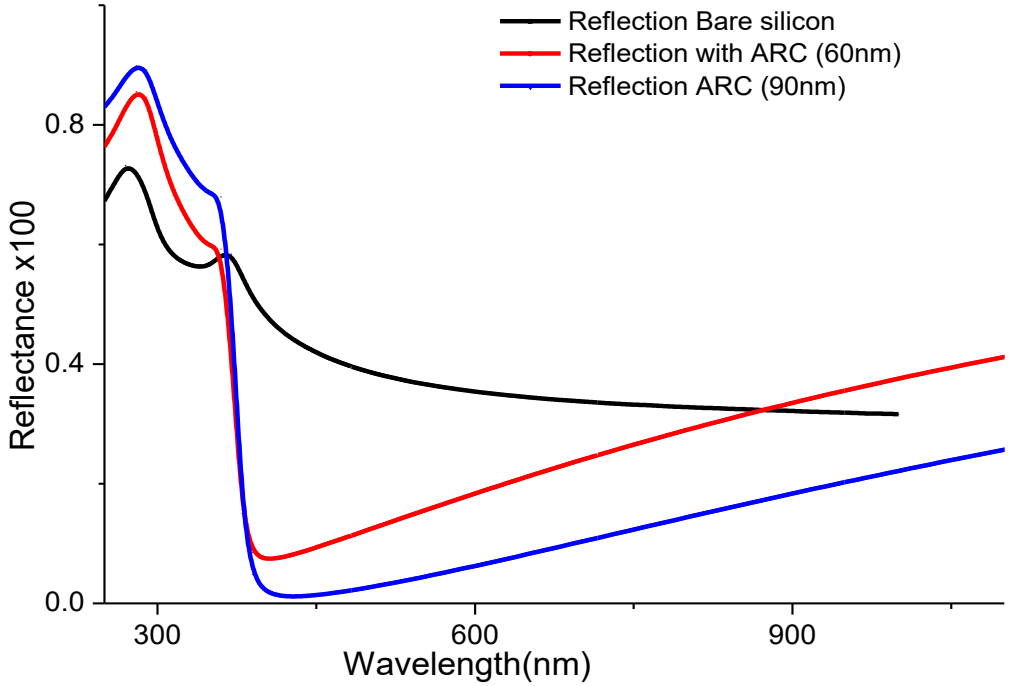

Figure 2.30 Surface reflectance with various ARC thicknesses

2.5.3 Surface texturing

Surface texturing either in combination with antireflection coating or itself can be used to reduce surface reflection. Any roughness (grooves or pyramids) on the surface minimizes the reflection by the increasing the chance of reflected light to bounce back to the surface rather than reflected to surroundings. Random pyramid texturing is common methods for surface texturing of crystalline silicon solar cells. These pyramids act as light traps on silicon solar cell. When light impinges on textured surface, reflection occurs at different angles those are deflected into new points on surface. Multiple interactions occur at silicon surface, thus reducing amount of light lost through reflection.

Through surface texturing, average reflectance of light can be reduced down to the 12%. Using both ARC (Si_3N_4 n =2.03 at 600nm wavelength) with pyramid texturing surface, the reflectance can be reduced less than 4%. Texture surface also provides a reduction in path length to the junction which is pronounced for longer wavelength. Thereby increase the longer wavelength collection efficiency. In practice, the best results have been achieved with inverted pyramids [37-38].

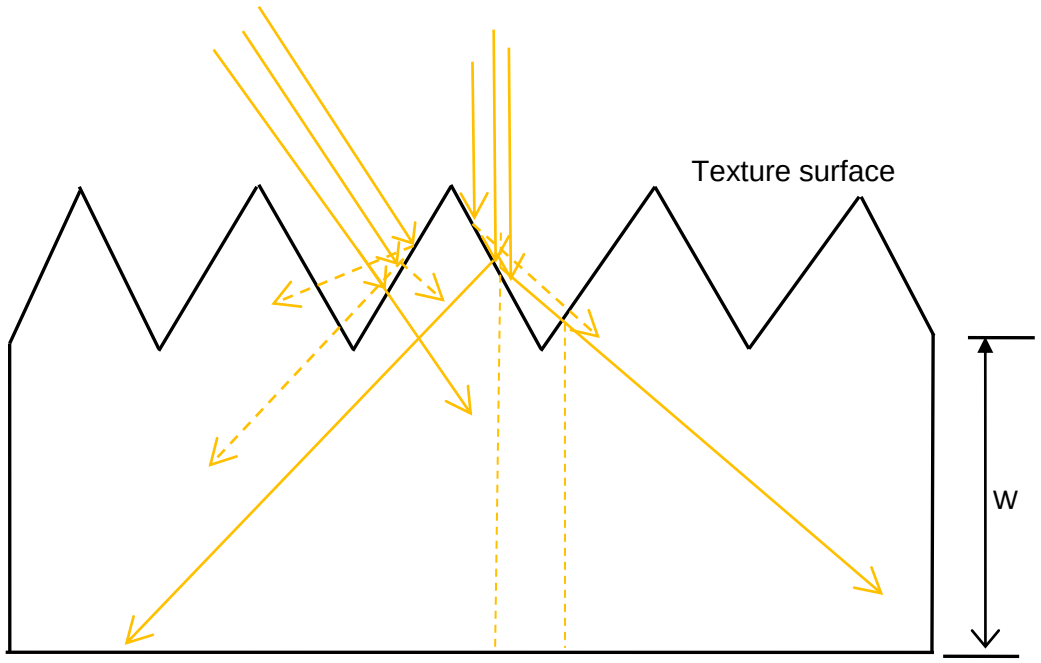

Figure2.31 Radiation (rays) path for a texture silicon wafer

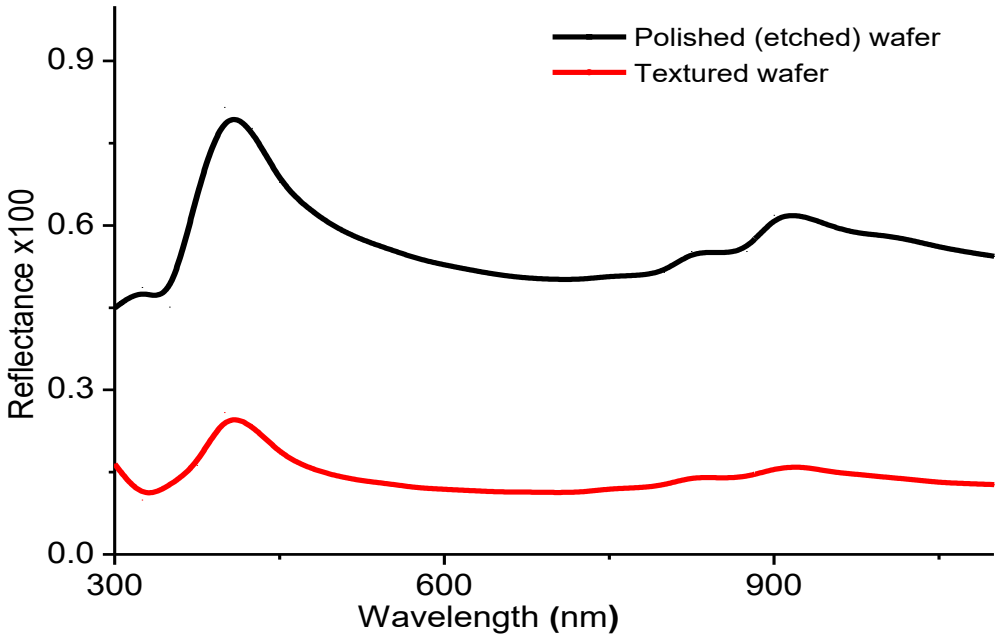

Figure 2.32 Reflection of polish wafer and texture wafer

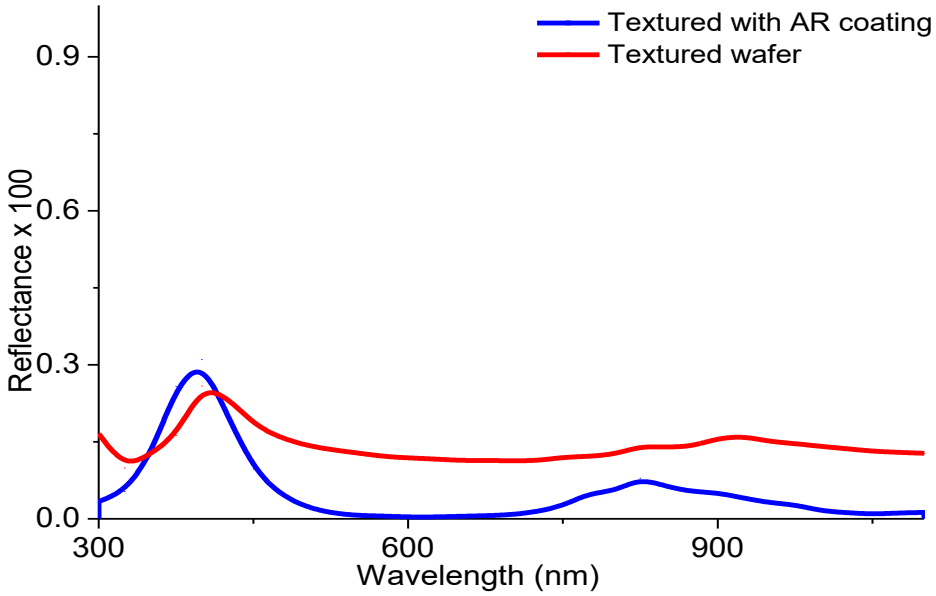

Figure2.33. Reflection of texture surface and texture with ARC

2.5.4 Parasitic absorption in ARC

Absorption of light passing through a solid material (silicon) is described by beer lambert law.

$$I(x) = I_0 e^{-\alpha x} \quad (2.51)$$

While

$$\alpha = \frac{4\pi k}{\lambda} \quad (2.52)$$

Whereas, I_0 is intensity of incident light, $I(x)$ is intensity of light absorbed by material and α is absorption coefficient, (Absorption coefficient determines how much light of certain wavelength is penetrated into material), it is function of imaginary part of complex reflective index or extinction coefficient k of a material.

In case of SiO_2 and Si_3N_4, as antireflection coating materials for solar cell, It has negligible value of absorption coefficient (α) and values of their extinction coefficient is almost zero over the 300-1200 wavelength range [36].There are some other materials, can be used as ARCs materials for solar cells such as ZnO, SiOxNy, ITO and SiCN, which show appreciable absorption. Name and chemical formulas of these materials are given in table 2.1 [39-42].

Table 2.1 Material used as antireflection layers

Chemical formula	Name of material	Reflective index
SiO_2	silicon dioxide	1.46
Si_3N_4	silicon nitride	2.0
ZnS	zinc sulfide	2.4
MgF_2	magnesium fluoride	1.4
Al_2O_3	aluminum oxide	1.6
TiO_2	titanium dioxide	2.5

Ta_2O_5	tantalum pentoxide	2.2

2.5.5 Free carriers absorption (FCA)

It is an intraband (within band) process, carriers are excited to higher energy state within the same band, valence band or conduction band. But this absorption does not generate additional electron hole pair. This process does not contribute photocurrent and extra energy is lost as heat. FCA process is important in heavily doped region such as emitters and it is observed as an enhanced the absorption of long wavelength as compare to lightly doped emitter or intrinsic silicon. FCA is an undesirable process; PC1D simulations show that FCA in emitters has much smaller impact on current loss than Auger and BGN (band gap narrowing) in emitters [43-44].

2.5.6 Rear Reflectance/Absorption

Absorption of photon from incident ray of sunlight depends on the absorption coefficient, which is high for shorter wavelength and low for longer wavelength. From equation 2.52, it shows that absorption coefficient of silicon is function of wavelength, as shown in figure 2.34. Red and infrared light penetrate deeper into silicon material and a huge portion of light is scattered or absorbed at rear side contact. In practice BSR has reflection less than 100%, which mean some amount of radiation is absorbed in this region. Depostions of Aluminum or silver on back side of solar cell minimize absorption and have reflectance greater than 90%. In high efficiency PERL solar cell, Al layer deposited on backside of solar cell as BSR and as rear contact [29]. In commercial solar cell, screen printed paste is used as BSR, which may have higher parasitic absorption. Figure 2.35 represents that light in range of 850-1200nm have nearly 25% of optical energy in AM1.5 spectrum.

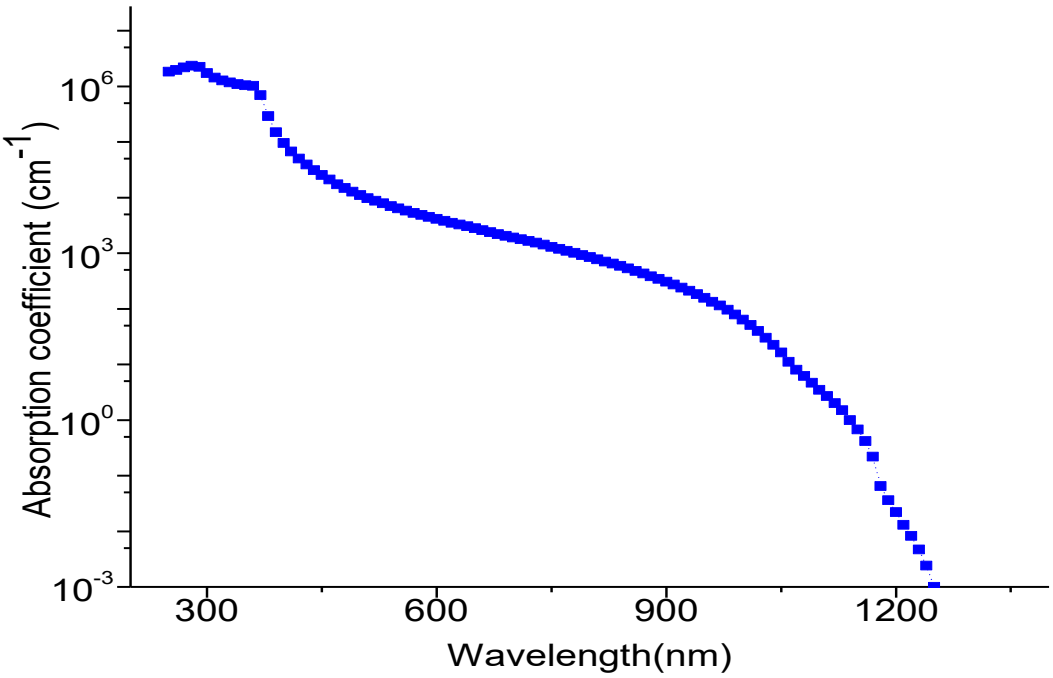

Figure 2.34 Absorption coefficients for silicon [45].

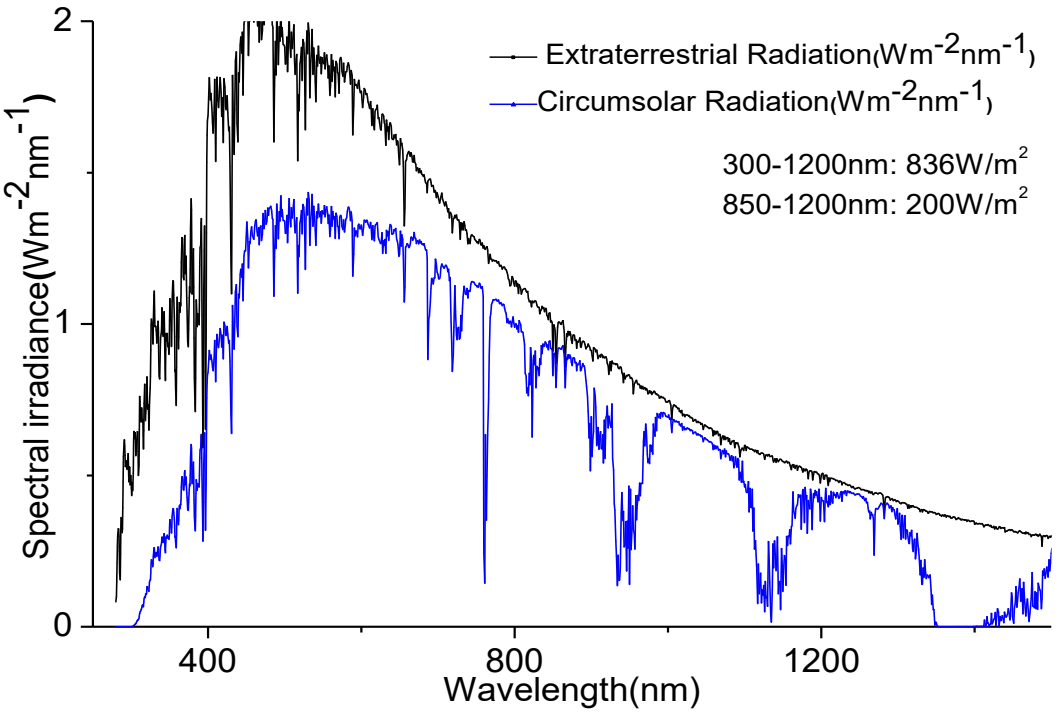

Figure 2.35 AM1.5G (IEC 60904-3) spectrums [46].

The weak absorption of silicon, wavelength closer or beyond to optical band-edge of silicon at 1100nm, which means that silicon solar cell need to be fairly thick for complete absorption in single pass. Sun light in range from 800-1200nm nearly hold 25% of optical energy in AM1.5 spectrum. If the rear surface of solar cells has a back surface reflector (BSR) with 100% reflectance, the same amount of absorption can be achieved by with thin wafer. This BSR will reflect the long wavelength light back for second pass through the cell, as shown in figure 2.36. In practice BSRs have reflectance less than 100% due to parasitic absorption. In high efficiency solar cell, parasitic absorption is minimized by back surface reflector (BSR), by evaporating pure metals such as silver and aluminum which have reflectance ≥ 95% at long wavelength. [47-48]. Low cost screen printed Al- paste solar cell can have higher parasite absorption low BSR. As we know that reflectivity of aluminum as back reflector is > 95% and less than 80% for oblique incidence, while reflectivity of distributed bragg reflector (DBR) is higher than 99% over a wide range of wavelength (figure 2.36(b)). The main limitation for back reflector is that it can enhance optical path length to twice of the solar cell thickness. [49].

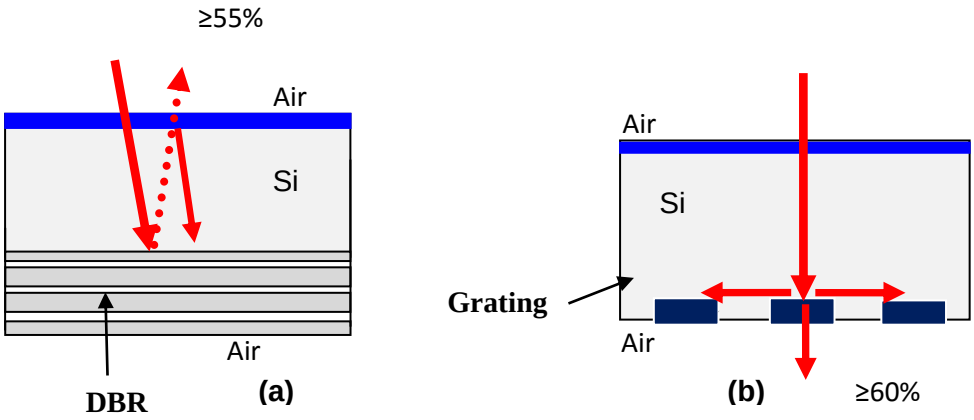

Figure 2.36 Transmission losses (a) when DBR is used alone (b) when grating is used alone

To overcome this limitation, diffraction grating is used on back surface to diffract the light inside the solar cell to certain angles based on different diffraction order. When DBR is coupled with diffraction grating (DG), they are complement to each other, light lost is negligible as shown in figure 2.37 [49].

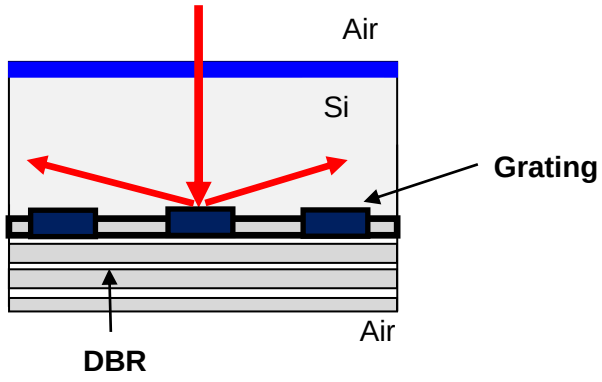

Figure 2.37 Integration of DBR and Grating for maximum reduction of transmission losses on front and backside of silicon solar cell

DBR consists of pairs of Si and SiO_2 layers in 8 stacks, deposited by using PECVD. The DBR is deposited at temperature less than 450 ^{0}C but even it is stable at high temperature, having thermal history at 1000 ^{0}C for 3 hours. Diffraction grading can be fabricated by using interference lithography and directional etching using plasma ion etching (RIE). It is expensive laboratory technique, far away from industrial point of view [50].

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Chapter 3

3Fabrication of P/Al solar cells

Silicon solar cells of P/Al high efficiency technology arrived in IES (Institute of solar energy Madrid) in late of 1980. At that time A. Cuevas and M. Balbuena presented an investigation on high efficiency solar cell working under one sun of irradiance. They have concluded that it is possible to obtain high efficiency with lightly doped deep phosphorus emitters and aluminum as back surface field, P/Al (P-emitters/Al-BSF). They have obtained efficiency around 19% by using high quality FZ (float zone) monocrystalline silicon wafers [1]. In fact when the process was described in mid of 1980´s, efficiency achieved was remarkable and among the best silicon solar cell efficiency reported at that time.

In this P/Al technology, phosphorus emitters are relatively deep about 2 microns (2 µm) and moderately doped surface concentration of dopant impurities is near to 1E19/cm^3 ($10^{19}\,cm^{-3}$), which corresponds to a sheet resistance of 100 ohm/square. While on backside of wafer, 1μm thick layer of aluminum is deposited which diffused into silicon at high temperature and create a BSF (back surface field). The resulting structure of the P/Al technology is n^+pp^+ in which the emitters which are produced by phosphorus diffusion, creates n^+ on front side of wafer while on back side aluminum is diffused to produce p^+. The typical structure of P/Al technology which produces a n^+pp^+ structure is shown in figure 3.1

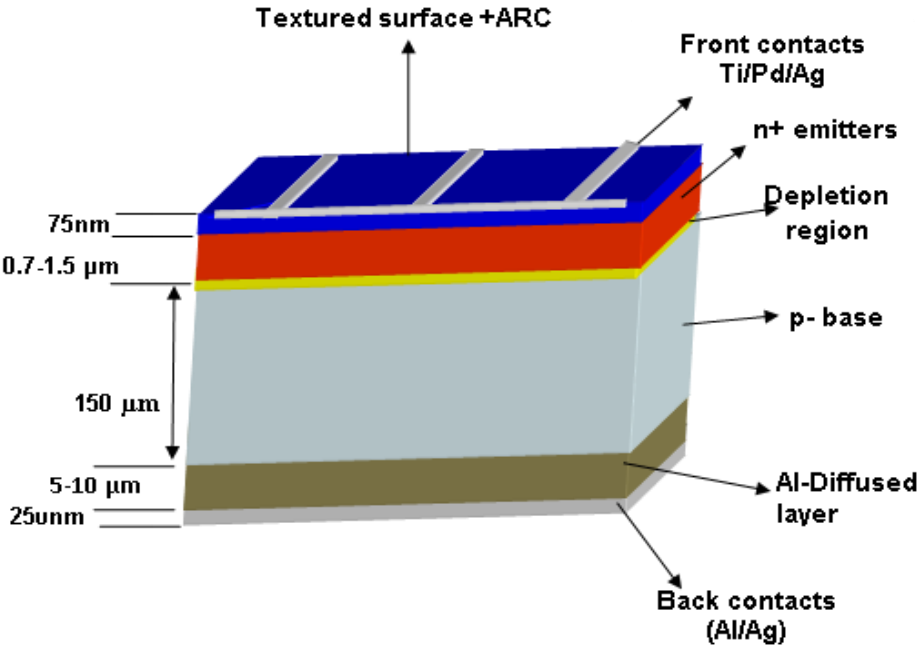

Figure 3.1 Standard Structure of P/Al (n+pp+) solar cell

Fabrication scheme of P/Al technology, which is also called standard fabrication scheme for $\boldsymbol{n^+pp^+}$ silicon solar cells, is described in figure 3.2. Fabrication process is started from

chemical etching of P-type monocrystalline silicon wafers obtained by Czochralski growth (Cz), a low quality wafers than float-zone wafers. Description of wafers are given below:

Monocrystalline silicon wafers (Cz)
Resistivity: 0.5-2 ohm.cm
Thickness: 200±10 µm
Dopant: B
Conductivity: P type
Size: 125mm

New wafers of above mentioned characteristics have been taken for fabrication process. Process is started from chemical etching process. Wafers used for process were about 150 ± 5 µm thick.

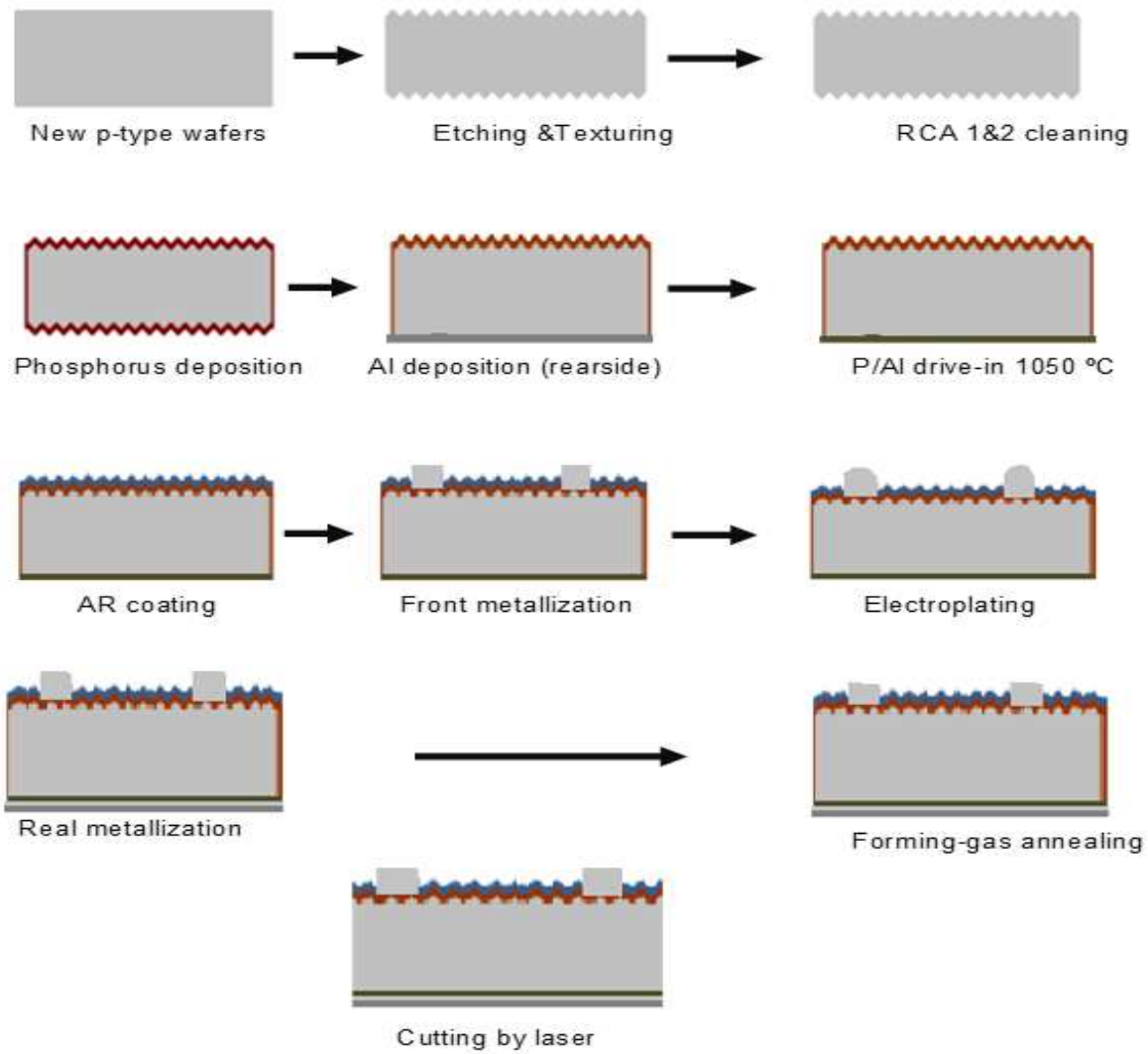

Figure 3.2 Standard fabrication process of P/Al technology for (n+pp+) silicon solar cell

Wet chemical etching process for thinning of wafers is quick, instrument free, cost effective process and widely used in industrial fabrication of silicon solar cell. The wet chemical etching process for any material usually consist of three steps: transport of reactant

to surface of wafer, reaction at the surface of wafer and movement of reaction products into the volume of etchant solution. An etch process which is limited by rate of surface reaction will tend to enhance surface roughness and promote faceting. Since surface reactivity is function of localized defects and crystallographic orientation. On the hand etching can be limited by rate of diffusion of etchant through a stagnant layer at the surface. This changes polished wafer into rough surface with protuberances and facets will tend to become smooth in this process. Although etch characteristics of silicon with wet etchants are well documents, but the best results for various micromachining structure are obtained by trial and error methods. [2-5]. Silicon ingot which is obtained by Czochralski (CZ) crystal growth process can by pulled in a defined orientation (100). There is one big economic advantage of this process is that during solar cell process, we can use this crystallographic plane for homogeneous texturing with cost effective wet chemical etching process. During anisotropic etching, the surface structure with random pyramids is built that enhance the absorption of incoming light effectively into solar cell. Etching rate Si (100) depends on NaOH concentration, temperature and etching time. Maximum etching rate was observed in our case is about 3.5 µm/min at 90 ^{0}C at 25% NaOH concentration. Etch rate increased with increasing temperature. According to literature maximum etching rate was observed near the boiling point of solution is 4.5µm/min for Si (100) orientation at 100 ^{0}C.

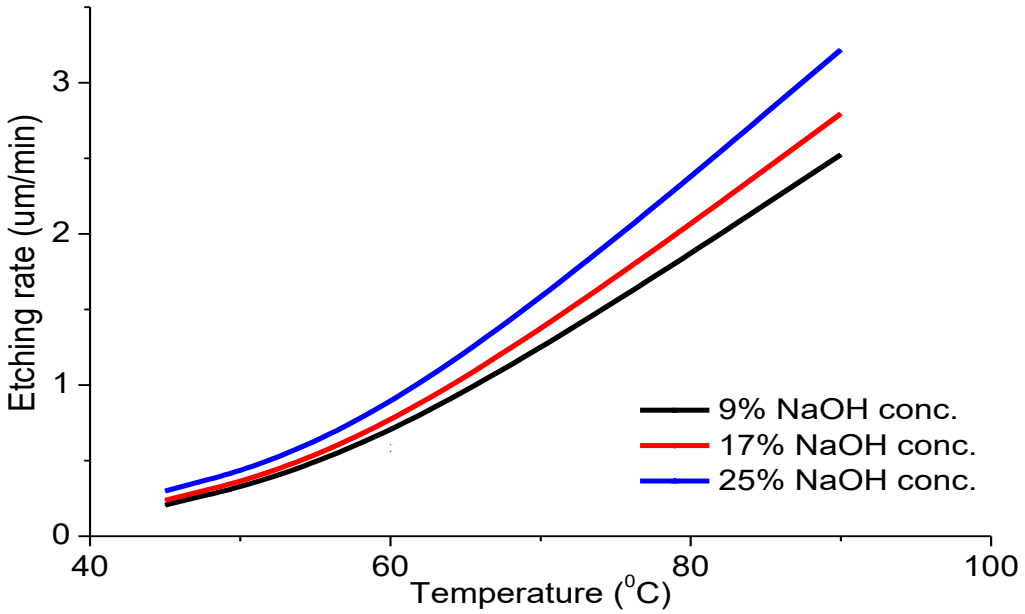

Figure 3.3 Silicon (100) etch rate in NaOH solution

After etching process, wafers were characterized by measuring the reflectance of etched wafer as well as under microscope. Etched wafers behaves like a mirror, reflected most of incident light. Reflectance of etched wafer is shown in figure 3.4.

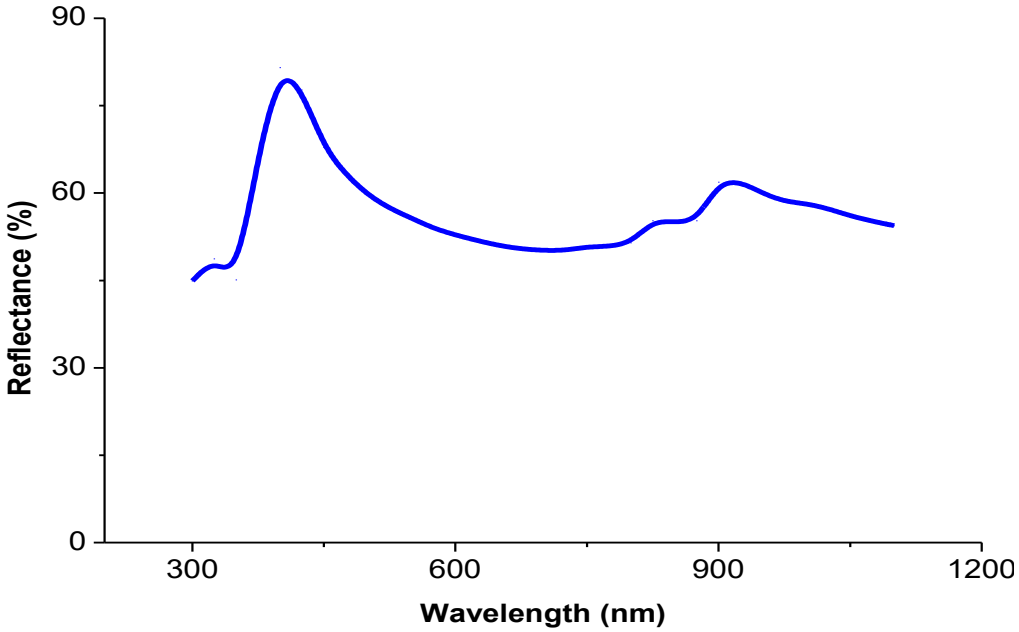

Figure 3.4 Reflectance of etch wafer (Alkaline etching)

Images of etched wafers which are taken under microscope is shown in figure 3.5.

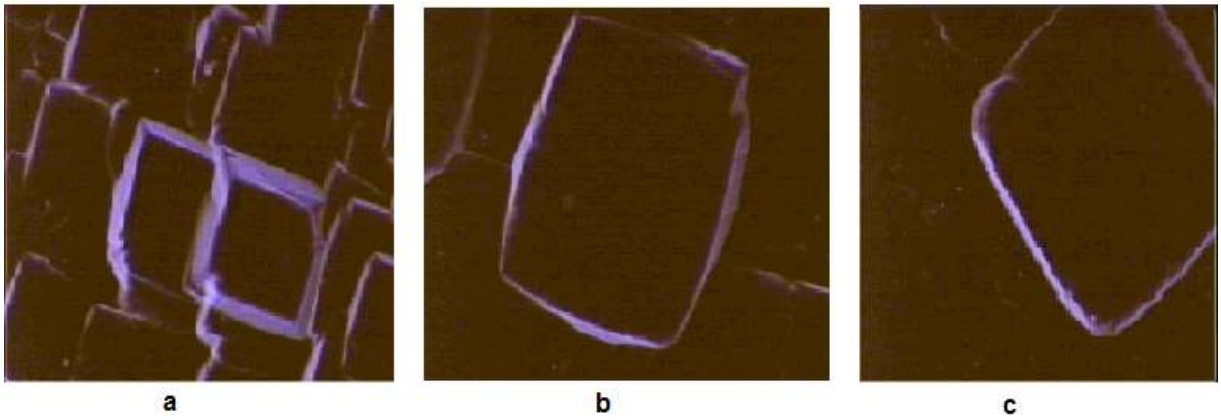

Figure 3.5 Microscopic images of anisotropically etched wafer of silicon by NaOH under different resolution (a, b and C).

3.1 Texturization of Silicon wafers

Silicon texturization of (100) oriented silicon substrate is an important step to reduce of optical losses of monocrystalline silicon solar cell. During texturization, pyramids are created on silicon surface either by chemical methods or by physical methods. Monocrystalline silicon wafers can be textured by etching along with faces of crystal planes which results in pyramids formation, if the surface is appropriately aligned with respect to internal atom. This type of texturing is also random pyramids texturing [6-15]. Any roughness on the surface of wafers reduces the reflection by increasing the chances of reflected light to bounce again onto the surface rather than reflected back.

In industry, texturization with a subsequent deposition of antireflection coating (ARC) is well established method to reduce the optical losses.

Texturization is a slow etching process which leads to microscopic pyramids formation on silicon surface. Their size must be optimized, small size pyramids lead to high reflection, while optimized size decrease the reflection. In order to make sure the complete coverage of wafer with adequate size of pyramids, concentration, temperature and agitation of solution must be controlled. In fact high concentration and temperature etching leads to anisotropic etching, which is used for saw damage removal. Normally texturing is carried out at low concentration with continuous agitation, Alcohol is also added in this process to improve homogeneity of texturing bath which enhance the wettability of wafer surface. Typical parameters which vary from one laboratory to other laboratory are concentration 1-5% NaOH solution, temperature 70-90 ºC and time 10-30 minutes.

3.1.1 Texturing Recipe (TIM recipe)

In our experiments, we have used a texturing recipe formulated by our institute for the texturing of silicon wafers. [16]. This recipe is considered as an economical recipe due to less consumption of NaOH and 2-propanol and it can easily apply for large scale industrial texturing for solar cell fabrication. This recipe consists of following chemicals and their weights are given below:

118.4grams of sodium hydroxide (NaOH)
265ml of 2-propanol ($C3H_8O$)
358ml of sodium (ortho) silicate ($Na2SiO_3$)
12 liters of deionized water

3.1.2 Characterization of Texture wafers

Anisotropic texturing of silicon wafers with alkaline solution is a standard process in silicon solar cell fabrication. Textured wafers are usually characterized by reflectance measurements and microscopic studies. Reflectance of textured wafers indicates the amount of absorbed light. Sometime reflectance of textured wafers is high due to randomly oriented grains etch rates is not same as for (100) wafers. Reflectance of etched wafer and texture wafer is shown in figure 3.6.

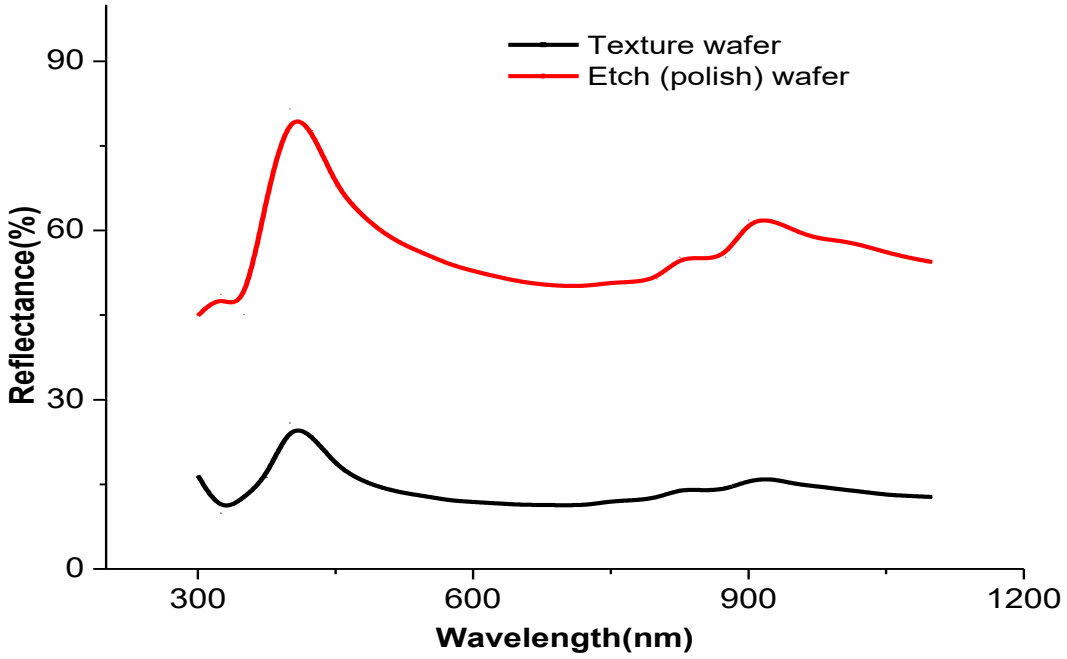

Figure 3.6. Reflectance of Etch (polish) wafer and texture wafer

Reflectance measurements which is shown in figure 3.8, shows that polish wafer has reflectivity near 40-50%, while texture wafer has reflectivity 10-15%. Even it is still high with respect to high efficiency solar cell. Microscopic and electron microscopic images are shown in figure 3.7.

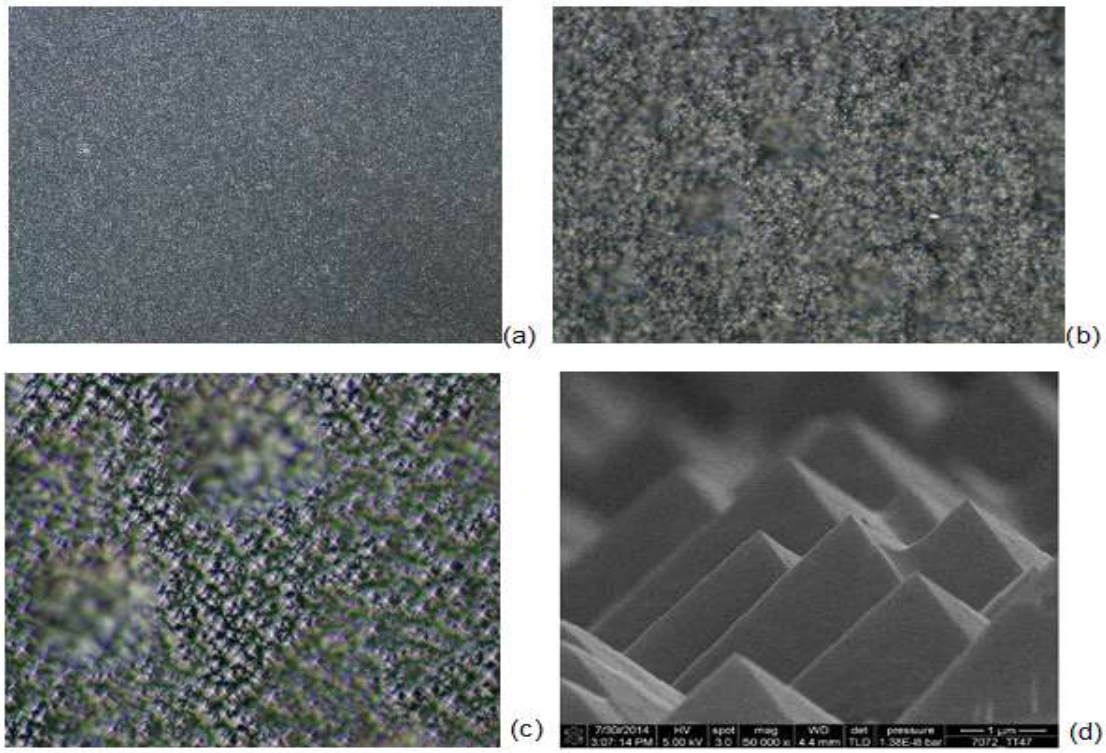

Figure 3.7 Microscopic image of texture wafers under different resolution (a, b and c), (d) image of texture wafer under SEM.

One of drawback is grains size of crystal, which can cause interruption in the screen printed metal contacts. Due to this reason alternatives are also being considered, during evaluation we should take into account not only reflectivity but also surface damage due to texturing and compatibility with metallization.

Reduction in reflection either by surface texturing or by other means is still a broad field of investigation and many research groups are investigating reduction in reflectance. Reflectance can be reduced by forming porous silicon layer on surface of silicon wafers which represented about 6% optical loss under optimum conditions [17]. But compatibility of porous silicon layer with screen printed contacts still need to optimize.

Recently developed, black silicon layer deposited by different techniques such as electrochemical HF etching or reactive ion etching, or laser irradiation process which also act as AR coatings, show the reduction in reflectance as low as 2%. However black silicon is not still suitable for PV cells due to high recombination rates due to its nanostructures [18]. Y. Wang et al has developed new methods to create maskless inverted pyramids for silicon texturization. In this method wafer scale arrays of silcon inverted pyramids were fabricated by using cupper nanoparticles (Cu-NPs) assisted anisotropic etching in a $Cu(NO_3)_2$ / HF/ H_2O_2/H_2O mixture at 50 ºC for 5-20 minutes. Reflectivity was lower than 4.4% without any AR coating [19]. Electron microscopic images of texture wafers are shown in figure 3.8.

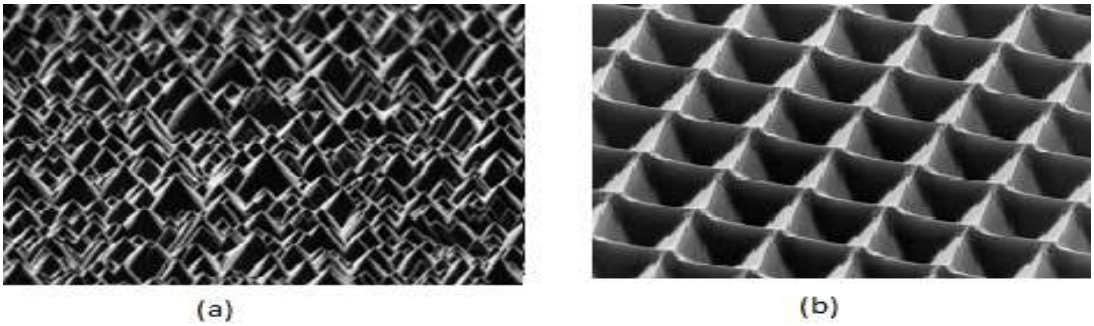

Figure 3.8 Electron microscopic images of (a) random pyramids and (b) inverted pyramids

3.2 Wafer cleanings (RCA1&2)

Contaminants which appears on the surface of silicon wafers during etching and texturing process must be remove. For high efficiency, surface of wafers must be clean and free from all of kind of impurities both organic and inorganics. For cleaning purpose, RCA1&2 process is carried out to get to ultraclean wafers. RCA cleaning play important role to get high performance and high reliability of semiconductor devices. This cleaning further prevent contamination of processing equipment, especially high temperature oxidation, diffusion, and deposition process. The RCA clean is the standard industrial process used to remove contaminants from wafer´s surface.

The RCAs cleaning process has three major functions sequentially:

- Organic Clean: Removal of insoluble organic contaminants with a 5:1:1 $H_2O:H_2O_2:NH_4OH$ mixture.
- Oxide Strip: Removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of step 1, by using a diluted 50:1 H_2O: HF solution.

- Ionic Clean: Removal of ionic and heavy metal atomic contaminants using a mixture of 6:1:1 H_2O:H_2O_2: HCl.

3.2.1 RCA1 chemicals recipe:

600 ml of Ammonia solution (NH_4OH)
600ml of hydrogen peroxide (H_2O_2)
3 liters of deionized water
Ratio: 1:1:5

We took 3 liters of deionized water in RC1 bath and also added 600 ml of Ammonia solution (NH_4OH), in same bath and allowed to stand for some time to reach the temperature at 90 ^{0}C. For heating bath, we used paraffin oil bath. At 90^{0}C we added 600ml of hydrogen peroxide (H_2O_2) carefully in RC1 bath just 5-10 minutes before the wafers cleaning. When we added hydrogen peroxide (H_2O_2), violent bubbling were started and it is not recommended to cover the bath with lid for 1-2 minutes. Wafers were taken in RCA1 cleaning carrier and tied the carrier with handle carefully. Wafers were placed in RC1 bath at 90 ^{0}C for 15 minutes. After 15 minutes wafers were taken out, washed with 1% hydrofluoric acid.

3.2.2 RCA2 chemical recipe:

600 ml of hydrochloric acid (HCl)
600ml of hydrogen peroxide (H_2O_2)
3 liters of deionized water.
Ratio: 1:1:5

RCA2 bath is prepared in similar way as RCA1 but with above mentioned recipe. After RC1 cleaning process, RC2 process was carried out to remove the metal particles. After washing with deionized water, wafers were put in RC2 bath at approximately 90 ^{0}C for 15 minutes. After 15 minutes wafers were taken out, washed with water then treated with 1% hydrofluoric acid and washed once again with water. Wafers were dried in furnace under IR radiation before further processing.

3.3 Doping (Phosphorus diffusion)

Process in which we Introduce impurities into a semiconductor crystal to define modification of conductivity and electronic properties is called doping. There are two most important materials which are used in silicon doping. Boron (B) atom is trivalent (3 valence electrons) and phosphorus (P) is pentavalent (5 valence electrons) impurities. Atoms which are trivalent (3 valence electrons) are used for p-type doping and atoms which are pentavalent (5 valance electrons) are used for n-doping. Diffusion is a process of the redistribution of atoms, molecules and ions from regions of high concentration of mobile species to regions of low concentration. It occurs at all temperatures, but the diffusivity has an exponentially dependent on temperature. High temperature diffusion is one of the important process in solar cell fabrication and other monolithic integrated circuits (IC) in microelectronics devices. Today, diffusion process has been used in the formation of deep layers of emitters below one micron in depth. Diffusion has been the primary method of introducing impurities phosphorous (P), into silicon to control the majority-carrier type and resistivity of doped layers formed on the wafer surface. Phosphorus diffusion is used to form

n+ emitters in silicon solar cells and bipolar power device technology, to form source and drain regions and to dope crystalline silicon wafers in MOS device technology.

3.3.1 Phosphorus pre-deposition (825 ^{0}C)

Phosphorus diffusion was carried out at 825^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas. Steps are given below for phosphorus deposition. Prior to "P" diffusion, textured wafers are passed through HF solution in order to remove oxide layer on the surface of wafers produced by aerial oxidation. Flow of gases for phosphorus diffusion is controlled manually in following order as mentioned in table 3.1. Flow of nitrogen gas through bubbler ($POCl_3$ flask) is also controlled at fix flow rate of nitrogen. Usually furnace is turned on at least one hour prior to diffusion, (Run the desire recipe in order to get required temperature). In this P/Al technology, Phosphorus diffusion is carried at 825 ^{0}C and left the furnace for some time to stabilize the temperature in all zone of furnace, then started the flow of gases in following order:

Table 3.1

Step	Gases flow	Time
Entrance (wafers loading)	N_2 8 *l*/min +O_2 0.45 *l*/min	(5 minutes)
Stabilization	N_2 8 *l*/min +O_2 0.45 *l*/min	(5 minutes)
Doping (P pre-deposition)	N_2 8 *l*/min +O_2 0.45 *l*/min + N_2/$POCl_3$ 60-85 cc/min	(30 minutes)
	Final selected flow: N_2 8 *l*/min +O_2 0.45 *l*/min + N_2/$POCl_3$ 85 cc/min	(30 minutes)
Oxidation	O_2 10 *l*/min	(10 minutes)
Annealing	N_2 6 *l*/min	(10 minutes)
Exit (wafers unloading)	N_2 6 *l*/min	(5 minutes)

Chemical reaction for phosphorus diffusion is given below, phosphorus oxychloride reacts with oxygen to produce phosphorus pentoxide (P_2O_5) which reacts with silicon to produce free phosphorus to diffuse into silicon. The Rate at which phosphorus diffuse into silicon depends on the temperature of furnace. The amount of dopant entering into furnace must be control in order to get desire sheet resistance, uniformity and repeatability of process. This control is achieved by maintaining a constant temperature of furnace and gaseous flow. It is also important to control the flow gas through bubbler and temperature of bubbler. Usually bubble temperature is fixed at 20ºC, a 5 ºC less than room temperature in order avoid condensation of chemical in the flow line leading from bubble to furnace tube.

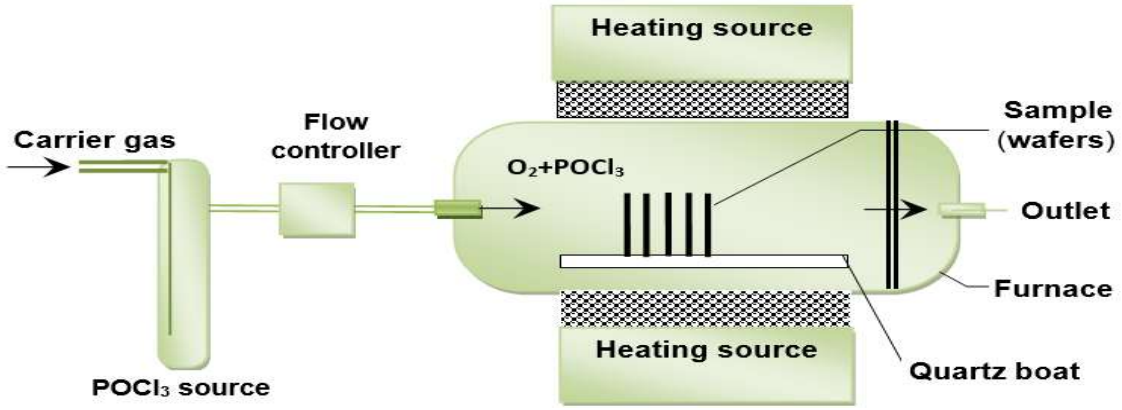

Figure 3.9 Flow sheet representation of phosphorus diffusion furnace.

$$2POCl_3 + O_2 \longrightarrow 2P_2O_5 + 3Cl_2$$

$$2P_2O_5 + 5Si \longrightarrow 4P + 5SiO_2$$

At 825^0C we have taken out the boat (carrier) from furnace with the help of long glass rod by using safety gloves and adjusted the wafers in the boat carefully at minimum distance among the wafers. Wafers were introduced into furnace carefully by using handle of boat and protective gloves. Wafers were moved slowly inside the furnace especially at high temperature in order to avoid cracks. Wafers were allowed to homogenize in the furnace for 5 minutes prior to start flow of gases into furnace as mentioned in table 1. This step is used for stabilization of wafers inside the furnace. After 5 minutes we opened the N_2 flow through bubbler (flask containing $POCl_3$) for 30 minutes at above mentioned rate as given in table. This step is called pre-deposition. After 30 minutes, we opened O_2 gas flow at the above mention rate for 10 minutes and closed the flow of nitrogen toward the furnace and also closed the flow of N_2 through the bubbler. This is called oxidation process, after oxidation phosphorus neither diffuses into the wafers nor effuses outside the wafers. After 10 minutes, we closed the O_2 and opened again N_2 for 10 minutes for annealing process at above mention flow rate. Fast movement of wafers inside the furnace can produce cracks due to carrier and different dilatation coefficient of stirring wafers.

At oxidation step in pre-deposition process, a layer of SiO_2 is grown by the oxidation of silicon by oxygen gas which acts as a barrier for further diffusion of phosphorus inside or outside from silicon lattice. After oxidation, phosphorus neither diffuses into the wafers nor effuses outside the wafers. This layer not only acts as a barrier for phosphorus but also reduce the surface recombination velocity. Annealing process improves material properties such as hardness and strength. Care should be taken while the wafers processing, inside the furnace high temperature stress can produce cracks. All gaseous flow is controlled manually and manual control system is shown in figure 3.10.

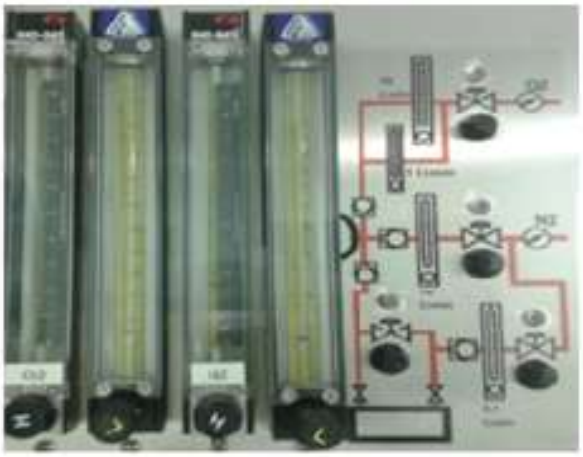

Figure 3.10 Manual control system of gases flow

3.4 Sheet resistance and emitter characterization

The most important and most delicate step is phosphorus pre-deposition. The main problem is uniformity on the wafer surface and from one wafer to other wafer. The sheet resistance vary from wafer to wafer, even on same wafer. Other problem is lack of repeatability from batch to batch. It is really different to get desire sheet resistance in a batch process. We have repeated many time this process to get desire sheet resistance. As I have already described that our aim was to get sheet resistance Rs 100 Ω/□ with deep junction depth.

There are many ways to control the process to get desire values either by changing the dose of phosphorus atoms which goes to silicon by modification of $POCl_3$ flow time or concentration of oxygen. We can also change flow rate of $POCl_3$ concentration by changing flow of nitrogen through bubbler [20-21]. In this technology during phosphorus pre-deposition a thin layer of oxide is also grown to passivate the surface. In furnace heavily contaminated with phosphorus and oxides acts as an additional source of dopant during drive-in process. This step also helps to get reasonable uniformity in sheet resistance values. 10 minutes of oxidation is thin enough and do not affected by AR coatings. The sheet resistance measured immediately after pre-deposition, sheet resistance values were very high ranging from 400-650 Ω/□. But after drive-in, the final sheet resistance measured after distribution show some kind of uniformity in final values ranging from 80-150 Ω/□. Final sheet resistance values are better to make a good emitters. The decrease of sheet resistance values during drive-in (distribution) process at high temperature indicate that thin layer of phosphosilicate glass (PSG) act as an impurities sources. Due to high mobility, surface concentration increase which decrease the sheet resistance. [20-21].

We have performed many experiments to get to desire results but not all experiments were reliable. There are many factors which effect on reliability, most important is the proper maintenance of furnace, to keep it in working condition. Others factors are flow of nitrogen gas through the bubbler and temperature of bubbler, pre-deposition time and temperature. E.g. at high temperature pre-deposition of 900 ºC for 5 minutes is similar like low temperature pre-deposition of 800 ºC for 30 minutes. All above mentioned variables should be optimized to improve the uniformity and repeatability of the process.

Sheet resistance is one of most useful parameter from electronic point of view and easily to characterize. For emitter's characterization including junction depth and surface

dopant concentration, these parameters are difficult to measure but they can be estimated from sheet resistance data. Sheet resistance is easily measureable parameter. It is difficult to model “P” pre-deposition in order to estimate in advance process variables which produce a certain surface dopant concentration and sheet resistance. Junction depth mainly depends on drive-in time and temperature. A theoretical model was developed by A. Cuevas [20-21] to determine the junction depth by SUPREM 3 (one dimension model used for generate a doping profiles resulting from given processing steps), although our results are little bit different, but help to evaluate junction depth. See figure 3.11.

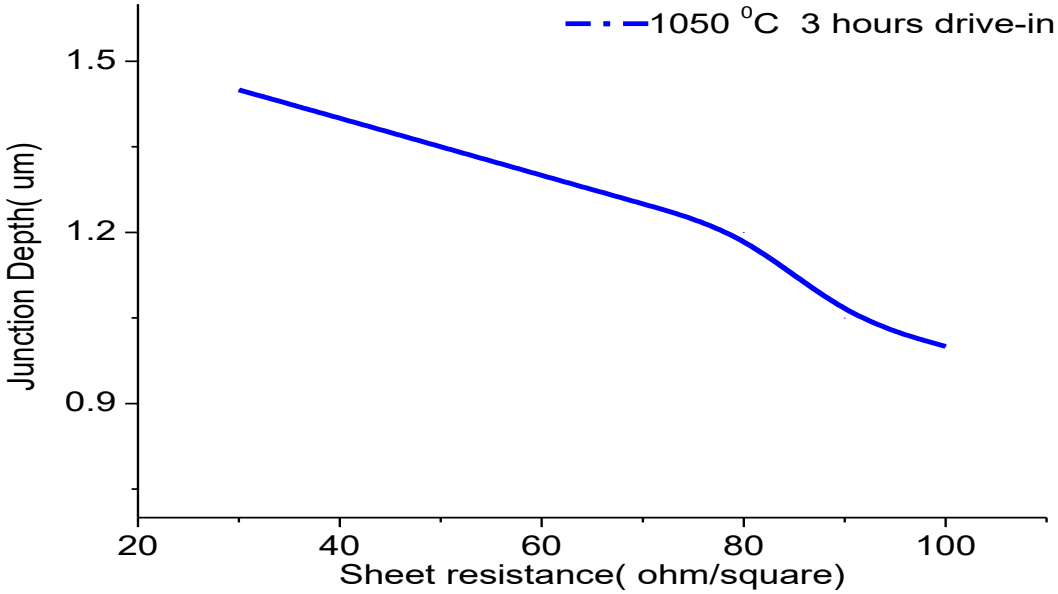

Figure 3.11 Graph between sheet resistance vs junction depth [20]

Impurities concentration of phosphorus is calculated by PC1D simulation with Gaussian adjustment by using sheet resistance data. A graph between concentration and sheet resistance is given in figure 3.12.

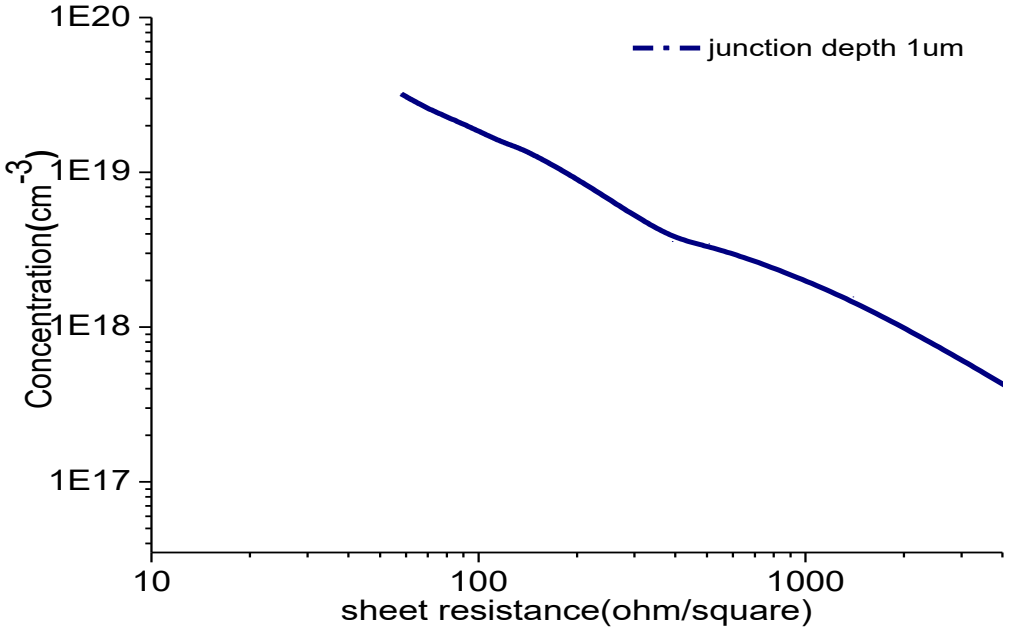

Figure 3.12. Graph between sheet resistance and impurities concentration

After Phosphorus pre-deposition at 825 ºC for 30 minutes and with 3 hours of drive- in at 1050 ºC. Alkaline etching was carried out in order to determine the junction depth and impurities concentration. We used dilute concentration of 2% by weight NaOH at 60 ^{0}C. After 15 seconds of etching, wafers were cleaned and dried to measure the sheet resistance by four probe method. This process is repeated again and again until concentration of impurities or sheet resistance was similar with base doping. In this way we have measured the junction depth. Doping concentration is calculated by PC1D simulation with Gaussian adjustment by using sheet resistance data. Diffusion profile is given in figure 3.13.

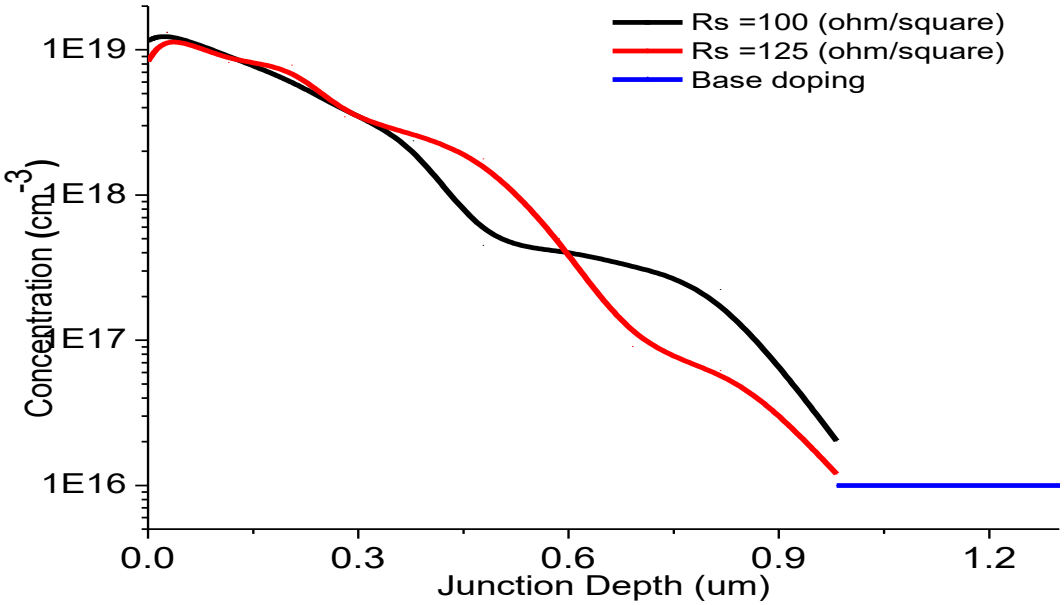

Figure 3.13 Phosphorus doping profile after 30 minutes of pre-deposition at 825 ºC and 3 hours of drive-in inert environment.

In the figure 3.13, diffusion profile of phosphorus is measured after pre-disposition and drive-in a redistribution process in a furnace with temperature high than pre-deposition temperature, 1050 ºC for 3 hours in an inert environment. Graphs in this figure show Gaussian adjustment which are simulated by using a PC1D program. Although there is a difference in experimental and theoretical values for sheet resistance100 Ω/□ but difference is not significant in term of efficiency. From experimental data, it is observed that with increase of resistivity of base of substrate (wafers) also increase the short circuit current and decrease the open circuit voltage. Figure 3.14 and 3.15 show the effect of base doping on open circuit voltage and short circuit current in case of float-zone wafers (FZ) by considering fixed lifetime of base. This trend is also supported by theoretical predictions of A. Luque [22]. It was observed that efficiency and fill factor almost remain constant over a wide range of base doping from 1X10E13 cm^{-3} to 1X10E16 cm^{-3} as shown in table 2. Detail of technological knowledge is given in the doctoral thesis of J. Alonso and R. Lago [23-24] and following articles [25-26].

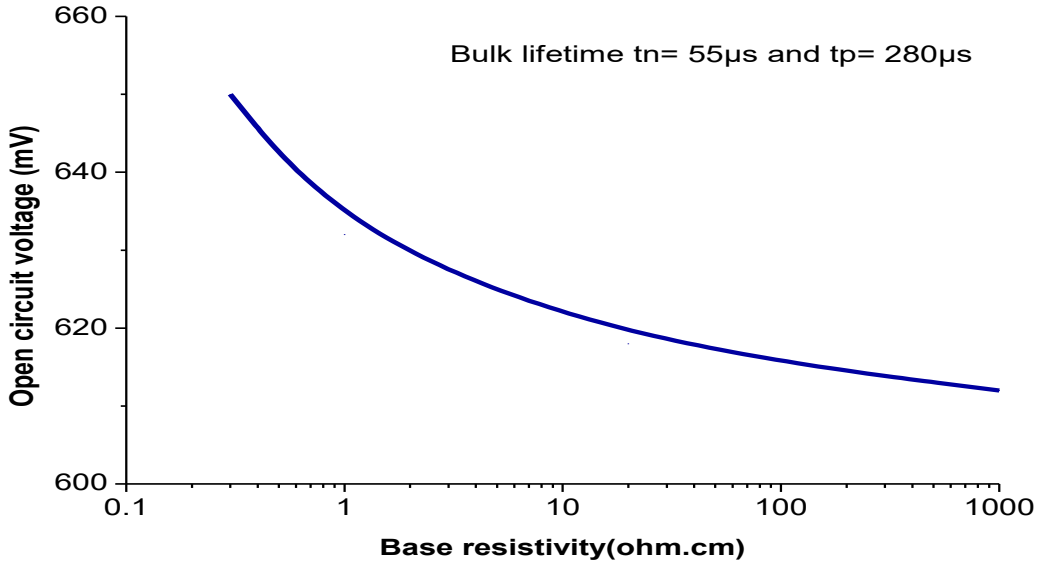

Figure 3.14 Effect on base doping on open circuit voltage

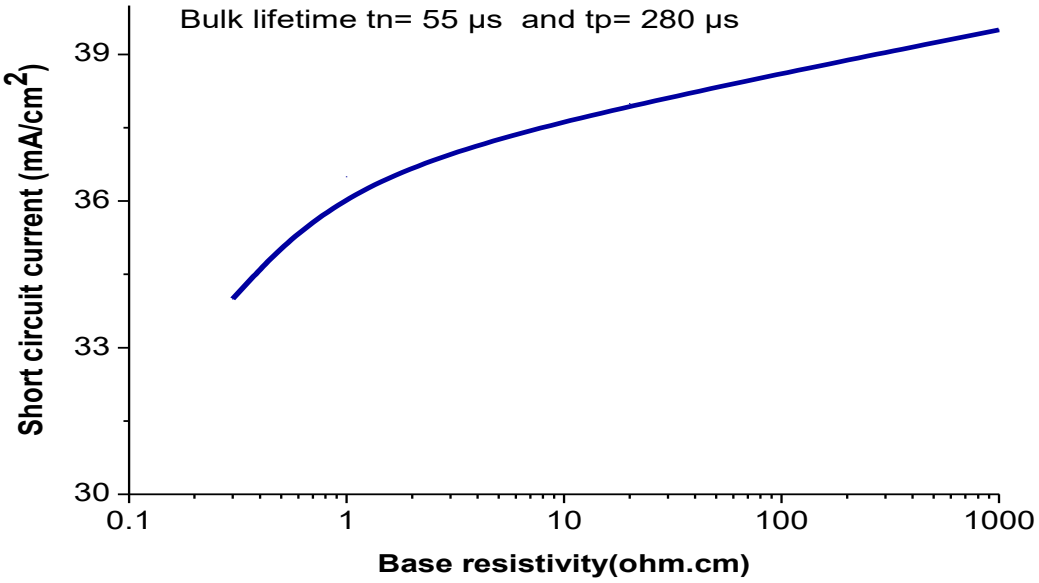

Figure 3.15 Effect of base doping on short circuit current

Table 3.2

Type of wafers (Resistivity in Ω.cm)	Voc (mV)	Jsc (A/cm^2)	FF (%)	Efficiency (%)	References
Monocrystaline FZ (0.3)	645-650	35	75-83	17.5-19	[1]
Monocrystaline FZ (0.3)	645-650	35	81-83	18.5	[24]
Monocrystaline FZ (1)	628-632	37-38	81	18.5-19.5	[24]
Monocrystaline FZ (20)	612-618	38-39.5	79-81	18.5-19	[24]

This technology has been developed and applied in the IES (Institute solar energy Madrid) for particular cases with satisfactory results. After invention of this technology, improvement was carried out by many researchers at IES. Results obtained by these researchers are already discussed in first chapter. The Moussaui [27-28] presents the process for formation emitters by using P/Al technology in one step, as an optional simplification, the results obtained are shown in table 3.3.

Table 3.3

Material	FZ wafers	Multicrystalline (Bayer)	Multicrystalline (Eurosolare)
Efficiency	17.1%	16.1%	17.4%
Observation (P/Al technology)	Without Texturing and AR coating	With P Pre gettering 950ºC	With P Pre-gettering 950ºC

These results are obtained on $4cm^2$ by using P/Al fabrication scheme. (Look at figure 1.10 of 1st chapter) In the case of multicrystalline material it has raised the need for simultaneous diffusion P/Al at temperatures lower than 1000 $^{\circ}C$ (low quality substrates), and the wafers were subjected to a supersaturation phosphorus to remove impurities from the volume before starting the fabrication process. With these innovations, efficiency has reached 16 to 17% cells in 2 to $4cm^2$ on multicrystalline material. [27-28] After P pre-deposition step, Wafers were ready for Al deposition.

3.5 Aluminum Deposition (By PVD)

Deposition of metals by using an electron beam machine is a physical vapor deposition technique (PVD), in which target anode is bombarded with high energy beam of electron release from a tungsten filament under high vacuum. Electron beam evaporate atoms of solid material (Al metal) and transform into gaseous state, later these gaseous atoms precipitated into solid form. Everything inside the chamber is coated with a thin layer of target material. Physical vapor deposition is carried at low deposition temperature and without corrosive product. Deposition rate not only depends on current supply and voltage but also on pressure of chamber. At low vacuum level, evaporation rate is higher, higher will be deposition rate. Flow sheet diagram of electron beam machine is shown in figure 3.16.

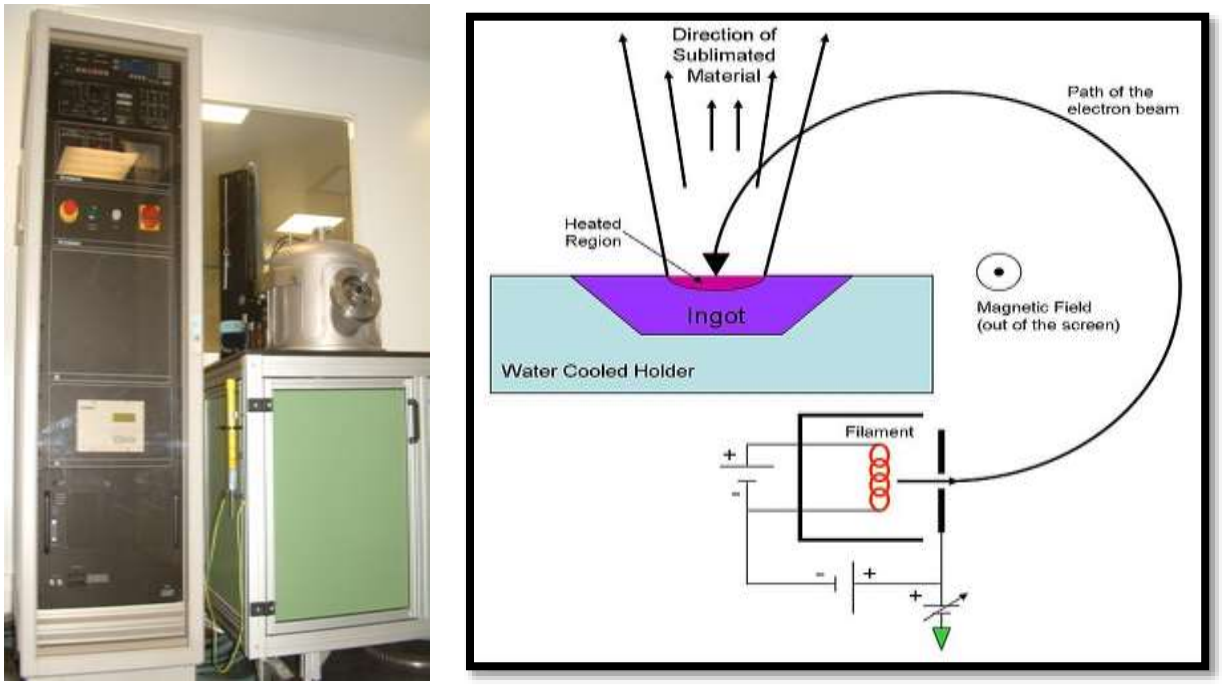

Figure 3.16 Flow sheet diagram of chamber of electron beam machine.

For electromagnetic alignment, ingot is placed at a positive potential relative to filament. To avoid a chemical interaction between filament and ingot material, filament is kept out of ingot area. A magnetic field is employed to direct and control electron beam from its source to ingot location. Additional electric field is applied, which is used to steer the beam over ingot surface for uniform heating. Usually ingot is enclosed in a copper crucible or hearth. Crucible and socket must be cooled and this usually done by water circulation. Evaporation rate can be control, slow and continuous evaporation is recommended for uniformity of thin film.

After introducing the wafers, closed the chamber and turn on vacuum machine to create high vacuum, at desire vacuum, first apply the high voltage up to 6 KV and then apply the current from 5 mA to 250mA. Voltage and current supply vary from metal to metal. E.g. in case of aluminum we need high voltage and current supply while in case palladium we need less power supply. Higher current supply increases the evaporation rate as well Al deposition. During this process care should be taken that electron beam must focus in the center of crucible. During deposition process, make sure that water is flowing in the chamber for cooling purpose.

Metal	Vacuum (Torr)	Voltage (kV)	Current (mA)	Tooling factor (%)	Thickness (A^0)
Al	5×10^{-5} to10^{-6}	7	120-220	45	10000

(Voltage 7kV, Mini. Vacuum 5×10^{-5} to10^{-6} Torr and Current 120-220 mA)

During aluminum deposition, make sure that crucible contains enough amount of aluminum to get 1µm thickness. The best way is complete the process in two steps, 0.5um in each step. Although process is remote control, after desire thickness machine is stopped automatically but still we can calculate the thickness by measuring weight gain by wafers during deposition of aluminum for accurate results by using following equation 3.1.

$$t = \frac{W}{\rho \times area\ of\ wafer} \quad (3.1)$$

W= difference in weight (gain in weight)

ρ= density of Al 2.7g/cm^3

t= thickness of A layer

3.6 P/Al Drive-in process

During drive-in process, aluminum diffuse into the p-type silicon base and it produced a p p+ junction at the rear zone. As we already know that rear side of wafers have n+ emitters, but alloying with aluminum after phosphorus pre-deposition make unnecessary to remove the n+ emitters from rear side. This p p+ junction generates an electric field opposite to the electron movement from the base to the p+ contact, so less carriers arrive to the rear surface and in this way effective values of *S* is improves. Lifetime is decreased by the presence of defects and impurities in the crystal and it is strongly dependent on the contamination in the fabrication process. Impurities may be removed from the back by gettering process, so lifetime is increase. Gettering effect is produced by the molten aluminum layer during drive-in process [29-32]. Phosphorus and aluminum redistribution was performed in a single furnace step. At 1050 ^{0}C drive-in process for P/Al is performed under inert atmosphere using nitrogen gas for 3 hours. Drive in facilitate to move impurities deeper into the semiconductor (silicon wafers). The front emitter (collector) obtained is 1.1µm deep with a sheet resistance of 100-150 Ω/ □. Drive in process has three advantages;

1. Impurities which are presented in bulk of silicon are cleaned by aluminum via gettering process and lifetime is improved.
2. Aluminum diffuses inside the silicon which gives a p+ zone with p base and metal rear contact and BSF effect appear.
3. Back aluminum layer acts as a back reflector, the photons that travelled through the cell and have not been absorbed, reflected back to the bulk of the silicon and have another opportunity to be absorbed.

Table 3.4

Step	Gases flow
Entrance (wafers loading)	N_2 2 *l*/min + O_2 6 *l*/min (5 minutes)
After 5 minutes	N_2 10 *l*/min (5 minutes)
After 10 minutes	N_2 2 *l*/min (2h and 50 minutes)

N_2 gas flow 2l/min from starting of furnace to get 1050^{0}C

3.7 Aluminum redistribution process (Redistribution of aluminum in silicon)

Aluminum is responsible for creating BSF effect on rear side of P/Al cells to form the p^+ layer and redistribution of aluminum at high temperature produces an effect of removing impurities through gettering process, which can reduce recombination in volume significantly. This process modify the lifetime of the volume due to BSF effect during drive-in

process. This feature redistribution of aluminum in silicon can be analyze, both from theoretical and experimental perspective. [29-32]

The Al-Si phase diagram is a straightforward, classic example of a eutectic system where each element has little, if any solubility in the other. Aluminum melts at 660°C while silicon melts at 1414 ºC shows the eutectic at 12.6 wt. % Si and 577 °C. The maximum solubility of Si in Al is about 1.7% at 577°C, while solubility decreases with decreasing temperature. There is virtually no solubility for Al in Si at any temperature to the melting point. Phase diagram of aluminum-silicon (Al-Si) alloy is shown in figure 3.17. As we can see in figure 3.19, it has a eutectic temperature of 577 ºC corresponding to a composition of 88.5% Al and Si 11.5%.

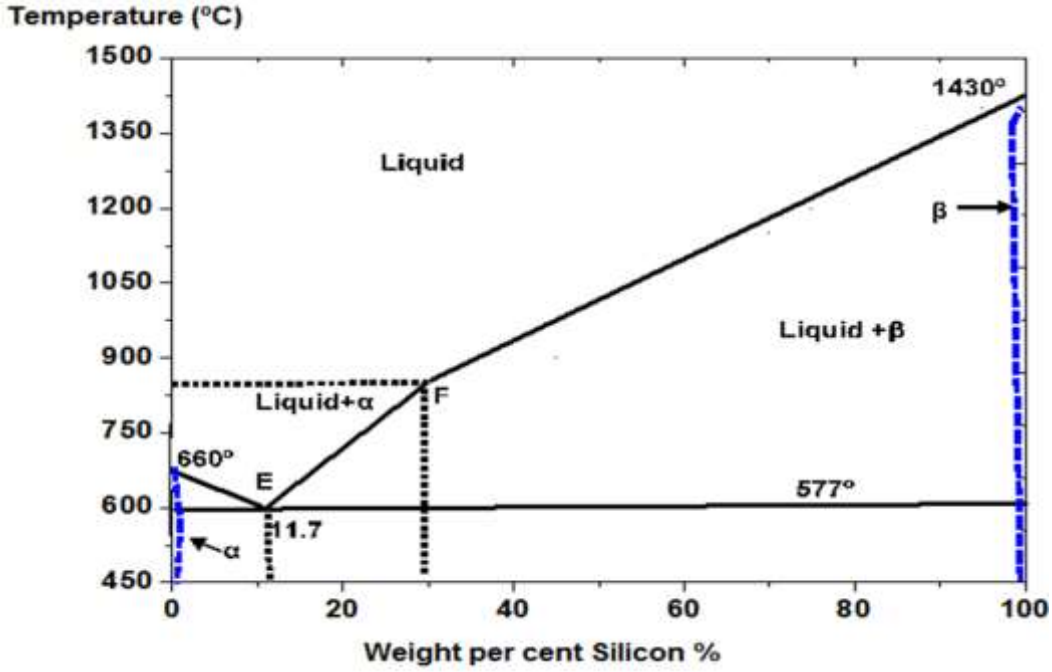

Figure 3.17 Phase diagram of Al-Si

In the fabrication of silicon solar cells with P/Al technology, aluminum layer is deposited on the backside of silicon wafers and redistributed at high temperature (higher than eutectic temperature). The process which occurs in shown in figure 3.18.

The phenomena which take place is shown in figure 3.18(a), shows the deposition of aluminum on backside of wafer, 3.18(b) represents high temperature step in an inert atmosphere but in this case we used nitrogen gas. It forms a liquid layer of Al-Si, which consume deposited aluminum and a certain amount of crystalline silicon. Concentration will be high at high temperature (as in phase diagram). In figure 3.18(C) indicates that Al also diffuse into silicon and dope the silicon. During cooling which occurs when we took out the wafers from furnace is shown in figure 3.18(c). A liquid layer is also capable of dissolving small amount of silicon at low temperature as shown in phase diagram. Progressively excess of silicon recrystallized epitaxial and has aluminum doping profile according to the solid solubility for each temperature of the cooling curve. Finally in figure 3.18(d) shows that once reached the eutectic temperature the remaining liquid layer solidified Al-Si eutectic with the proportions of (88% Al, 11.7% Si).

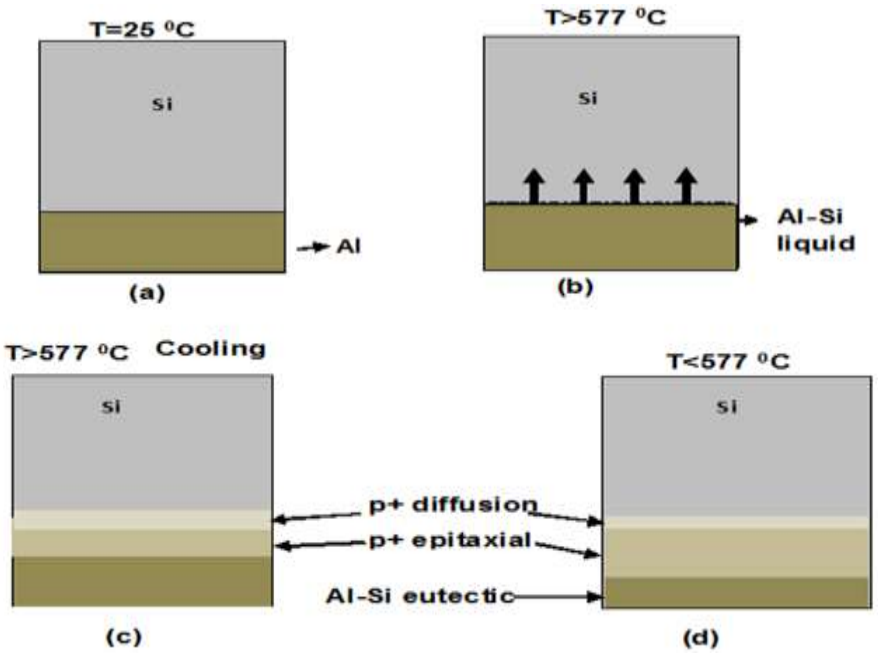

Figure 3.18 Redistribution of aluminum in silicon at a temperature higher than eutectic temperature (a) It represents deposition aluminum layer on the silicon (b) high-temperature processing (higher than the eutectic temperature). (c) Cooling during removal of the wafers from furnace at temperature higher than the eutectic temperature. (d) Cooling to a lower temperature than the eutectic temperature.

J.D. Alamo et al [33] estimated the thickness of recrystallized silicon epitaxially layer W_{P^+}, referred in figure 3.20(d). Layer p^+epitaxial in mathematical expression is written in equation 3.2. By the using this expression we can calculate depth of p^+ layer in silicon.

$$W_{P^+} = \frac{P_{Al}}{A\rho_{Si}}\left(\frac{F}{100-F} - \frac{E}{100-E}\right) \qquad (3.2)$$

While P_{Al} is weight of Aluminum deposited, A is the area of the wafer ρ_{Si} is the density of silicon and F and E are percentage of silicon at liquid (surface) zone to the temperature of process and of the eutectic temperature respectively, Figure represent thickness of this layer for various temperatures, by evaporating aluminum 1µm thick layer. Values for W_{P^+} obtained by using above equation on different firing temperature is shown in figure 3.19.

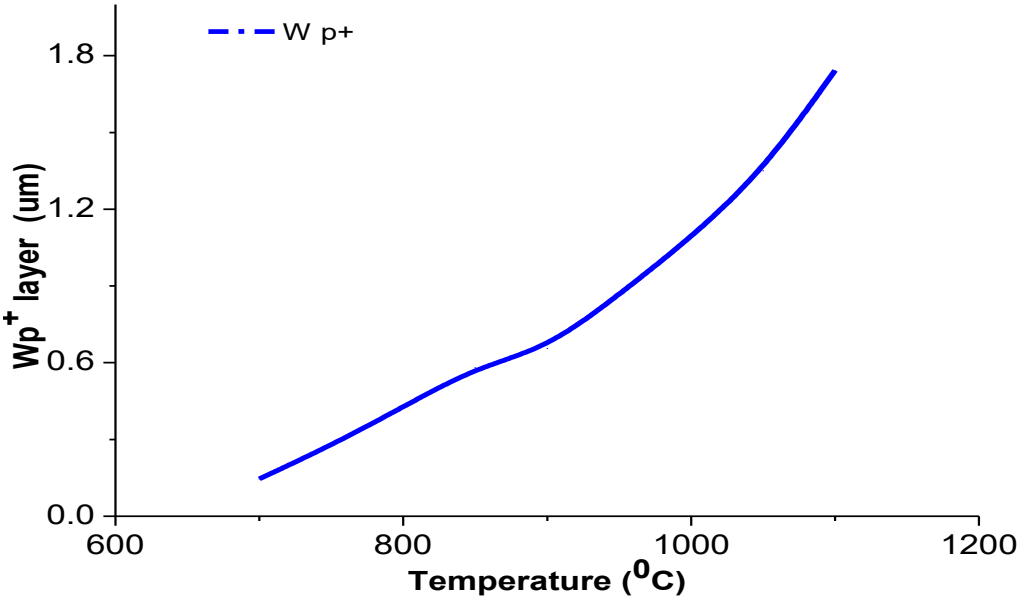

Figure 3.19 Thickness of the silicon layer epitaxially recrystallized with respect to the temperature of the redistribution process after evaporation 1 μm of Aluminum

As indicated earlier, the area which is grown epitaxially in aluminum profile according to solid solubility corresponding for each temperature of the cooling curve, if it has been slow and allowed balance, or it will be a more complicated profile. Its peak doping is on the border with p^+ diffused and the solid solubility at temperature of redistribution, assign value for doping p^+ epitaxial entire area posterior simulations, as this profile is not decisive. In table 3.5 shows the solid solubility (C_S) of aluminum in silicon for various temperatures. While D is diffusion coefficient of Al.

Table 3.5; solid solubility of Al in Silicon with respect to temperature

Temperature (ºC)	D cm^2/sec	Cs (cm^{-3})	Reference
750	2.20E-17	9.00E+18	23, 34
800	1.33E-16	1.10E+19	23, 34
850	6.87E-16	1.40E+19	23, 34
900	3.08E-15	1.60E+19	23, 34
950	1.22E-14	1.70E+19	23, 34
1000	4.37E-14	1.90E+19	23, 34
1050	1.41E-13	2.00E+19	23, 34

From the theory of solid state diffusion can apply to profile of aluminum diffusion into the silicon in the process of high temperature redistribution. Because the liquid aluminum phase acts as infinite source of diffusion in this process, its diffusion profile has shape of a complementary error function according to the expression eq.3.3 [35].

$$C_{(x)} = C_s erfc\left(\frac{x}{2\sqrt{D_{Al}t}}\right) \tag{3.3}$$

For simplicity doping profile can be considered in Gaussian form

$$C_{(x)} = C_s\, exp\left[\frac{(x - x_{p+})^2}{4D_{Al}t}\right] \qquad C_{(x)} = C_s\, exp\left[\frac{(x - x_{rec})^2}{4D_{Al}t}\right] \tag{3.4}$$

As we have mentioned early, that peak doping is equal to the solid solubility of Al in Si at the process temperature. The profile depends on the temperature (through diffusion coefficient) and process duration. We considered the diffusion coefficients Y. C. Kao et al, [36-37] as the best fit to the experimentally measured profiles. From these values and with base doping silicon, we can estimate thickness of the layer W_{dif} by using equation 3.5. In figure 3.22, W_{dif} calculated for the various processes at different temperature with redistribution.

$$W_{dif} = \sqrt{4Dt \ln\left(\frac{C_s}{C_B}\right)} \tag{3.5}$$

By using above equation (eq. 3.5) which is a simple form and facilitate to calculate the thickness of diffused layer after several hours of process, if we know the values of diffusion for one hour. We can calculate for rest of hours. Equation is given below (eq. 3.6). Depth of aluminum diffusion depends on time of drive-in and temperature as shown in figure 3.20.

$$W_{dif} = W_{dif,1hour}\sqrt{t} \tag{3.6}$$

While “t” is time in hours.

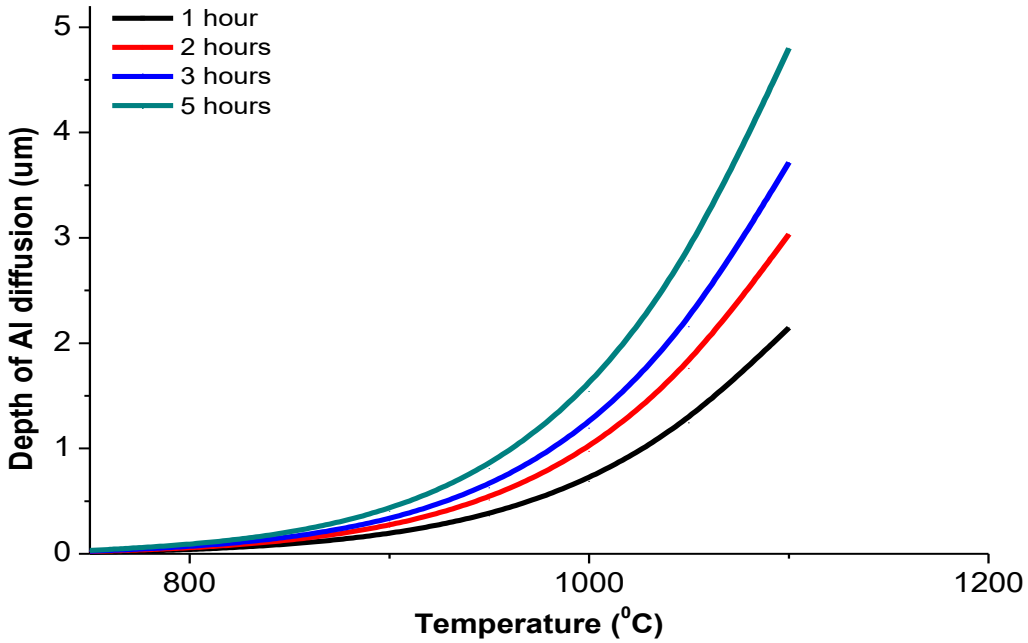

Figure 3.20 Depth of Al diffusion in silicon for various process.

In P/Al technology, we have deposited 1 µm thick layer of Aluminum and all batches of wafers having P emitter on front side and Al on backside were processed at 1050 ºC for 3 hours for distribution of impurities. Usually p+ region of doping is characterized by scattering experimentally by Spreading sheet resistance or ECV (electrochemical capacitance voltage measurement). Although experimentally we did not measured Al doping profile but we have

estimated theoretically and compare with already published results under same conditions. [23 and 28].

Total thickness of p+ layer is the sum of W_{p+} and W_{dif} as it given in equation 1&2. In figure 3.25 a doping profile of P/Al solar cell is shown, in which theoretical data is compare with experimental measurements for maximum doping have been assigned experimental profile for P diffusion (100 Rs(Ω/□) that is fitted with Gaussian profile and while in case of Al diffusion data is taken from already published data. [23 and 28]. In case of figure 3.21. Aluminum layer is 1.5 µm thick, and redistribution was carried out at different temperatures.

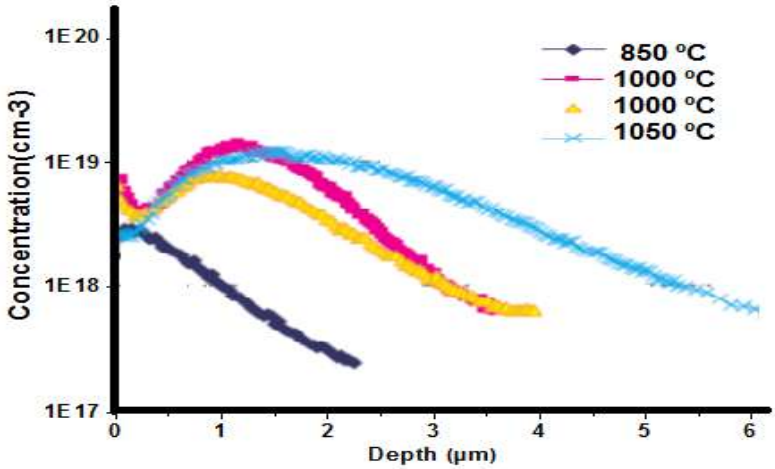

Figure 3.21 Experimental doping profile of aluminum in silicon after different redistribution process. (1.5 µm layer of Al is deposited by evaporation. Profile is measured by using ECV technique. [23]

Various diffusion coefficient of aluminum was determined from aluminum profiles by different research groups. A summary of diffusion coefficient can be found in the graph of figures in Arrhenius expression. In all cases energy of activation was in range of 2.92 to 3.47 eV. By using equation (3.7) diffusion coefficient values are calculated and plotted in figure 3.22, there is difference in diffusion constant and energy of activation values which are given in table 3.6 .

$$D = D_0 Exp\left(\frac{-Ea}{k.T}\right) \tag{3.7}$$

Table 3.6

D_0 (cm^2/s)	E (eV)	D (1200 ºC) (cm^2/s)	Reference
8	3.47	9.24E-12	C.S. Fuller [38]
2800	3.8	1.28E-10	B. Goldstein [39]
1.38	3.41	2.98E-12	R.N. Ghoshtagore [40]
1.8	3.2	2.04E-11	Rosnowski [41]
1530	4.1	4.29E-11	Cuevas and R.B.Fair [20-42]

Data which is available for aluminum diffusion coefficient is very scattered and R.B.Fair [42-43] critically reviewed all the available data corrected it by multiplying it electric field enhancement factor. So above equation for diffusion coefficient for Al is written as follow:

$$D_{Al} = h\,1530Exp\left(\frac{-4.1}{k.T}\right) \tag{3.8}$$

While h is the time in hours and in our case time is 3 hours and we have calculated diffusion coefficient of Al by using equation 3.8.

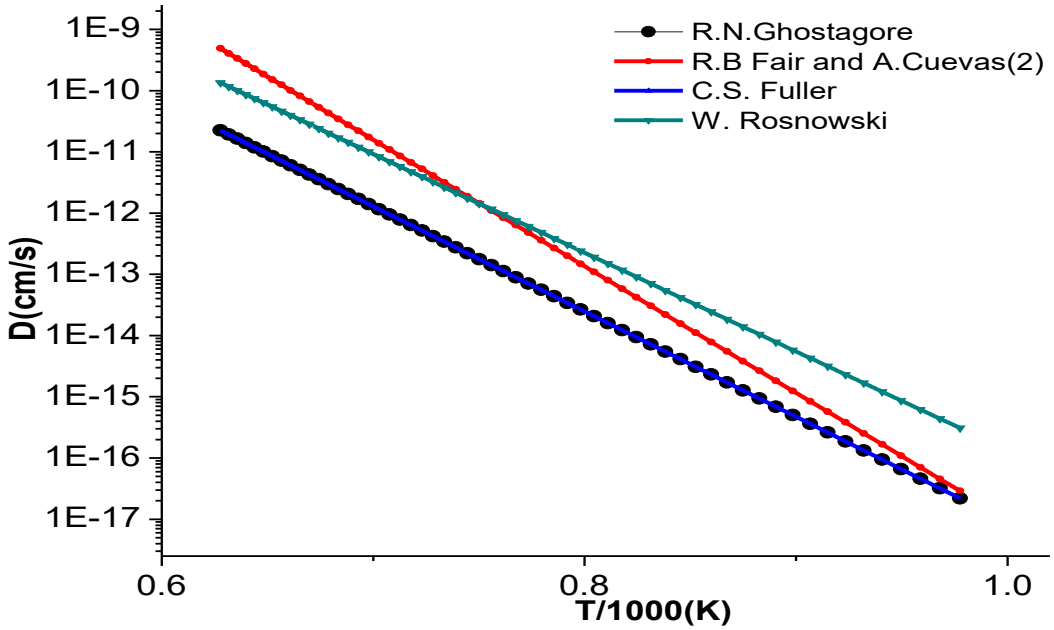

Figure 3.22 Diffusion coefficients of Aluminum in silicon (diffusivity) Al in Si (log of diffusivity of Al in Si verses reciprocal of temperature (in Kelvin)

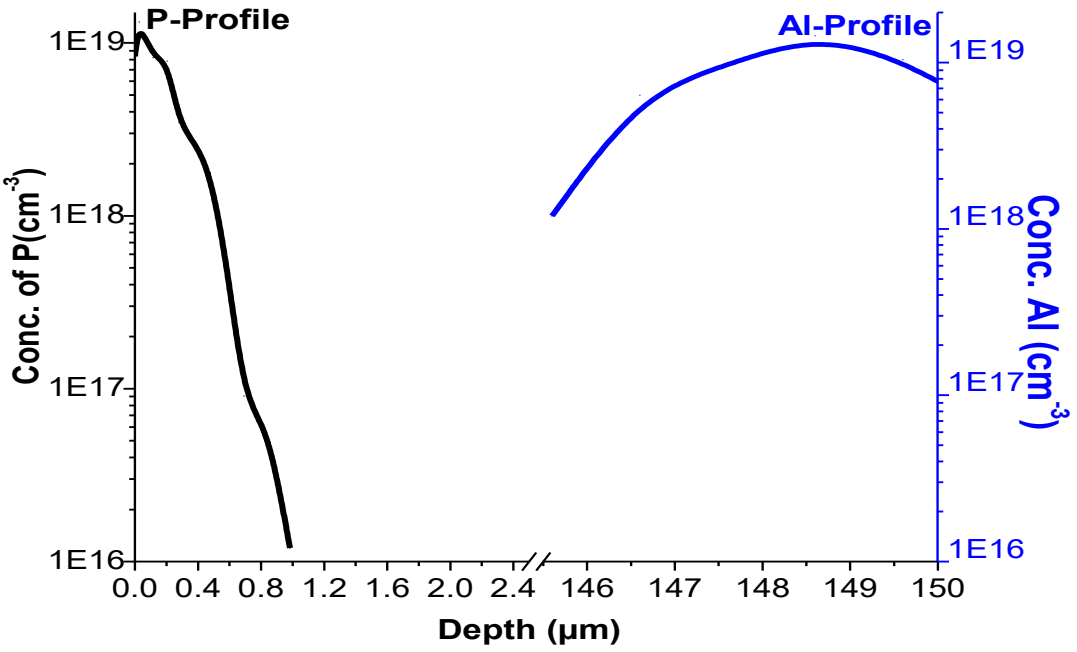

Figure 3.23 Phosphorus and Aluminum profiles after 3 hours of drive-in (re-distribution of impurities)

Figure 3.23 shows a phosphorus and aluminum profiles plotted for typical n+pp+ structure of solar cell fabricated by P/Al technology. In this process, we have used wafer 150 µm thick with base resistivity around 1.46 Ω.cm. After all thermal step, wafers have lowly doped thick (deep) emitters on front side with sheet resistance around 100Ω/□.

Table 3.7 Description of structure of P/Al solar cell

n+ pp+ cell	Front surface	Rear surface BSF
Doping source	P by $POCl_3$	Aluminum by evaporation
Base doping concentration (cm^{-3})	1E+16 (cm^{-3})	1E+16 (cm^{-3})
Drive-in (time)	3 hours	3 hours
Temperature (ºC)	1050 ºC	1050 ºC
Sheet resistance (Rs) After drive-in	100 (Ω/□)	
Surface concentration (cm^{-3})	1.16E+19 (cm^{-3})	8E+18 (cm^{-3}) Max. 2E+19(cm^{-3})
Junction Depth (µm)	1.01 (µm)	3.5 (µm)

3.8 PC1D evaluation of p+ layer

By using PC1D program simulation, we have calculated the effect of thickness of p+ layer on short circuit current, open circuit voltage and efficiency for different base thickness of solar cells. Effect of thickness of p+ layer can be seen in following figures (figure 3.24, 3.25 and 3.26) [44].

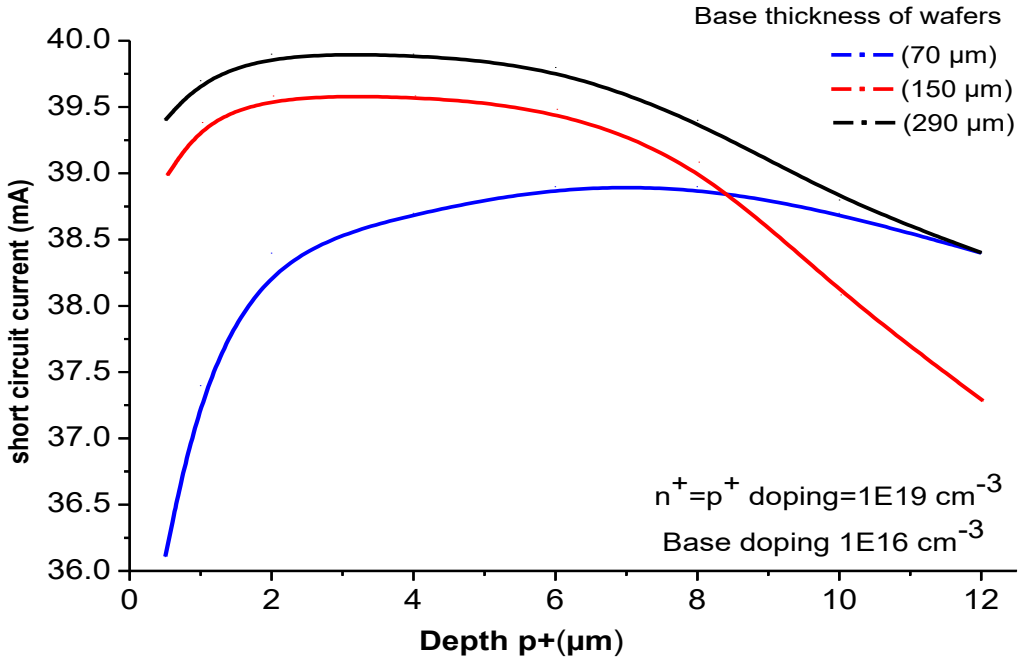

Figure 3.24 Effect of thickness of p+ layer on short circuit current

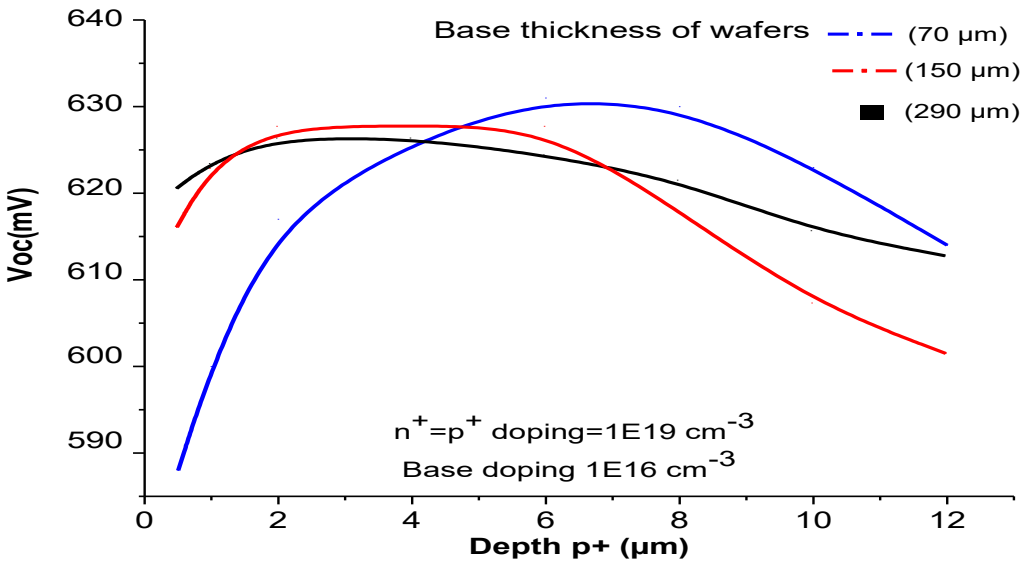

Figure 3.25 Effect of thickness of p+ layer on open circuit voltage

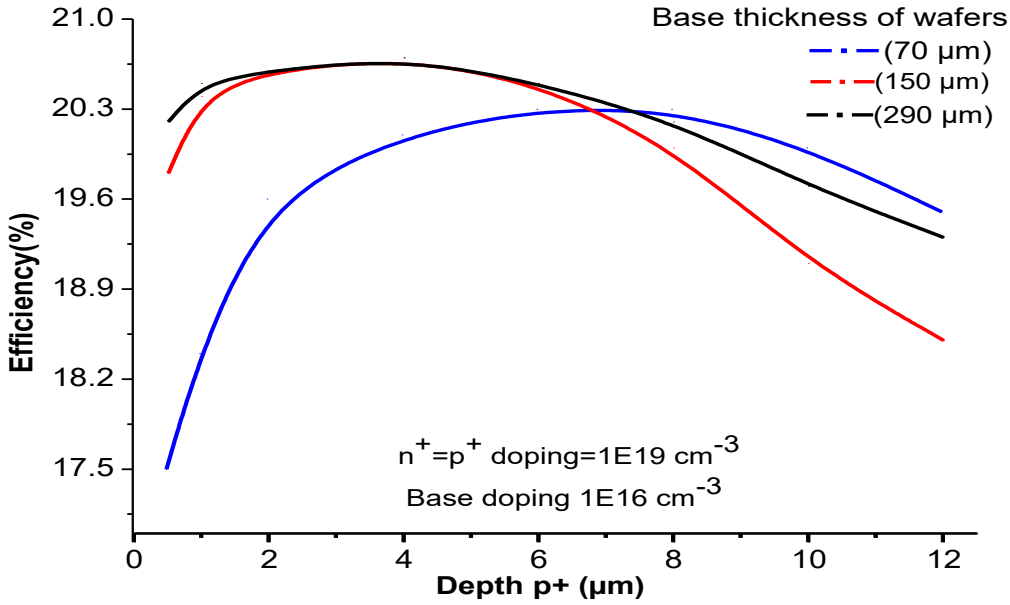

Figure 3.26 Effect of thickness of p+ layer on efficiency of P/Al solar cell

3.8.1 Disadvantages of high temperature drive-in

At high temperature in case of Al diffusion on backside of wafers, it creates stress on crystal orientation of wafers and wafers were bended even broken due to high temperature. In addition this lifetime is affected too much due to high temperature. A photograph of tilted and broken wafers is shown in the figure 3.27.

Figure 3.27 Wafers are bended due to Al diffusion at high temperature

3.9 Antireflection coating (ARC)

It is a type of optical coating applied on the surface of wafers and light reflecting materials and optical devices to reduce back reflection. Silicon nitride has been extensively used in research since last two decades**.** Silicon nitride film provides excellent surface passivation, transparency, antireflective properties and stability under ultraviolet light exposure and high thermal treatment. Coating layer improves the efficiency of the solar cell by absorbing maximum light. A layer of silicon nitride also acts as antireflection layer typically deposited using chemical vapor deposition process (CVD). Precursor gases of silane (SiH_4) and ammonia (NH_3) are fed into a chamber and break down due to a plasma enhancement (PECVD). PECVD is a technique used to deposit thin films from gas state (vapors) to solid state on a substrate. Chemical reaction, which takes place after creation of plasma of reacting gases (vapors). Plasma is generally created by RF (radiofrequency) or DC discharge between two electrodes and space is filled with reacting gases. In silicon solar cell fabrication, PECVD technique is used to deposit antireflection layer of silicon nitride (SnxNy). Silicon nitride layer not only acts as antireflection layer but also use for passivation of dangling bond.

Plasma enhanced chemical vapor deposition (PECVD) forms a thin film from precursor gaseous mixture, whose molecules are broken by using electric field. The gaseous excitation is used to produce plasma between two electrodes of electric field. Other systems use microwaves to cause the silane/ammonia reaction to take place. The complete reaction is given below;

$$3SiH_4+4NH_3 \longrightarrow Si_3N_4+12H_2$$

But the usual reaction to produce a non-stoichiometric film with the incorporation of large amounts of hydrogen (Si_xN_y:H). The process which is used to deposit silicon nitride is based on decomposition of hydrogenated gases. High content of hydrogen gas ensure to improve the surface passivation by saturating dangling bonds. This hydrogen is also beneficial for passivation of the defects in bulk of low quality grade silicon material. Oxygen content also improves surface passivation by saturating the dangling bonds. In order to obtain a good AR coating, we have to make sure that the oxide layer is after drive-in is very thin, therefore we have to check the reflectance measurements after drive-in. We also have to check the measurement of reflectance after AR coating. Silicon nitride not only acts as antireflection coating but also passivate the silicon surface [45-47].

Silicon nitride deposition was carried at 450ºC.
Silane (SiH_4): 50 sccm
Ammonia (NH_3): 65 sccm

Argon (Ar): 40 sccm

In this chapter we will discuss the deposition of AR coating, and its optical characterization. Detail of AR coating with respect to passivation and lifetime improvements, we will discuss in passivation chapter. Microscopic images of texture wafer and texture with AR coating is shown in figure 3.28. AR coating is characterized by antireflection measurements. Texture wafers with AR coating have average reflectance less than 5%. Graph of reflectance measurement is shown in figure 3.29.

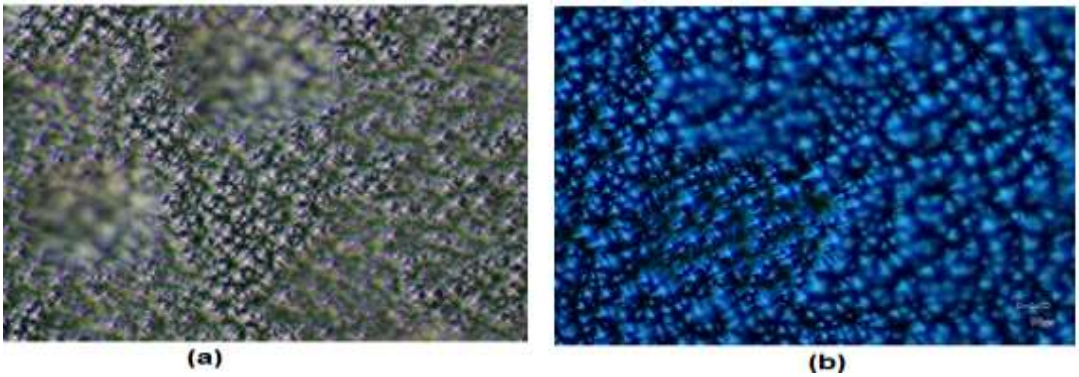

Figure 3.28 Microscopic images of (a) Texture silicon wafer (b) Texture silicon with AR coating

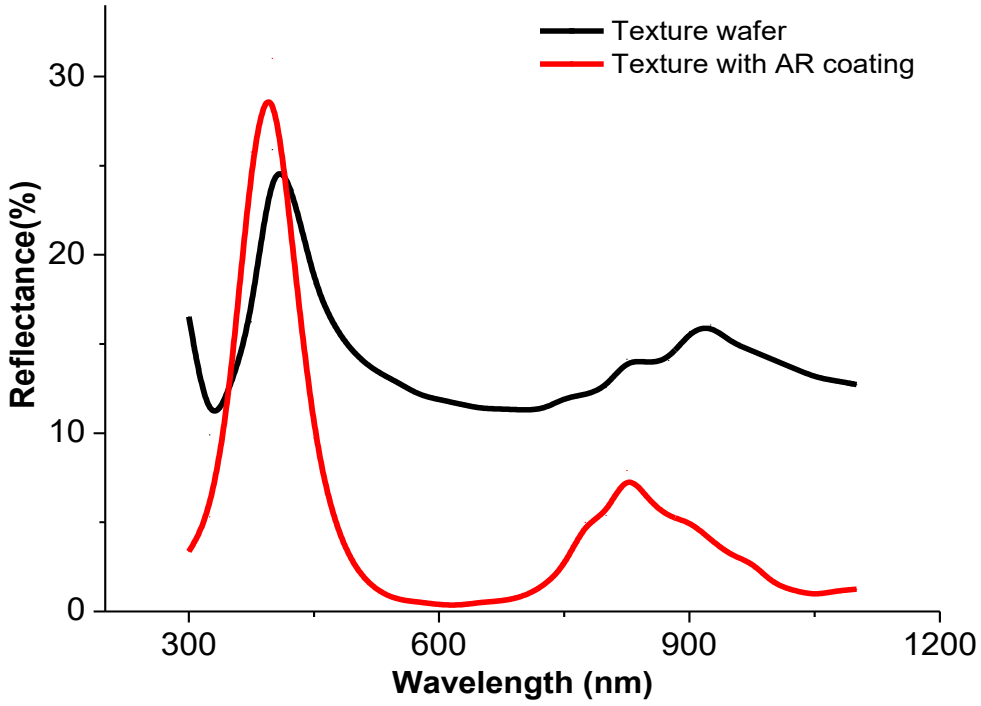

Figure 3.29 Reflectance of measurements of texture wafer and texture with Antireflection layer

Front surface of wafer after AR coating is shown in figure 3.30 , while back side of wafer have diffused aluminum after 3 hours of drive-in. Wafers are ready for further processing, for photolithographic step.

Figure 3.30 Front and back side of silicon wafers after drive-in and AR coating.

3.10 Frontal metallization (By photolithography)

In P/Al technology, for front metallization we have used more sophisticated and highly efficient photolithographic technique. For industrial fabrication of silicon solar cell, usually used screen printing technique for front as well as back contacts. To obtain maximum process reliability in photolithography, substrates should be clean and dry prior to applying the photoresist. Process is Started with the wafers cleaning, or a rinse with deionized water. A photoresist (resin) is a light sensitive polymeric material used in several industrial processes and in photolithography to form a patterned coating on a surface for fabrication of solar cell and electronic devices [48]. Systematic procedure for front metallization is shown in figure 3.35. Photoresist is synthesized to produce low defect coatings over a broad range of film thickness. The film thickness is related to spinning speed of spin coating machine, it is very important to control the spinning speed in order to achieve the desired film thickness. [49-50].

3.10.1 Recommended coating conditions:

(1) **Static dispense:** Approximately 5ml (130-140 drops) of resin (photoresist) for 125×125 mm (4.9×4.9 inches^2) of wafers area.

(2) **Spread cycle:** Ramp to 100 rpm acceleration for 30 seconds but at the end we did not used this spread cycle.

(3) **Spin cycle:** Ramp to final spin speed at an acceleration of 1500 rpm for 50 seconds

(4) **Heat treatment (Prebake step):** All wafers after photoresist deposition were dried in oven at 95 ^{0}C for 15 minutes. We adjusted the tray in furnace and we introduced the wafers inside the furnace by using carriers and kept these wafers in oven for heat treatment and polymer stabilization. For heat treatment, turn on the oven at least couple of hours before prior to use. Wafers containing photoresist are normally heated in oven at already fixed temperature of 95^{0}C for 15 minutes for solidification of photoresist. Make sure that temperature of oven remains fixed during introducing wafers in and out. Higher temperature or over heating may destroy or decompose the photoresist (resin) [49-50].

3.10.2 Photolithographic step (Expose to light)

The mask used for front contacts metallization by using photolithography is already designed by our research group and it consists of specific pattern of 9 cells with dimension of 2X2 cm^2 cells for 125X125 mm^2 wafer. Each cell has different width of fingers and distance between them. Picture of photolithographic machine is shown in figure 3.31.

Figure 3.31 Photolithographic machine used in photolithographic step for front contacts.

The mask is placed in mask holder and locked the mask holder, locked the keys/clamps which is used to tight the mask and to make ready for processing. Wafers were placed in a carrier for photolithographic step.

Adjustment of the mask in mask holder is done in such a way that wafer and mask had a minimum distance. Exposure time is adjusted by hit and trial methods by doing some experiments in order to control the width of fingers. We finalized exposure time 45 seconds. With exposure time 45 seconds we had a fingers width 28µm while in mask we have 25 µm. Which is more or less similar with mask design, so 45 seconds is recommended time for exposure time (photolithographic step). By the increasing exposure time, we observed degradation of photoresist (polymer) and width of fingers were increased.

After photoresist deposition and heat treatment, this photo sensitive polymer layer is exposed to UV light. A photomask is used as patterning template leaving an image on the photoresist. Photoresist is optimized for near UV (350-400nm) exposure. Photoresist is virtually transparent and insensitive above 400nm but has high actinic absorption below 350nm. Excessive dose below 350nm may result in over exposure of the top portion of the resist film, resulting in exaggerated negative sidewall profiles. The optimal exposure dose depends on film thickness (thicker films require higher dosage) and process parameters. Normally expose time 30–60 seconds. Recommended exposure time is 30-45 seconds which are based on previous experience.

3.10.3 Development of photoresist:

After photolithographic step, pattern development was carried out in developer solution for 1 minute developing time and1-3 minutes cleaning time. The solvents which are used for development purpose mainly depends on the type of photoresist. Chemical supplier

also supply developer solution for the development of photoresist. Recommended developing time is one minute but it also depends on concentration and type of developer. During development, image of mask is produced in the photoresist, which is transferred on the wafer surface. These layers are then etched to form a permanent pattern in the film. It is a simple method for patterning films that are deposited on wafers. A pattern is defined on a substrate using photoresist. A thin metallic film which is deposited by using electron beam machine is deposited all over the photoresist as well as images produced after development of photoresist. Wafers after photoresist development is shown in figure 3.32.

Figure 3.32 Image of wafer after development of photoresist

Metallization was carried out in following order by using three different kind of metals whose detail is given in table 3.8. Before deposition of metals, wafer were treated with HF to remove the silicon nitride under the contacts areas. (To remove the oxides, silicon nitride and make the surface hydrophobic in 5-7% HF)

Table 3.8

Metal	Vacuum	Voltage (kV)	Current (mA)	Tooling factor (%)	Thickness (A^0)
Ti	5×10^{-5} Torr	6.5	50-120	45	500
Pd	5×10^{-5} Torr	5.5	50-70	45	200
Ag	5×10^{-5} Torr	6.5	40-60	45	1000

3.10.4 Liftoff of photoresist

Acetone treatment for 2-4 hours
Isopropyl alcohol 5-10 minutes
Deionized water 2-5 minutes

After metals deposition, liftoff step was carried out to get front contacts. For liftoff process we used acetone as solvent. During lifting-off process the photoresist under the metallic layer is removed with solvent taking the film with it, and leaving only the film which was deposited directly on the substrate where photoresist was already removed by developer after photolithographic step. Selection of the solvent for lift-off process depends of type of photoresist. Different solvents or mixture of solvents have been reported in the

literature. After liftoff process we had metallic fingers on wafer surface according to mask design but resolution is not same as we have in mask used. Lift-off process can be accomplished by immersing in acetone. The time duration for lift-off depends on the quality and thickness of metallic film. At least 2-3 hours are necessary to complete lift off process. At the end wafers were cleaned with isopropyl alcohol and de-ionized water before drying [51].

Photoresist (resin) which we used in our experiments was soluble in acetone. Acetone not only liftoff photoresist but also metals deposited on photoresist layer except fingers area. This process took more than three hours to remove the photoresist with metals. In our experiments, we used photoresist which were expired couple of months ago, we had some problems in liftoff due to expired date. Due to this reason, our liftoff was not only time consuming but also destroying silicon nitride layer, we had problems in liftoff, even it took longer time and poor cleaning of photoresist which resulted small silver spots on wafer surface.

- Deposition of resins (photoresist) on wafers must be carry out in dark room because photoresist is sensitive to light.
- Open the valves of all gases necessary for photolithographic machine and turn on the photolithographic machine at least 15 minutes before the processing.
- Adhesion of the deposited film on the substrate should be very good.
- Photoresist film can be easily wetted by the solvent for liftoff process.

Overall front metallization process by using photolithographic technique is shown in figure 3.33. It is considered as a laboratory technique for front metallization, in industry metallization is carried by screen printing technique.

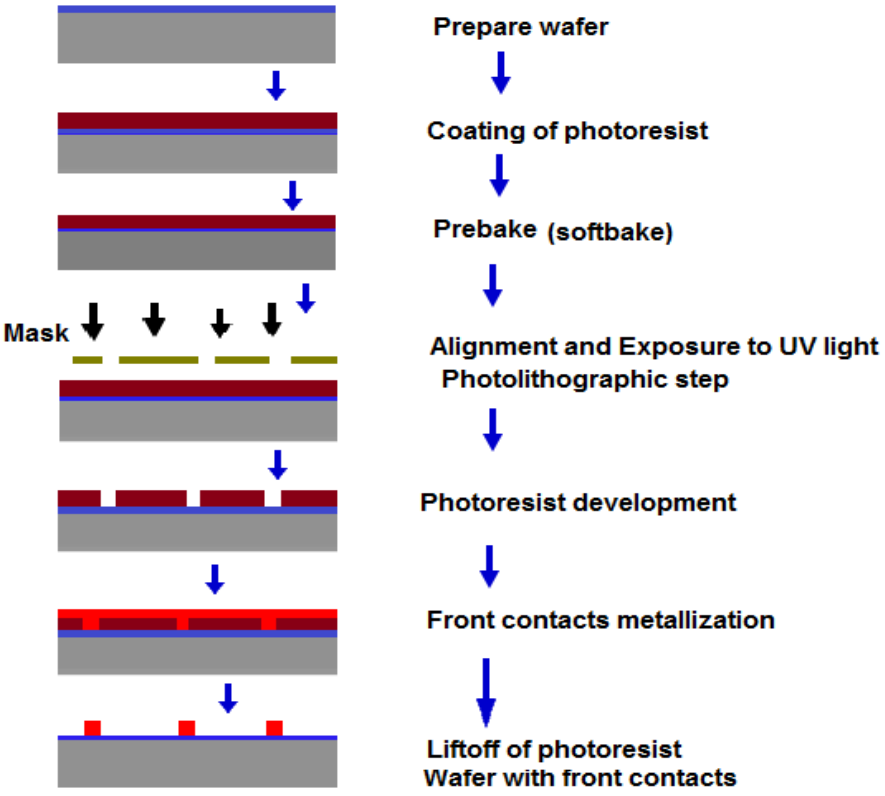

Figure 3.33 Front metallization process by photolithography.

3.11 Electroplating or electro-deposition

Electroplating is a metal deposition process in which metal ions in a solution are transferred by an electric field to coat an electrode connected metal growing area. The process uses electrical current to reduce the concentration of cations of a desired material from a solution and coat conductive object with a thin layer of the material, such as a metal. Electroplating is primarily used for depositing a layer of material to bestow a desired property to a surface that otherwise lacks that property. Other application of electroplating is grow thickness of undersized parts. In our work we used electroplating to grow silver on silver fingers to get desire thickness of silver fingers (5-8µm).

Conditions for electroplating process:

Anode: 99.9% pure silver anodes is used.
Anode/cathode ratio: 2:1 anode to cathode ratio is required.

E-Brite 50/50: It is supplied as a liquid concentrator, which contains 4 oz/gallon of silver. Concentration of E-Brite 50/50 is diluted with D.I. water. It is an alkaline, cyanide free plating solution, which can plate bright silver for electronic, industrial and decorative uses. It operates at room temperature and can be utilized in both rack and barrel plating.

E-Brite 50/50	50%
Deionized water	50%
pH	8.8, (range 8.5-9.5)
Temperature of bath	68-72°F (20-22 ^{0}C)
E-Brite 50/51 electrolyte	5%
45% KOH solution to adjust pH to 9.0	
50% Nitric acid to decrease pH	

It is very important to operate E-Brite 50/50 at pH range 8.8 to 9.5. If pH is below than 8.8, we have to adjust it with KOH. If pH is over than 9.5, we have to adjust it with 50% nitric acid.

E-Brite 50/51 electrolyte is added on a regular basis to complex the silver dissolved from the anodes. Additions of E-Brite 50/51 are made based on ampere hours, Hull Cell tests or as recommended by EPI. Typically 1% of E-Brite 50/51 is added every day to the solution used for silver plating and the pH is adjusted to 8.8 to 9.2. If silver is not plated on a particular day. Use a 1-micron filter to take out small particles in the bath. Continuous carbon filtration or normal paper filtration of the bath is required even when the bath is idle before using. The solution must be kept free from suspended matter (material) in order to prevent roughness. Continuous filtration with 2 micron carbon filter is recommended. We do not have this facility and used simple filtration using filter paper. It removed the micro and suspended particles and it could not remove the turbidity.

Took the filtered with maintained pH electrolyte solution in plastic tray, adjust the wafers inside the apparatus and connect the power supply as shown in the flow sheet or real figure. Take care during adjustment of wafers on platform. Use voltmeter to adjust the voltage supply to the system. Electroplating process takes 3-5 hours' time depending on the number of cells to be plated. It also depends on concentration and pH of solution. After the electroplating process rinsing is important process to get neat and clean surface. Rinsing is followed cold and hot deionized water. In some cased with 10% dil. H_2SO_4.

In our work, we used electroplating to grow silver on silver finger to get desire thickness of front contacts (5-8um). The results of electroplating are quite different under same

experimental conditions; even fingers have a variable thickness. We are still optimizing experimental conditions to get desire thickness with uniformity.

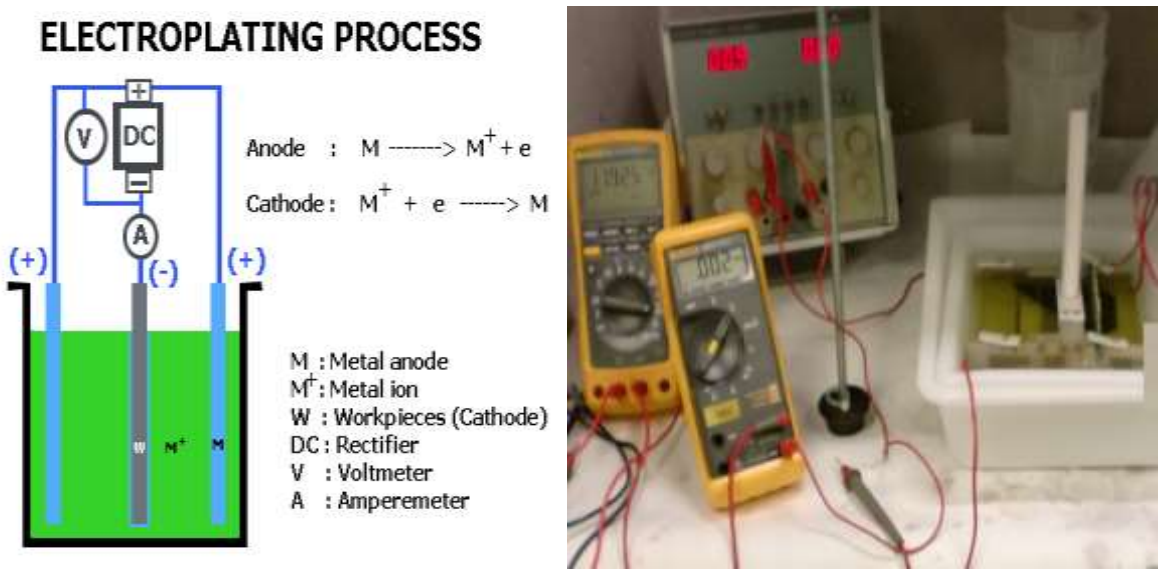

Figure 3.34 Electroplating process for front contacts growth (Ag electroplating)

The metals which were deposited by EBM, were in nanometers scale, it was difficult to extract current by these thin fingers and busbar. Electroplating process helped us to grow the finger thickness and height to extract the current easily. Fingers height were in range of 6-10µm and width was in 25-35 µm after electroplating. Their thickness were measured by using optical microscope by focusing on the top of fingers and on the base of bottom area of fingers as shown in figure 3.35 [52].

3.11.1 Characterization of Electroplated cells.

After electroplating, their thickness were characterized under microscopic study.

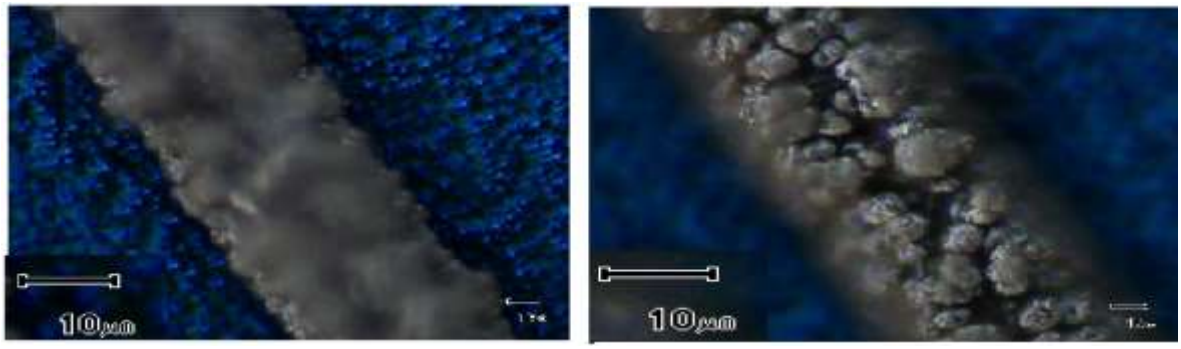

Figure 3.35 Thickness measurements of fingers grown by electroplating

We can also calculate the thickness of finger after electroplating by using following equation 3.9;

$$h = \rho_{Ag} \frac{l \times I}{W \times V} \qquad (3.9)$$

While h= height of finger (to be calculate), W= width of finger, l= is length of finger

"I" = applied current to finger. ρAg =specific resistance of silver (1.59E-8Ω.m) and V= voltage to be measured. Flow sheet of measuring apparatus which is called 4 point contacts measurements is shown in figure 3.36. Length and width of fingers can be measured easily by optical microscope. Height which is in few micrometers, can we measure by using equation 10. [52]

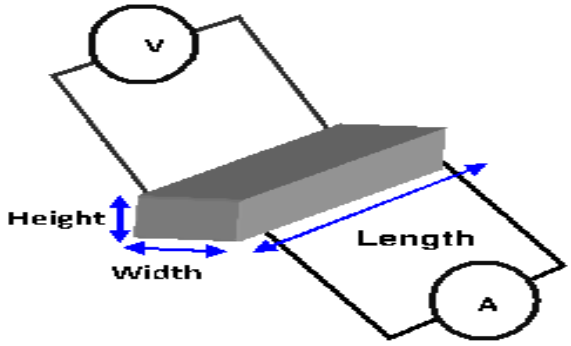

Figure 3.36 Thickness measurement procedure of finger by 4 points current voltage apparatus.

3.11.2 Drawbacks:

Electroplating electrolytes are alkaline in nature. Due to alkalinity of chemicals, it starts etching the surface of AR coating (silicon nitride), even etching rate is slow but due to long electroplating time surface is affected by chemicals. Scratches are appeared on front surface of the cell. Secondly, due to etched AR coating, Ag is deposited among the fingers as shown in figure 3.37. It strongly effects on performance of solar cells.

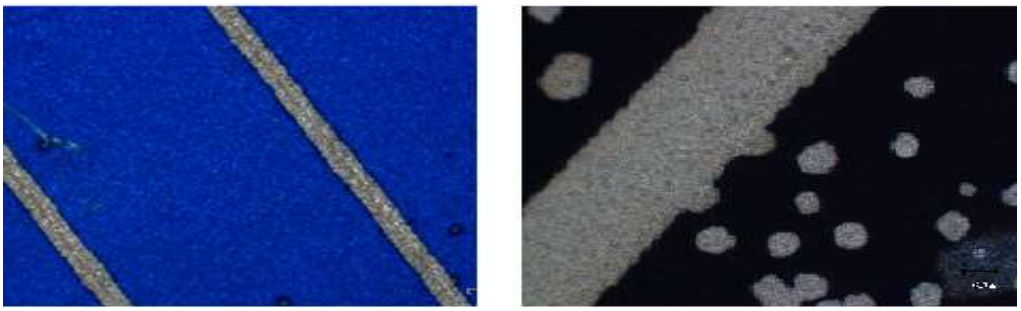

Figure 3.37 Optical microscopic images of electroplated cells. Cell (b) is over electroplated and Ag is deposited among the fingers.

3.12 Metallization (Back contacts)

For back contacts, a layer of aluminum and silver were deposited on back side (rear face) of wafers by using electron beam machine. Same procedure was adopted as it was adopted for aluminum or other metals deposition by using electron beam machine. Conditions for evaporation and desire thickness is mentioned in the table which is given below;

Metals	Vacuum (Torr)	Voltage (kV)	Current (mA)	Tooling Factor (%)	Thickness (A^0)
Al	5×10^{-5} to10^{-6}	7	120-220	45	1000
Ag	5×10^{-5} Torr	6.5	40-60	45	1500

On backside of wafer, second layer of aluminum acts like a mirror which reflects back all unabsorbed radiation to silicon wafer for further absorption.

3.13 Forming gas annealing

Forming gas annealing (FGA) is an effective process to repair low efficiency crystalline silicon solar cells. The major effect of forming gas treatment on solar cell performance is the fill factor values, which increase from 3 to 8%. It also effect on internal quantum efficiency, it confirm that hydrogen passivation has become most important in photovoltaics and microelectronics. Forming gas annealing treatment is carried out in P/Al solar cell by using N_2/H_2 (95%:5%) for 30 minutes at 450 ^{0}C by using following procedure.

Table 3.9

Step	Gases flow at 450^{0}C	
Turn on the furnace 1st step	$N_2 + H_2$ 6*l*/min +	(20 minutes)
Wafers in (after 20 minutes)	$N_2 + H_2$ 6*l*/min	(30 minutes)
Turn off the furnace (after 30 minutes)	$N_2 + H_2$ 6*l*/min	(90 minutes)

It is a low cost process used for hydrogenation purpose to improve the surface damage due to high temperature processes during diffusion or deposition techniques. In forming gas annealing, hydrogen gas interact with impurities at appropriate temperature to enhance conversion efficiency in silicon solar cells. Passivation effect of hydrogen gas is used to improve the grain boundaries of crystalline silicon to improve the efficiency. As we have mentioned early major effect of forming gas annealing is to improve the fill factor, which can be increase up to 8%. In some case 15% of hydrogen gas is used in forming gas, improvement in efficiency was observed in case of higher percentage of hydrogen use. During annealing process, dissociated hydrogen diffused rapidly in region of low oxides (having low concentration of oxygen at surface). Damages produced by impurities in phosphorus diffusion depends on P concentration. High temperature diffusion of P helps the diffusion of hydrogen deeper in the junction. PECVD during passivation also damage the silicon surface. It is proved that FGA improves the lifetime of silicon solar cell. Results and observation made by some researchers show that FGA only improve the lifetime and surface damage when there is a junction. It is mandatory to have n+ junction in order to observe the improvement in lifetime [53-56]. Forming gas Annealing have two benefits, first it produce good alloys between different metals, as a result series resistance of the cell decrease and second is that it recovers the damage produced at the surface by electron beam and x-rays during metals deposition process. [53-56].

3.14 Isolation of solar cells by laser:

Laser micromachining processes being used in monocrystalline and polycrystalline solar cells include laser edge isolation, laser micro via drilling, laser fired contacts, and laser surface structuring as well cutting of wafers and . All of the above mentioned machining technologies have a guarantee for high efficiency of the complete solar cell at a minimum of materials damage and least material's loss. For the achievement of high opto-electronic efficiency, differently doped front and rear sides of crystalline solar cells need to become isolated at the edges. There are two kind of laser one is green which works in visible region and other red laser, works in IR region. Green laser of visible region has a wavelength 515nm use for cutting of wafers and edges isolation. Silicon wafers are conventionally diced

off by a thin diamond blade, currently green wavelength with milliseconds low power pulsed fiber lasers and high beam quality continuous wave fiber lasers are being used to cut these materials. The cut quality is poor and micro cracking can occur due to excessive heat input, which can lead to failure of some components during process steps and associated reduction in yields. [57]

3.14.1 Laser Description:

Different parts of lasers are shown in figures 3.38. For operation we used computer program Ast06. For proper functioning we have to adjust scanning speed which is from 20 to 3000mm/sec and pulse repetition frequency 10-200 kHz and power is variable under different conditions. The laser system which we have used in our experiments, consists of a Q-switched fiber laser, which generates pulses of 10 ns duration, Gaussian beam, working at two wavelengths (infrared, IR, λ_1 = 1030 nm and green, GR, λ_2 = 515 nm). We have used green laser, which is more efficient than IR laser.

We have used following parameters for cutting of cells:

Laser frequency: 50 kHz
Laser power 34.2 A
Scanning velocity 500 mm/sec
No of scan= variable (2-8)

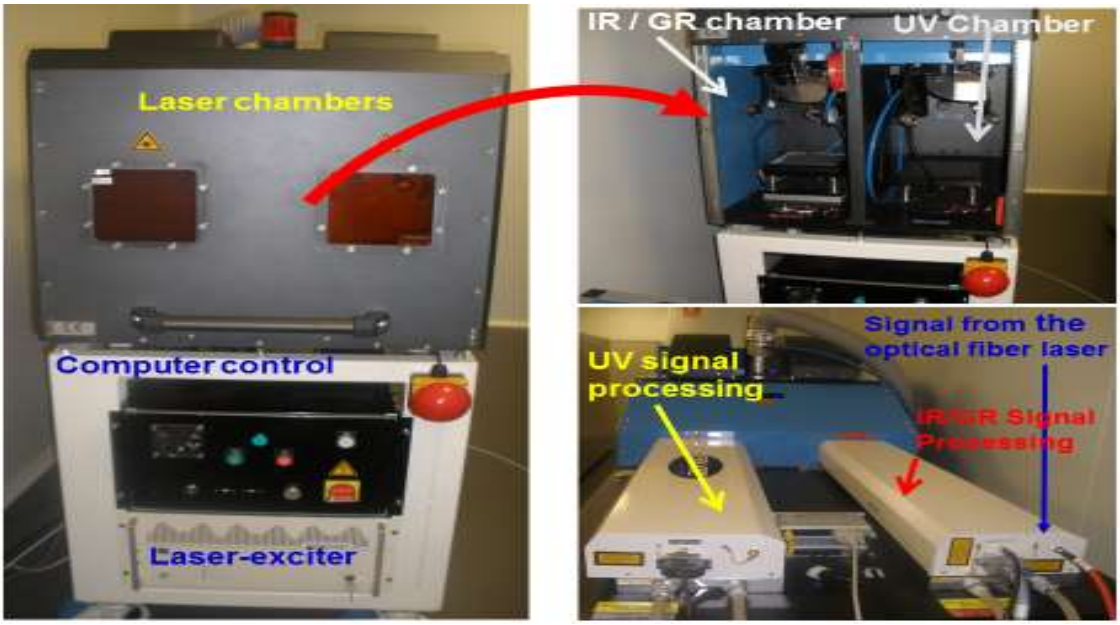

Figure 3.38 Description of laser (Different parts of laser is shown in figure)

By using laser, we have isolated different cells of area 2×2 cm^2. Although laser is advance and fast technique for processing and cutting but it has some disadvantages, in some cases we observed that due to melting of silicon by laser, silicon starts depositing on the edges of cells which cause in shunt conductance.

We have observed through optical microscope that silicon and aluminum due to laser energy, melted Si or Al, which is deposited on edges, even in some case it was in contact with backside. This process decreased short circuit current.

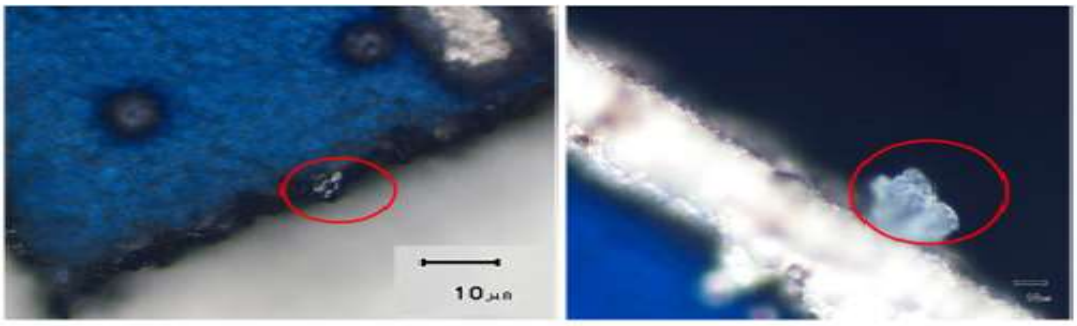

Figure 3.39 Due to laser energy, Melted Al cause a shunt conductance

After laser cutting/isolation, cells of 4 cm^2 area are obtained, pictures of some cells are shown in figure 3.40.

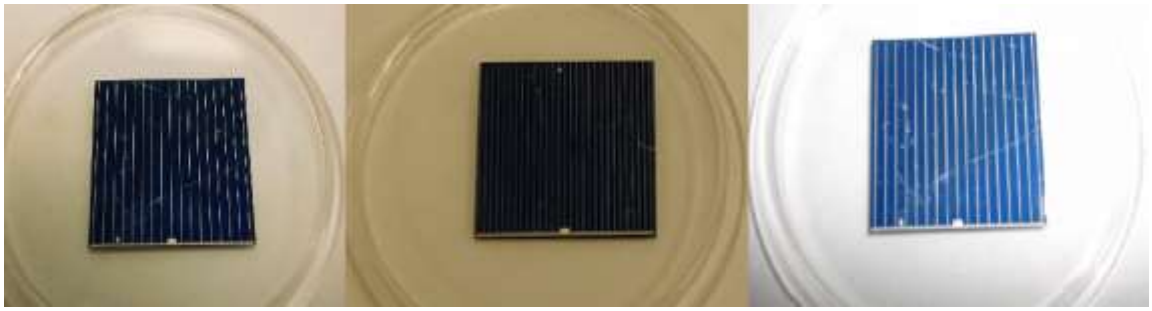

Figure 3.40 Real pictures of solar cells with area of 2x2 cm^2

Description of P/Al silicon solar cell structure with respect to thickness of different layers is given in below in figure 3.41.

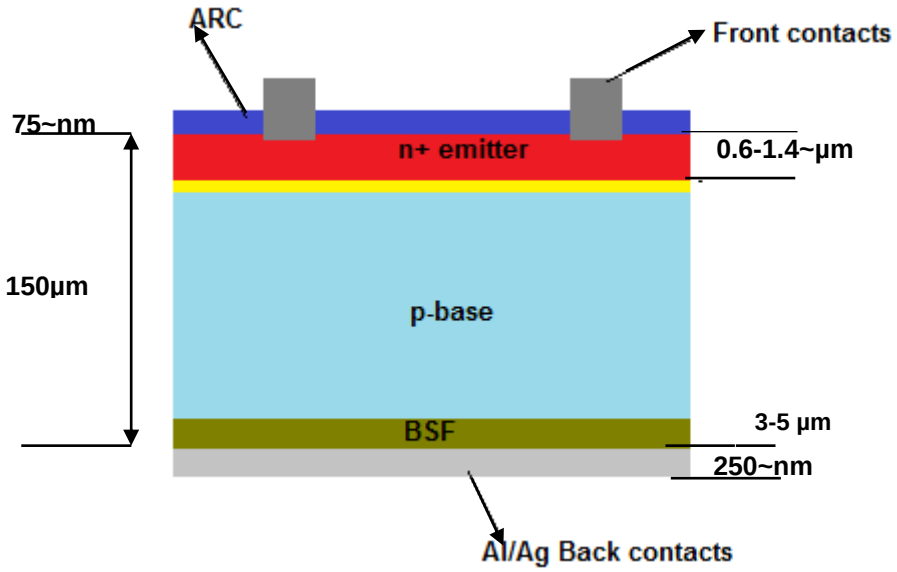

Figure 3.41 Thickness description of solar cell fabricated by P/Al technology

3.15 Characterization of P/Al solar cells

In solar cells fabrications, it is necessary to characterize solar cell during fabrication process. There are many destructive and nondestructive techniques which are used to analyze fabrication steps and performance of solar cell.

There are two/three of characterization techniques:

Electrical characterization

Optical characterization

Electro-optical characterization

In electrical characterization, there are 3 basic measurements which are used to characterize solar cells, which are as follows:

- IV curve under illumination, where cell is illuminated at one sun and basic parameters are measured
- Dark IV curve, where the cell is in under dark condition and IV dark characteristics are measured.
- *Jsc* (*Isc*) and Voc are also recorded at different illumination.

These three measurements consider as one technique because above three measurements are measured together and curves are plotted in same graph. Solar cell parameters are extracted from these curves. Details of these techniques are already discussed in chapter 2. In this part we will focus on instrumentation and measuring procedure for IV characterization.

3.15.1 IV Curve measurement System

The system, which we have in our institute for measurement of IV curve, is valid for both small size as well as large size solar cells. It consists of solar simulator with a xenon lamp as source of light. It is fixed at approximate air mass 1.5. As shown in figure 3.42.

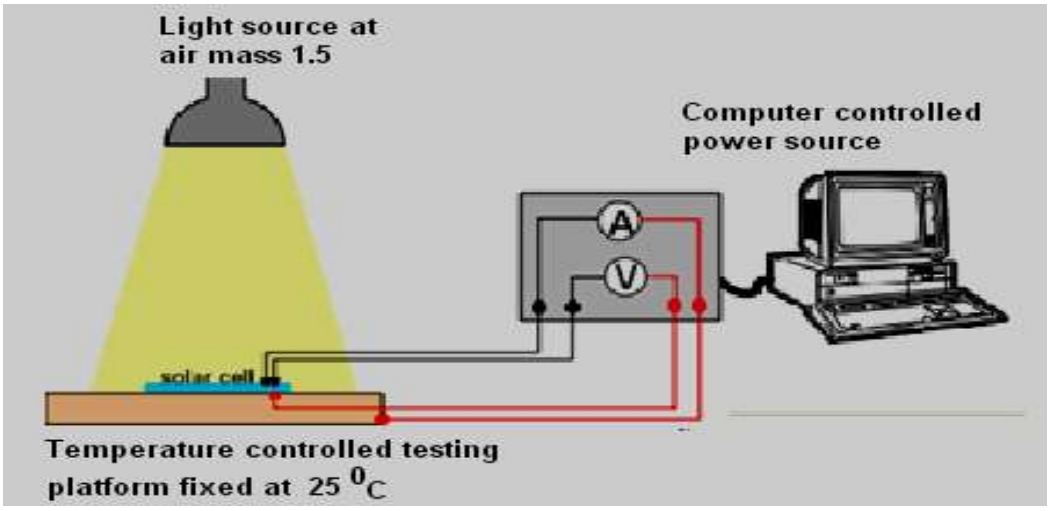

Figure 3.42 Schematic diagram showing Measurement system for IV characteristics

The system (equipment) whose picture is shown in figure 3.43.

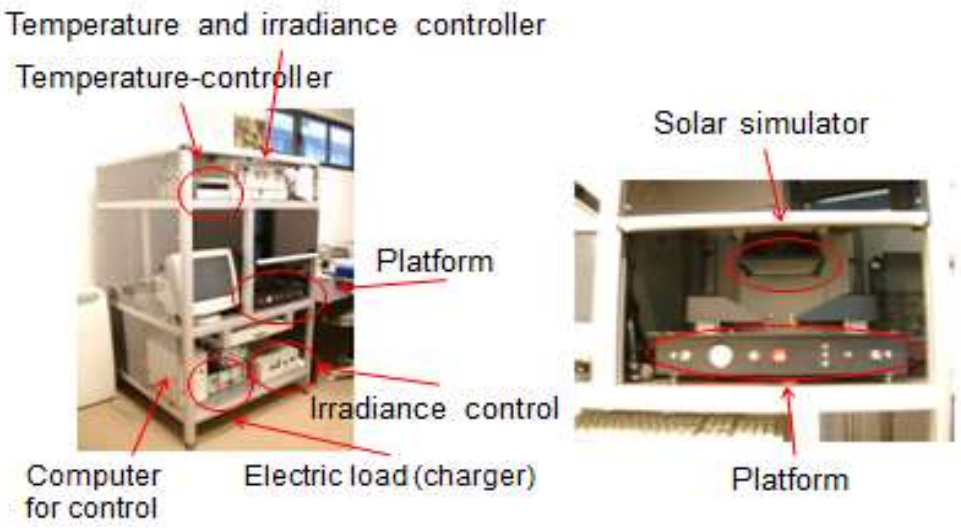

Figure 3.43 Solar simulator systems

In solar simulator there is an artificial source of sun light from solar simulator lamp which has xenon lamp attached with various filters and connect with power source. This system is accompanied by a program (Solar TiM) developed in our institute for the operation of solar simulator and automatic measurement of IV curves. Main screen of program is shown in figure 3.44 [58-59].

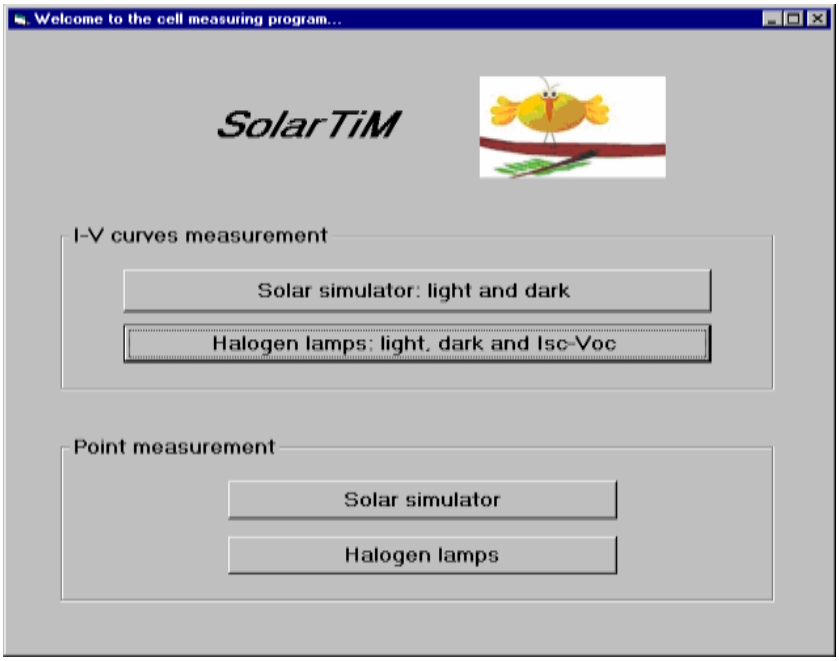

Figure3.44 Principal Screen of the program

By using this program, we can select procedure for desire measurements but usually we used solar simulator (light and dark) for measurement. After selecting the solar simulator, second screen of program appears, where we have to fill the information about our cell (emitter type, active and total area etc). In this way we can measure both dark and illumination IV curves in short time. Measurement results appear in the form of data which is shown in figure 3.45 [1-3].

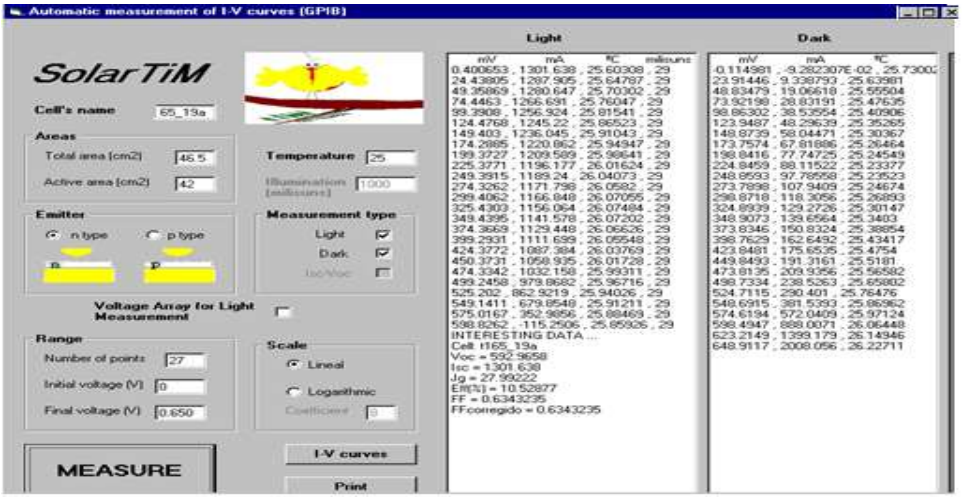

Figure 3.45 Screen for IV curve measurement data of solar cell by solar simulator

From the data, which appears on the screen we plotted IV curve and calculated efficiency and fill factor. IV curve plotted by solar simulator is shown in figure 3.46. We also have other relevant information about short circuit current and open circuit voltage. [58-59].

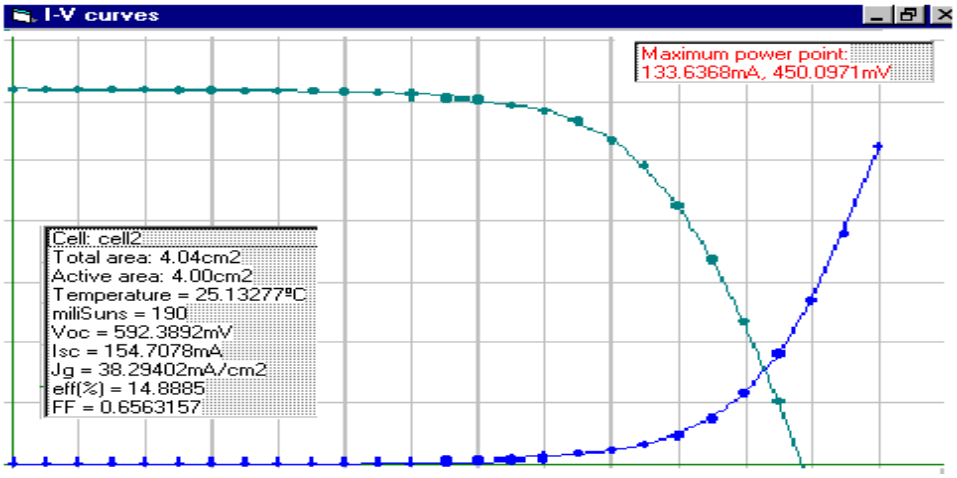

Figure3.46 IV curves measured with solar simulator

Furthermore, the data which we have obtained from solar simulator appears in the forms of 3 files, each file has specific information about data of IV curve under illumination, under dark and solar cells measuring parameters (such as total area of cell, active area and temperature of platform). These files are further processed by using fitting program, MultiV (developed by faculty members of our institute TiM). By the fitting the curves of our data with standard curves, we can obtain electrical parameters of cell. In this way, we can extract all information about solar cell. MultiV data appear on screen in MultiV program is shown in figure.3.47 [58-59].

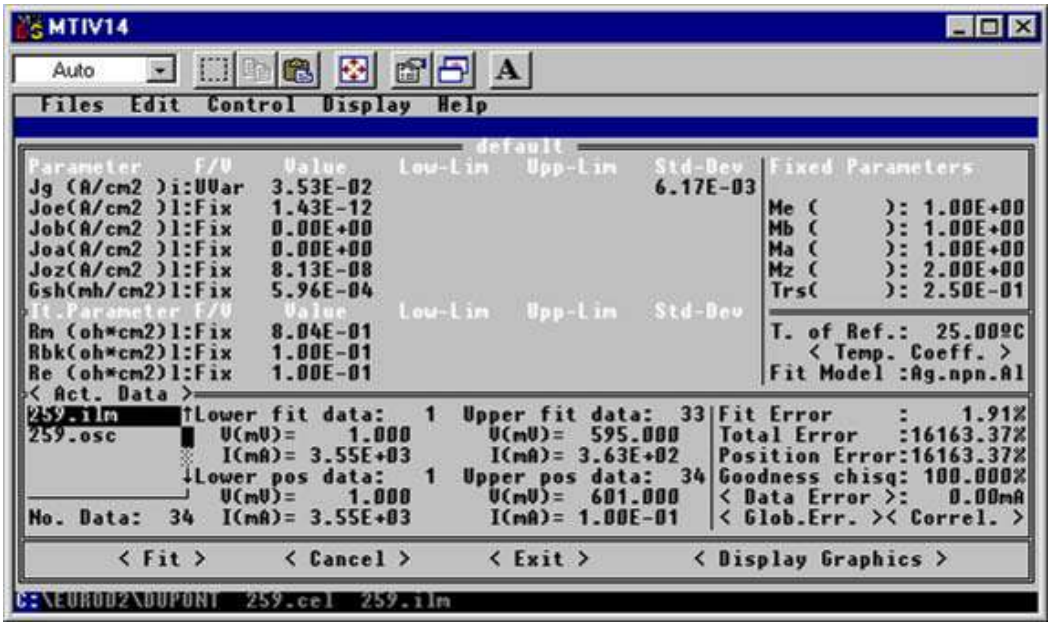

Figure 3.47 Screen of MultiV fitted data of Solar cell

By the using MultiV fit program, we have plotted I-V curves data of solar cell with MultiV program and graph is shown in figure 3.48. Spots (dots) represent our data, from solar cell and lines on the spots (dots) represent the fitting of data.

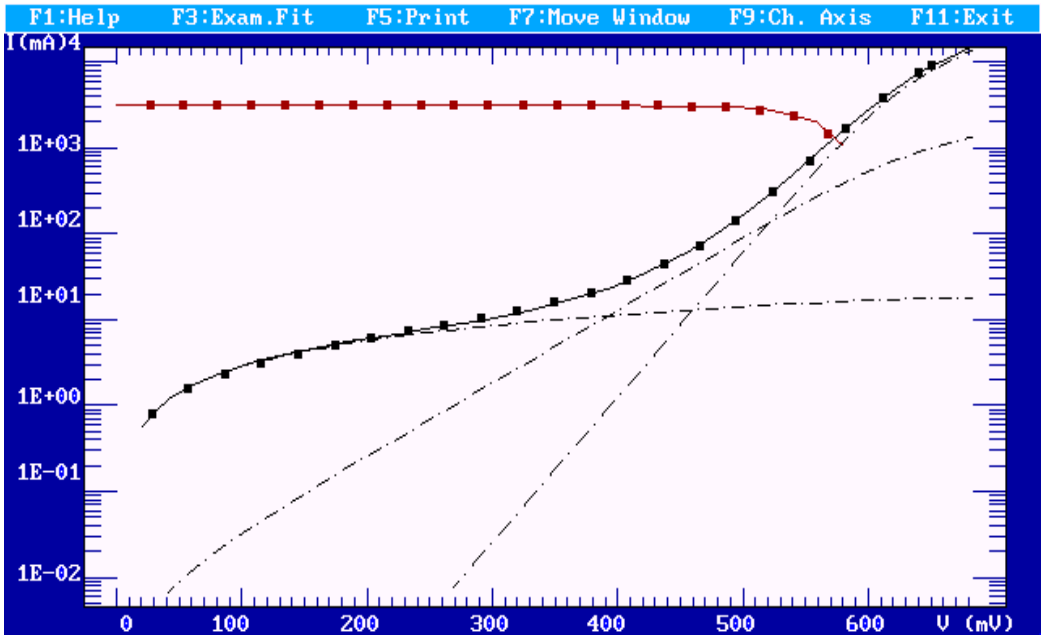

Figure 3.48 IV curves fitted with MultiV program

3.15.2 I V curve measurements and characterization of solar cell (batch1)

After laser isolation and cutting, IV characteristics were measured by solar simulator by using computer program. IV data which we have obtained after measurements are plotted in the form of IV curve and results are given in table 3.10. Graphs of IV curves under illumination and dark of first batch is shown in figure 3.49 and figure 3.50 shows the logarithmic plot of IV curve under dark.

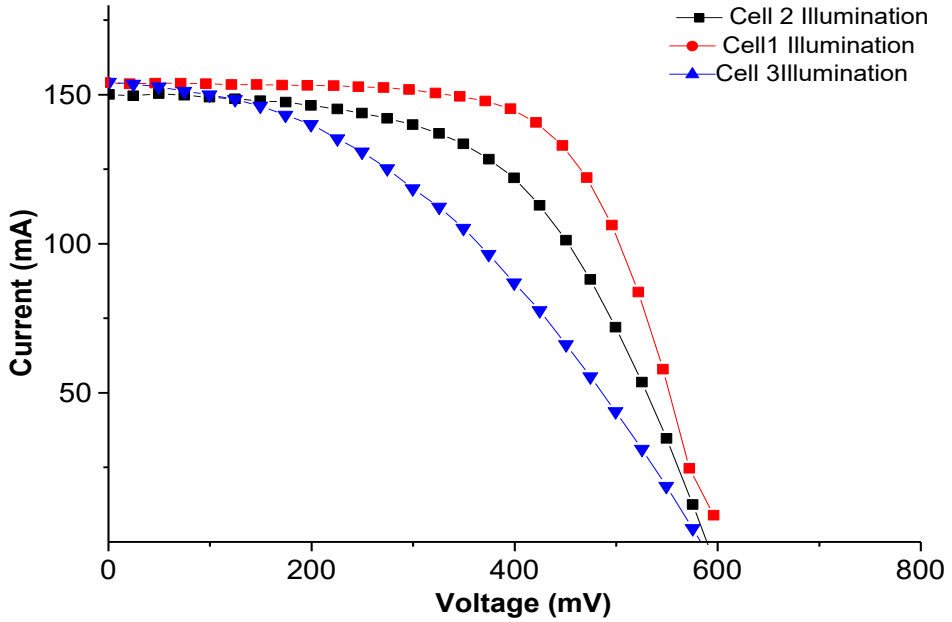

Figure 3.49 IV curves of P/Al solar cells of batch 1 under illumination conditions

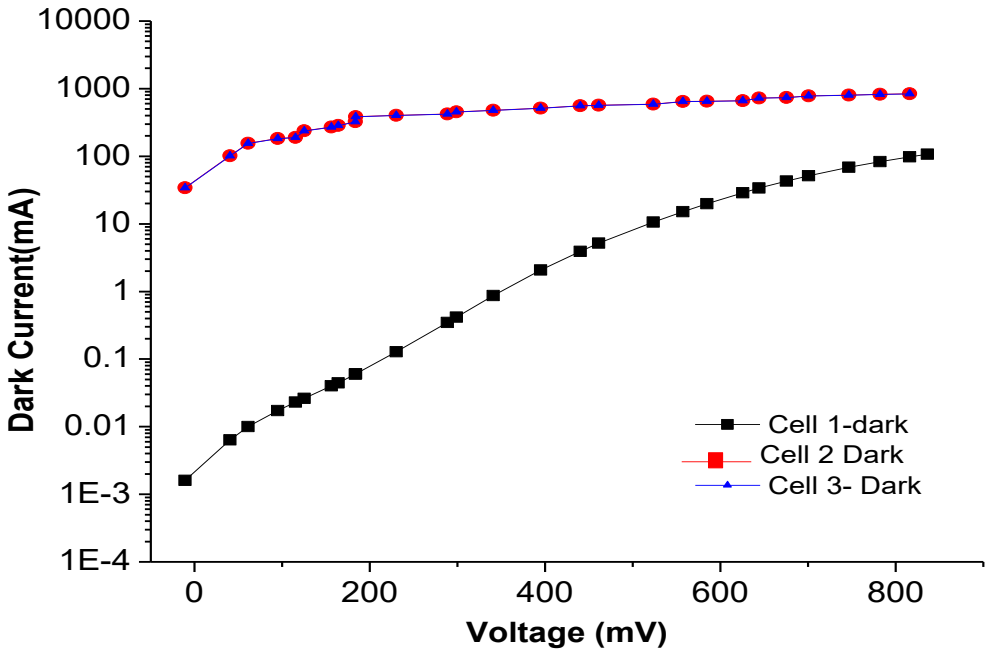

Figure 3.50 logarithmic plot of IV curve under dark conditions for P/Al solar cell.

Electrical characteristics which we have obtained from IV curves are shown in table 3.10. In this batch we have used 4cm^2 active area of solar cell.

Table 3.10

No.	**Cell 1**	**Cell 2**	**Cell 3**	**Cell 4**
Pmax. (mW)	52.43	60.14	36.54	48.95
Efficiency (η) (%)	12.85	14.74	8.95	11.99
*J*sc (mA/cm^2)	36.76	37.914	37.5	36.94
*V*oc (mV)	594.76	603	598.89	598.94
FF	0.60	0.67	0.41	0.56

3.15.3 Sun-Voc Measurements and Characterization

This measurement is very similar to IV measurement except Jsc, Suns-Voc uses a separate solar cell to monitor the illumination intensity of the solar cell instead of Jsc. Suns-Voc curve allows us to characterize lifetime of minorities carriers and its analysis also provides detailed information on the internal components of recombination in the solar cell. Sun-Voc measurements provide information of IV curves without the effect of series resistance of diode. Fitting of Sun-Voc curve is easier than illuminated curve since there is no dark current or series resistance. [60-61].

This measurement can be carried out with minimum extraction of current which are applicable for both structure with metals contacts or without metals contacts. This technique allows us to monitor the wafers and solar cells quality in early fabrication steps. System which is used to get data and curves is composed of a flash lamp with constant (specific) attenuation, a detector of illumination which are based on silicon photodiode and logarithmic converter, platform for measuring voltage and a micromanipulator to measure the voltage of open circuit structure. Flash lamp illuminates both the cell (to be measure) and detector, in this way voltage induced in both cell and detector are collected by an oscilloscope and transferred to computer. Measuring apparatus is shown in figure 3.51.

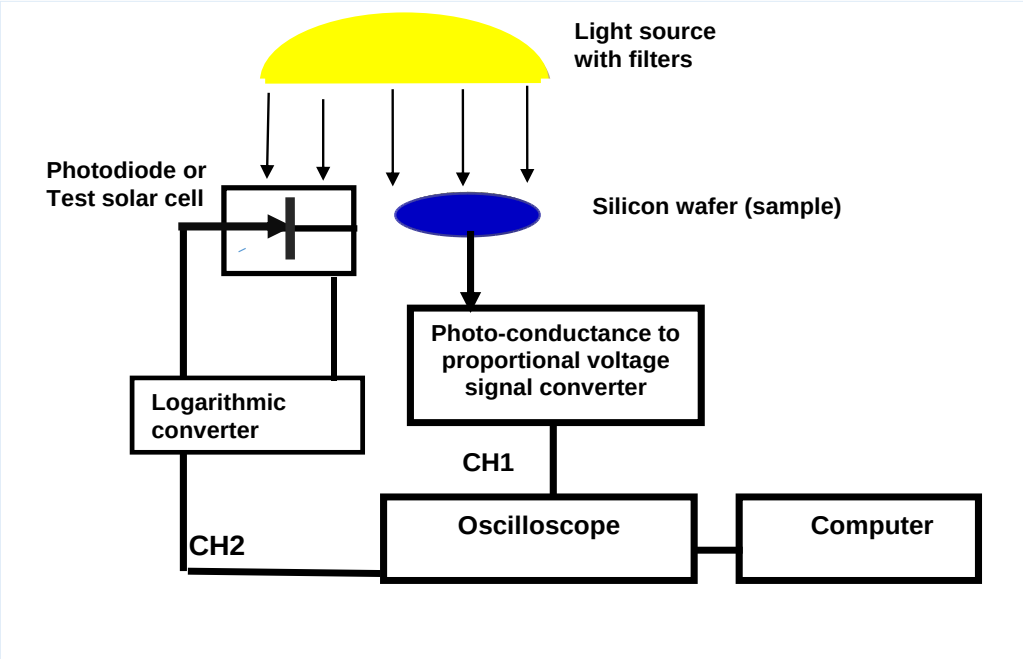

Figure 3.51 Schematic measurement system of Suns-Voc.

Measurements which are carried out by two different procedures. Frist is accomplished by slow decaying of light intensity, it can be considered as a quasi-steady statement measurement, (QSS-Voc). In our case we have two different kind of quasi-stationary phases, a flash with 2 different decay constants. For this measurement, we do not need to use coil or RF Bridge, we can measure directly from oscilloscope without any bridge adjustment. During this measurement, we do not only get the voltage but also get the diode parameters of solar cell (Joe, Joz Gsh and Rs) which is one of our objective of this measurement. These characteristic of solar cell are obtained by plotting Voc verse function of intensity of light. We do not measure electric current directly but this current is replaced by the intensity of light. A linear relationship exist between electric current and intensity of light which hold for most solar cell.

Second procedure in which illumination is reduced abruptly, this structures is considered as transient conditions. Where the decay of open circuit voltage is detected in dark. In order to process a collected data in each measurement, a template in excel has been created to extract the curves of suns-Voc, with applying the correction factors which are related capacitive associated effect of space charge zone. A reconstruction of Jsc-Voc curve by varying internal parameter of structure, we can obtain data/curves for Voc under one sun and effective lifetime depending on injection level. [62]. A graph of sun-Voc verses intensity of sun is shown in figure 3.52 and graph for sun-voc vs Voc is given in figure 3.53.

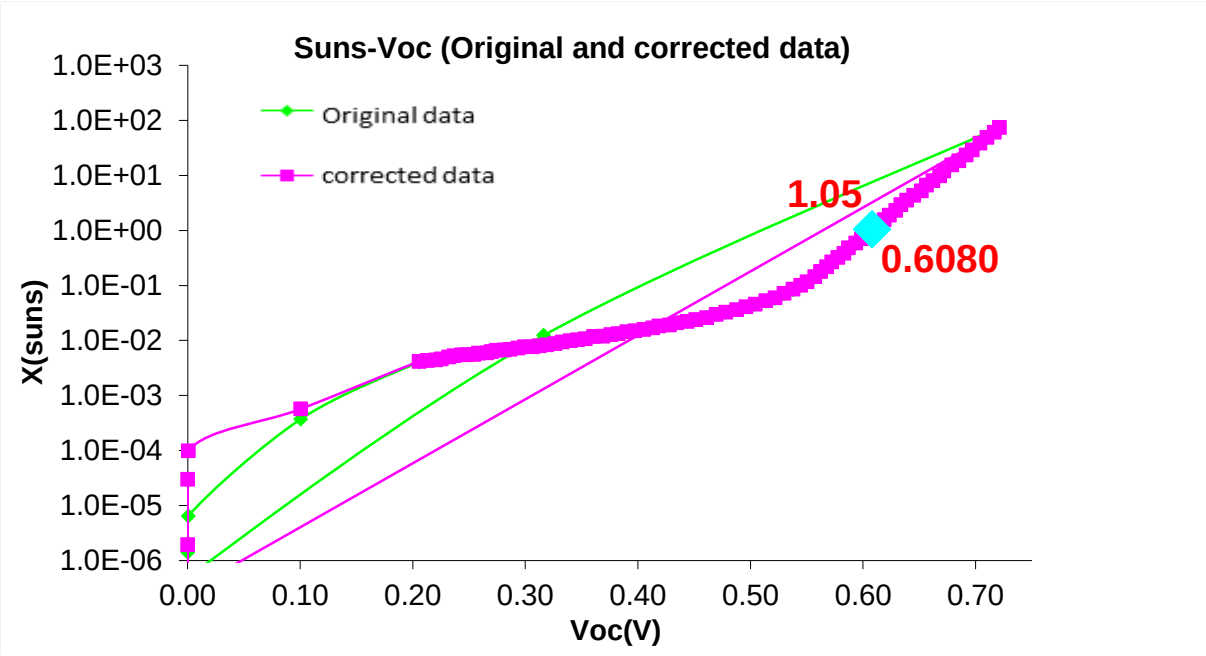

Figure 3.52 Graph of Suns verses Voc by suns- Voc measurement

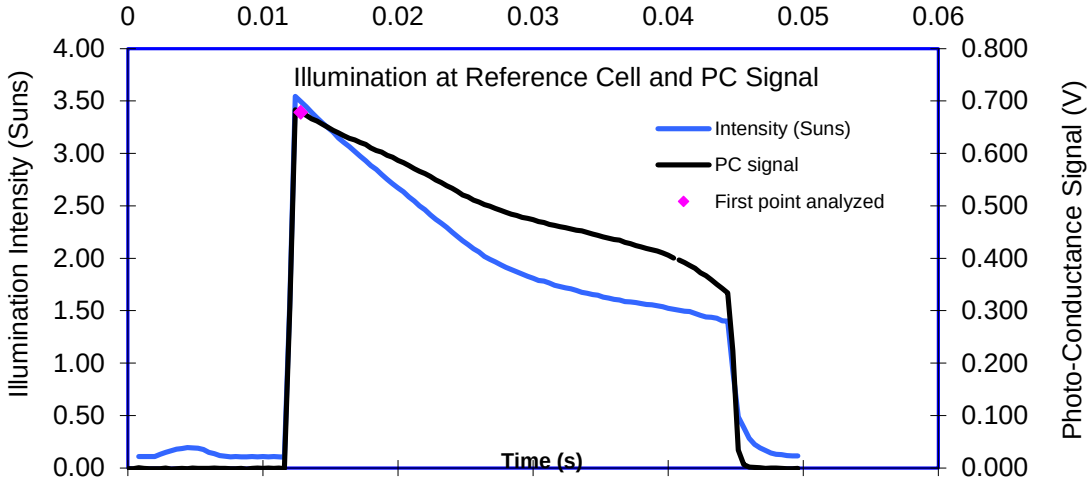

Figure 3.53 Illumination vs time from the flash lamp and right hand open circuit voltage of the wafer. Measurement system Suns-Voc.

Our objective to use Suns-Voc technique is not only to measure sun-Voc measurement but also use to extract solar cell diode parameters (Joe, Joz, Gsh and Rs) by fitting the curves of sun-Voc fit with our curve (real data). Graphical representation of sun-Voc fit is shown in the figure 3.54.

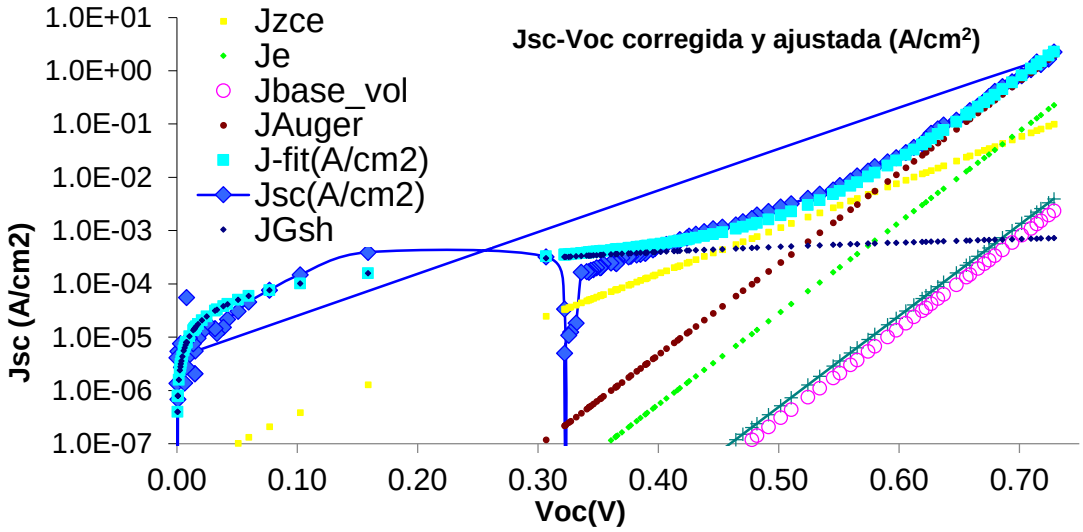

Figure 3.54 Sun-Voc curve fitting to extract solar cell diode parameters

P/Al solar cell parameters which are extracted from Multiv and sun-Voc measurements are given in table 3.11. Sun-Voc measurements are carried out with metal contacts.

Table 3.11

Parameters.	Cell 1		Cell 2	
	From multiv	From Sun Voc	From multiv	From Sun Voc
Gsh (ohm.cm^2)	4.73E-04	8.00E-04	4.21E-03	4.00E-04
Joz (A/cm^2)	1.68E-07	1.00E-08	2.10E-07	1.46E-09
Joe (A/cm^2)	1.00E-13	1.50E-12	9.06E-13	1.50E-12
Rm (ohm.cm^2)	4.00E-04		4.00E-04	
Voc (mV) IV curve	594.7		603	
Sun-Voc (1sun) mV	600.7		610. 9	

3.16 Fabrication of silicon solar cell by P/Al technology (Batch 2)

Fabrication steps which are used in standard P/Al technology for fabrication of silicon solar cells are given in the table 3.12, Fabrication process is same as it is mentioned early in this chapter. We have repeated this process to improve the fabrication process by investigation with respect to time. It is approximate time for fabrication of P/Al silicon solar cell.

Table 3.12: General* fabrication *steps:

Step No.	Step Name	Time consumption (in hours)
1	Etching + texturing	4 Hours
2	RCA (1&2) cleaning	4-6 Hours
3	HF treatment	20-30 Minutes
	"P" pre-deposition	3-4 Hours
4	Aluminum deposition	5-7 Hours
5	Drive in process P/Al	5-6 Hours
6	Antireflection coating (AR coating)	6-8 Hours
7	**Frontal metallization** (By photolithography)	
	Mask development	2-3 Hours
	HF treatment	10-15 Minutes
	Ti/Pd/Ag deposition (electron beam machine)	3-4 Hours
	Liftoff of photoresist	3-5 Hours
8	Electroplating process	5-6 Hours
9	Back side Al/Ag deposition Back contacts	4-5 Hours
10	Forming gas annealing	3-4 Hours
11	Isolation of solar cell by laser (cutting by laser)	3-5 Hours

Time which is given in the table 3.12 is for overall batch process, in each batch process we have used 10 wafers. Average time for each fabrication step is given in table 3.12.

3.17 IV characterization of P/Al solar cell of batch 2.

IV characteristics were measured by solar simulator by using computer program. IV data which we have obtained, are plotted in IV curve and results are given in table 3.13. Graphs of IV curves under illumination and dark of first batch are shown in figure 3.55 and figure 3.56 shows the logarithmic plot of IV curve under dark.

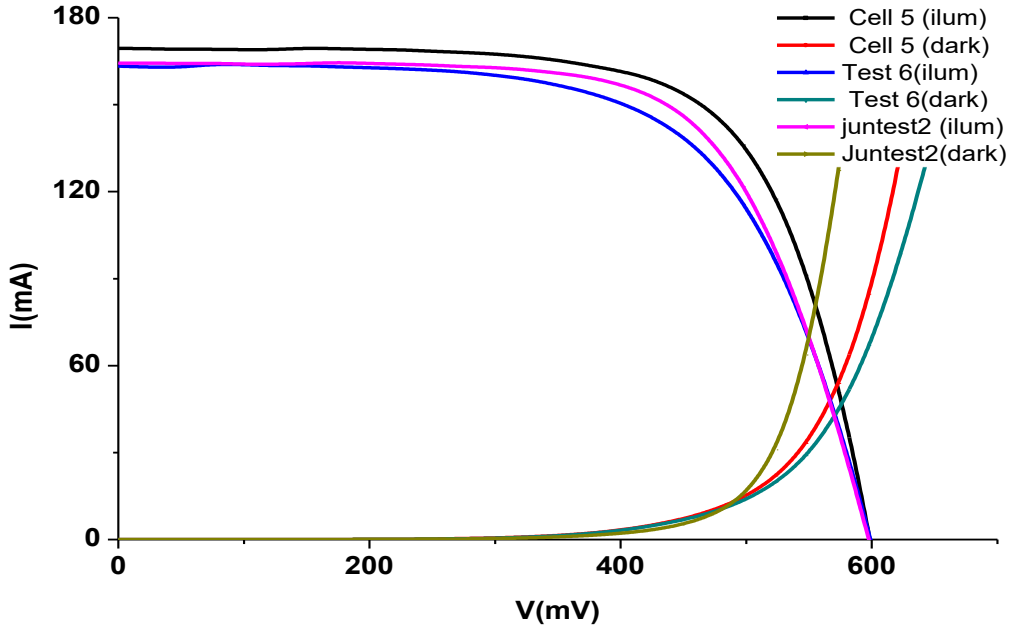

Figure 3.55 Illumination and dark IV curves of P/Al silicon solar cells (batch 2)

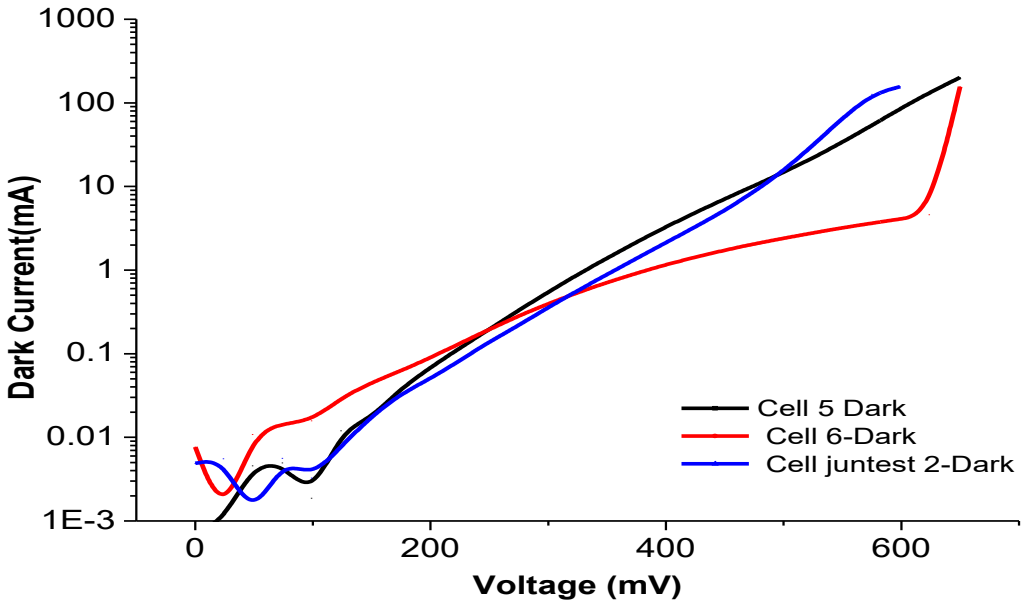

Figure 3.56 Logarithmic plot of IV curves of P/Al silicon solar cells (batch 2)

Batch 2, Electrical parameters of batch 2 which are extracted from IV curve under illumination are given in the table 3.13.

Table 3.13 IV characteristics and parameters of P/Al silicon solar cells (batch2)

Cell No.	**Cell 5**	**Cell 6**	**Cell Juntest2**	**Cell Juntest3**
*P*max. (mW)	69.83	66.06	61.05	54.48
Eff. (η) (%)	16.22	15.5	14.2	12.851
Jsc (mA/cm^2)	39.3	38.3	37.8	35.01
Voc (mV)	599.03	599.07	599.074	599.1
FF	0.70	0.69	0.63	54.48

Sheet resistance of these cells after "P" doping were in range of 140-190Ω/□. Electrical parameters of batch 2 of IV under dark which are extracted from Multiv fitting program and Sun-Voc fitted are given in the table 3.14. Sun-Voc measurement graph is given in figure 3.57.

Table 3.14 Multiv and sun-Voc fit characteristics and parameters of P/Al silicon solar cells (batch2)

Cell ID	Cell 5		Cell 6		Juntest2		Juntest3	
	From Multiv	From Sun-Voc	From Multiv	From Sun-Voc	From multiv	From Sun-Voc	From Multiv	From Sun-Voc
Gsh (ohm.cm^2)	2.00E-04	5.0E-4	2.92E-04	9.0E-4	8.00E-4	9.1E-4	9.50E-04	2.00E-4
Joz (A/cm^2)	2.03E-07	2.4E-7	2.62E-07	2.65E-7	1.74E-7	1.00E-7	2.03E-07	1.2E-7
Joe (A/cm^2)	1.12E-12	1.72E-13	3.00E-13	5.01E-13	4.5E-12	2.00E-13	9.89E-13	2.8E-13
Rm (ohm.cm^2)	9.01E-01		1.80		2.23E-1		2.39	
Voc (mV) IV curve	599.02		599.07		599.32		599.10	
Sun-Voc (1sun) mV	608.37		597.99		603.32		596.69	

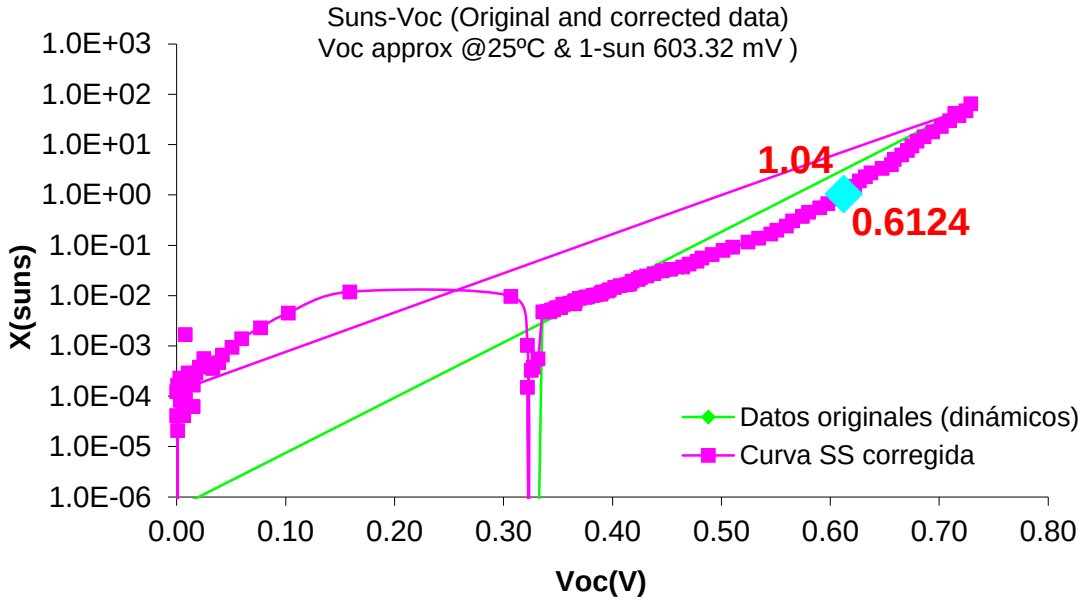

Figure 3.57 Sun-Voc values under 1 sun of P/Al cell (cell 5)

3.18 Thin silicon solar cells

The photovoltaic industry tends to reduce the thickness of the silicon wafers from 350 µm to 100-150µm to save starting material. This is sought to not only reduce the cost of the cells but also to face the dreaded problem of supply solar grade silicon in near future [63]. According to assessment, economic benefits can be taken by decreasing the thickness of solar cell and by increasing the efficiency. A massive improvement has been progressed since 2000 as shown in figures 3.58 and 3.59. For further reduction of cost, innovative

fabrication process by using highly efficient technology is necessary to use. Cost of solar module is described in the graph is given below in figure 3.60.

As it is shown in figure 3.58, economic benefits can be taken, if we used thin wafers for silicon solar fabrication. More than 50% cost of material decrease, if we use thin wafers. A major trend to use thin wafers appeared after 2004. If we used wafers of 150 µm thin, for fabrication, which is less than half of starting material. It would be a 12% reduction in total fabrication cost of solar module in case of multicrystalline silicon wafers. In case of monocrystalline silicon wafers, which are expansive than multicrystalline wafers, saving of total cost will be higher. (21% of total cost drop) [63 and 23]. If cells of 150 µm wafers were manufactured half of the starting material about (keep in mind that much is lost in the silicon wafer sawing) would be spent. This would be a 12% decrease in the total manufacturing cost of the module to the multicrystalline silicon, serving only to reduce the starting material. In the case of monocrystalline silicon as the basis for being a more expensive material, the saving would be even higher (21% of total cost).

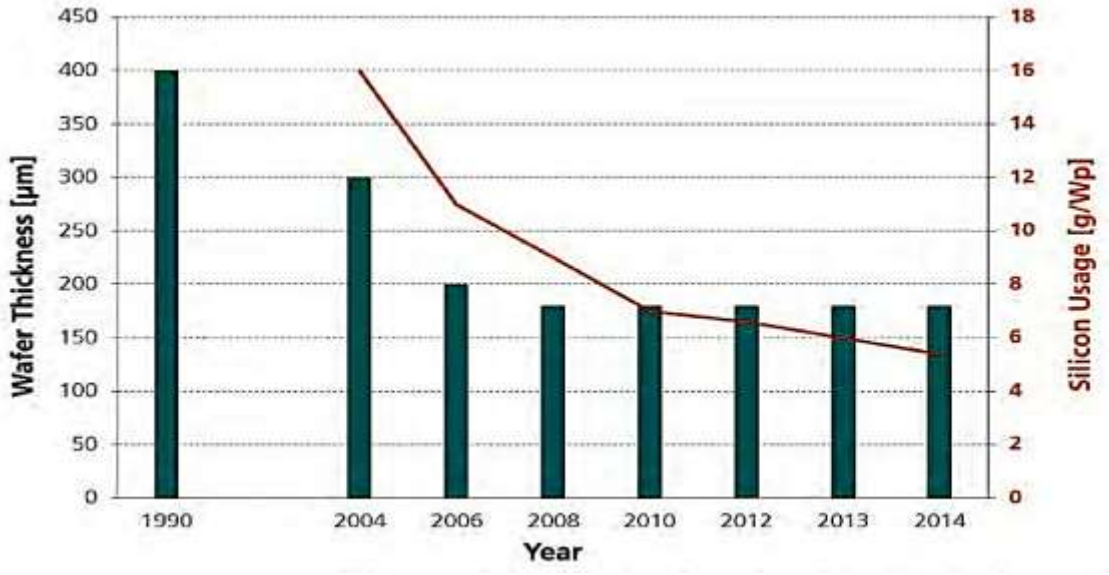

Figure 3.58 Silicon solar cell development (wafer thickness in micrometer (µm) and silicon usage in gram/watt (g/Wp)

In the graph in figure 3.59, the decrease of module price is due to two reasons, one is the solar module cost and other is raw material cost. Module cost from 2005 to 2015 is decreased from 3.25 $ to 0.50$ which is more than 75% drop, which is historical achievement in solar energy world. The cost of raw materials is also dramatically decreased in last decay from 400$ to 25$. This decline is also due to increasing efficiency of solar cell and electrical energy production from sun light due to improvement in fabrication technologies.

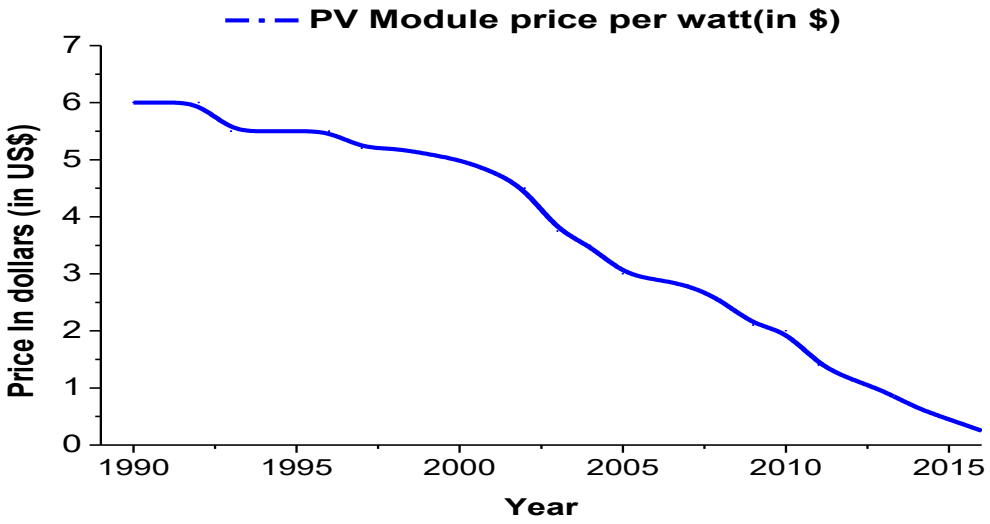

Figure 3.59 Fabrication cost of module in last 2 decays

Detail Information can be found in solar cell central webpage [64]. Fabrication cost of solar module from raw material to end point (lamination) is shown in figure 3.60 in percentage. This is calculated cost of thick silicon solar cell which are in range of 300-350 µm. If decrease the thickness of wafer, we will not only save the raw material silicon but also ingot used for wafer preparation. By using thin wafers we can save more than half amount of silicon for each wafer. Amount of silicon used in each wafer preparation is already discussed. Fabrication cost which is shown in figure 3.60 is average fabrication cost for module but it may vary from country to country depending on the circumstances available.

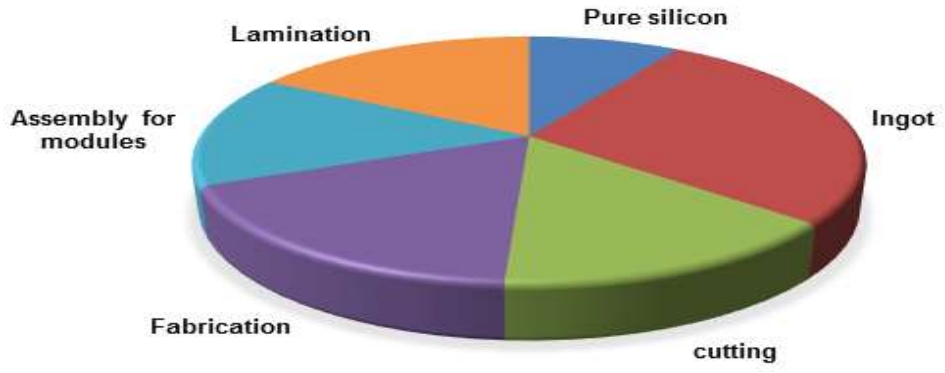

Figure 3.60 Costs distribution of fabrication of a cell module by Cz silicon wafer. If the cell thickness will be decrease, there's a saving both ingot grown and in the material cost.

These calculation assumed that efficiency does not change or decrease if the thickness is reduced. Even if the efficiency decrease little bit under certain conditions is feasible in order to reduce the cost. Obviously benefits are greater if efficiency is maintained or further increase efficiency under certain conditions of fabricated structure with decreasing of thickness. There are many parameters which provides attention to pursue high efficiency. These parameters are very important in order to maintain or even improve efficiency of solar cell. Lifetime in volume of cell (τ), surface recombination velocity (S) and absorption and reflection of light. The lifetime reduces due to existence of crystal defects and impurities present in crystal structure, it also depends on fabrication process. These impurities can be removed from volume through process of gettering and lifetime values can be increase. By

aluminum gettering, 19% efficiency has been achieved by using P/Al technology on FZ material [23, 37].

When lifetime of carriers is higher, it becomes more important for carriers to stay in surface of the cell, where dominant recombination take place but not in the volume of cell but also on the surface. Therefore interesting point is to decrease recombination by minimizing it electrically well passivated surface. In case $n^+p\,p^+$ structure which is based on P/Al, front surface of n+ emitters have a good passivation due to SiO_2 growth or due to silicon nitride passivation. Major problem is on the backside of wafer and this problem is solved by Aluminum deposition. During redistribution step of aluminum, it diffuses into the base of p-type of silicon, which appears $p\,p^+$ homounion (homojunction) on backside the wafers. This union generates an electric field opposite to the movement of minority electrons from base region toward the rear metal contacts, which improves the effective surface recombination velocity (*S*).

3.18.1 Thinning effect of P/Al solar cell.

The objective of this section is to show the simulation results for fabrication $n^+p\,p^+$ silicon solar cell on CZ wafers thin substrates about 100 µm in thickness by applying P/Al technology. It is experimentally confirmed that that the absorption and reflection of light is affected if thickness of wafers decrease from 300 to 120 µm is reduced unless entrapment techniques are used to absorb maximum amount of light [65].

In case of thin film solar cell, when we use textured wafers, maximum light is absorbed due to texture structure of wafers which provides second chance to rays to be absorbed in base of silicon. Any roughness on the surface of wafers reduces the reflection by increasing the chances of reflected light to bounce again onto the surface rather than reflected back. In addition this texturization with a subsequent deposition of antireflection coating (ARC) is well established method to reduce the optical losses. Due to texture surface, thin wafers are not affected by reflection. Mechanism of reflection is shown in figure 3.61. Normally rays are reflected back due to plan surface but texture surface deflect them at certain to strike again on the surface. [66, 68-69]

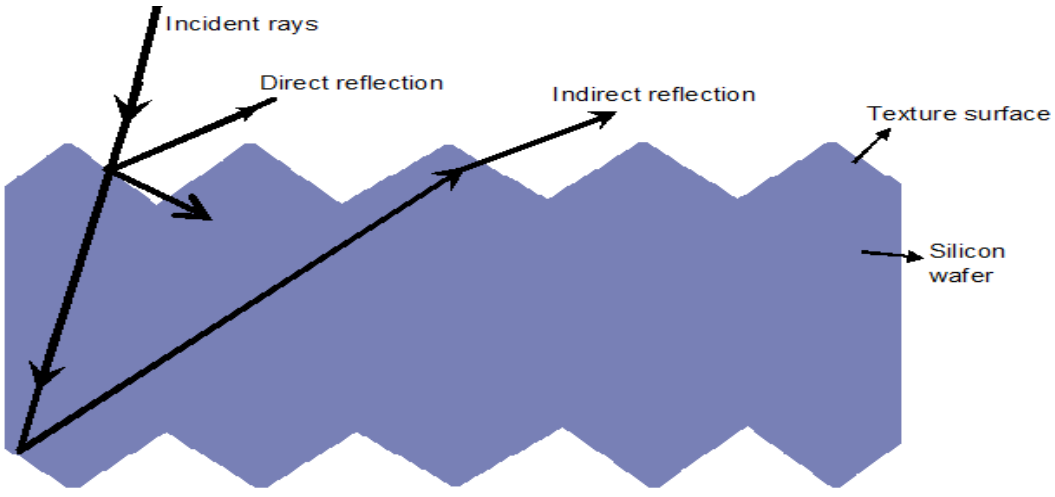

Figure 3.61 Reflectivity in texture wafer with rays' path for absorption and reflection

We have prepared a theoretical model in order to predict behavior through PC1D simulations of P/Al solar cell, when its thickness is reduced. For this purpose, we have simulated solar cell data with PC1D and energy losses are analyzed where the thickness of

solar cell change. All other parameters are same and presented in a table which are given below ;(see the table 3.18).

Table 3.18 parameters for simulation in PC1D for P/Al solar cell

PC1D Simulations for P/Al silicon solar cell	
Parameters	Specifications
Cell structure	$n^+p\,p^+$ silicon solar cell
substrate	P-type silicon with ρ_{base} =1.46 with base doping conc. N_b = 1E16 cm^{-3}
Thickness	Variable 70-350 µm
Front diffusion (n^+)	Doping concentration with junction depth N_s = 1E19 cm^{-3} and x_j = 1.01 µm Sheet resistance 100 Ω/□
Back diffusion p^+	N_s = 1E19 cm^{-3} x_j = 5 to 10 µm
Internal reflectance	Internal reflectivity of front internal ρ_{front} = 90%, and internal reflectivity of the backside $\rho_{backside}$ = 70%
Bulk Recombination	$\tau_n = 55$ µs and $\tau_p = 280$ µs
Temperature	298 K
Recombination in volume SRH (τ (µs))	Variable
Auger recombination	In case of low injection $C_{An} = 2.2 \times 10^{-31} cm^6/s$ and $C_{Ap} = 0.99 \times 10^{-31} cm^6/s$; in case of high injection $C_A = 1.66 \times 10^{-30} cm^6/s$
Recombination coefficient in emitters type (n^+)	$B_n = 7.8 \times 10^{-13} cm^3/s$
Recombination coefficient in type (p^+)	$B_p = 3.45 \times 10^{-12} cm^3/s$
Surface Recombination of metallic contacts	10^7 cm/s
Surface recombination	7000cm/s
Parallel diode.	$J_0 = 3.99 \times 10^{-10}\ A/cm^2$, m=2

Solar cells parameters such as efficiency, short circuit current and open circuit voltage, their dependence on the thickness are studied by using PC1D simulations. Effect of these parameters are plotted verses thickness which are shown in figures 3.62, 3.63 and 3.64 [67].

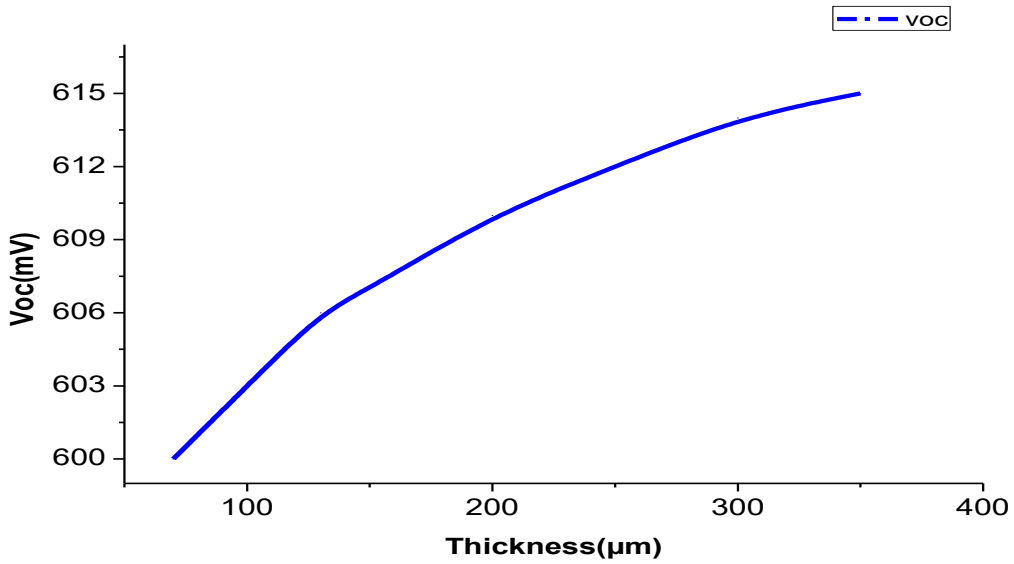

Figure 3.62 PC1D prediction of the behavior of a of P/Al cell according to different thicknesses of cell to the evolution of open circuit voltage

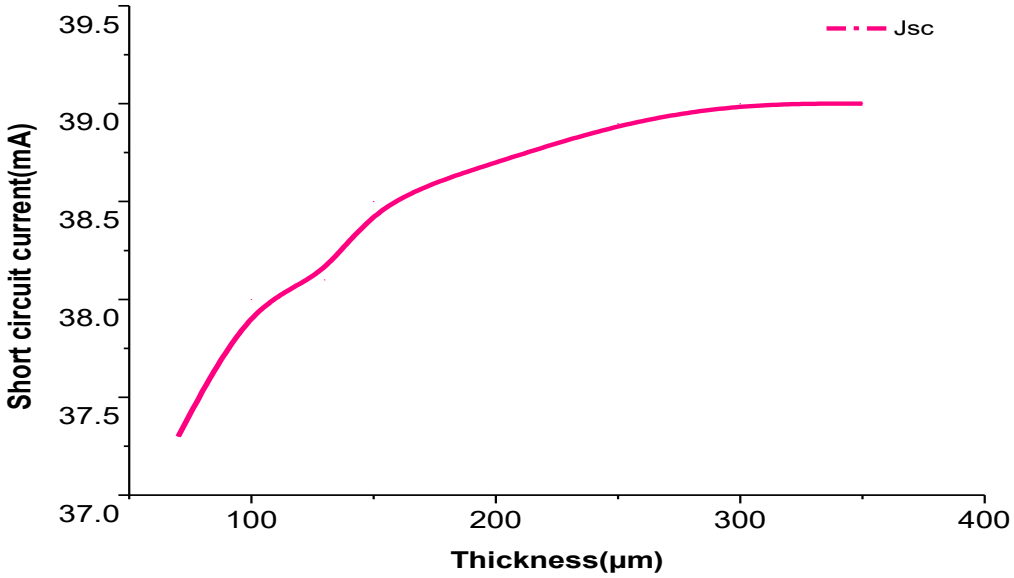

Figure 3.63 PC1D prediction of the behavior of a of P/Al cell according to different thicknesses of cell to evolution of short circuit current.

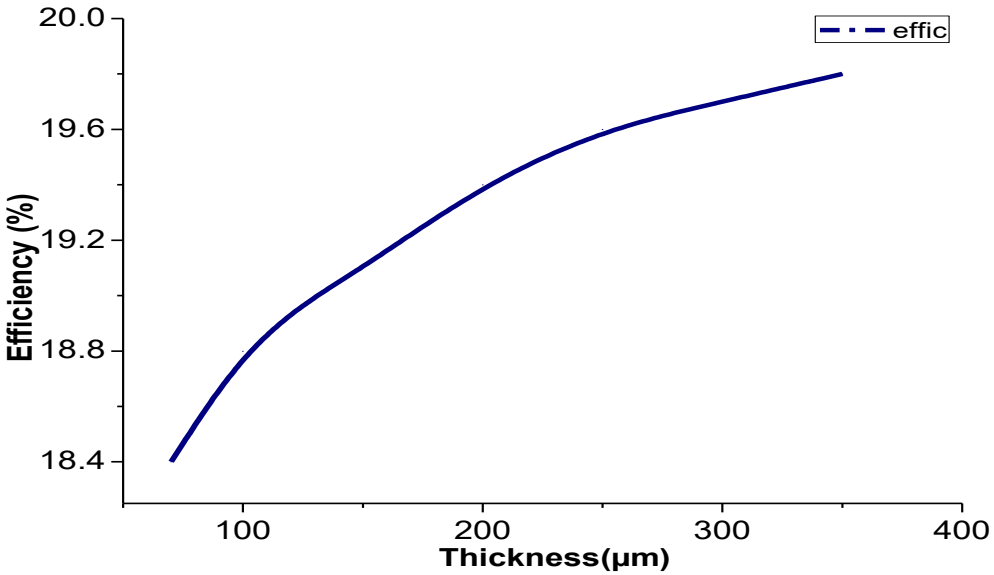

Figure 3.64 PC1D prediction of the behavior of a of P/Al cell according to different thicknesses of cell evolution of efficiency

It is also possible to predict effect of lifetime on performance of silicon solar cell by PC1D prediction under different cell thickness. PC1D predicted results are shown in figure 3.65.

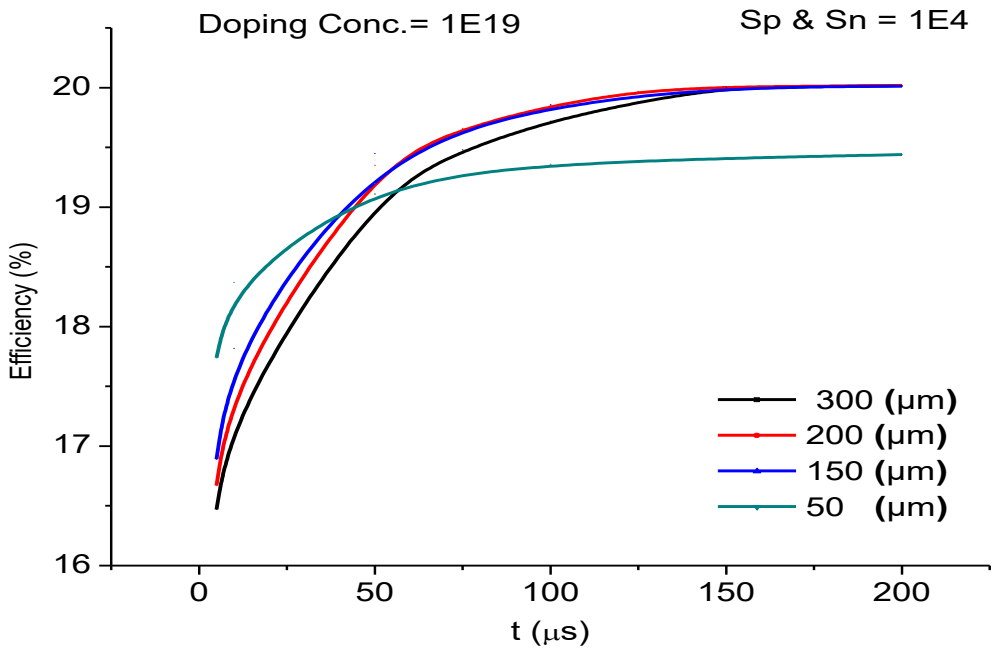

Figure 3.65 PC1D prediction for effect of lifetime on efficiency for of P/Al cell under different cell thickness.

3.19 Gettering process by Al and lifetime measurement of P/Al solar cells

In silicon solar cell, recombination must be reduced in order to achieve high efficiency solar cells, therefore intrinsic gettering process is used in most semiconductor device technology (formed in a region near the surface) are unsuitable. There extrinsic gettering procedures which can reduce the concentration of contaminating impurities confining on the surface that are not active, which can be removed easily. There are major techniques used

for gettering process in fabrication process of silicon solar cell are gettering by phosphorus and gettering by aluminum.

In this process, after phosphorus pre-deposition, an aluminum layer is deposited on back side of silicon wafer and subsequently annealing was carried at high temperature improve the performance of solar cell due to two effects, which are back surface field effect (Al-BSF) and effect of gettering of metallic impurities from volume of the device. BSF effect is explained that annealing of Al, p-type dopants forms the basis of homojunction with p base silicon and reflect back the minority carriers from superficial. The gettering effect is due to solubility of metallic impurities, which is higher in liquid aluminum silicon (Al-Si) due to high temperature as compare to solid silicon.

Gettering techniques consist of P deposition in silicon saturation conditions (from a solid or liquid source), when temperature increases a layer of PSG is formed which segregate the impurities. This phenomenon of gettering of impurities by phosphorus was observed first time by Meek et al in 1975 [70]. When he deposited a layer of gold and copper on side of wafer, which was subjected to P diffusion in saturation conditions of $POCl_3$ source to measure profiles of gold and copper and observed the reduction in the volume of wafer. In gettering by phosphorus, solubility of impurities is higher in PSG than volume of silicon. Some experiments were carried out by A.E. Mousssaoui and C. Cañizo in order to extract impurities by phosphorus diffusion during doctoral studies at IES (Madrid). [27 and 71].

A. Mousaousi has studied deeply Fz, Cz and multicrystalline silicon materials for P/Al solar cell fabrication process. In this new process, he introduced novelty in initial step of extracting the impurities by phosphorus that is called pre-gettering. He has found that 825 º C temperatures is the best temperature for Cz and multicrystalline material to extract (getter) the impurities. While in Fz material, decrease in lifetime was observed due to high temperature ranging from 825 to 975 ºC. We have to take into consideration before applying this gettering process. The lifetime measurements have permitted us to observe the effect of phosphorus gettering. In A. Mousaousi P/Al fabrication process, high lifetime was measured along with high efficiency on multcrystalline wafers. Although this process has advantage of high efficiency with high lifetime but this process has disadvantage of long duration of P pre-deposition step and redistribution of impurities. Its high thermal load made this process unsuitable for other substrate. In addition to this process has low reproducibility [27].

Initial lifetime (µs)	After P pre-gettering (µs)	Final lifetime (µs)
30	100	105

Fabrication process of P/Al solar cell and, detail of each step is already given early in chapter 1. In order to assess the effect of contamination and gettering during fabrication process, lifetime of each thermal step was measured during fabrication by using PCD and QSSPC techniques. Lifetime measurement results are given in figure 3.66.

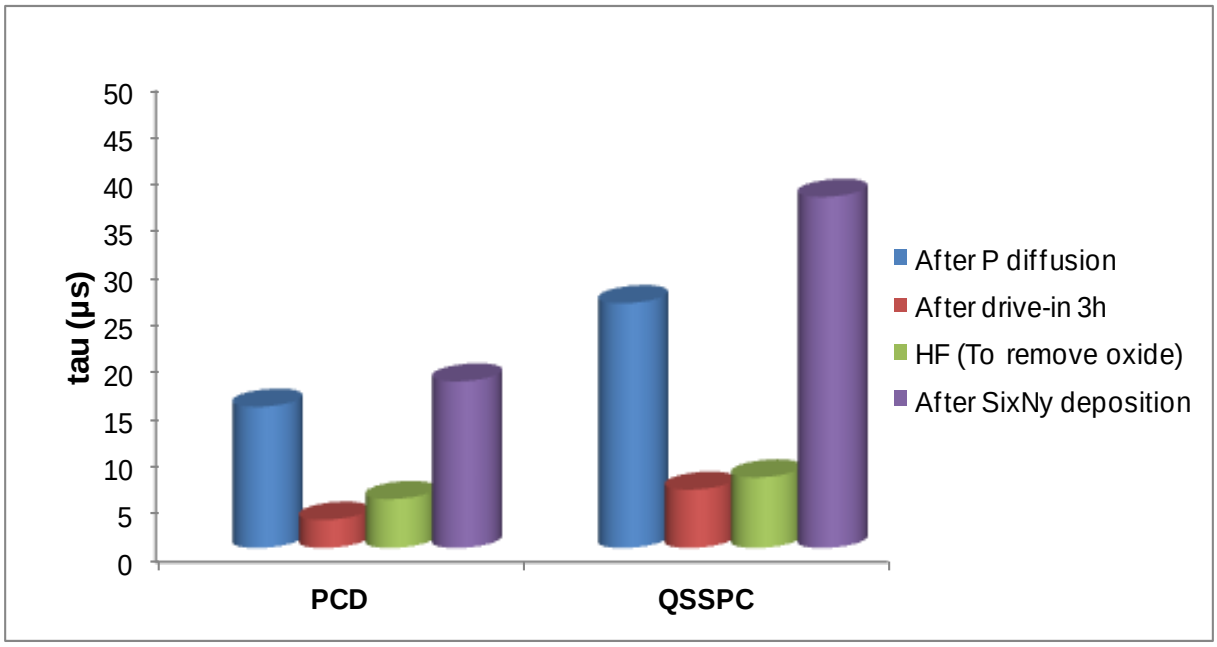

Figure 3.66 Lifetime measurements by using PCD and QSSPC techniques after thermal, chemical treatment step and SiNx deposition

. In P/Al silicon solar cell, we have calculated effective surface recombination velocity (*S*) from lifetime measurements, which is around 500cm/s. This value is consider high surface recombination velocity. We have made some PC1D simulations, in order to determine the effect of surface recombination velocities for different concentration of emitters. From 3.67, it is shown that efficiency of silicon solar cells is higher at low surface recombination rate. Higher surface recombination velocity lower the efficiency of silicon solar cells.

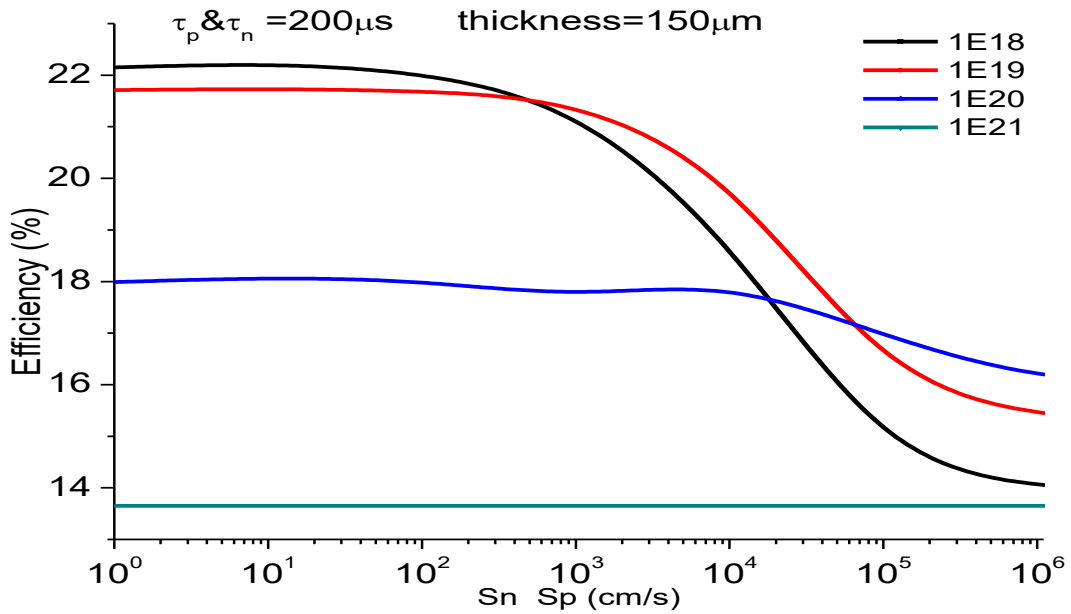

Figure 3.67 Graph between efficiency against at surface recombination velocity with different surface concentration of emitter Ns. (Thickness =150µm, τ_p&τ_n=200µs)

3.20 Conclusion:

High efficiency P/Al technology has been developed in the mid of 80´s by theoretical and experimental studies of A. Cuevas and M. Balbuena at IES-UPM. They have concluded that it is possible to obtain high efficiency with lightly doped deep phosphorus emitters and aluminum back surface field, P/Al (P emitters- Al BSF). They have obtained efficiency above 19% by using high quality FZ monocrystalline silicon wafers [1]. In fact when P/Al technology was described at that time, efficiency achieved was remarkable and among the best silicon solar efficiency reported in the world. The main objective of this work was to improve high efficiency P/Al technology by using low grade silicon thin wafers for solar cells, which are industrializable exceed the efficiency and thickness estimation provided by industry.

Fabrication process is started from chemical etching and texturing of P-type monocrystalline silicon wafers obtained by Czochralski growth (Cz) with base resistivity in range of 0.5-2 Ω.cm and having thickness around 160 µm. Phosphorus pre-deposition was carried out at 825 ^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under standard conditions. Diffusion profile has been made in order to know doping concentration and junction depth. Surface concentration is around $1 \times E19\, cm^{-3}$ with junction depth about 1.05 µm. Optimization analysis of homogeneous phosphorus emitters is key step of this technology in order to maintain high efficiency. Phosphorus emitters are necessarily to be a homogeneous, for this purpose P diffusion is investigated deeply to get lightly doped and deep emitters. Detail of phosphorus diffusion and emitter's optimization is given in next chapter 4 (diffusion).

1 µm thick layer of aluminum (Al) is deposited on backside of wafers by an electron beam machine (EBM) and diffused in quartz furnace simultaneously with phosphorus for 3 hours at 1050 ºC in nitrogen ambient. For optimization of aluminum diffusion on backside of wafers, we have taken into account that amount of deposited of metal, temperature, process time and composition of environment of the furnace to improve the lifetime and passivation. Doping profile of Al is shown above, which represents the doping concentration of Al in Si is around $1 \times E19\, cm^{-3}$ and junction depth on rear side of wafer is around 3.5 µm. Simultaneous diffusion P and Al in P/Al technology resulted a n^+pp^+ structure in which the emitters are produced by phosphorus diffusion, creates n^+ on front side of the wafer while on back side aluminum is diffused to produce p^+ on backside of the wafer. Diffusion of aluminum into silicon at high temperatures also creates a BSF effect (back surface field).

Silicon nitride layer is deposited by PECVD on front side of wafers in order to achieve passivation, this layer also acts as an antireflection layer. Although we did not have reasonable results of passivation but still silicon nitride is used as an antireflection layer to decrease the reflectivity. Fronts contacts are defined by metals (Ti/Pd/Ag) evaporation by EBM by using photolithographic technique and to gain desire thickness (about 8 µm high and 25 µm wide) of fingers and busbar, electroplating process was carried out. A layer of Al/Ag is also deposited by evaporation by using electron beam machine100/150nm respectively on backside of wafer.

Final structure of P/Al technology (n^+pp^+) was annealed at low temperature in a forming gas atmosphere in order to produce a good alloy between different metals which reduces series resistance and recover the damages produced by electron beam machine, when electrons hit the metal to evaporate, during this process they produce x-rays. Edge isolation and cutting of solar cells were carried by Laser application. By applying P/Al technology, we

have fabricated different batches of $n^+p\,p^+$ (P/Al) solar cells, their characterization were carried out by Sun-Voc and lifetime measurements during fabrication and IV characteristics were measured under dark and illumination at the end of fabrication process.

The best results which we have obtained in batch 1 have efficiency around 14.75% with open circuit voltage around 600mV, short circuit current 37mA/cm^2. Although shunt conductance is higher but still we have a good efficiency. In this batch emitters are poorly passivated. While in second batch, we have obtained efficiency around 16.5% with open circuit voltage 600mV and Sun-Voc around 610 mV with short circuit current 39.2mA/cm^2. Although fill factor is low due to series resistance which is around 70. From PC1D simulations, it is clear that it is possible to get efficiency around 18% by P/Al technology.

During fabrication process of P/Al silicon solar cells we have obtained emitter saturation current density for worse emitters around 1E-11A/cm^2 and good emitters around 5E-13 A/cm^2. The quality of emitters play important role in the performance of silicon solar cells. It depends on diffusion temperature with flow of gases and doping time. At high temperature, concentration of phosphorus (P) exceed the solubility in Si (10^{21}/cm^3) which form a dead layer [72-73] which is electrically inactive and has effect on surface P concentration and junction depth. It produces recombination centers that increase Auger recombination, as a result it increased the emitter's saturation current density (Joe) [74-75]. Moreover high surface P concentration reduced the passivation effect which lowers the open circuit voltage (Voc) and overall solar cell efficiency [76]. It is observed that at high temperature, phosphorus is precipitated in the form of dead layer due over solid solubility limit. Due to this layer recombination centers appear, as a result Auger recombination increase.

There are some technological steps, involved in a fabrication process which are sources of impurities are almost inevitable. Those are identified as transitions metals which are common source of contaminating impurities. These contaminating impurities have negative impact on the lifetime of minority's carries which supposed to degrade the performance or efficiency of solar cells. There are two strategies which are pursued in complementary form to alleviate effect of contaminations. On one hand high cleanliness of process including wafer cleaning after etching and texturing process by RCA1&2 cleaning and second cleaning by integrating gettering process by P or Al during diffusion process. These two processes are used to reduce the concentration of contaminating impurities of active area of device.

There are various techniques which are used to characterize the impurities, some of them are used to measure the concentration of impurities and some of them are used to measure its effects. In particular lifetime measurement techniques by photoconductivity decay which in term of surface passivation is used to measure impact of impurities on surface and in the bulk are reliable measurement techniques. We have measured lifetime of P/Al solar cell structure after each thermal step. Due to high temperature and impurities, lifetime was destroyed. After diffusion and P/Al drive-in process, we tried to measure lifetime but it was difficult to measure due to low values. After SixNy deposited by PECVD, which is used to passivate the surface, we had measured lifetime of solar cells around 20µs by PCD and 40 µs By QSSPC technique. In this our P/Al fabrication process, we did not observe improvement in of lifetime after Al-gettering step during drive-in as it is shown in graph in figure 3.69. Although some authors have observed improvement in lifetime after gettering by P/Al but they have used FZ wafers during fabrication process. In some cases improvement in lifetime was observed, when they used phosphorus pre-gettering or pre-oxidation step

prior to fabrication on Cz or multicrystalline material. According to theoretical knowledge, lifetime of the silicon wafers should be improved due to gettering step by aluminum. The gettering effect is due to solubility of metallic impurities, which is higher in liquid aluminum silicon (Al-Si) due to high temperature as compare to solid silicon but most of authors did not observe this phenomena of lifetime improvement in after Al-gettering step. This may be because most of the impurities present in the substrate are trapped in crystal defects (dislocations and grain boundaries) or to occupy substitutional positions within the network, which makes difficult its removal by aluminum.

Low quality emitters produce the recombination centers due poor passivation which decrease the lifetime of the solar cell. As a result effective surface recombination velocity increase. In P/Al silicon solar cell fabrication process we have calculated effective surface recombination velocity, which is around 500cm/s. PC1D simulation showed that efficiency of silicon solar cells is higher at low surface recombination rate. Higher surface recombination velocity lower the efficiency. Efficiency of P/Al structure will be around 20%, if we will have passivated emitters as shown by PC1D simulations. In next chapters we will focus on fabrication of passivated softly doped and deep emitters.

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Chapter 4

4 Diffusion

4.1 Doping:

Introduction of impurities into a semiconductor crystal to the defined modification of conductivity and electronic properties is called doping process. There are two important materials which are used in silicon doping. Boron (B) atom is trivalent (3 valence electrons) and phosphorus (P) is pentavalent (5 valence electrons) impurities. Other materials are aluminum, indium (trivalent) and arsenic, antimony (pentavalent). The dopant is integrated into the lattice structure of the semiconductor crystal and the number of valence electrons define the type of doping. Elements which are trivalent (3 valence electrons) are used for p-type doping and elements which are pentavalent (5 valance electrons) are used for n-doping. The pentavalent dopant has outer electrons more than the silicon atoms. Four outer electrons combine with silicon atoms to form covalent bond while the fifth electron is free to move and serves as charge carrier. This free electron requires much less energy to be moved from the impurities level into the conduction band, than the electrons which cause the intrinsic conductivity of silicon. The dopant which emits an electron is known as an electron donor.

4.1.1 N-type doping:

These dopants are positively charged in nature due to deficiency of electron in valence band by the loss of negative charge carriers and are built into the lattice, only the negative electrons can move. Doped semimetals whose conductivity is based on free (negative) electrons are n-type or n-doped. Due to the higher number of free electrons those are also named as majority charge carriers, while free mobile holes are named as the minority charge carriers. Arsenic is used as an alternative to phosphorus, because its diffusion coefficient is lower. This means that the dopant diffusion during subsequent processes is less than that of phosphorus and thus the arsenic remains at the position where it was introduced into the lattice originally. Due to negative charged electrons these semiconductors are called n-conductive or n-doped. In p-doped semiconductors, the electrons are the majority charge carriers while holes are the minority charge carriers.

4.1.2 P-type doping:

In contrast to phosphorus, Boron has totally different effect. It is trivalent dopant which can catch an additional outer electron, thus leaving a hole in the valence band of silicon atoms and producing positive charge (hole). Therefore the electrons in the valence band become mobile. The holes move in the opposite direction to the movement of the electrons. The necessary energy to lift an electron into the energy level of indium as a dopant, is only 1 % of the energy which is needed to raise a valence electron of silicon into the conduction band. Due to positive charge (holes) these semiconductors are called p-conductive or p-doped. Analog to n-doped semiconductors, the holes are the majority charge carriers, free electrons are the minority charge carriers.

In semiconductor technology, there are couple of methods, which are used for doping in fabrication processes.

- Diffusion
- Ion implantation
- During crystal growth
- Epitaxy

4.1.3 Diffusion:

Diffusion is a process of the redistribution of atoms, molecules and ions from regions of high concentration of mobile species to regions of low concentration. It occurs at all temperatures, but the diffusivity is an exponentially dependent on temperature. High temperature diffusion is one of the important process one the important process in solar cell fabrication and other monolithic integrated circuits (IC) in microelectronics devices.

Today, diffusion process has been used in the formation of deep layers below one micron (1µm) in depth. Diffusion is a primary method of introducing impurities such as boron (B), phosphorous (P), and antimony (Sb) into silicon to control the majority-carrier type and resistivity of layers formed in the wafer. Diffusion is used to form emitters and resistors in bipolar device technology, to form source and drain regions and to dope crystalline silicon wafers in MOS device technology. Therefore we are interested in diffusion process in order to understand its limitation and various problems associated with redistribution of impurities. There are mainly two methods of diffusion which are given below.

- Diffusion from a chemical source in vapor form at high temperature.
- Diffusion from a doped-oxide source

4.1.4 Phosphorus diffusion:

Phosphorus diffusion usually is carried out in a tube furnace at high temperature to create n^+emitters for silicon solar cell fabrication. A liquid source in form of phosphoryl chloride is used as source of phosphorus for phosphorus diffusion in a quartz close tube. Boat on which wafers are loaded is also made of quartz. Process is started from heating of furnace. Diffusion process is divided into two stages, phosphorus pre-deposition and drive-in, both are usually carried out at different temperatures.

In pre-deposition step, nitrogen gas is used at carrier gas to carry $POCl_3$ vapors into furnace, where it reacts with oxygen to produce phosphorus pentoxide, a real source of phosphorus for doping. While in drive-in step, supply of phosphorus is suppressed and deposited P_2O_5 interacts with silicon to produces silicon dioxides on wafer surface and release phosphorus atoms which diffuses into silicon. During pre-deposition silicon is oxidized and form a thin layer of silicon dioxide at surface. In addition to this P_2O_5 also reacts with silicon dioxide to for phosphorus silicate glass which is called as PSG on silicon dioxide surface. Due to PSG and SiO_2 layers, diffusion of phosphorus in silicon is retarded, for diffusion, P has to overcome these layers in order to reach the silicon region to create n^+ emitters. Diffusivity of phosphorus in silicon dioxide is lower than silicon and silicon dioxide is continuously grows creating a barrier is P in silicon diffusion [1-2]. In this work, pre-deposition is carried at different temperature ((800-875 ºC) and drive-in was carried at fixed temperature 950 ºC to investigate emitters concentration and junction depth.

4.1.5 PSG (Phosphorus Silicate Glass):

In phosphorus diffusion, P_2O_5 is produced from $POCl_3$ during pre-deposition process, P_2O_5 is rich in oxygen and oxidize the silicon into silicon dioxide. This reaction is carried at high temperature, which is diffusion temperature. When silicon surface is oxidized, P_2O_5 reacts again with SiO2 to phosphorus silicate glass (PSG) at diffusion temperature. Chemical reaction is given in equation 4.1

$$xSiO_2 + yP_2O_5 \rightarrow\rightarrow\rightarrow\rightarrow xSiO_2.yP_2O_5 \quad (PSG) \tag{4.1}$$

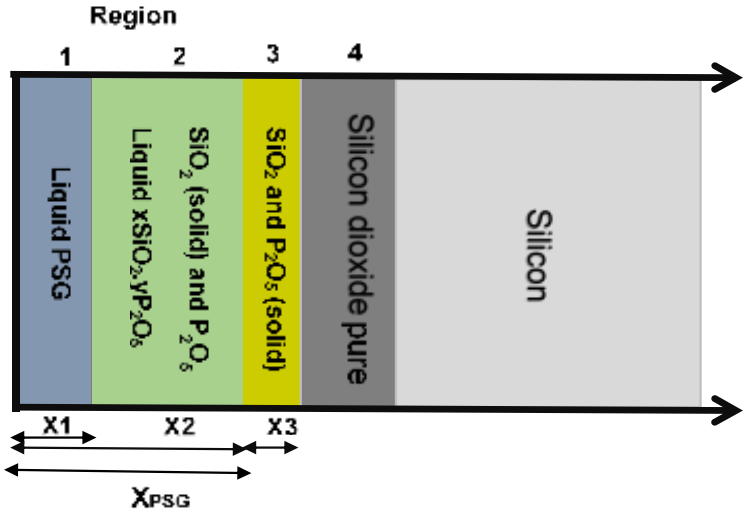


Figure 4.1 Systematic representation of PSG layer [3]

In figure 4.1, a flow sheet diagram has been made in order to explain the formation of PSG and thickness of PSG. According to that model, a layer of silicon dioxide is created on silicon (pure Si). In region 1, PSG exist in liquid state and in region 2 there is a mixture of solid SiO_2 and liquid PSG. After that a layer of mixture of SiO_2 and P_2O_5 (in solid state) is appeared in region 3. PSG thickness during diffusion can be calculated by as $X_{PSG} = x1 + x2 + x3$ but it was found that x3 is negligible as compare to x1 and x2. Due to this reason PSG thickness is estimated as $X_{PSG} = x1 + x2$. [3-4].

$$X_{PSG} = x1 + x2 \tag{4.2}$$

P_2O_5 concentration starts decreasing when phosphorus species react with Silicon or silicon dioxide. Eutectic reaction represented as

$$L \rightleftharpoons SiO_2 + SiO_2.P_2O_5 \quad \textit{at 870 °C} \tag{4.3}$$

It is observed that below 870 ºC, formation of crystallite take place and temperature dependent solubility of P_2O_5 changes from 800 ºC to 900 ºC. A theoretical equation has been used to calculate the thickness of PSG layer during diffusion process. This equation depends on time (t in second) temperature (T in kelvin) and concentration Cp of phosphorus in gas phase (In volume %). Equation is given below (equation 4.4). Thickness of X_{PSG} can be controlled by controlling the time, temperature and phosphorus source ($POCl_3$).

$$x_{PSG} = (9.032 \pm 0.170)10^5 . \sqrt{C_p t} \, . exp\left(\frac{-0.815eV}{k_B T}\right) \qquad (nm) \tag{4.4}$$

4.1.6 Diffusivity of *P* in *Si*.

In case of silicon, phosphorus diffusion can takes place by two mechanism which are interstitial and vacancy mechanism. In case of interstitial diffusion, dopant atoms in interstitial position jump to another interstitial positions without replacing atoms in the lattice. In case vacancy diffusion, a substitutional dopant atoms exchanges positions in the lattice with a vacancy. Interstitial diffusion take places at higher rate than vacancy diffusion, since number of vacancies is limited and depends on temperature. Vacancies are always present through thermal equilibrium processes and these are thermodynamics defects and their nature is different from dislocations and stacking faults. We can estimate the vacancies by following equation.

$$vacany\ (f) = exp(-Ea/kT) \tag{4.5}$$

$Ea = 1\ eV,$

For 1eV energy of activation, from this equation we have estimated 0.004% vacant sites at 875 ºC and their percentage at different temperature is shown in figure 4.2:

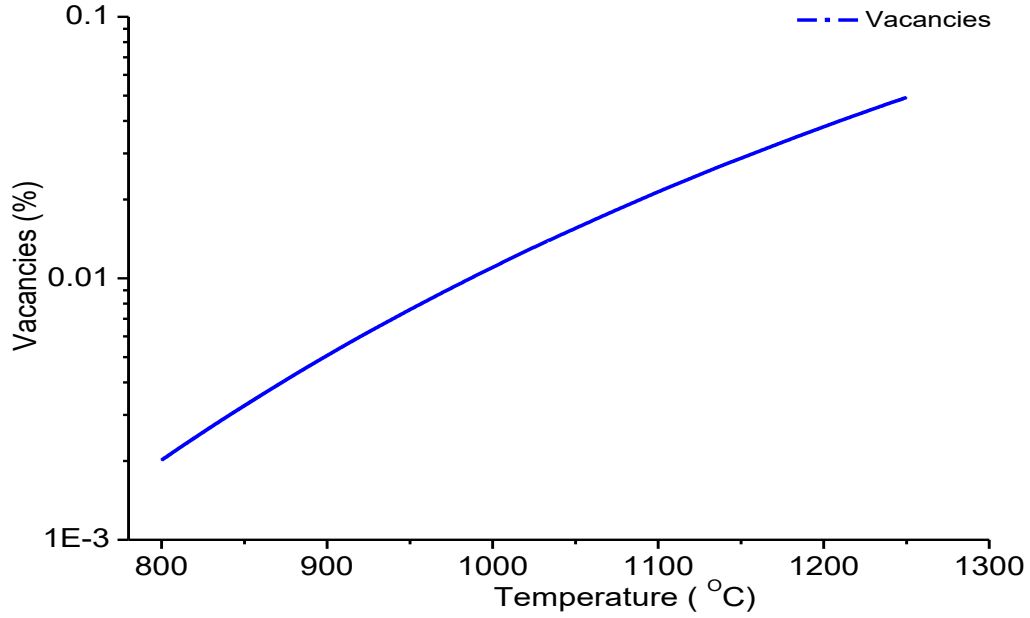


Figure 4.2 Graph between temperature and vacancies

In case of interstitialcy mechanism, phosphorus atoms replaced silicon atoms in the lattice and silicon atoms are displaced to interstitial sites [5]. There are two mechanisms which describes how impurities may return to the lattice. Kick out mechanism where impurity atom replaces a lattice atoms and dissociative or Frank-Turnbull mechanism where an interstitial impurity atom is captured by a vacancy. For these 2 mechanisms do not need the presence of self-interstitials as it is regulated by the interstitialcy mechanism.

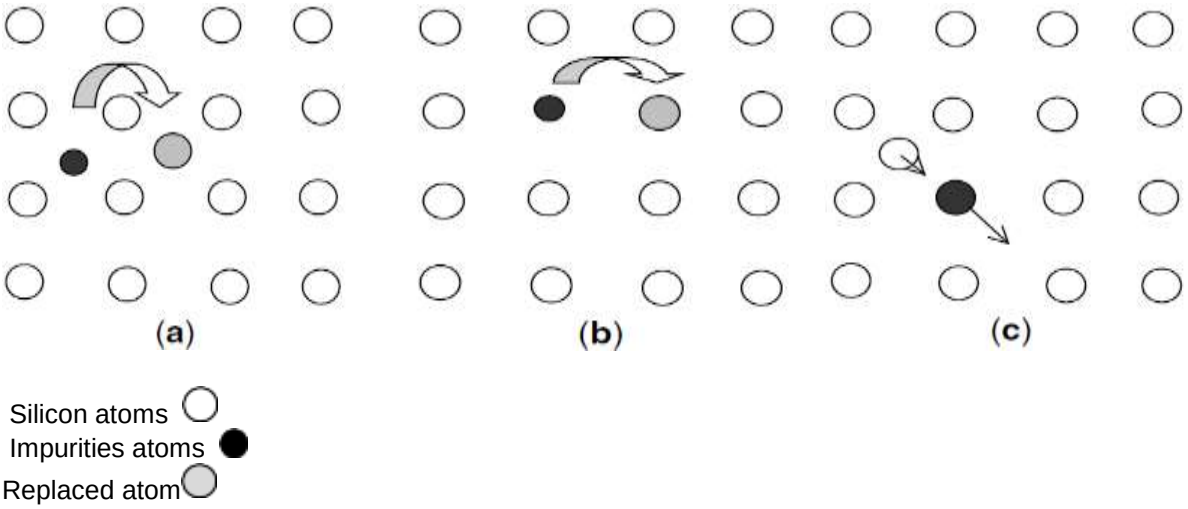


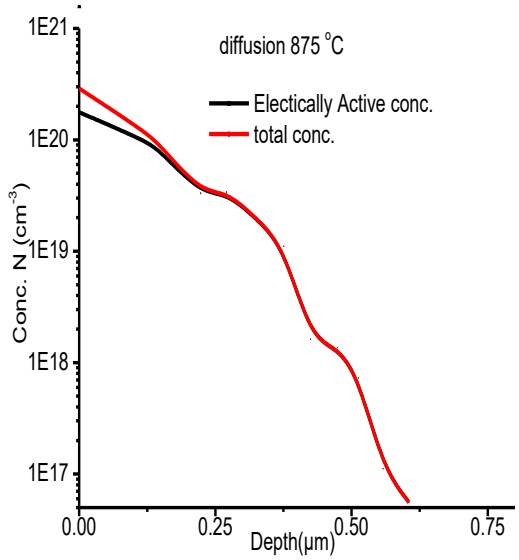
Figure 4.3 Diffusion mechanisms: (a) interstitial, (b) substitutional/vacancy and (c) interstitialcy

A model which describe diffusion of phosphorus in silicon is based on assumption that diffusivity of phosphorus is dominated by vacancy mechanism. This model is proposed by Fair and Tsai in 1977 [6]. According to this model, diffusivity of phosphorus behave differently depending on concentration of dopant atoms. In the graph, there are three different regions. In high concentration region, diffusivity of impurities $D\ \alpha\ n^2$(n is electron concentration) and tail region where $D\ \alpha\ n_e^3$ (n_e is electron concentration at the plateau level).

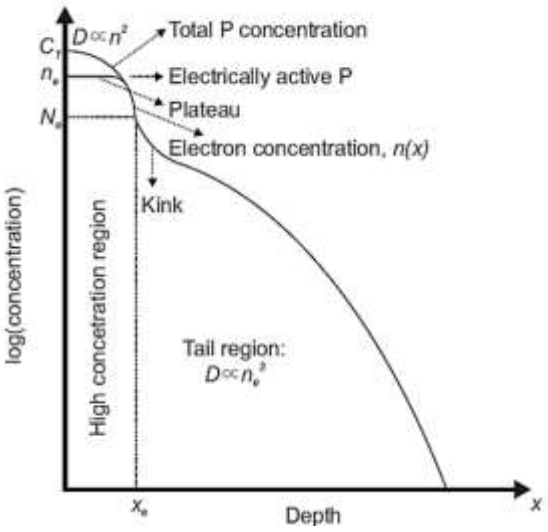
According to Fair and Tsai model, diffusion of dopants such as phosphorus into silicon from higher surface concentration is accompanied by an injection or generation of point defects which causes a radical enhancement in diffusion of dopant diffused previously. (Dopant which already present due to base doping). A model which explains observation of enhanced boron base diffusion of phosphorus emitters at high concentration was that of injection of vacancy or vacancy complexes. It is assumed that boron is diffused through a vacancy mechanism. More recent models have concentrated on the role of E-centers phosphorus vacancy pairs, both to explain the anomalous features in the diffusion of phosphorus itself and its effects on other dopants.

At low surface concentration (lower than 1E19 cm^{-3}) Profiles follow a simple diffusion process, that is possibly of charged defects including E-centers being involve in phosphorus diffusion. Fair and Tsai proposed a recent model which they have developed for quantitative prediction of doping profiles is shown in figure 4.3 and proposed that high concentration region of profile ($n > 1\times 10^{20}$ cm^{-3}) equilibrium concentration of $P^+ V^=$ pair dominates phosphorus diffusion and electrically active.

Profile



a



b

In figure 4.4 (b), Phosphorus profile and vacancy generation model, $P^+ V^=$ pairs formed in surface region dissociate when electron concentration decrease to $n = n_e$. At this concentration Fermi level coincides with second accepter level of $V^=$.Free vacancies diffuse until the recombine with P^+ atoms in region to form $P^+ V^-$ pairs (Fair and Tsai [6]).

With respect to energy requirement for phosphorus atoms to diffuse into silicon or displace the silicon atoms requires lower energy for interstitial diffusion as compare to vacancy diffusion. Interstitial atoms are loosely bound as compare to substitutional atoms. In case of vacancy mechanism the energy of activation is defined as energy required to create a vacancy in silicon instead of energy required to move the impurities as in interstitial diffusion. The intrinsic diffusivity values for phosphorus can be calculated by following equation (4.6).

$$D_i = D_0\, exp(-Ea/kT) \tag{4.6}$$

$Ea = 3.66\, eV, D_0 = 3.85\ (cm^2/s)$

In high concentration region, total P concentration is higher than active P concentration. P^+ ion unite with vacancy $V^= or V^{2-}$ (double negative charge) to form $P^+V^=$ pairs represented as $(PV)^-$ and extrinsic diffusivity is given be equation (4.7).

$$D_x = D^0 + D^= \left(\frac{n}{n_i}\right)^2 \qquad (cm^2/s) \tag{4.7}$$

$D^0 = D_i$ And $D^=$ can be calculated by following equation (4.8).

$$D^= = 44.2.\, exp\left(\frac{-4.37}{k_B T}\right) \quad (cm^2/s) \tag{4.8}$$

Concentration of electron in kink region can be calculated by equation (4.9).

$$N_e = 4.65 \times 10^{21} exp\left(\frac{-0.39}{k_B T}\right) \ (cm^{-3}) \quad (4.9)$$

Diffusivity in tail region can be calculated by equation given below (5.0).

$$D_{Tail} = D^0 D^- \frac{n_e^3}{N_e^2 \, n_i} \left[1 + exp\left(\frac{-0.39}{k_B T}\right)\right] \ (cm^2/s) \quad (4.10)$$

While $D^0 = D_i$

$$D^- = 4.44 \times 10^{21} exp\left(\frac{-4}{k_B T}\right) \quad (cm^2/s)$$

There are different opinions about interstitial mechanism is proposed to play important role in phosphorus diffusion. It is observed that oxidation of silicon strongly influence on the diffusion of phosphorus. Some experiments were performed in order to know prominent diffusion mechanism among the vacancy and interstitial mechanism. According to evidences simultaneous diffusion take places through vacancy under saturation and self-interstitial in super saturation conditions and concluded that conversion of P interstitialcy to substitutional form is due to emission of self-interstitials [7-8].

At lower electron concentration when Fermi level is about 0.11eV below the conduction band, $V^=$ give up an electron and lower binding energy of resulting $P^+ V^-$ pair enhances the probability for pair dissociation. This effect creates steady state excess of concentration of V^- vacancies which flow away from point of pair dissociation and interact with phosphorus to enhance the tail diffusion. In npn structure, Fair and Tsai propose charge state of vacancies become V^+ in the base region and enhancing the diffusivity of the base dopant. By Fair and Tsai model which is reinforced by Willoughby model [15] concluded that the cause of phosphorus tail and emitter push effect are very closely linked. It is well characterized enhancement factors now allow the process design of double diffusion process to be accepted on a comprehensive basis. However effect of emitter surface concentration is still uncharacterized and need a comprehensive study of function of total and electrically active phosphorus concentration.

4.1.7 Solid Solubility of P in Silicon:

Maximum amount of P which can be diffuse into silicon lattice has been investigated, there is a solubility limit, above that limit no more P is can diffuse into silicon lattice. Above solubility limit, precipitation of monoclinic and orthorhombic *SiP* particles takes place in the doped regions or on the surface [9].

$$Si + P \rightarrow \rightarrow \rightarrow SiP \quad (4.11)$$

The P which is deposited in form *SiP* in doped regions appear in the form of inactive P, this inactive P forms a point defects or E centers. E center is a pair of phosphorus atom with a charged or neutral vacancy. As a result dopant appear electrically inactive, if phosphorus is inactive, it does not contribute to current or charge transport. All inactive phosphorus atoms act as a defects which increase the recombination losses, as a result open circuit voltage decrease [10]. Silicon surface which contain electrically inactive dopants at the

surface or near to surface commonly called as dead layer. Many investigators have investigated the presence of SiP in order to know active concentration and inactive concentration of phosphorus in the superficial layer and in the depth [11]. By using following equation (4.12 and 4.13) we can calculate active phosphorus (n_e), saturation concentration (C_{sat}) and inactive mobile concentration ($C_{sat} - n_e$) at specific temperature. Curves obtained from these equations are plotted in figure 4.5.

$$n_e(T) = 1.3 \times 10^{22}\, Exp\left(\frac{-0.37}{k_B T}\right)\ (cm^{-3}) \tag{4.12}$$

$$C_{sat}(T) = 2.45 \times 10^{23}\, Exp\left(\frac{-0.62}{k_B T}\right)\ (cm^{-3}) \tag{4.13}$$

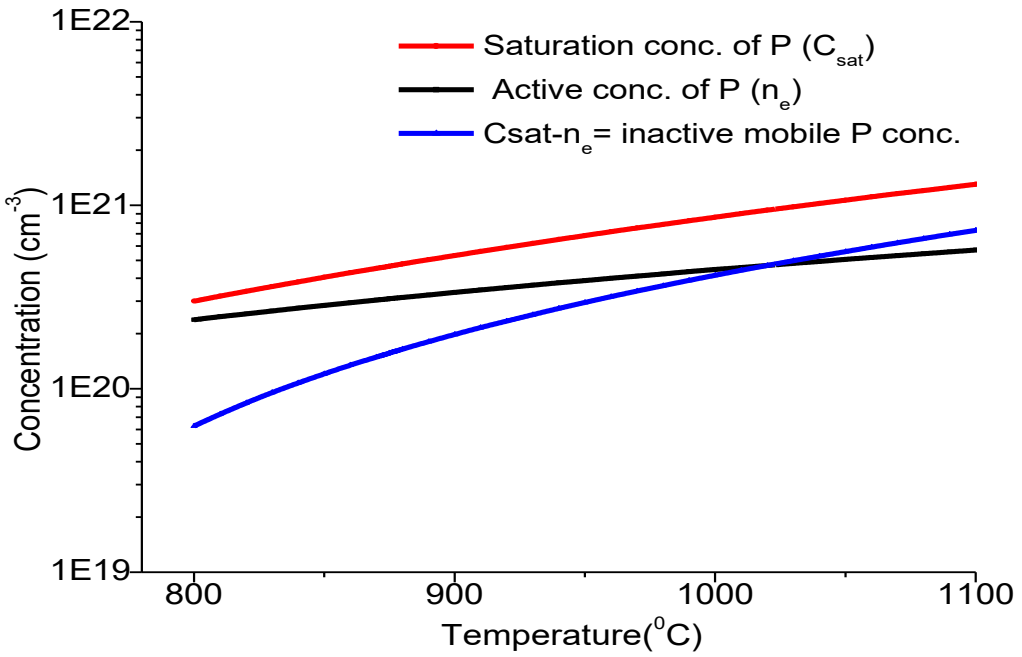


Figure 4.5 Active phosphorus, saturation and inactive mobile phosphorus concentration.

Fair and Tsai model is used to calculate the electrically inactive phosphorus (total concentration of phosphorus) and also for kink and tail doping profile [6]. This model is used to explain the phosphorus diffusion into silicon by interacting with vacancies in 3 different charge states, which can be represented as $P^+V^\times$, P^+V^- and $P^+V^=$ where $V^\times$ is neutral vacancy. When concentration of phosphorus is higher than Ne (as shown in Fair and Tsai model plot) then $P^+V^=$ will be dominate. In this case, electron will be removed from conduction band by $P^+V^=$ pair and reform the second accepter level of vacancy generating an electrically inactive phosphorus atom. It is concluded that when concentration is approximately similar to Ne , then $V^=$ vacancy has high probability to lose an electron and become V^- thus lower binding energy of P^+V^- pair enhances probability of pair to dissociate into to excessive V^- above the equilibrium values. Latter is responsible for enhanced diffusion in the tail region. It is concluded that vacancy mechanism occurs during slow diffusing components and insterstitialcy mechanism occurs during fast diffusion. Electron concentration in flat zone (at solid solubility level) is a function of temperature only and independent of source or surface concentration. The super saturation of P arises from

the fact that a part of PSG during diffusion and atomic P is formed exceeding solid solubility. Thus precipitate of SiP is formed [12-13].

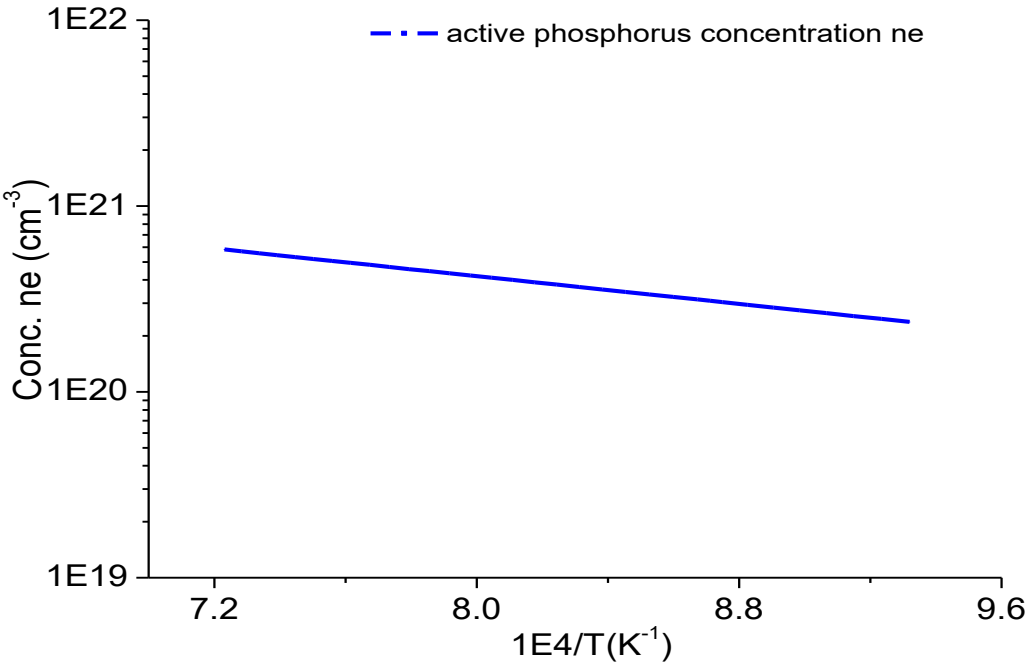


Figure 4.6 Electron concentration n_e at which diffusivity becomes proportional to n^2 vs 1/T.

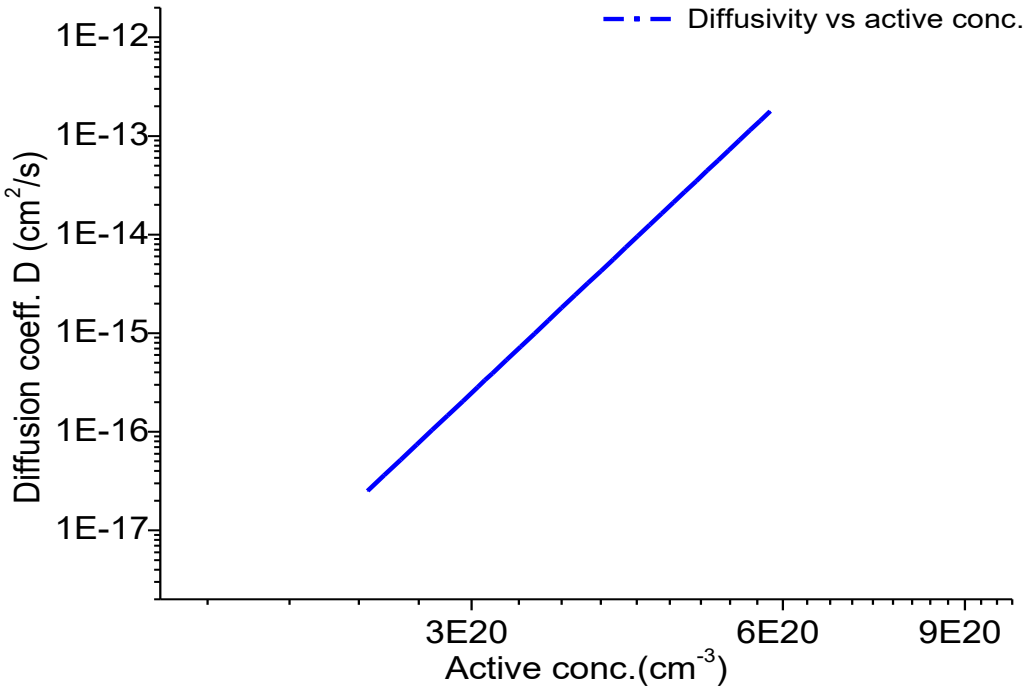


Figure 4.7 Phosphorus diffusivity (diffusion coefficient) vs. electron concentration in silicon

Arrhenius plot of diffusivity D as function of temperature for shallow impurities in Silicon can be used to calculate energy of activation E_d and average nature, independence of

concentration. They are calculated by diffusing impurities into silicon of opposite to background dopant, to form a PN junction. Energy of activation for different dopant is given in literature [16].

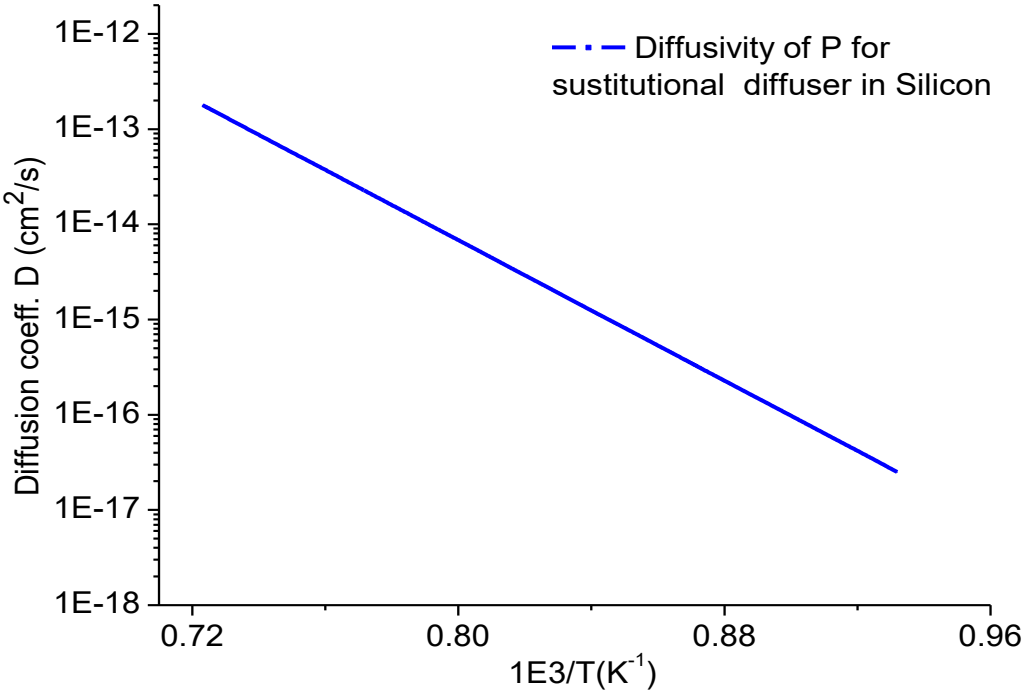


Figure4.8 Arrhenius plots of diffusion coefficient vs. 1/T

4.2 Objective of P diffusion:

The objective of this work was to get lowly (softly) doped and deep emitters for high efficiency solar cells. High efficiency silicon solar cells are related to low recombination currents and high open-circuit voltages. Parameters which are used for emitter's characterization are sheet resistance (R_s), surface impurity concentration (N_s) and junction depth. , In this work we have performed several experiments in order to study the effect phosphorus diffusion on emitters under different temperature (800, 820,840 and 875 ^{0}C) to get shallow and deep n+ emitters. The emitter saturation current density which limits the open circuit voltage depends on active phosphorus concentration and junction depth. Due to high temperature, P diffusion form dead layer which increased Auger recombination and decrease overall cell efficiency. For high quality emitters, we have investigated phosphorus diffusion process in which oxidation step is incorporated during diffusion to reduce J_{oe} values for softly doped emitters with moderate surface concentration values and to get deep junction depth. A wet oxidation step is used to minimize the dead layer and the peak surface concentration. Effects of both dry and wet oxidation on phosphorus diffusion are investigated in this work.

4.3 Phosphorus diffusion (800- 875ºC)

4.3.1 Phosphorus Pre-deposition

For P diffusion p-type monocrystalline Cz-Silicon ($\rho = 0.8\,\Omega \cdot cm$; thickness= $150\mu m$) with base doping N_{base} = $1.92\text{E}16\ \text{cm}^{-3}$ and size $10\ cm \times 10\ cm$ has been taken for

processing after chemical etching and cleaning. P pre-deposition is carried out at 800-875^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under following conditions as shown in table 4.1. It is common to perform phosphorus diffusion in two-steps, pre-deposition and drive-in. In this work we have introduced a step of wet oxidation between phosphorus pre-deposition and drive-in in order to remove the dead layer or area which is not electrically active, which originates during emitters formation. Numerous phosphorus diffusion processes are carried out at various temperatures from 800 °C to 875 °C in order to get doping uniformity for different set of wafers. Usually wafers were loaded in the middle of the boat (carrier for wafers) to avoid the problem of inhomogeneous distribution. The proper position of the boat with wafers within the furnace is also important for maximum and uniform interaction of carrier gases with doping material. In our experiments, we had placed wafers at the last zone of furnace where carrier substrates were entering into the furnace, to seek that the flow is adequate to obtain uniform doping. There was one drawback in this process, wafers had a greater influence of flow on bottom. As a result, there was more doping at position 4 than position 2 in the wafer area.

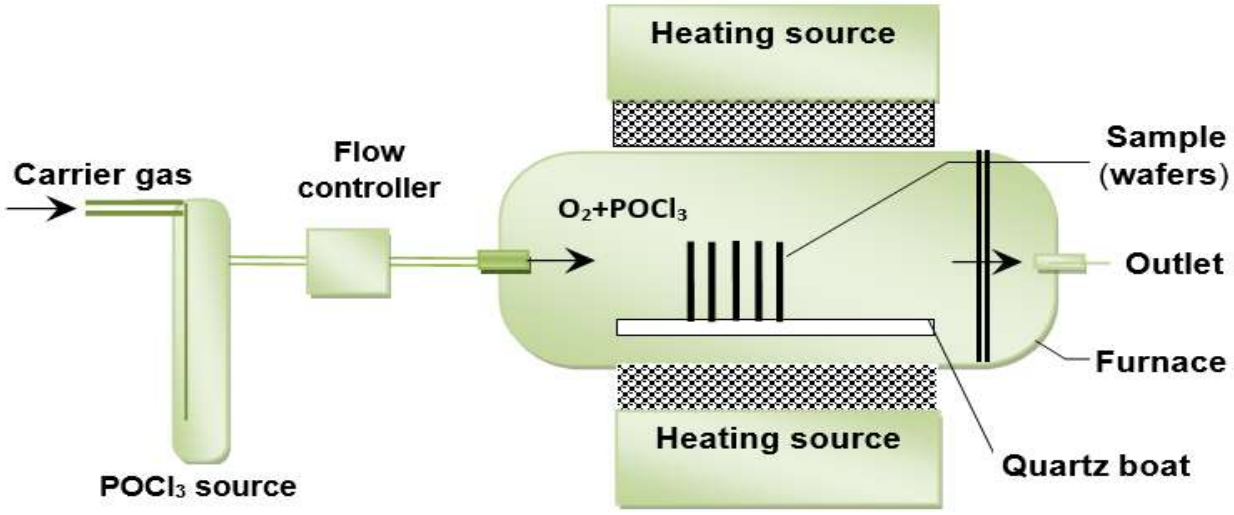


Figure 4.9 Flow sheet representation of phosphorus diffusion furnace.

We have performed series of experiments of P diffusion under different conditions of temperature and in some cases with different gaseous flow. Phosphorus diffusion is carried out at different temperatures ranging from 800ºC to 875^{0}C. During this process when temperature reached at 750 ^{0}C, then wafers were loaded in order to start the process. The flows of gases are in following order table 4.1:

Table4.1

Steps	Time in minutes (T in ºC)	Gases flow
wafers loading	5minutes at (750^{0}C)	N_2 6 *l*/min +O_2 0.1 *l*/min
Stabilization	5-15 (800-875^{0}C)	N_2 6*l*/min +O_2 0.1 *l*/min
Bubbler temperature and flow rate. 20 ^{0}C		240 cc/min N_2/$POCl_3$
Doping	30 (800-875^{0}C)	N_2 6 *l*/min +O_2 0.1 *l*/min +
Oxidation	5 (800-875^{0}C)	O_2 2 *l*/min

Exit (wafers unloading)	5 (750^{0}C)	N_2 2 *l*/min

$$2POCl_3 + O_2 \longrightarrow 2P_2O_5 + 3Cl_2$$

$$2P_2O_5 + 5Si \longrightarrow 4P + 5SiO_2$$

At 750^{0}C we took out the boat (carrier) from furnace with the help of long glass rod by using safety gloves and adjusted the wafers in the boat carefully with at least 4 mm distance between wafers. After that we introduced (put) wafers into furnace carefully by using handle of boat and protective gloves. During introduction of wafers into furnace, a care should be taken in handling of wafers in the furnace especially at high temperature in order to avoid cracks. At same temperature and gaseous flow allow wafers to homogenize in the furnace for 5-15 minutes. This step is for stabilization of wafers inside the furnace and to get desire temperature. At adjusted diffusion temperature, process were started and N_2 flew through bubbler (flask containing $POCl_3$) for 30 minutes at the rate of 240cc/min. This step is called pre-deposition. After 30 minutes according to programmed recipe, flow of nitrogen stopped automatically and flow O_2 gas started at the above mention rate for 5 minutes and also stopped the flow of nitrogen through the bubbler. This is called oxidation step. After oxidation phosphorus neither diffuses into the wafers nor effuses outside the wafers. After 5 minutes, programmed recipe stop the flow of O_2 and open again start the flow of N_2 for stabilization and to decrease the temperature to take the wafers out of furnace. After that wafers were taken out of the furnace by using long glass rod. Move boat very slowly inside the furnace, sometime fast movement of boat with wafers inside the furnace can produce (introduce) cracks due to high temperature stress. [17-18]

4.3.2 Oxidation and drive in process

As we have mentioned we have used p-type wafers of 0.8 Ω.cm resistivity for phosphorus diffusion at different temperatures (800, 820, 840 and 875 ºC). For each diffusion temperature for 4 sets of five wafers were processed under above mentioned conditions of P diffusion and their sheet resistance (Ω/□) were measured after processing. One from each set of wafers is maintained with the corresponding diffusion process (diffusion temperature), three of them (each set) were used to perform wet oxidation at 950 °C for three different time duration (10, 15 and 20 minutes) last wafer of each set were processed with wet oxidation for drive-in process. Detail of each process is given in table 4.2. Drive in process was carried in oxidation furnace. N_2 gas flow 2*l*/min was selected from beginning of furnace to get 950^{0}C (Nitrogen gas flow is optional in beginning). After Phosphorus pre-deposition, wafers were divided in 5 sets for different oxidation time and drive in process.

- Wafer 1, only doping without drive-in.
- Wafer 2, after doping, 60 minutes drive-in only.
- Wafer 3, after doping, 10 minutes wet oxidation+ HF + 10 minutes dry oxidation, 60 minutes drive-in.
- Wafer 4, after doping, 15 minutes wet oxidation + HF+ 10 minutes dry oxidation with 60 minutes drive-in.

- Wafer 5, after doping, 20 minutes wet oxidation + HF+ 10 minutes dry oxidation 60 minutes of drive-in.

Table 4.2. Characteristics of different process variations which were completed for each diffusion temperature 800, 820, 840 and 875ºC

Diffusion (ºC)	Process (time in minutes)
800(ºC)	Diffusion
	Diffusion + wet oxidation (10, 15 and 25 minutes)+ dry oxidation (10 minutes)+ 1hour drive-in
	Diffusion + dry oxidation (10 minutes)+ 1hour drive-in
820(ºC)	Diffusion
	Diffusion + wet oxidation (10, 15 and 20 minutes)+ dry oxidation (10 minutes)+ 1hour drive-in
	Diffusion + dry oxidation (10 minutes)+ 1hour drive-in
840(ºC)	Diffusion
	Diffusion + wet oxidation (10, 15 and 20 minutes)+ dry oxidation (10 minutes)+ 1hour drive-in
	Diffusion + dry oxidation (10 minutes)+ 1hour drive-in
875(ºC)	Diffusion
	Diffusion + wet oxidation (10, 15 and 25 minutes)+ dry oxidation (10)+ 1hour drive-in
	Diffusion + dry oxidation (10 minutes)+ 1hour drive-in

During drive-in with oxidation process gaseous flow and time is given below in table 4.3;

Table 4.3

Step	Gases flow (time)
Entrance wafers loading)	N_2 2 *l*/min (optional) (5 minutes)
Wet oxidation	N_2 2 *l*/min+ O_2 2 *l*/min + O_2 through water flask (10-25 minutes)
HF	Wafers are taken out to remove dead layer
Dry Oxidation	N_2 2 *l*/min+ O_2 2 *l*/min (10 minutes)
Drive-in	N_2 2 *l*/min (1h=60 minutes)

During drive in process each set of wafers are processed separately.

4.4 Oxidation Process:

In microelectronics, the term oxidation is used to convert silicon material into silicon dioxide. In silicon solar cell fabrication, oxidation is used to convert a layer of silicon into

silicon dioxide layer. There are two different methods used in microelectronics to covert silicon layer into silicon dioxide.

Thermal oxidation
Electrochemical oxidation

Deposition of silicon dioxide layer by chemical vapor deposition is not considered as oxidation process. In silicon solar cell fabrication and industrial fabrication oxidation is carried by thermal process, it is similar process like doping of N-type or P-type material which are added into silicon to modify its properties. Silicon oxide have most important application in microelectronics. In CMOS transistor, oxide is essential component which is used as gate (dielectric layer) to separate two terminals of transistors. Silicon dioxide layer acts as a passivation layer to protect the silicon surface and a good insulator used between wires and transistors. When silicon is exposed to air or moisture, it automatically form a thin layer of silicon oxide by aerial oxidation in range of 2 nm thick. It is recommended that wafers must be clean by HF before processing.

There are two types of thermal oxidation,

Wet oxidation
Dry oxidation

Chemical reactions for dry oxidation and wet oxidation is given below.

Reaction for dry oxidation $Si + O_2 \rightarrow\rightarrow\rightarrow SiO_2$

For wet oxidation $Si + 2H_2O \rightarrow\rightarrow\rightarrow SiO_2 + 2H_2$

When silicon react with oxygen, it produces silicon dioxide (SiO_2) which is also called silica. In case of monocrystalline, silicon dioxide produced by dry oxidation have higher density than amorphous silicon. In wet oxidation water vapors are introduced into oxidation furnace system by a carrier gas which is nitrogen or oxygen into the bubbler filled with de-ionized water at fixed temperature (95°C). In wet oxidation process structured produced by chemical reaction of silicon with water vapors is more porous than pure silicon dioxide. For highly good quality surface, dry oxidation process is recommended. Still wet oxidation is a good process to grow silicon oxide very quickly as compare to dry oxidation. It is frequently used for growing sacrificial oxides (oxides to be grown at later stage of process, or later it will be removed (sacrificed). Since it is not going to be a part of permanent structure [16].

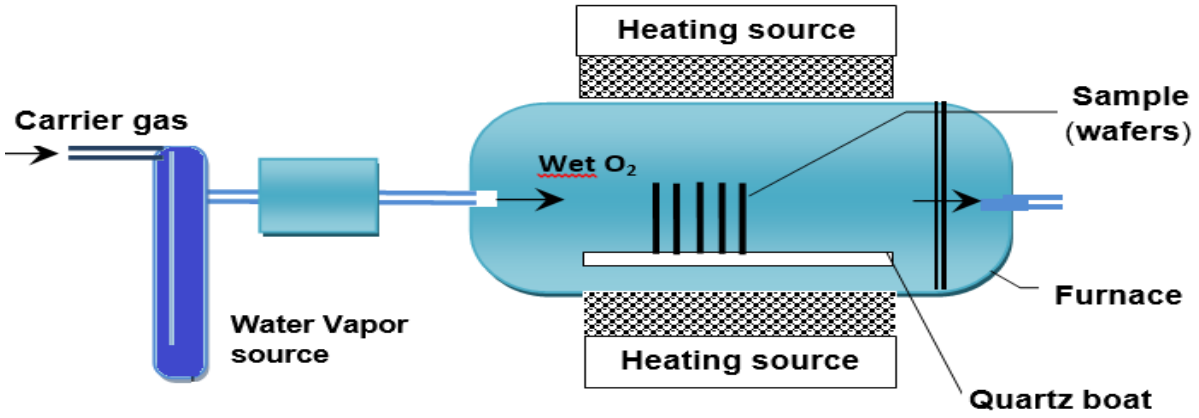


Figure 4.20 Systematic representation of furnace used for wet oxidation.

Furnace which we have used for oxidation is suitable for both dry and wet oxidation process for growth of oxides. In the dry oxidation method, oxygen gas is allowed to pass into the quartz tube. During this process, high-purity gas is used to ensure that no unnecessary impurities are incorporated in the layer of oxides. In the wet oxidation method, the water vapor are introduced into the furnace system is created by flowing a carrier gas into a container or bubbler (flask) filled with de-ionized water and maintained at a constant temperature below its boiling point (95 °C). As the carrier gas passed through the water, it became saturated with the water vapor. The distance to the quartz oxidation tube must be short enough to prevent water vapors from condensation. The bubbler used in the wet oxidation process are simple and quite reproducible, but it has disadvantages associated with the fact that with passage of time, its level decrease, we have to refill it from time to time [16]. Proposed processes of P diffusion with oxidation at different temperature with sequence of all steps are shown in flow sheet diagram 4.11.

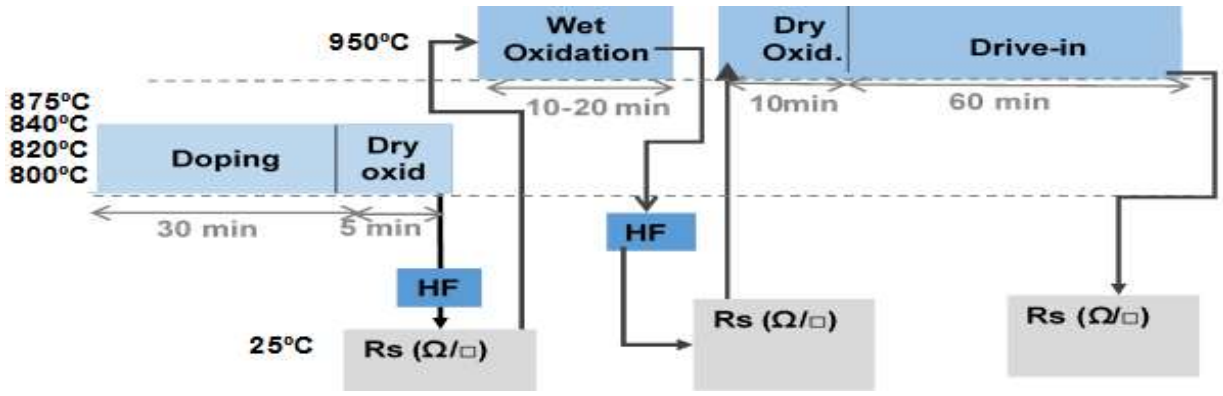


Figure 4.11. Flow sheet diagram for the proposed processes, a sequence of all the steps used in P pre-deposition with drive-in to corresponding temperature with time description.

4.4.1 Calculation for growth of silicon oxide in wet and dry oxidation

$$x^2 + Ax = B(t + \tau) \tag{4.14}$$

For shorter time, $t \downarrow\downarrow \rightarrow parabolic$ $x^2 \cong B(t + \tau)$

For longer time, $t \uparrow\uparrow \rightarrow linear$ $x \cong \frac{B}{A}(t + \tau)$

"x" is thickness of oxide, *t* is time of oxidation, τ this quantity corresponds to shift in time coordinate, which corrects the initial thickness of oxide at t=0

Detail of above equation and oxidation process and oxide growth mechanism is given reference [16]. In this work, we have calculated theoretically and experimentally thickness of oxide layer at 950 ºC for 10 to 25 minutes both dry and wet oxidation process.

First we have calculated coefficients (B/A) and B for both dry and wet oxidation, in order to calculate the thickness of oxide growth.

4.4.1.1 Wet Oxidation

$$\left(\frac{B}{A}\right)_{wet} = C_2 exp\left(\frac{-E_2}{kT}\right) \tag{4.15}$$

$C_2 = \left(9.70x10^7 \frac{\mu m}{h}\right)$

$E_2 = 2.05eV$

$$\left(\frac{B}{A}\right)_{wet} = \left(9.70x10^7 \frac{\mu m}{h}\right) exp\left(\frac{-2.05eV}{kT}\right)$$

$$\left(\frac{B}{A}\right)_{wet} = \left(9.70x10^7 \frac{\mu m}{h}\right) exp\left(\frac{-2.05eV}{8.61\ 10^{-5} \cdot 1223}\right) = 0.340$$

$$(B)_{wet} = C_1 exp\left(\frac{-E_1}{kT}\right) \tag{4.16}$$

$C_1 = \left(386 \frac{\mu m^2}{h}\right)$

$E_1 = 0.78eV$

$$(B)_{wet} = \left(386 \frac{\mu m^2}{h}\right) exp\left(\frac{-0.78eV}{kT}\right)$$

$$(B)_{wet} = \left(386 \frac{\mu m^2}{h}\right) exp\left(\frac{-0.78eV}{8.61\ 10^{-5} \cdot 1223}\right) = 0.234$$

In both case, oxidation for was carried at 950 ºC. (Wet and dry oxidation) [16]

4.4.1.2 Dry oxidation

$$\left(\frac{B}{A}\right)_{dry} = C_2 exp\left(\frac{-E_2}{kT}\right) \tag{4.17}$$

$C_2 = \left(3.71x10^6 \frac{\mu m}{h}\right)$

$E_2 = 2eV$

$$\left(\frac{B}{A}\right)_{dry} = \left(3.71x10^{6}\frac{\mu m}{h}\right) exp\left(\frac{-2eV}{kT}\right) = 0.03569$$

$$(B)_{dry} = C_1 exp\left(\frac{-E_1}{kT}\right) \tag{4.18}$$

$C_1 = \left(772\frac{\mu m^2}{h}\right)$

$E_1 = 1.23eV$

$$(B)_{dry} = \left(772\frac{\mu m^2}{h}\right) exp\left(\frac{-1.23eV}{kT}\right) = 0.00659$$

E_1& C_1 and E_2& C_2 values are taken from literature [16] in order to calculate the values of A and B. Values of A and B depend on the operating temperature. Linear and parabolic rate constants are exponentially related to temperature for both dry and wet oxidation process as in figure 4.12. Usually oxidation temperature range is from 900-1200 ºC.

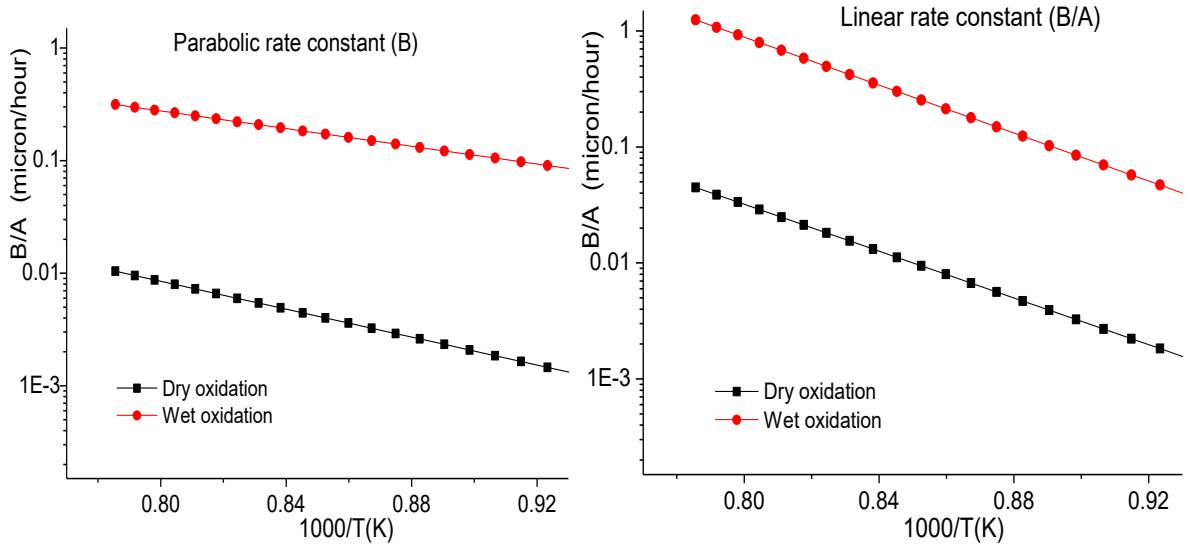


Figure 4.12 Arrhenius plot of linear and parabolic rate constants for dry and wet oxidation.

These coefficients A and B are applied to the oxide growth equation: By using this equation (4.19), we can calculate the thickness of oxide grown during oxidation process. This equation applied for both dry and wet oxidation process.

$$tox = \frac{B}{2\left(\frac{B}{A}\right)}\left[\sqrt{1+\frac{4\left(\frac{B}{A}\right)^2}{B}t} - 1\right] \tag{4.19}$$

$$tox = \frac{0.234}{2(0.340)}\left[\sqrt{1+\frac{4(0.340)^2}{0.234}t} - 1\right]$$

While *t* is the time for oxidation in hour. By using this equation, we have calculated thickness of oxide layer in oxidation process. Experimentally we have performed oxidation experiments at 950 ºC, for good estimation of oxidation behavior we have theoretically calculated thickness of oxide layer for different time duration as shown in figure 4.13 and 4.14. As I have mentioned early that we have used wet oxidation for 10 to 25 minutes, theoretically thickness of layer is given below for different time in table 4.4.

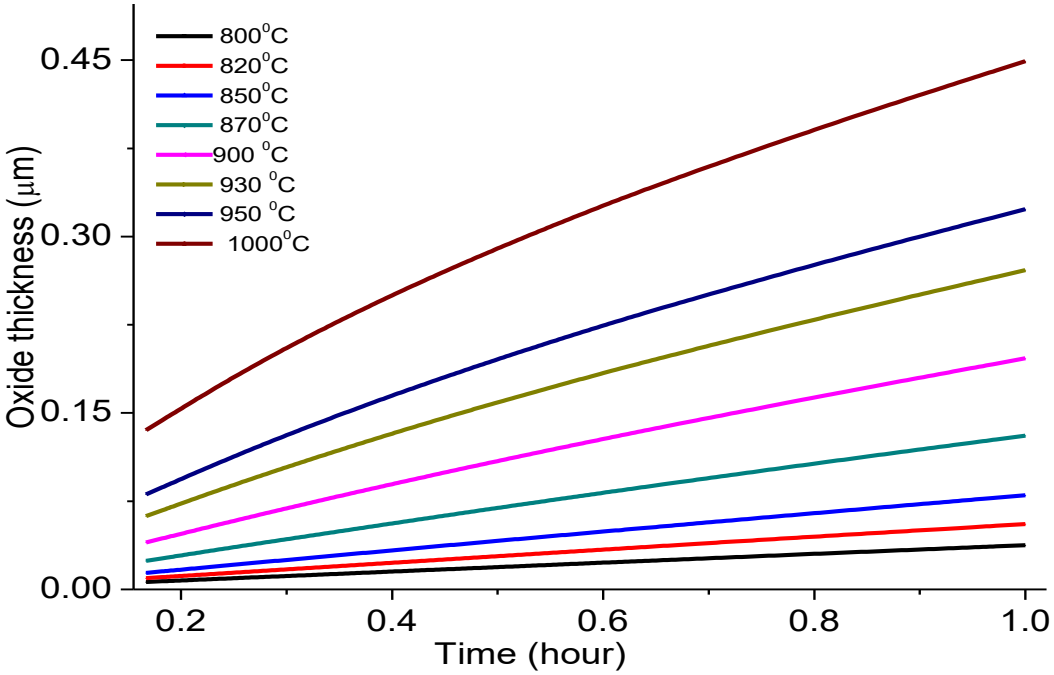


Figure 4.13. Growth of oxide by wet oxidation, growth of oxide which depends on temperature and time of the process. (Growth of oxide by wet oxidation process in µm).

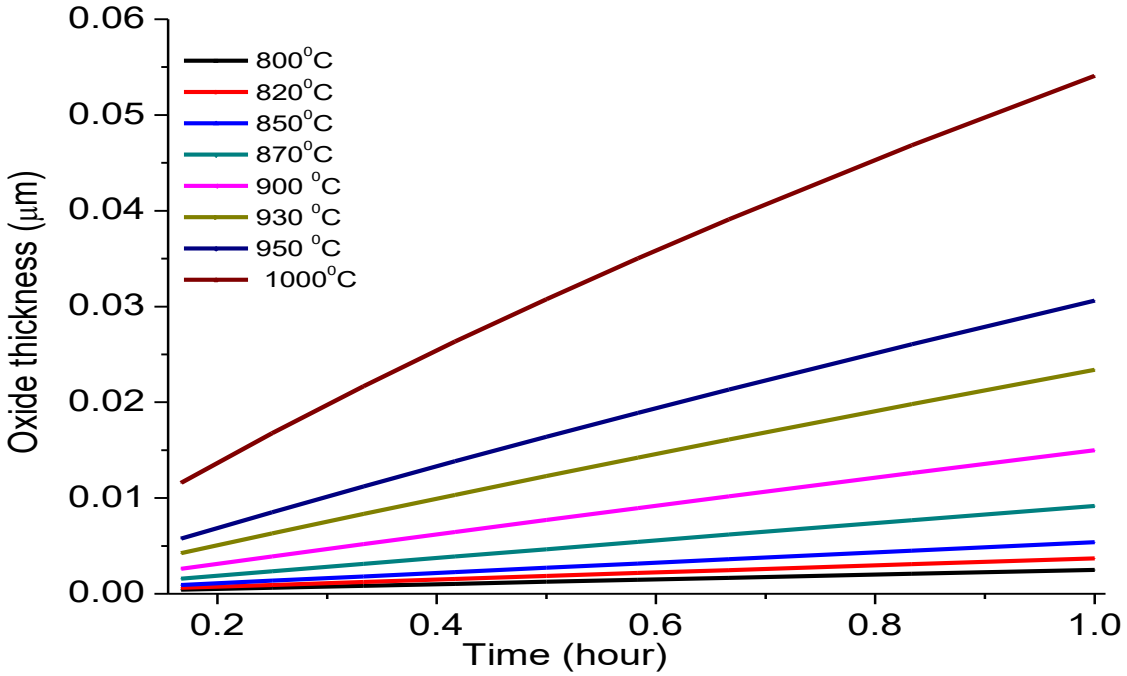


Figure 4.14 Growth of oxide by dry oxidation, growth of oxide which depends on temperature and time of the process. (Growth of oxide by dry oxidation process in µm).

Table 4.4 Growth of oxide layers in oxidation process for different time (theoretically).

Time (in Minutes)	Process	Thickness (nm)
10	Wet oxidation	53
15	Wet oxidation	77
20	Wet oxidation	97
10	Dry oxidation	6
15	Dry oxidation	8.5
20	Dry oxidation	11

After this wet oxidation, the ellipsometer is used to measure the resulting oxide layer. After that this oxide layer is removed by HF and difference in weight loss of silicon wafers were noted to calculate the thickness removal of oxide layer for each wafer. We measured the sheet resistance, *Rs* (Ω/□) of all wafers used in oxidation process. These wafers were processed for drive-in in an oxidation furnace, where dry oxidation was performed for 10 minutes with 1hour for drive-in at temperature of 950 °C. After drive-in sheet resistance of all wafers were measured again by four point probe instrument. Each wafer is measured at 5 different points of each surface as shown in the figure 4.15. Arrangement of the wafer position in the diffusion furnace and lower part shows 5 zones where *Rs* (Ω / □) is measured on wafer front and back surface.

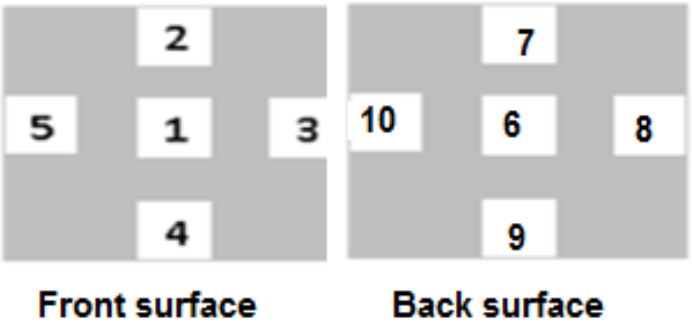


Figure 4.15 Points for wafer measurements

Experimentally thickness of oxide layer is measured by ellipsometer and also calculated by weight loss of silicon dioxide layer by HF for different temperature of phosphorus diffusion and oxidation. Results of both measurements are given in figures 4.16 and 4.17.

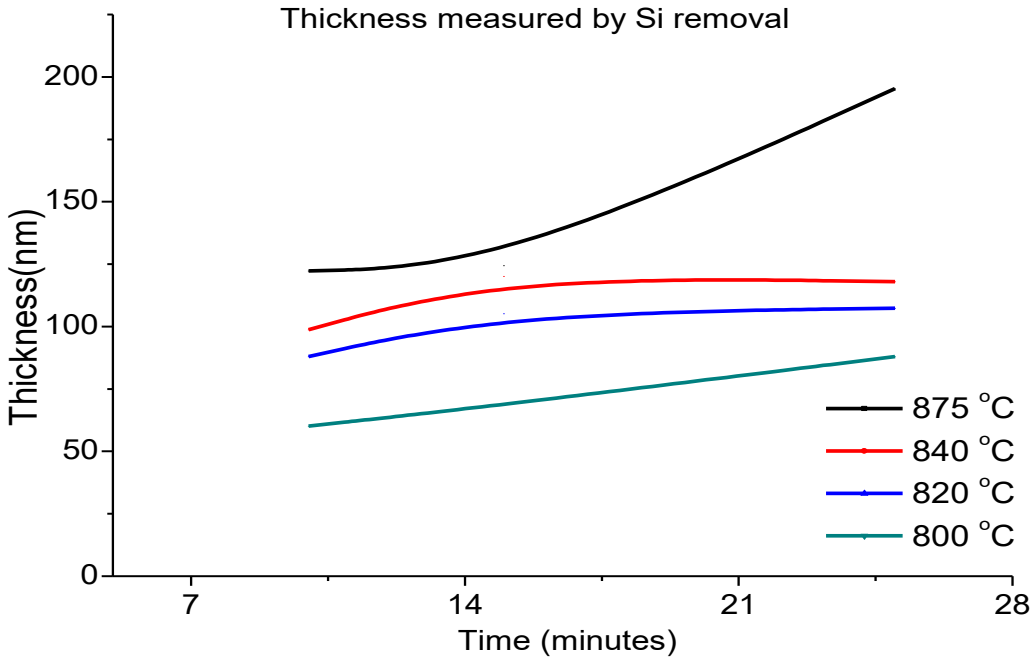


Figure 4.16 Growth of silicon dioxide during wet oxidation process, measured by Si removal.

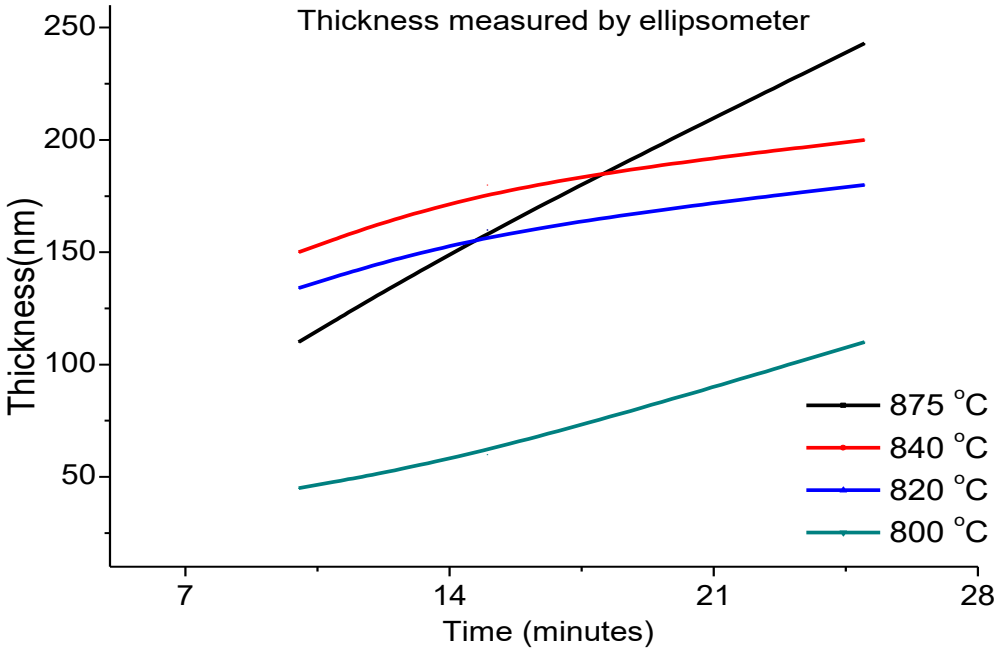


Figure 4.17 Growth of silicon dioxide during wet oxidation process, measured by ellipsometer

In table 4.5, the thickness of oxide obtained in the oxidation depends on the level of doping of the wafer in pre-deposition step and doping temperature. At high temperature diffusion, we had high values of doping concentration, as a result the thicker oxide layer, we obtained in wet oxidation. There is variation in observed thickness of oxides obtained and theoretically values due to difference in crystal orientation, base doping and surface concentration.

Table 4.5. Values of Rs (Ω/□) and thicknesses of oxide layers measured experimentally by ellipsometer.

Diffusion				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	220-294	73-192	50-62	27-35
Wet oxidation				
10 Minutes (Option A)				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	214-320	46-66	47-56	30-45
Thickness oxide layer experimentally (nm)	40-50	138-144	140-160	85-110
15 Minutes (Option B)				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	199-297	46-6	40-58	27-34
Thickness oxide layer experimentally (nm)	63-55	170	180-190	144-160

20 Minutes (Option C)				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	203-300	60-126	37-52	27-30
Thickness oxide layer experimentally (nm)	105-115	165-190	180-210	250-285
Dry oxidation (10 Minutes) + Drive-in (1hour)				
From option A (10 Minutes)				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	245-414	38-71	38-50	22-54
From option B (15 Minutes)				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	222-325	44-52	31-52	20-31
From option C (20 Minutes)				
Temperature	**800 ºC**	**820 ºC**	**840 ºC**	**875 ºC**
Rs (Ω/□)	221-355	64-143	32-60	18-22

In case of dry oxidation, growth of silicon dioxide layer was very thin, it was difficult to measure by ellipsometer.

During diffusion and drive-in process, wafers were evaluated by measuring their sheet resistance of each process at each step (for given temperature of diffusion). Sheet resistance data and concentration is given in the graphs below in figure 4.18, 4.19 and 4.20.

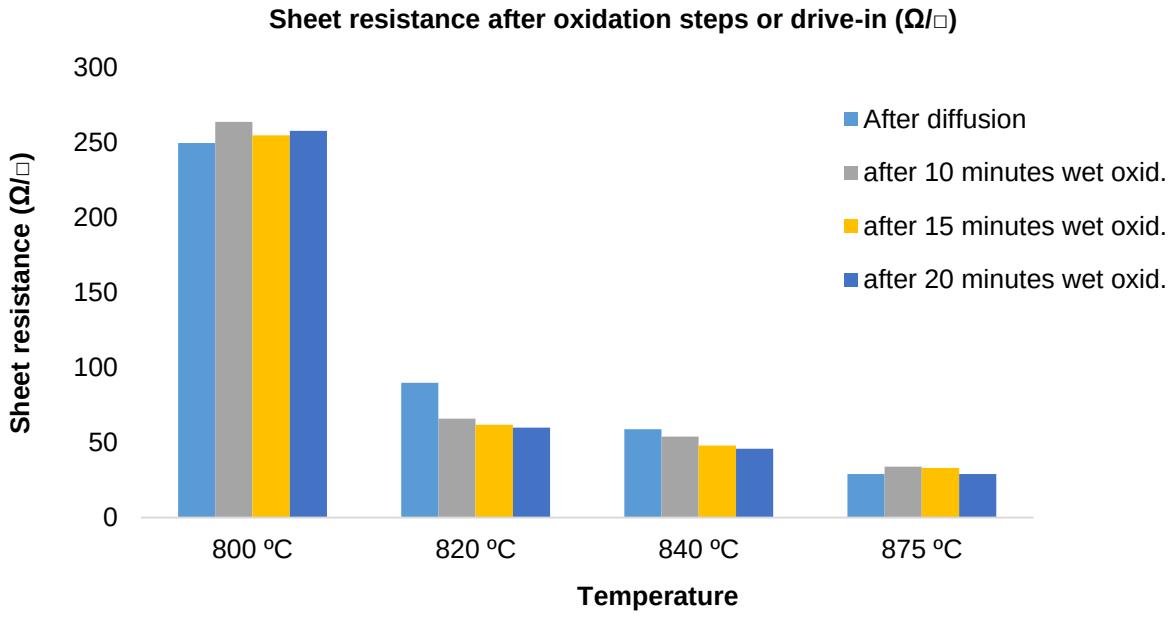


Figure 4.18 Sheet resistance values of silicon wafers resulted after P diffusion at different temperatures (a) after phosphorus diffusion (b) after 10 minutes, 15 minutes and 20 minutes of wet oxidation.

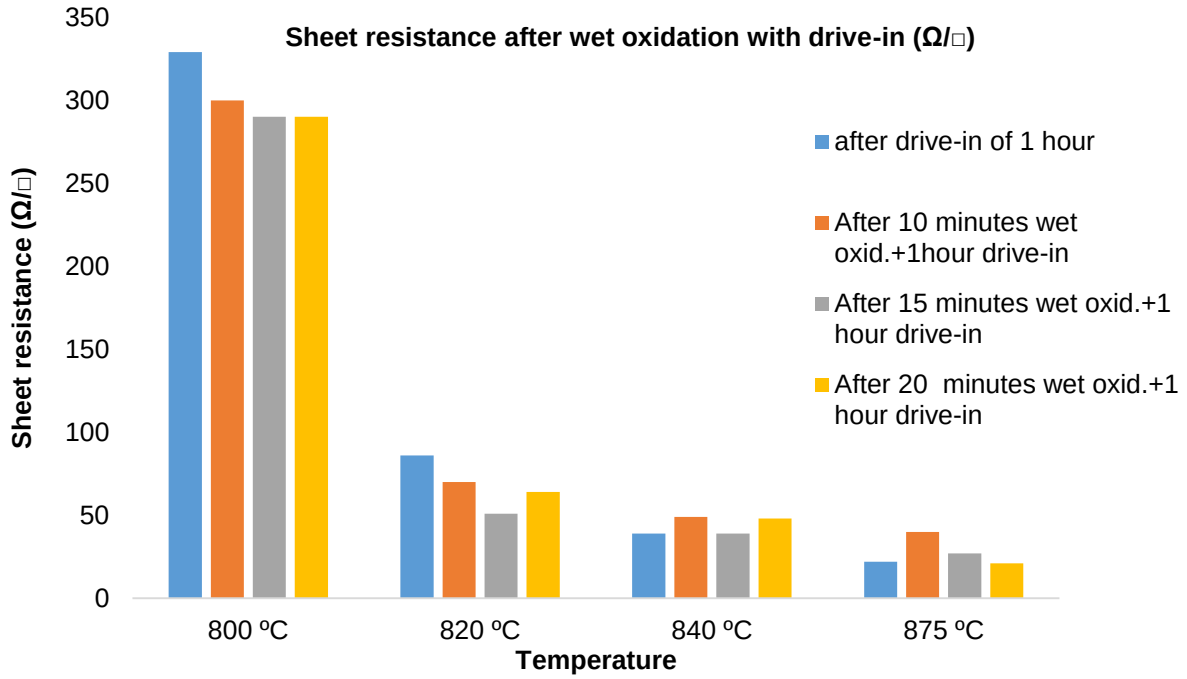


Figure 4.19 Sheet resistance values of silicon wafers resulted after P diffusion at different temperatures (a) after phosphorus diffusion with drive-in (b) after 10 minutes, 15 minutes and 20 minutes of wet oxidation and one hour of drive-in in nitrogen ambient.

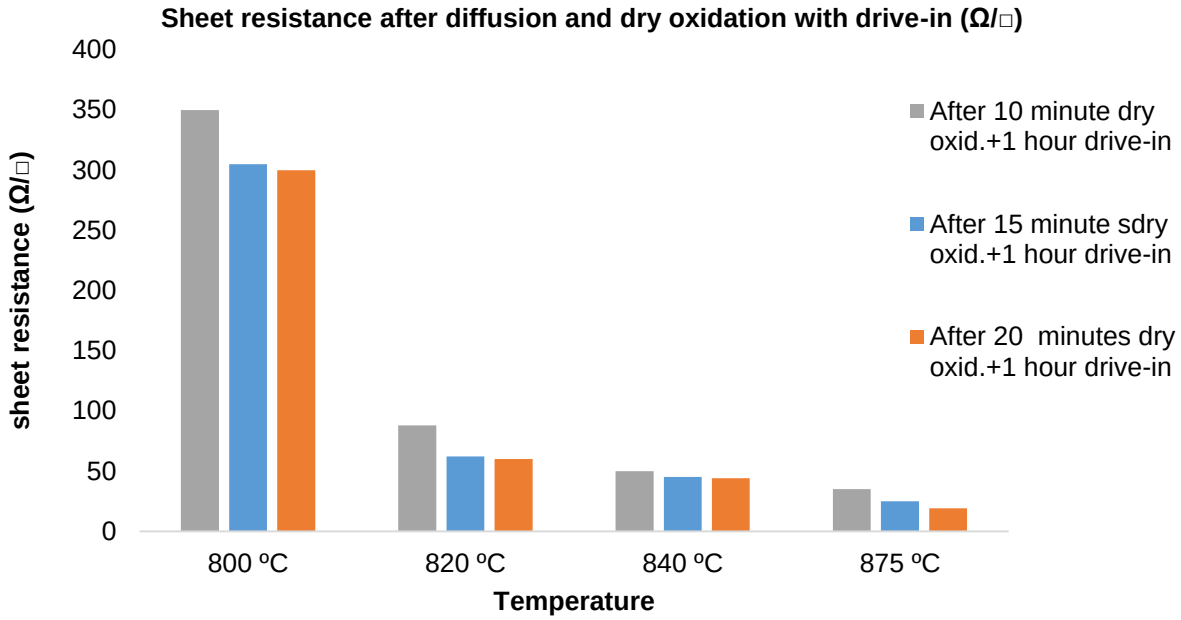


Figure 4.20 Sheet resistance values of silicon wafers resulted after P diffusion at different temperatures (a) after phosphorus diffusion with drive-in (b) after 10 minutes, 15 minutes and 20 minutes of dry oxidation and one hour of drive-in in nitrogen ambient.

Surface concentration of dopant for emitters resulted after phosphorus diffusion at different temperature after following steps (a) after phosphorus diffusion (b) P diffusion and 10 minutes of dry oxidation with one hour of drive-in (c) after 10 minutes, 15 minutes and 20 minutes of wet oxidation with drive-in (in N_2 gas) are given in the figure 4.21.

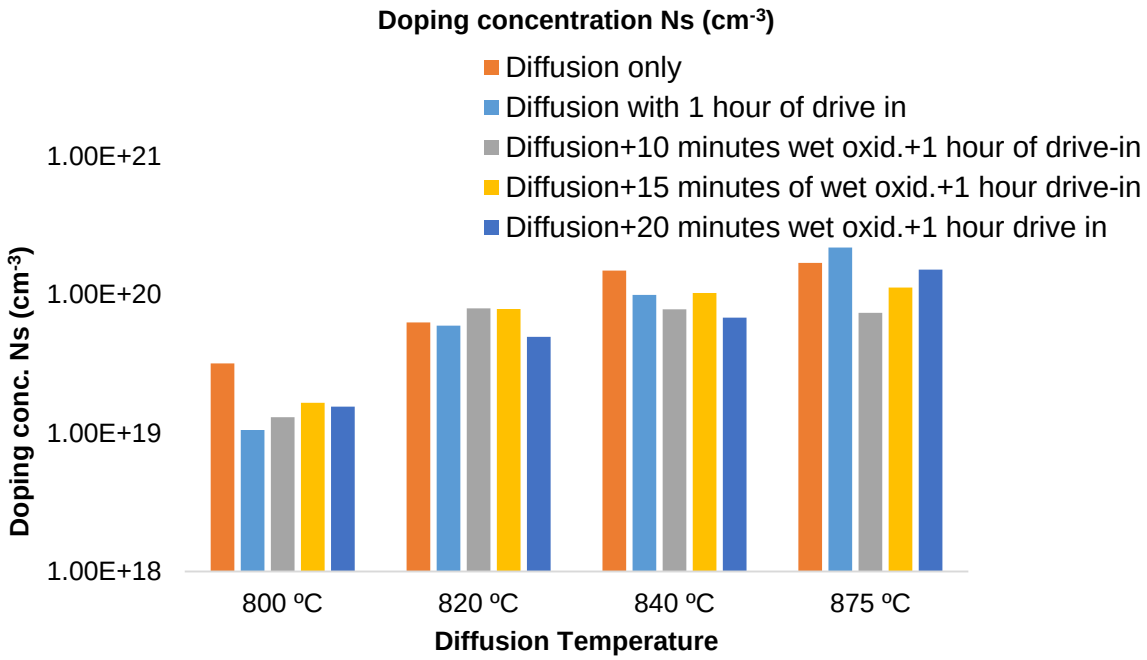


Figure 4.21 Surface concentration of dopant for emitters resulted after P diffusion at different temperature (a) after phosphorus diffusion (b) P diffusion and 10 minutes of dry oxidation with one hour of drive-in (c) after 10 minutes, 15 minutes and 20 minutes of wet oxidation with drive-in (N2 gas).

4.5 Diffusion profiles

After Phosphorus pre-deposition and drive-in process, etching was carried out in order to determine the junction depth and impurities concentration N_s (at/cm^{-3}). For this purpose selective etching was carried out in very dilute concentration of 2% NaOH at 60 ^{0}C. After 15 second etching, (about ~50 nm thickness of each surface of wafer is removed in this short etching time). Wafers were cleaned and dried to measure the sheet resistance of exposed surface by 4-point probes. This process is repeated again and again until sheet resistance shows complete removal of emitters and sheet resistance values were similar to base doping. In this way we can estimate the junction depth.

Finally, the calculation of N_s is carried out by PC1D, using a Gaussian model with values of the sheet resistance for the corresponding values of junction depth. It helped us to obtain the doping profiles of the emitters. We can calculate charge of emitter at specific in phosphorus doped region. Image of PC1D screen is shown in figure 4.22.

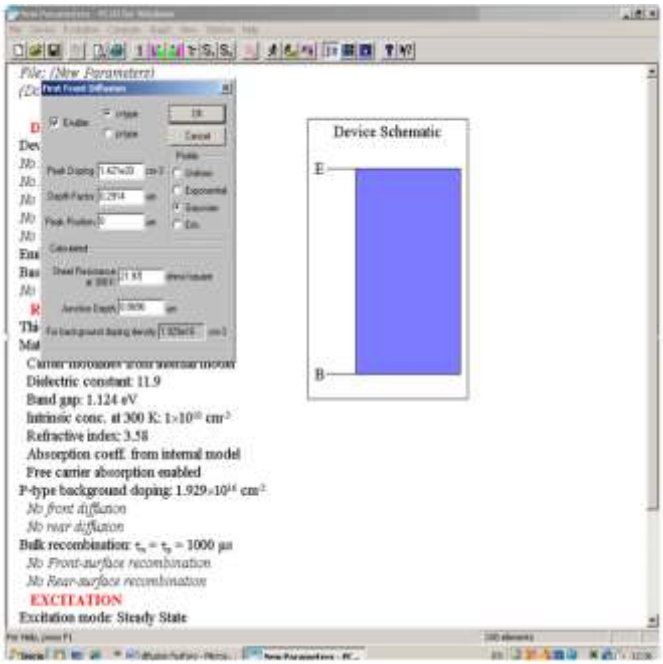


Figure 4.22 PC1D program screen page, used to calculate surface concentration.

By this PC1D program, doping concentration for various diffusion profiles of phosphorus emitters at 4 different temperatures under different oxidation and drive-in conditions are calculated. Emitters which are obtained through phosphorus diffusion with wet oxidation and drive-in are deeper than the emitters obtained normal phosphorus diffusion. As it is mentioned early that 4 different diffusion temperatures are processed with different duration of dry and wet oxidation time in order to get deep and lightly doped emitters. Diffusion profiles of all temperatures with different oxidation conditions and drive-in are shown below in figures 4.23-4.26.

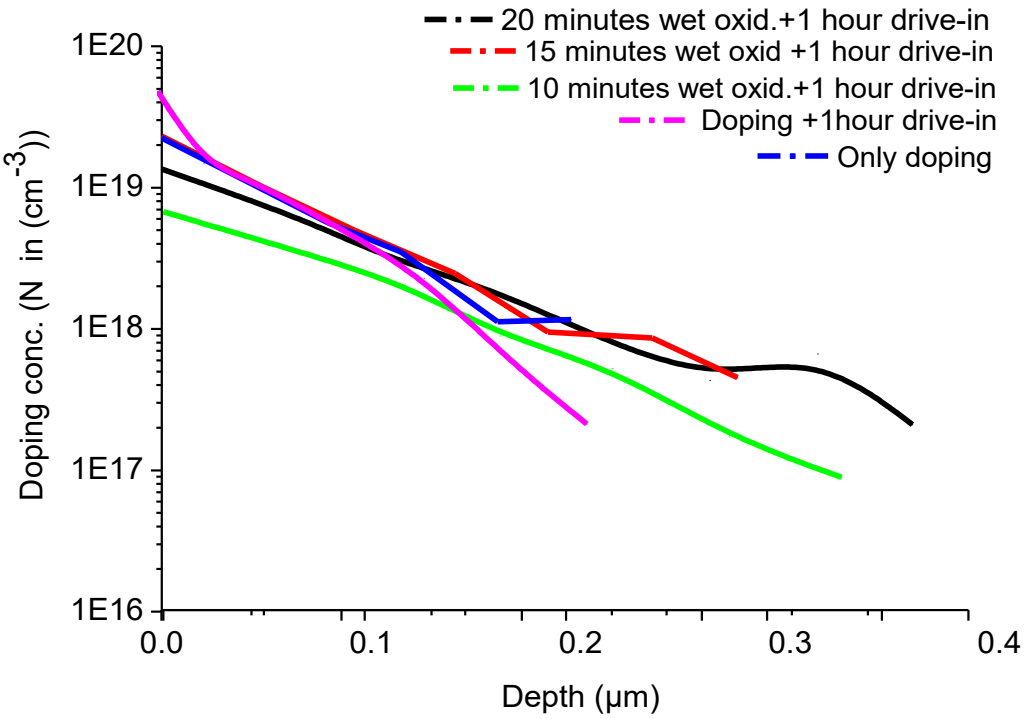


Figure 4.23 P diffusion profiles for 800 ºC

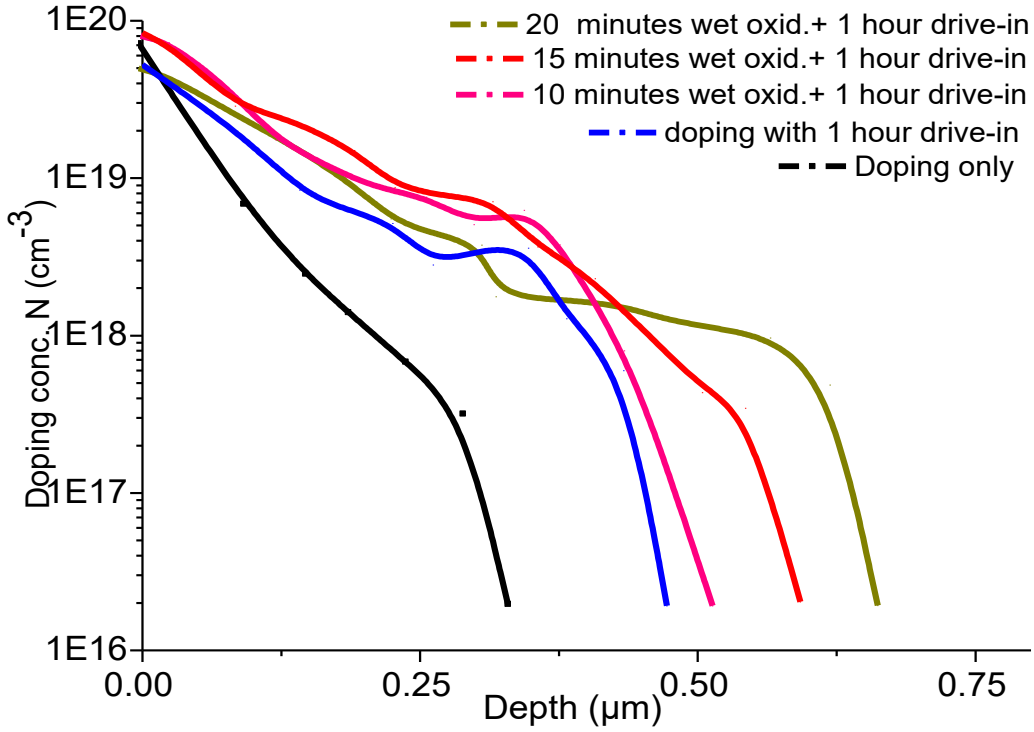


Figure 4.24 P diffusion profiles for 820 ºC

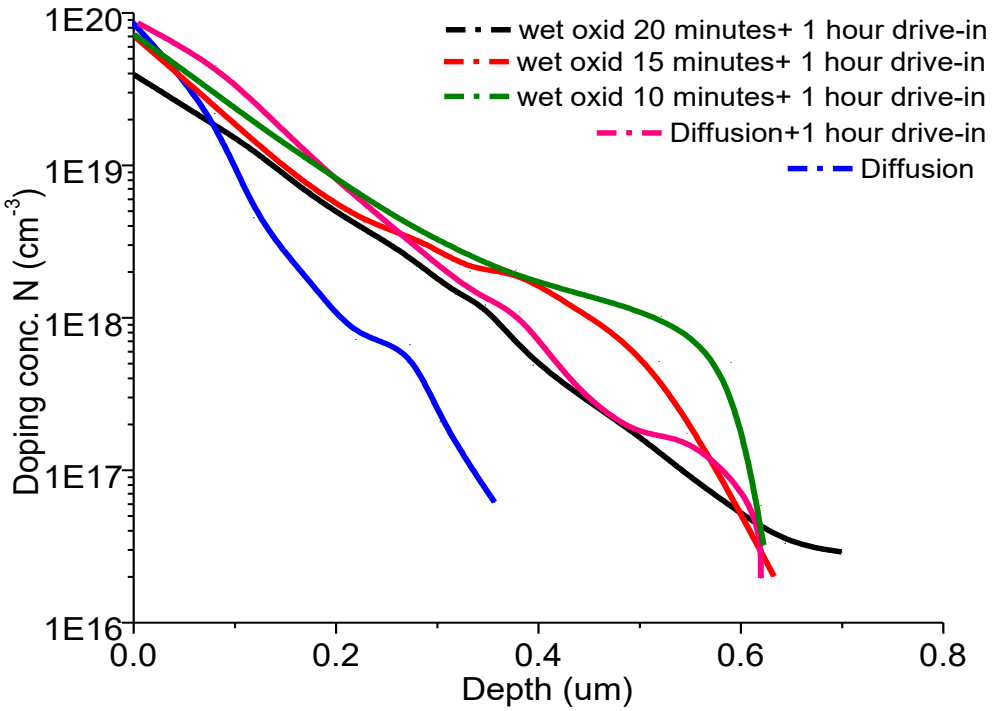


Figure 4.25 P diffusion profiles for 840 ºC

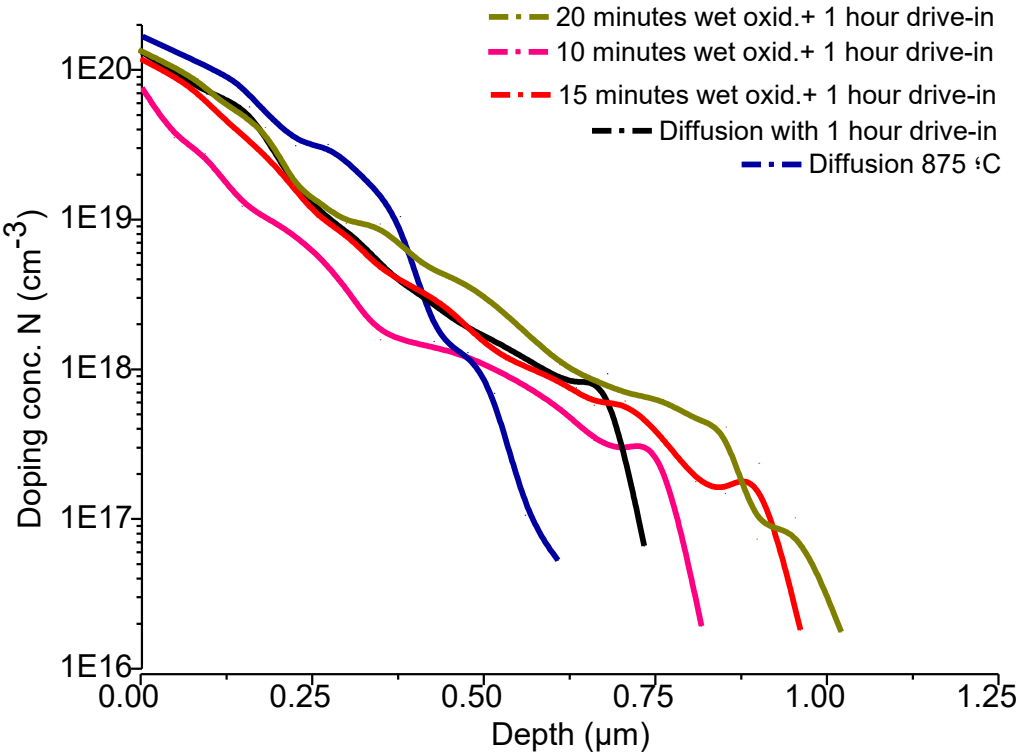


Figure 4.26 P diffusion profiles for 875 ºC

From above 4 figures 4.23-4.26, it is clear that high concentration is obtained at high temperature diffusion and in all cases of P diffusion, surface concentration of P diffusion in emitter is below than $2x10^{20}$ cm^{-3}. After the wet oxidation processes surface concentration is decreased even with dry oxidation process. Due to oxidation step with drive-in, junction depth move deeper than only diffusion process. Wet oxidation is one way to decrease the surface concentration in order to get desire sheet resistance values (doping concentration)

and junction depth. As we have mentioned early that our aim was to get softly doped and deep emitters for high efficiency silicon solar cells. Junction depth of dopant for emitters resulted after P diffusion at different temperature and after different steps such as (a) after phosphorus diffusion (b) P diffusion and 10 minutes of dry oxidation with one hour of drive-in (c) after 10 minutes, 15 minutes and 20 minutes of wet oxidation and one hour of drive-in in nitrogen ambient are shown in figure 4.27.

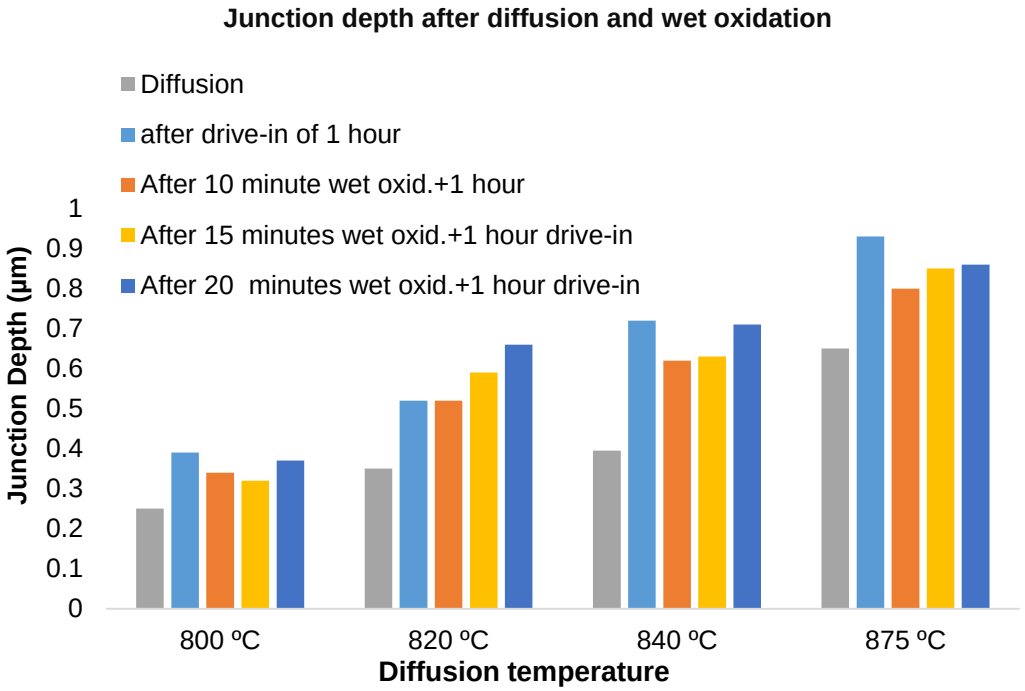


Figure 4.27 Junction depth of dopant for emitters resulted after P diffusion at different temperature (a) after phosphorus diffusion (b) P diffusion and 10 minutes of dry oxidation with one hour of drive-in (c) after 10 minutes, 15 minutes and 20 minutes of wet oxidation and one hour of drive-in in nitrogen ambient.

4.5.1 Q calculation

In complementary error function diffusion, Concentration profile of dopant in silicon is given by erfc.

$$N(x,t) = N_0 erfc \frac{x}{2\sqrt{Dt}} \tag{4.20}$$

Where N_0 is dopant concentration in surface layer (1/cm^3) x is depth (cm), t is time in second and D is diffusion coefficient at given temperature (cm^2/s). Longer diffusion time will lead to deeper diffusion but surface concentration is unchanged.

$2\sqrt{}Dt$ is calculated from the equation (4.21)

$$ln \frac{N}{N_0} = -\left(\frac{x}{2\sqrt{Dt}}\right)^2$$

This value applies in the following equation to obtain Q.

$$N_0 = \frac{Q}{2\sqrt{\pi Dt}} \tag{4.22}$$

Table 4.6. Charges Q calculated at given diffusion temperature under variable conditions.

Diffusion temperature	Profile step, at which charge (Q) is calculated.	Charge (Q) (cm^2/s)
875 ºC	After doping	5.23E15
	After doping with drive-in	3.58E15
	After doping+ 10 minutes wet oxid.+ 1 hour drive-in	1.85E15
	After doping+ 15 minutes wet oxid. +1 hour drive-in	1.15E15
	After doping+ 20 minutes wet oxid. +1 hour drive-in	2.37E15 1.72E15
840 ºC	After doping	1.55E15 2.06E15
	After doping with drive-in	1.75E15 2.14E14
	After doping+ 10 minutes wet oxid.+1 hour drive-in	1.28E15 1.98E15
	After doping+ 15 minutes wet oxid.+ 1 hour drive-in	4.14E14
	After doping+ 20 minutes wet oxid.+ 1 hour drive-in	4.49E14
820 ºC	After doping	7.04E14 9.3E14
	After doping with drive-in	7.35E14
	After doping+ 10 minutes wet oxid. +1 hour drive-in	5.75E14
	After doping+ 15 minutes wet oxid.+ 1 hour drive-in	4.23E14
	After doping+ 20 minutes wet oxid. +1 hour drive-in	3.44E14
800 ºC	After doping	2.67E14
	After doping with drive-in	1.85E14
	After doping+ 10 minutes wet oxid.+ 1 hour drive-in	2.5E14
	After doping+ 15 minutes wet oxid.+ 1 hour drive-in	6.74E13
	After doping+ 20 minutes wet oxid. +1 hour drive-in	8.83E13

In table charge Q has been given at different temperature under different conditions of wet oxidation as well as dry oxidation. Emitters on the surface have higher charge than emitters in depth. Amount of charge Q start decreasing with the drive-in process, after the diffusion with this drive-in, Q is decreased due to redistribution and due to trapping in SiO_2.

4.6 Total concentration of P diffusion

Total phosphorus concentration is measured accurately by secondary ion mass spectrometry (SIMS), although it is expensive technique but we can get accurate result. Fair and Tsai measured total phosphorus concentration by using SIMS analysis as well as by neutron activation analysis (NA) of same sample wafers: they have got similar results by using two different techniques. Neutron activation analysis is just used to calibrate the results of SIMS measurement. By using differential conductivity (DC) techniques, Fair and Tsai also measured electrically active P^+profile of phosphorus diffusion. Ratio of total phosphorus concentration and Active results were agreed with already published data by P.

Negrim et al (1975) [21]. The data obtained by Fair and Tsai is represented by an empirical equation, which is used to calculate total concentration of phosphorus [6].

$$C_T = n + 2.04x10^{-41}n^3 \quad (4.23)$$

Where C_T is total concentration of phosphorus and n is electrically active concentration of phosphorus.

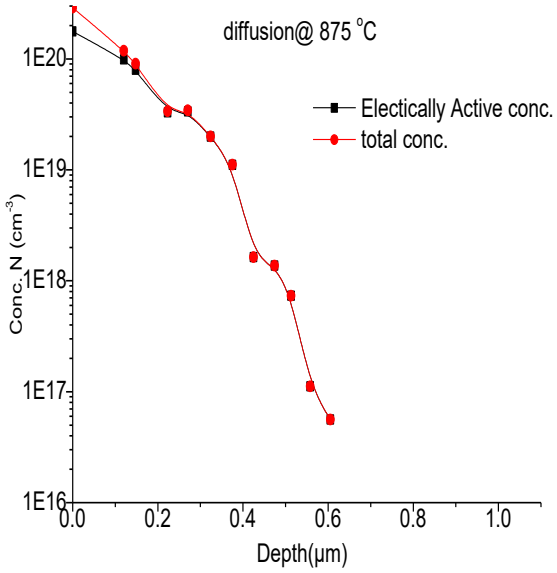
Figures 4.28,4.29,4.30 and 4.31 (a,b,c,d and e) represent the plots of electrically active phosphorus concentration obtained directly from the sheet resistance measurement for all above mentioned diffusion temperature with different process conditions. The total phosphorus concentration, calculated by using eq. (4.23) from Fair-Tsai model [6]. This total concentration includes both electrically active and inactive impurities. As it has been mentioned before this amount of inactive phosphorus correponds to the dead layer extent, which appear in the form of PSG. Table 4.7 contains the extent of electrically active phosphorus, which is obtained after different diffusion process conditions. Detail of each process is given in table 4.7.

It is observed that with increasing of temperature of P diffusion, surface concentration (Ns) is also increased and P is better and uniformly distributed in emitters. But at high temperature, phosphorus is precipitated in the form of dead layer due to over solid solubility limit. Due to this layer recombination centers appeared, as a result (Auger) recombination increase. These recombination centers increase saturation current density Joe; as a result cell *Voc* and *Jsc* decrease due to high recombination rate. At low temperature (800-820 ^{0}C) P diffusion is about 90-95% electrically active but at high temperature (875 ^{0}C) about 60-80% P is electrically active and electrically inactive P appeared in the form PSG as a deal layer.

However we have introduced a wet oxidation step with drive in, it converts electrically inactive P into active P and improves the recombination and surface quality for passivation. We have found a very thin surface region in which the surface concentration N may reach nearly 10^{20} atom/cc. However, this region is no more than 150 nm deep. Moreover PN junction depth can be control by drive in time but it also depends on pre-deposition condition (temperature, dopant and oxygen ratio). Lower level of oxygen increases the junction depth in P pre-deposition.

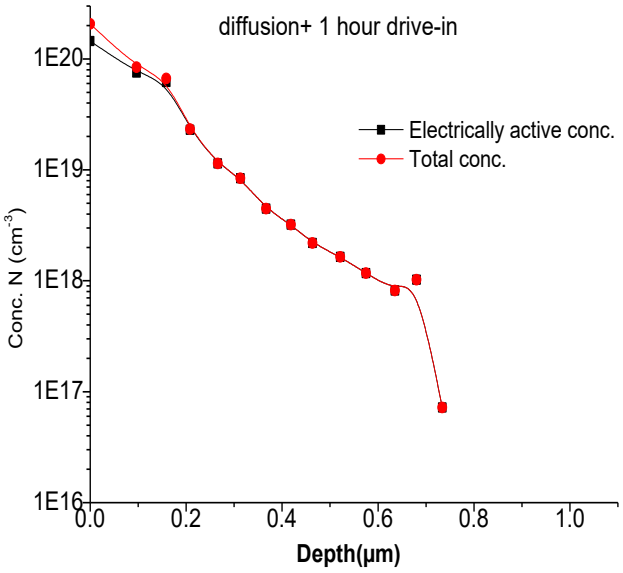
One of our aim was to remove this dead layer within the oxide growinng step in the wet oxidation step. We have grown an oxide layer as thick as 0.1 µm. Figures 4.28 given below, show an improvement in the emitter quality after 10-20 minutes of wet oxidation, the inactive phosphorus concentration has decreased considerably and due to the redistribution of impurities, junction depth slight increased and reduction in surface concentration took place due to redistribution. This phenomena is clear at high temperature P diffusion. P Profles of emitters with electrically active P concentration and total concentration of P doped at 875 ºC under different condition of drive in are given below in figure 4.28 (a,b,c,d and e)

4.6.1 Electrically active and total concentration of P diffusion profiles for 875 ºC



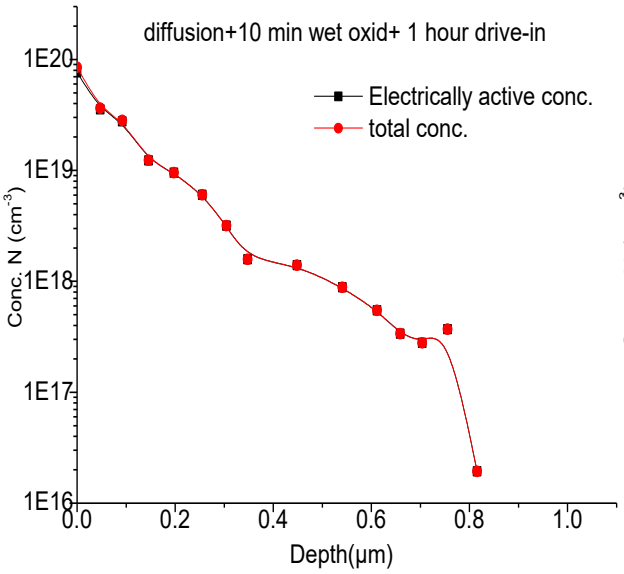
a

P profile of the emitter doped at 875ºC with electrically active and total concentration (only diffusion)



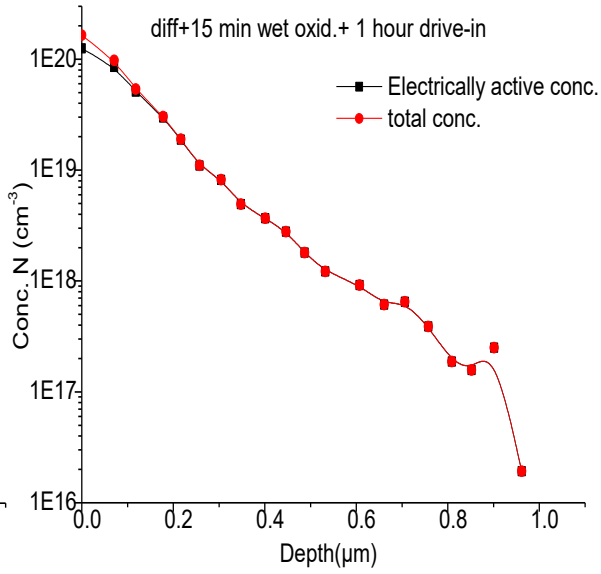
b

P profile of the emitter doped at 875ºC with electrically active and total concentration with 1 hour of drive-in, in nitrogen ambient



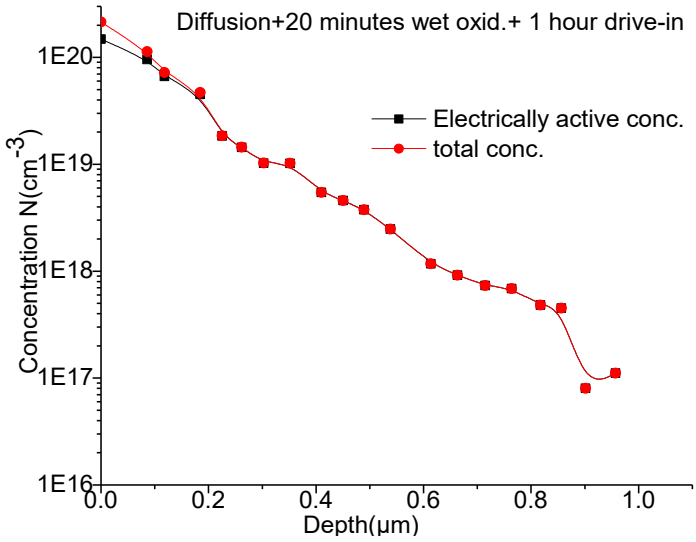
c

P Profile of the emitter doped at 875ºC with electrically active and total concentration after 10 minutes of wet oxidation with 1 hour of drive-in, in nitrogen ambient.



d

P profile of the emitter doped at 875ºC with electrically active and total concentration after 15 minutes of wet oxidation with 1 hour of drive-in, in nitrogen ambient.



e

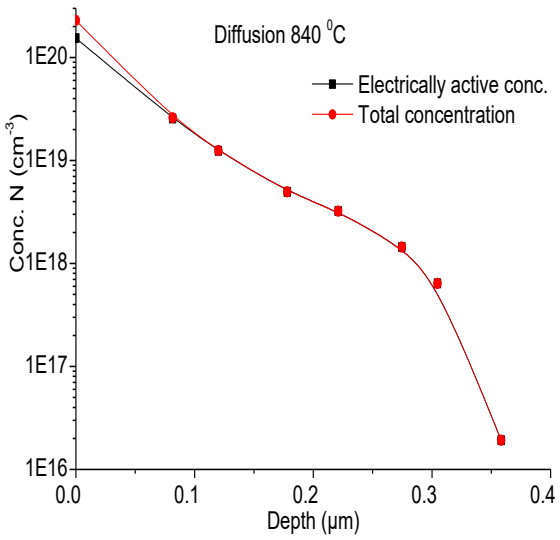
P profile of the emitter doped at 875ºC with electrically active and total concentration after 20 minutes of wet oxidation with 1 hour of drive-in, in nitrogen ambient.

Figure 4.28 P diffusion profiles for emitter doped at 875 ºC with electrically active concentration and total concentration under different wet oxidation conditions and with 1 hour of drive-in, in nitrogen ambient

From these graphs of figure 4.28 of high temperature P diffusion (875 ºC), it is clear that wet oxidation converts electrically inactive P concentration into electrically active P. At high temperature diffusion, concentration of electrically inactive P is very high, around 35% is electrically inactive. However by introducing a wet oxidation step with drive-in, it converts electrically inactive P into electrically active P. Up to 90% concentration of P is electrically active after 10-20 minutes of wet oxidation with drive-in step of 1 hour.

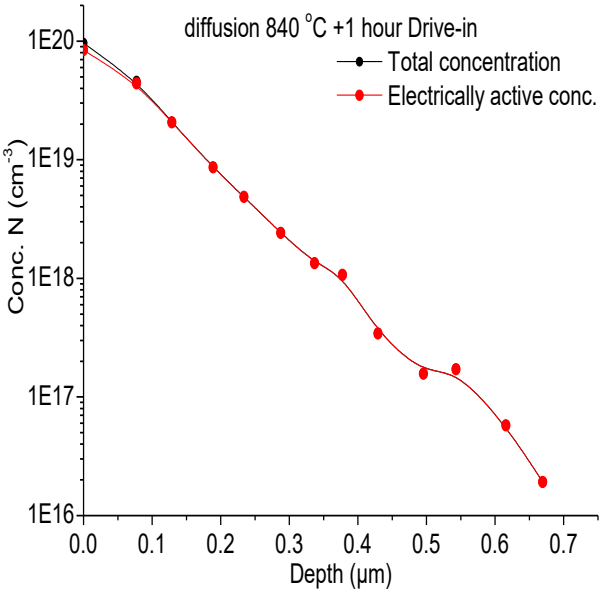
4.6.2 Electrically active and total concentration of P diffusion profiles for 840 ºC

P profles of emitters with electrically active P concentration and total concentration of P doped at 840 ºC under different condition of drive in are given below in figure 4.29, (a,b,c,d and e). These figures represent the plots of electrically active phosphorus concentration obtained directly from the sheet resistance measurement through etching process. The total phosphorus concentration, calculated by using eq. (4.23) from Fair-Tsai model.



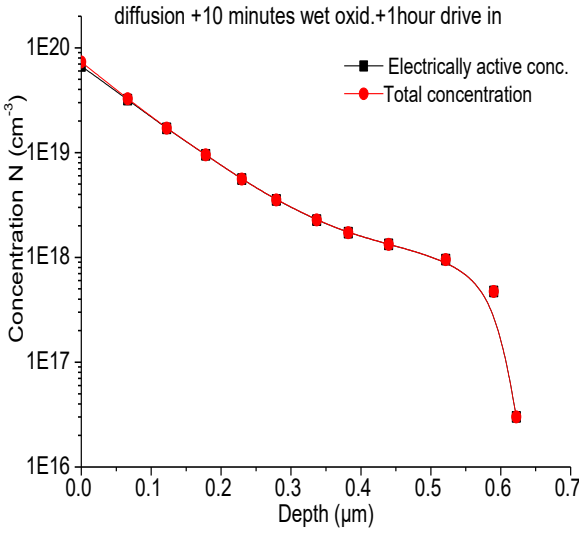
a

P profile of the emitter doped at 840 ºC with electrically active and total concentration (only diffusion)



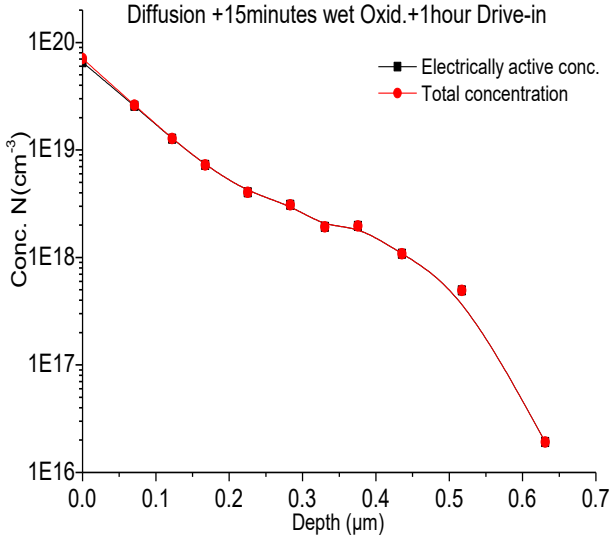
b

P profile of the emitter doped at 840ºC with electrically active and total concentration with 1 hour of drive-in, in nitrogen ambient.



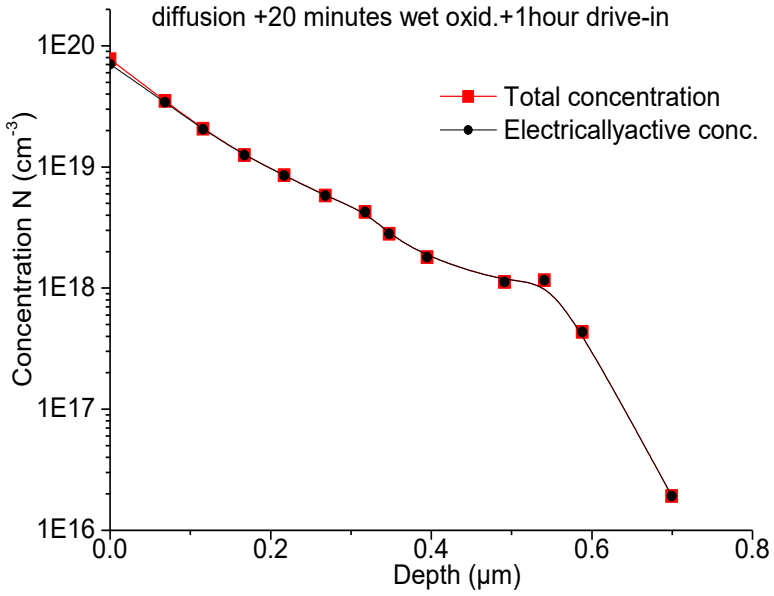
c

P profile of the emitter doped at 840 ºC with electrically active and total concentration after 10 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient



d

P profile of the emitter doped at 840ºC with electrically active and total concentration after 15 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.



e

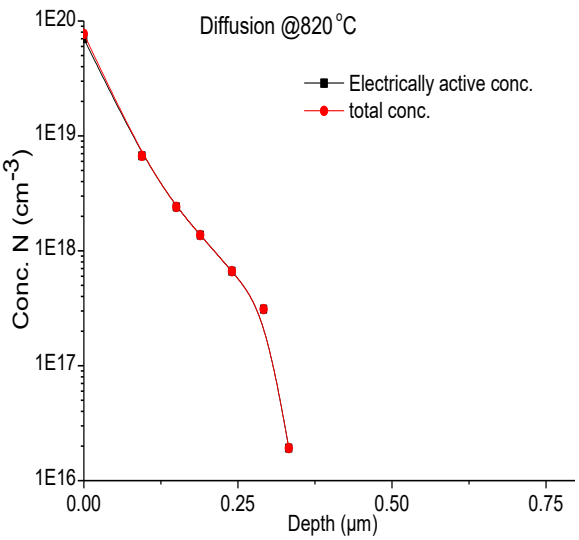
P profile of the emitter doped at 840 ºC with electrically active and total concentration after 20 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.

Figure 4.29 **P diffusion profiles for emitter doped at 840ºC with electrically active concentration and total concentration under different wet oxidation conditions and with 1 hour of drive-in, in nitrogen ambient.**

From these graphs of figure 4.29 of 840ºC P diffusion, it is clear that wet oxidation converts electrically inactive P concentration into electrically active P concentration. At 840 ºC temperature concentration of electrically inactive P is around 25%. However by introducing a wet oxidation step with drive-in, it converts electrically inactive P into electrically active P. Up to 90% concentration of P is electrically active after 10-20 minutes of wet oxidation with drive-in step of 1 hour.

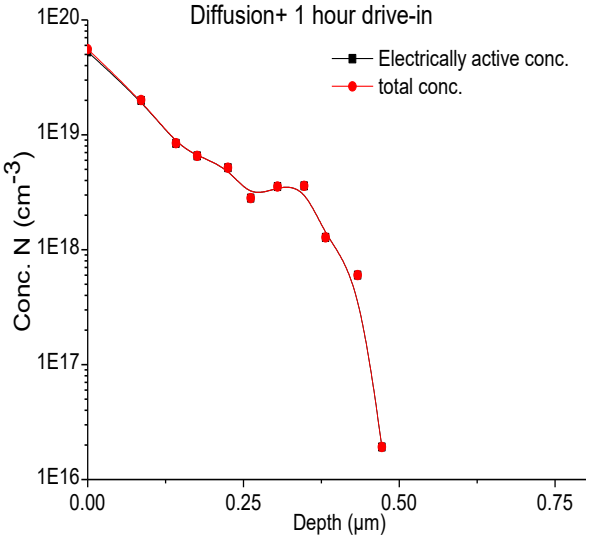
4.6.3 Electrically active and total concentration of P diffusion profiles for 820 ºC

P profles of emitters with electrically active P concentration and total concentration of P doped at 820 ºC under different condition of drive in are given below in figure 30, (a,b,c,d and e).These figures represent the plots of electrically active phosphorus concentration obtained directly from the sheet resistance measurement through etching process. The total phosphorus concentration, calculated by using eq. (4.23) from Fair-Tsai model. P Profles of emitters with electrically active P concentration and total concentration of P doped at 820 ºC under different condition of drive in are given below in figures 4.30.



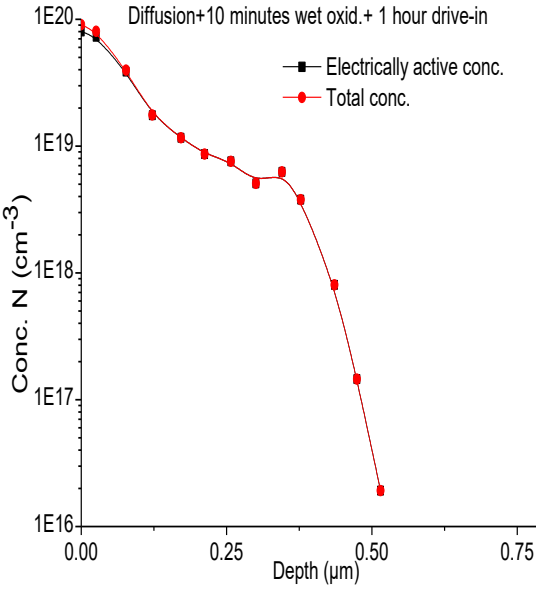
a

P profile of the emitters doped at 820 ºC with electrically active and total concentration (only diffusion)



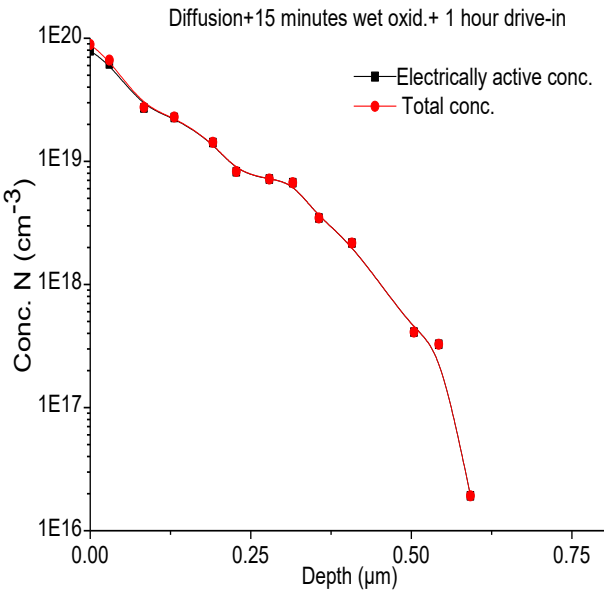
b

P profile of the emitters doped at 820ºC with electrically active and total concentration with 1 hour of drive-in, in nitrogen ambient.



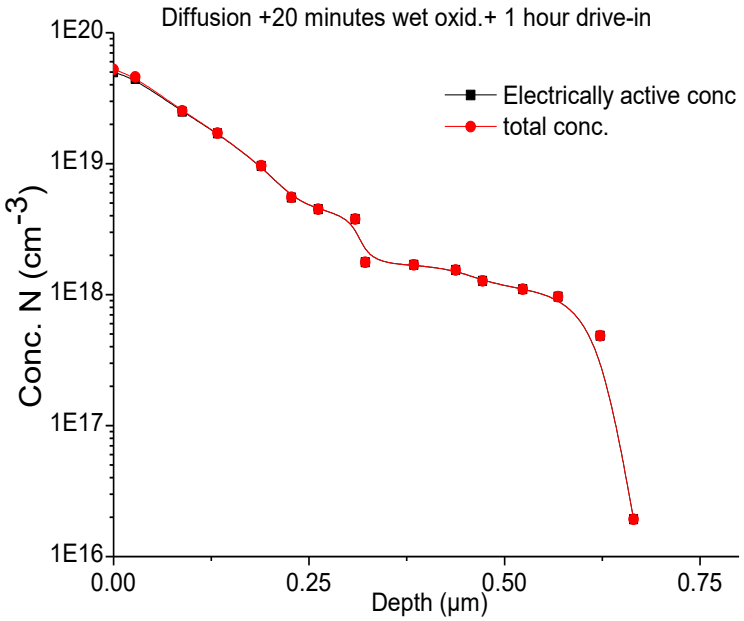
c

P profile of the emitters doped at 820 ºC with electrically active and total concentration after 10 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.



d

P profile of the emitters doped at 820 ºC with electrically active and total concentration after 15 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.



e

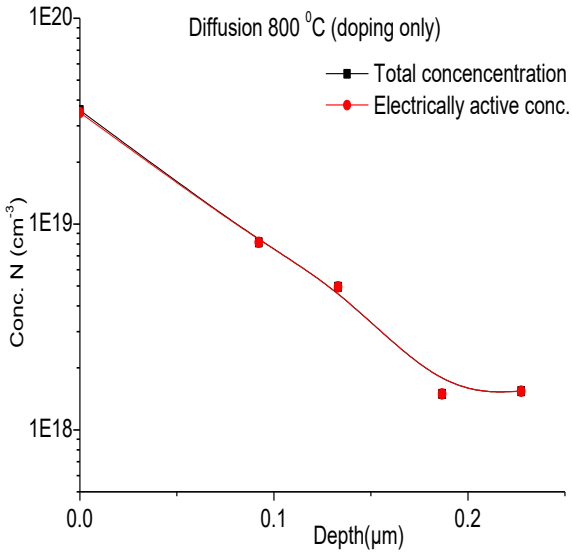
P profile of the emitter doped at 820 ºC with electrically active and total concentration after 20 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.

Figure 4.30 P diffusion profiles for emitter doped at 820 ºC with electrically active concentration and total concentration under different wet oxidation conditions and with 1 hour of drive-in, in nitrogen ambient.

From these graphs of figure 4.30 of 820ºC P diffusion, it is clear that wet oxidation converts electrically inactive P concentration into electrically active P concentration. At 820 ºC temperature concentration of electrically inactive P is around 10%. However by introducing a wet oxidation step with drive-in, it converts electrically inactive P into electrically active P. Up to 95% concentration of P is electrically active after 10-20 minutes of wet oxidation with drive-in step of 1 hour. P Profles of emitters with electrically active P concentration and total concentration of P diffusion of 820 ºC under different condition of drive-in are given in figures 4.30.

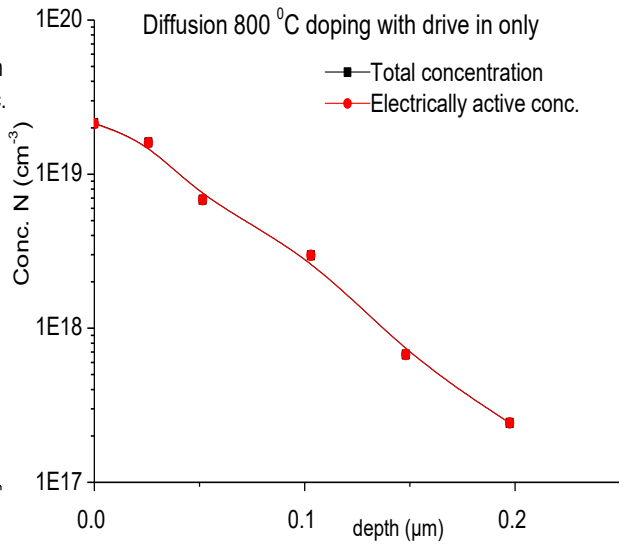
4.6.4 Electrically active and total concentration of P diffusion profiles for 800 ºC

P Profles of emitters with electrically active P concentration and total concentration of P doped at 800 ºC under different condition of drive in are given below in figure 4.31, (a,b,c,d and e). These figures represent the plots of electrically active phosphorus concentration obtained directly from the sheet resistance measurement after etching process. The total phosphorus concentration, calculated by using eq. (4.23) from Fair-Tsai model.



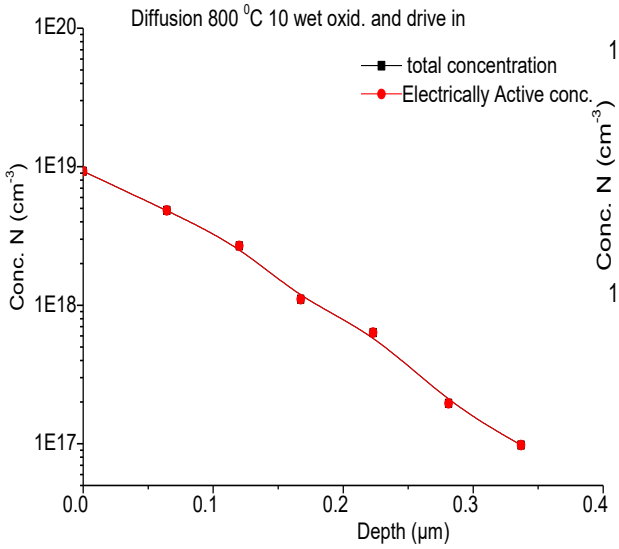
a

P profile of the emitter doped at 800 ºC with electrically active and total concentration (only diffusion)



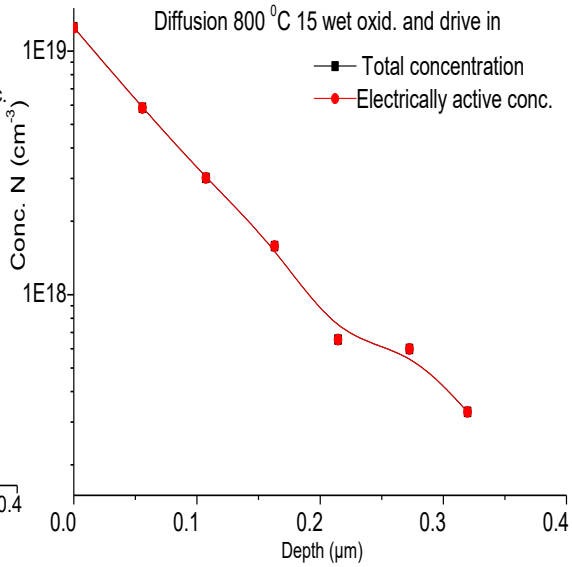
b

P profile of the emitter doped at 800ºC with electrically active and total concentration with 1 hour of drive-in, in nitrogen ambient.



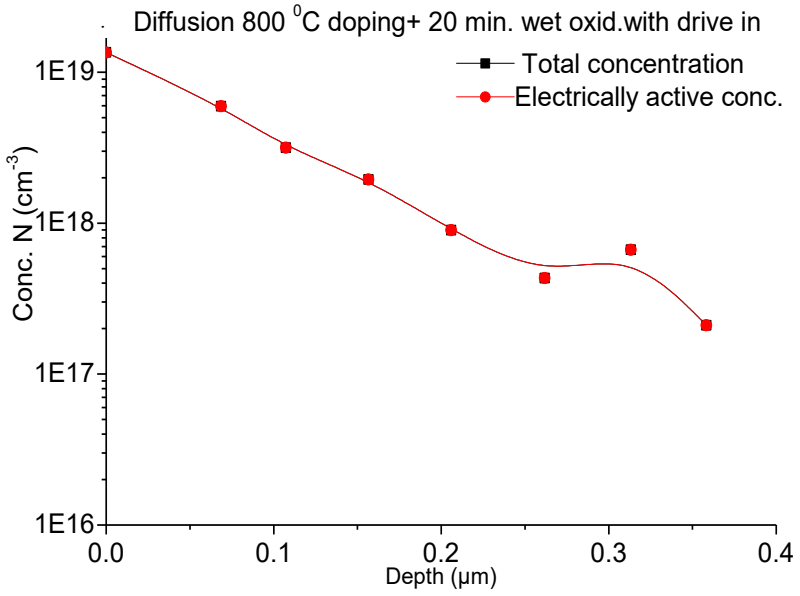
c

P profile of the emitter doped at 800 ºC with electrically active and total concentration after 10 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.



d

P profile of the emitter doped at 800 ºC with electrically active and total concentration after 15 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient.



e

P profile of the emitters doped at 800 ºC with electrically active and total concentration after 20 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient

Figure 4.31 P diffusion profiles for emitter doped at 800 ºC with electrically active concentration and total concentration under different wet oxidation conditions and with 1 hour of drive-in, in nitrogen ambient.

From these graphs of figure 4.31 of 800ºC P diffusion, it is clear that wet oxidation converts electrically inactive P concentration into electrically active P concentration. At 800 ºC temperature concentration of electrically inactive P is around 3%. However by introducing a wet oxidation step with drive-in, it converts electrically inactive P into electrically active P. Up to 99% concentration of P is electrically active after 10-20 minutes of wet oxidation with drive-in step of 1 hour. But at 800 ºC P diffusion, there is a problem of reproducibility of results. Sheet resistance values which we have obtained after each P diffusion of 800 ºC is variable. Electrically active concentration of phosphorus, which is calculated from sheet resistance values of emitters by PC1D as it is mentioned early and total concentration of phosphorus diffusion is calculated from Fair and Tsai model by using equation (4.23). From the graph between electrically active concentration and total concentration, we can draw the slope which gives us a percentage of electrically active phosphorus as shown in figure 4.32. We have calculated percentage of electrically active P in all diffusion processes. Percentages of electrically active concentration of phosphorus at different diffusion temperature under different drive-in conditions are given below in table 4.7.

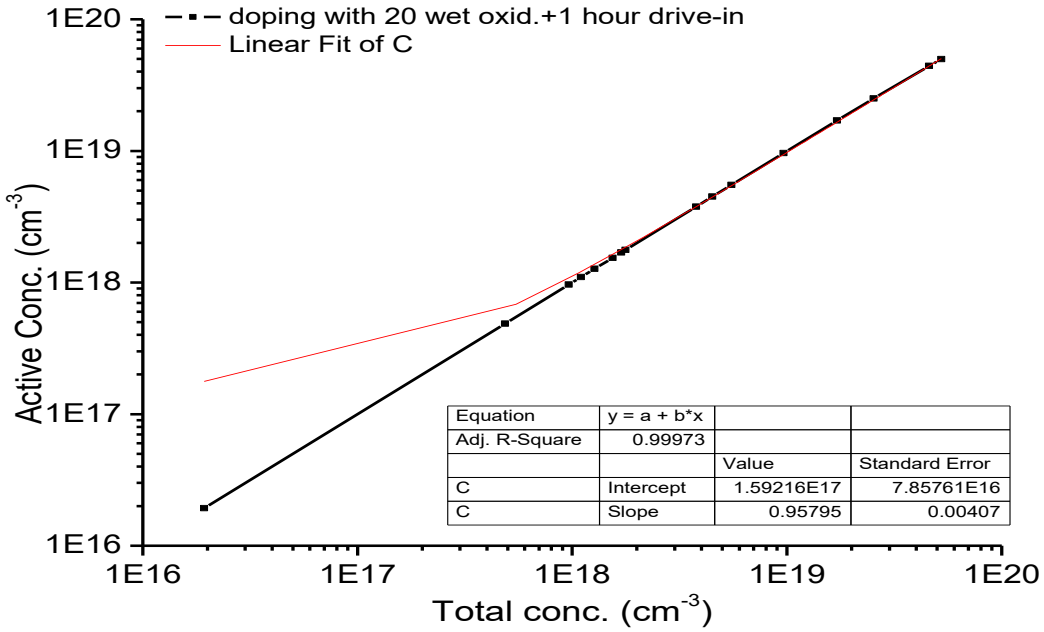


Figure 4.32 Graph between electrically active and total concentration of Phosphorus to plot a slope

In this way, we have plotted all above mentioned graphs into to calculate the percentage of electrically active concentration. Percentage of all electrically active concentration is given in table 4.7.

Table 4.7

Diffusion temperature	Profile step, at which electrically active concentration is calculated.	Electricall active P concentration (%)
875 ºC	After doping	63%
	After doping with drive-in	72%
	After doping+ 10 minutes wet oxid.+ 1 hour drive-in	90%
	After doping+ 15 minutes wet oxid. +1 hour drive-in	79%
	After doping+ 20 minutes wet oxid. +1 hour drive-in	73%
840 ºC	After doping	66%
	After doping with drive-in	88%
	After doping+ 10 minutes wet oxid.+1 hour drive-in	92%
	After doping+ 15 minutes wet oxid.+ 1 hour drive-in	92%
	After doping+ 20 minutes wet oxid.+ 1 hour drive-in	91%
820 ºC	After doping	90%
	After doping with drive-in	94%
	After doping+ 10 minutes wet oxid. +1 hour drive-in	92%
	After doping+ 15 minutes wet oxid.+ 1 hour drive-in	92%
	After doping+ 20 minutes wet oxid. +1 hour drive-in	94%
800 ºC	After doping	97%
	After doping with drive-in	99%
	After doping+ 10 minutes wet oxid.+ 1 hour drive-in	99%
	After doping+ 15 minutes wet oxid.+ 1 hour drive-in	99%
	After doping+ 20 minutes wet oxid. +1 hour drive-in	99%

It is observed that with the increase of the pre-deposition temperature increases the surface concentration (Ns) and makes the P distribution more uniform. At high temperature, phosphorus is precipitated in the form of dead layer due to over solid solubility limit. Due to this dead layer recombination centers appear, as a result Auger recombination increase. These recombination centers increase saturation current density; as a result cell *Voc* and *Jsc* decrease due to high recombination rate. At low temperature 800-820 ^{0}C, P diffusion is about 90% P electrically active but at high temperature (875 ^{0}C) about 65% P is electrically active and rest of concentration of P deposited is considered as electrically inactive.

However by introducing a wet oxidation step with drive in, it converts electrically inactive P into electrically active. We have found a very thin surface region in which the surface concentration N may reach nearly 1E20 cm^{-3}. However, this region is no more than 100 nm in depth. Moreover PN junction depth can be control by drive in time but it also depends on pre-deposition condition (temperature, dopant and oxygen ratio). Lower level of oxygen increases the junction depth in P pre-deposition.

As I have mentioned early that objective of this work was to get softly doped and deep emitters for high efficiency solar cells. We have simulated doping concentration of phosphorus diffusion data to predict efficiency of silicon solar cell by PC1D modelling program. Results which are shown in graphs of figure 4.33 and 4.34 represent that moderate or low doped emitters give high efficiency. The best efficiency, which we can obtain is based on softly doped, deep and passivated emitters. From figure 4.33, it is clear that with increase of doping concentration of P, efficiency starts decreasing. From our experimental data of phosphorus diffusion at different temperatures under different oxidation and drive-in conditions, we have concluded that diffusion at high temperature has high density of recombination centers due electrically inactive phosphorus. Although wet oxidation and HF treatment steps in between P pre-deposition and drive-in diffusion decrease the concentration of electrically inactive phosphorus but still there is high probability of having high density of recombination centers. Due to this reason, we have planned to investigate low temperature diffusion for softly or moderate doped and deep emitters for silicon solar cell fabrication process to gain high efficiency. The result which we have obtained at 800 ºC is not uniform as compare to 820 ºC, we preferred to 820 ºC instead of 800 ºC. In addition to this doping concentration of P at 820 ºC is 95% electrically active as compare to high temperature diffusion. Due to this reason, there is lower probability to have recombination centers due to low percentage of electrically inactive phosphorus.

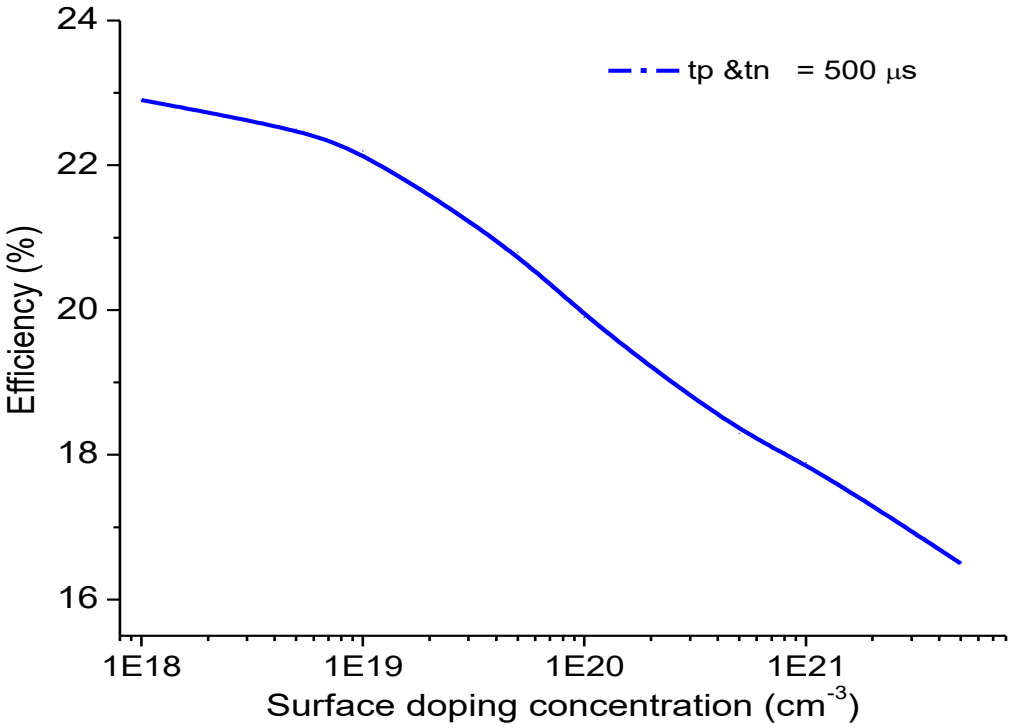


Figure 4.33 Efficiency verses doping concentration graph, results are obtained by PC1D modelling program

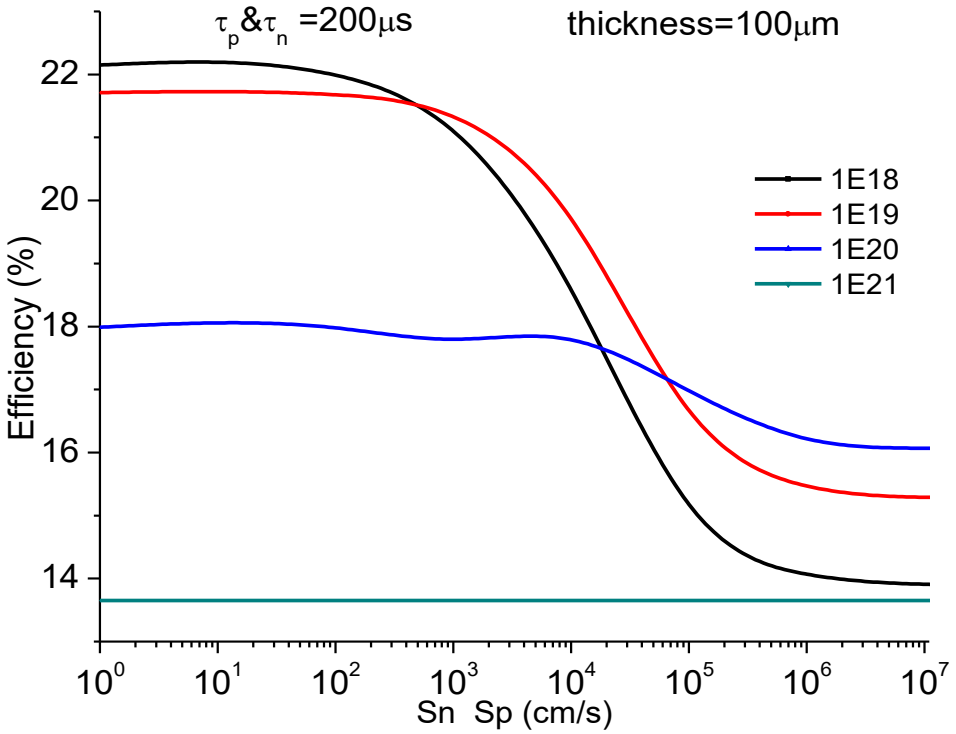


Figure 4.34 Graph between efficiency and recombination velocities at different doping concentration obtained by PC1D modelling program

From figure 3.34, it is clear that with the increase of surface doping concentration, open circuit voltage and overall efficiency of solar cell starts decreasing. When surface concentration is high and exceeds the intrinsic charge-carrier concentration, certain special features on electrical properties and conductivity of device appears. Due to over solubility limit, P appears as in the form of dead layer, an electrically inactive layer of P, which produces the recombination centers, as a result Auger recombination increases which decrease the lifetime and overall efficiency of the solar cell. In addition to this, electrically inactive P also introduces defects in the crystalline lattice of silicon, Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure and also take part in efficiency losses due to high recombination rate (low lifetime). At high P doping concentration, bandgap narrowing effect arises, which cause the absorption of photons in emitters region near the front surface.

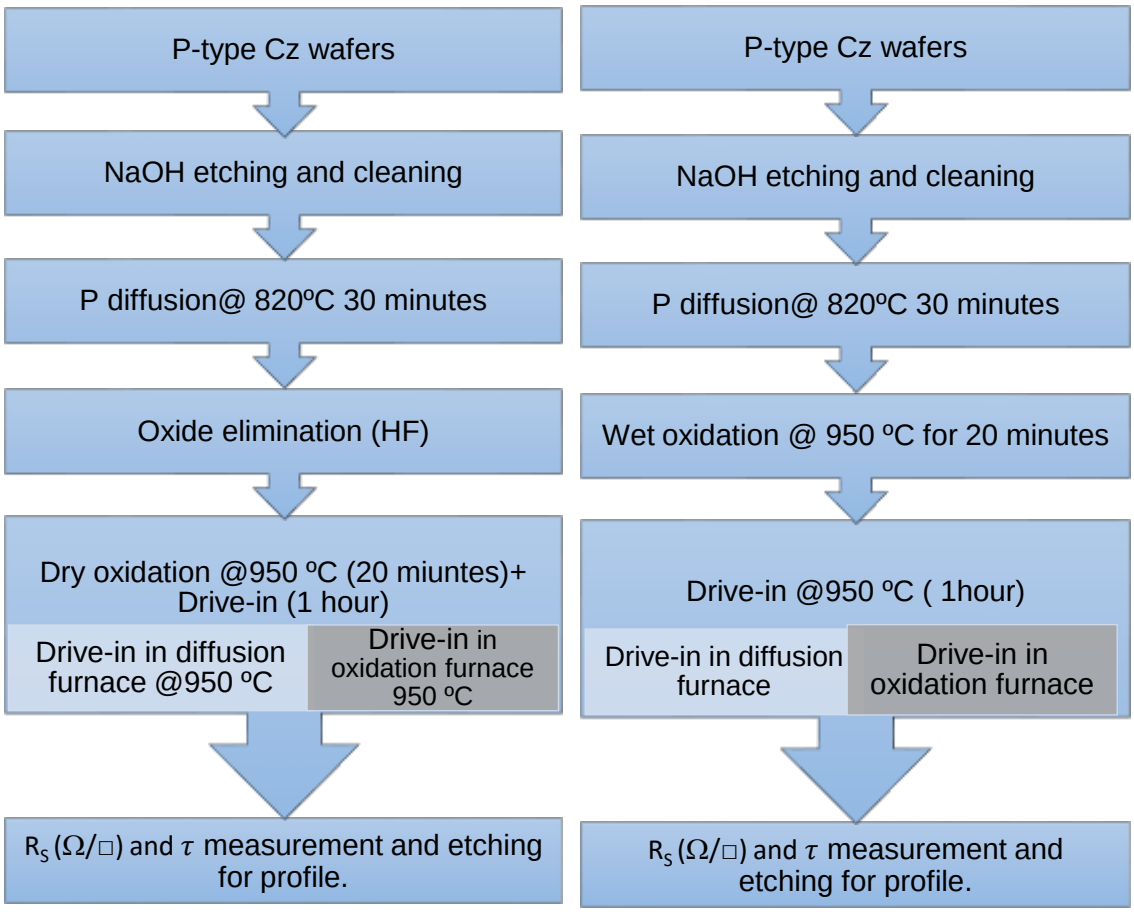
Due to high recombination rate, we have focused on low temperature P diffusion instead of high temperature. In low temperature diffusion, 820 ºC has higher degree of reproducibility of results in term of sheet resistance, surface concentration and junction depth than 800 ºC. We have preferred 820 ºC for low temperature P diffusion in order to get softly doped and deep emitters. In conventional emitters' formation, it is common to fabricate emitters by a heavy phosphorus diffusion followed by an etching process to get desire sheet resistance of open emitter in range of 60-100 Ω/□ [6]. It is common to combine chemical steps with thermal processes. One of our goal of this work/investigation was to make a single step diffusion process for softly doped and deep emitters.

We have conducted some experiments in order to achieve single step diffusion process. Prior to these experiments, we have investigated the effect of dry oxidation and HF free process to compare with wet oxidation. We have conducted three different P diffusion experiments under different condition of oxidation and HF free process. Emitter fabrication scheme of these experiments are modified which are shown in figure 4.35, scheme of low temperature diffusion as well as in process flowsheet diagram of these processes.

4.7 Low Temperature Diffusions

In low temperature diffusion experiments, we have modified the diffusion process, which is mentioned above. In first experiment, we have used dry conditions for oxidation and second experiment, we used wet oxidation but without HF treatment. Diffusion process for both experiments is given in the figure 4.35 as scheme A and scheme B. Further detail of experimental conditions for scheme A is given in figure 4.36 and for scheme B is given in figure 4.37.

Low temperature P diffusion process



Scheme A
P diffusion with water free oxidation (only dry oxidation)

Scheme B
P diffusion with HF free (without PSG removal)

Figure 4.35 Scheme A; P diffusion with water free oxidation (only dry oxidation) and scheme B; P diffusion with wet oxidation and without HF treatment.(HF free process)

Description of P diffusion process with respect to time and temperature is shown in figure 4.36. After phosphorus diffusion dry oxidation was carried out after HF treatment, which is used to remove the dead layer. In this process 20 minutes of dry oxidation is performed, prior to 10 minutes of dry oxidation and 1 hour of drive-in, wafers were treated again with HF to remove the oxides. This process is used to get softly doped and deep emitters.

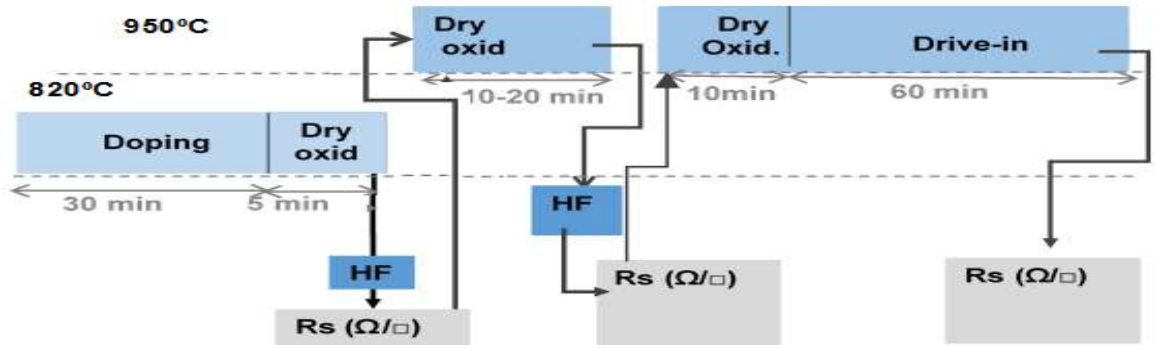


Figure 4.36 Systematic process for P diffusion at low temperature with water free oxidation (only dry oxidation)

4.7.1 Low temperature diffusion with HF free process

Usually in our standard process, we have cleaned the wafers with HF to remove the oxides and dead layer, but in this process, we have removed the cleaning step and wafers were directly processed for oxidation. Description of P diffusion process with respect to time and temperature is shown in figure 4.37. After phosphorus diffusion wet oxidation was carried out without after HF treatment, which is used to remove the dead layer. In this process 20 minutes of wet oxidation is performed with 1 hour of drive-in to get softly doped and deep emitters

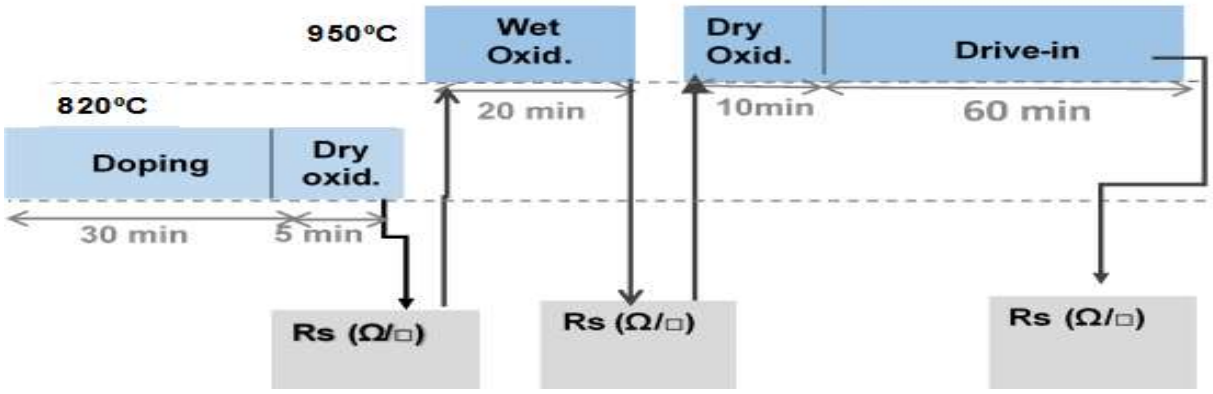


Figure 4.37 Systematic process for P diffusion at low temperature with wet oxidation but without HF treatment

After drive-in process, etching of emitters was carried out in a dilute solution of 2% NaOH at 60 ^{0}C as it is mentioned early in this chapter. After 15 second etching, (about ~50 nm thickness of each surface of wafer is removed in this short etching time). Wafers were cleaned and dried to measure the sheet resistance of exposed surface by 4-point probes. This process is repeated again and again until sheet resistance shows complete removal of emitters and sheet resistance values were similar to base doping. In this way we have estimated the junction depth.

Surface concentration was calculated by PC1D, using a Gaussian model with values of the sheet resistance for the corresponding values of depth junction. By using concentration data obtained from PC1D are plotted against the junction depth to get the doping profiles of the emitters

4.7.2 Low temperature diffusion profiles of HF free process

Phosphorus diffusion was carried out at 820 ºC for 30 minutes and wet oxidation with H_2O vapors at 950 ºC for 20 minutes in oxidation furnace. After wet oxidation process, drive-in was carried out in same furnace with 10 minutes of dry oxidation and 60 minutes drive-in step at 950 ºC. This process was HF free. No oxides and dead layer was removed by HF treatment. Low temperature diffusion profiles are shown in figures 4.38 and 4.39. (In figure 4.38, 2, 5, 6 and 7 are zones of the wafer which are used to analyze for diffusion profiles as shown in figure 4.15). Detail of sheet resistance, junction depth and surface concentration of each process is given in table 4.8.

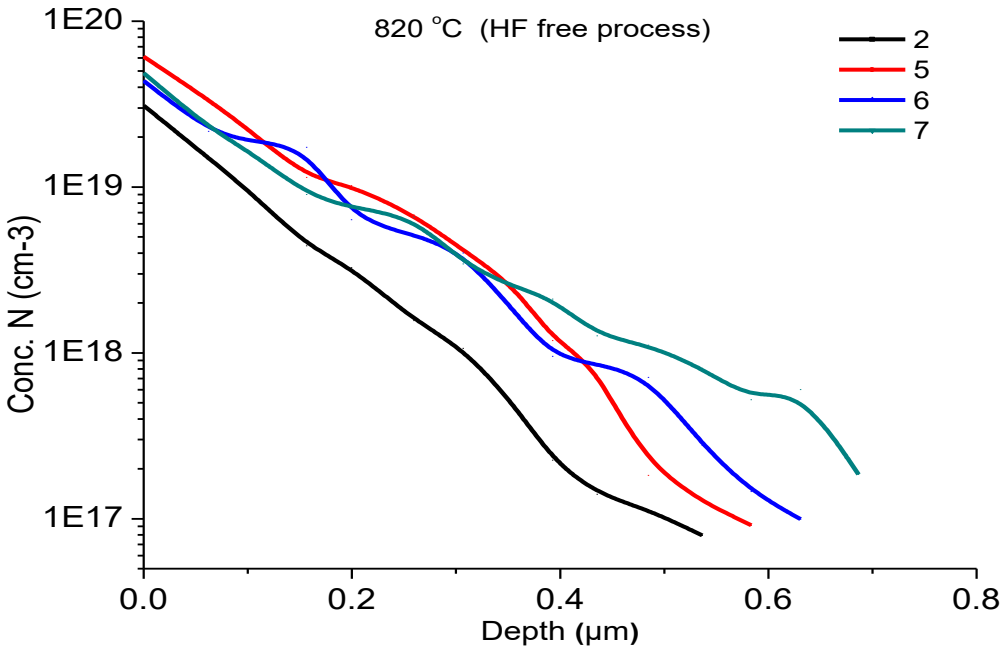
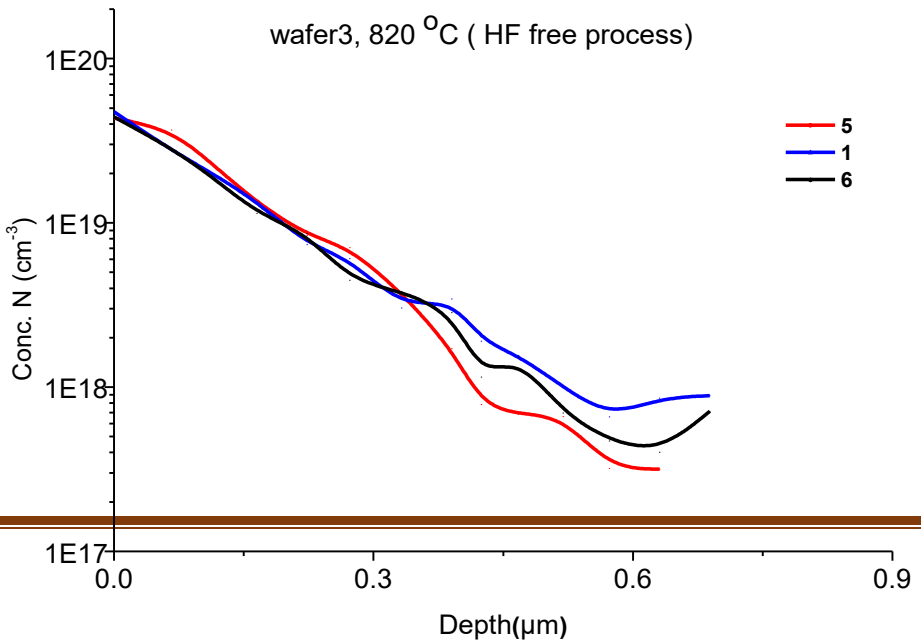


Figure 4.38 P diffusion profiles for emitter doped at 820 ºC with 20 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient, (HF free process)

In this low temperature diffusion profile of HF free process, surface concentration value ranging from $4.1x10^{19}$ cm^{-3} to $6.2x10^{19}$ cm^{-3} and depth junction values from 0.52 to 0.71 µm for sheet resistance ~60 Ω/□ has obtained. In profile of figure 4.39, Drive-in process was carried out in phosphorus diffusion furnace. According to our opinion, Phosphorus diffusion furnace cleaner than oxidation furnace. Results was more or less were similar like oxidation furnace but observed uniformity in sheet resistance values. (In figure 4.39, 1, 5 and 6 are zones of the wafer which are used to analyze for diffusion profiles as



shown in figure 4.15).

Figure 4.39 P diffusion profiles for emitter doped at 820 ºC with 20 minutes wet oxidation with 1 hour of drive-in, in oxyclean ambient, (HF free process in oxyclean ambient)

4.7.3 Low temperature diffusion profile of water free process

In water free process, P diffusion was carried out at 820 ºC for 30 minutes and dry oxidation was carried out at 950 ºC for 20 minutes in oxidation furnace. Prior to dry oxidation wafers were clean and dead layer was removed by HF treatment. Wafers were treated once again with HF prior to drive-in. Drive-in was carried out in same furnace with 10 minutes of dry oxidation and 60 minutes drive-in step at 950 ºC. This process was water vapor free process. Profile of water free process is given below in figures 4.40 and 4.41. (In figure 4.40, 1, 4 and 9 are zones of the wafer which are used to analyze for diffusion profiles as already shown in figure 4.15).

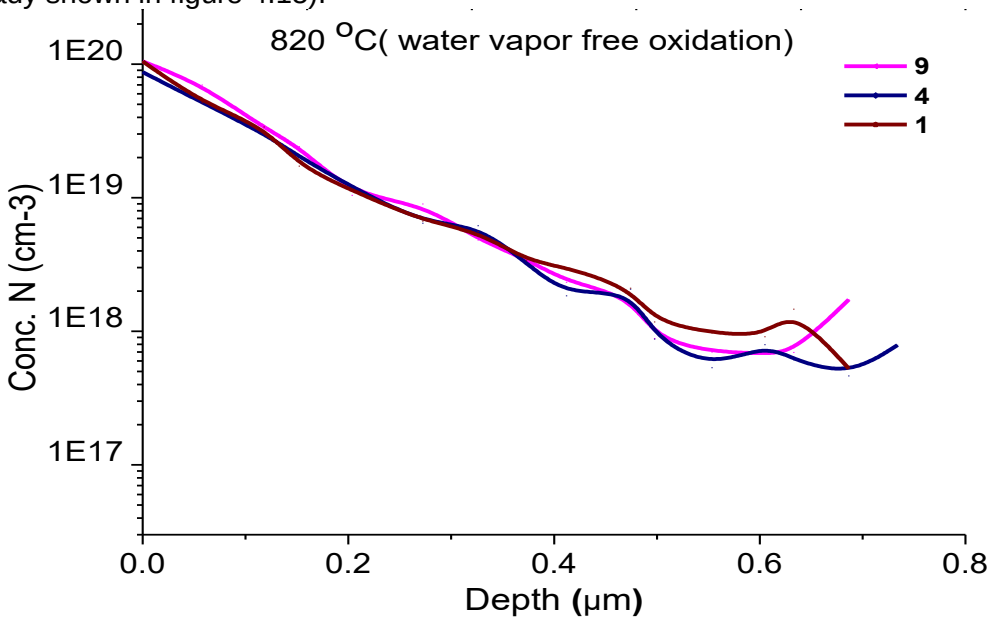


Figure 4.40 P diffusion profiles for emitter doped at 820 ºC with 20 minutes dry oxidation and 1 hour of drive-in, in nitrogen ambient, (Water free oxidation process)

In this low temperature diffusion profile of water free oxidation process, surface concentration value ranging from $4.1x10^{19}$ cm^{-3} to $1.2x10^{20}$ cm^{-3} and depth junction values is around 0.75µm for sheet resistance ~45 Ω/□ has obtained. (In figure 4.39, 1, 5 and 6 are zones of the wafer which are used to analyze for diffusion profiles as shown in figure 4.15).

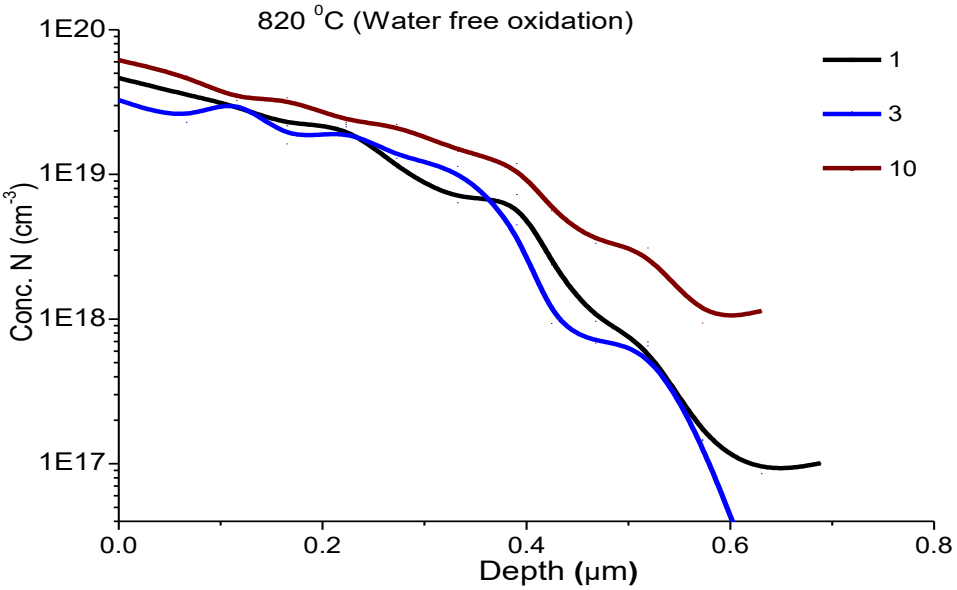


Figure 4.41 P diffusion profiles for emitter doped at 820 ºC with 20 minutes dry oxidation and 1 hour of drive-in, in nitrogen oxyclean ambient, (Water free oxidation process)

4.7.4 Results of low temperature diffusion

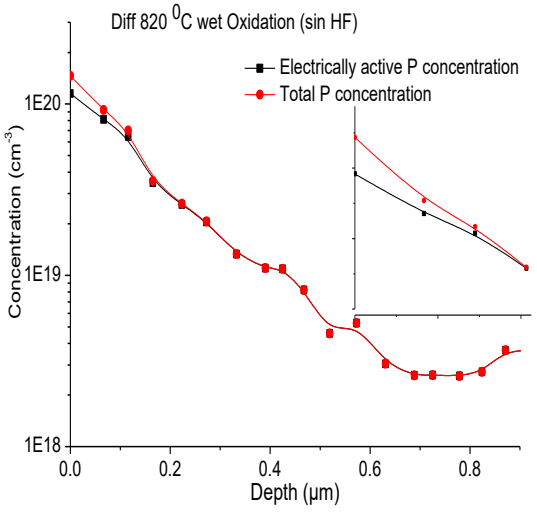
Wafer 2 belongs water free oxidation process of P diffusion and wafers 3 and 4 belong to HF free process of low temperature diffusion. Summary of the results is given in table 4.8

Table 4.8

Sheet Resistance $R_S(\Omega/\square)$	PC1D Conc. N (At/cm^3)	Q (cm^2/s)	Depth (µm)	By equation (theoretically) (N) (at/cm3)
Wafer 2	Only dry oxidation 30 mins + 1 hour drive in			
32	1.06E20	1.95E15	0.77	8.42E19
32	1.06E20	2.03E15	0.77	1.46E20
45	6.69E19	1.13E15	0.77	6.11E19
37	8.79E19	1.68E15	0.77	8.72E19
18	2.13E20	3.82E15	0.77	3.87E20
Wafer 3	HF free process (20 mins wet oxidation + 1 hour drive-in)			
58	4.75E19	8.55E14	0.73	4.0E19
60	4.42E19	8.80E14	0.72	3.27E19
55	5.11E19	1.02E15	0.72	4.65E19
48	6.16E19	1.05E15	0.72	5.28E19
61	4.42E19	7.99E14	0.68	2.93E19
Wafer4	HF free process (20 mins wet oxidation + 1 hour drive-in)			
66	5.66E19	5.66E14	0.77	2.95E19
32	1.03E20	2.13E14	0.77	1.12E20
87	2.88E19	5.43E14	0.77	3.29E19
33	1.14E20	1.74E15	0.77	1.31E20

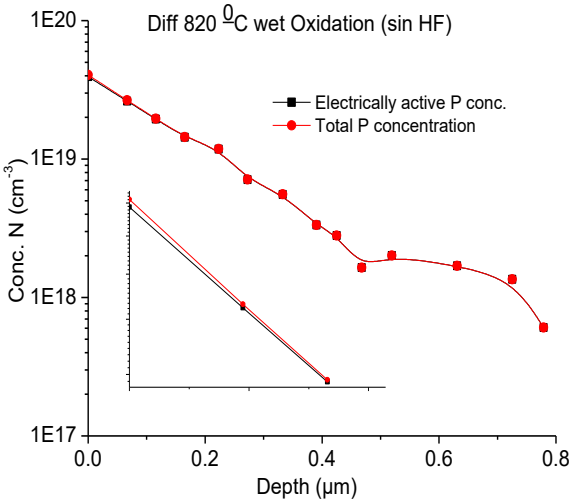
By using equation 4.23, derived from Fair and Tsai model [6], we have calculated total concentration of P diffusion in water free process and HF free process. Figures 4.42

(a&b) show the graphs for P Diffusion profiles of electrically active concentration and total concentration for HF free process while figure 42 (c & d) show the graphs for P diffusion profiles of electrically active concentration of P and total concentration of P diffusion of water free oxidation process**.** This total concentration includes both electrically active and inactive impurities. As it has been mentioned before this amount of inactive phosphorus correponds to the dead layer extent, which appear in the form of PSG.



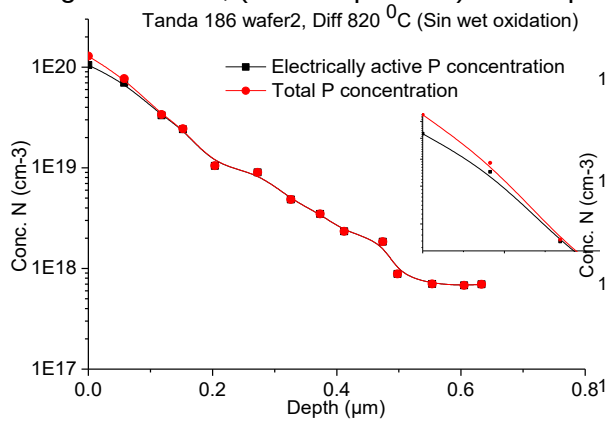
a

P profile of the emitter doped at 820 ºC with electrically active and total concentration after 20 minutes wet oxidation with 1 hour of drive-in, in nitrogen ambient, (HF free process)



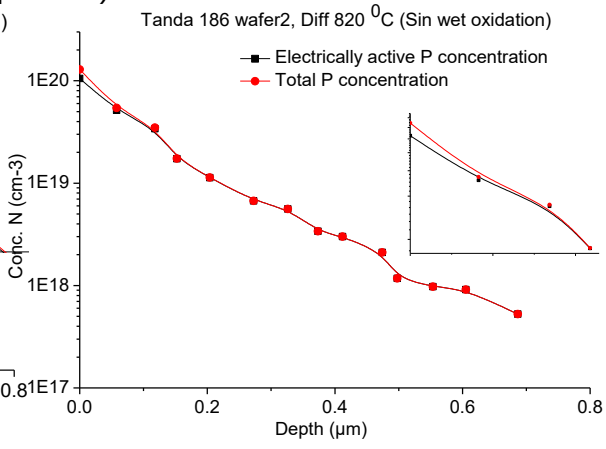
b

P profile of the emitter doped at 820 ºC with electrically active and total concentration after 20 minutes wet oxidation with 1 hour of drive-in, in oxyclean environment, (HF free process).



c

P profile of the emitter doped at 820 ºC with electrically active and total concentration after 20 minutes dry oxidation with 1 hour of drive-in, (Dead layer is removed by HF)



d

P profile of the emitter doped at 820 ºC with electrically active and total concentration after 20 minutes wet oxidation with 1 hour of drive-in, in oxyclean ambient, (Dead layer is removed by HF)

Figure 4.42 P Diffusion profiles of electrically active concentration and total concentration, a and b graphs show the plots for HF free process while c and d show the plots for water free process. (Graphs of figure 4.42b and 4.42d are oxyclean process)

From these graphs as shown in figure 4.42 of water free process and HF free process of low temperature P diffusion, it is clear that with dry oxidation with drive-in step and removal of dead layer by HF prior to drive-in step, it converts electrically inactive P concentration into electrically active P. Total concentration of P diffusion and electrically active P is almost overlapped in graphs, which represents that concentration of P diffusion is more than 96% electrically active. Electrically active concentration of phosphorus, which is calculated from sheet resistance values of emitters by PC1D as it is mentioned early and total concentration of phosphorus diffusion is calculated from Fair and Tsai model by using equation (4.23). In addition to this oxyclean ambient is recommended for oxidation and drive-in process.

4.8 Single step diffusion process (Industrial process)

Low temperature P diffusion process with water vapor free oxidation and without HF treatment was carried out at 820 ºC to see the effect of dry oxidation on sheet resistance and junction depth of emitters. Although we have performed this process in two step, just to check the sheet resistance values but this process feasible to perform in a single step diffusion and this process is applicable for emitter formation at industrial level for silicon solar cell fabrication. Step by step description of phosphorus diffusion is given in flow sheet diagram in figure 4.43.

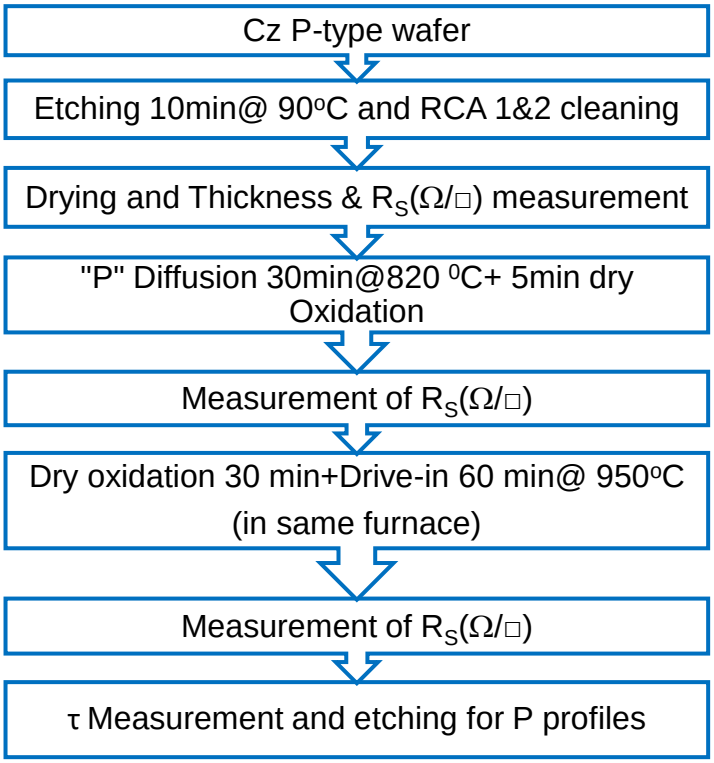


Figure 4.43 Flow sheet representation of P diffusion with water free oxidation and without HF treatment

Description of diffusion process with respect to time and temperature is shown in figure 4.44. After phosphorus diffusion dry oxidation is performed without HF treatment, which is used to remove the dead layer. In this process 30 minutes of dry oxidation is carried out with 1 hour of drive-in to get industrially feasible softly doped and deep emitters.

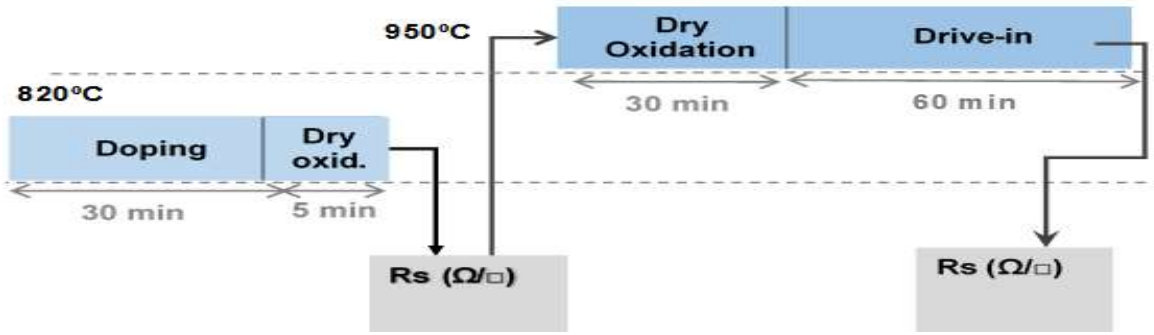


Figure 4.44 Flow sheet representation of P diffusion with water free oxidation and without HF treatment

After drive-in process, etching of emitters was carried out in 2% solution of NaOH at 60 ^{0}C as it is mentioned early in this chapter. After 15 second etching, (about ~50 nm thickness of each surface of wafer is removed in this short etching time). Wafers were cleaned and dried to measure the sheet resistance of exposed surface by 4-point probes. This process is repeated again and again until sheet resistance showed complete removal of emitters and sheet resistance values were similar to base doping. In this way we can estimate the junction depth. Surface concentration was calculated by PC1D, using a Gaussian model with values of the sheet resistance for the corresponding values of depth junction. By using concentration data obtained from PC1D are plotted against the junction depth to get the doping profiles of the emitters, low temperature diffusion with water and HF free process is shown in figures 4.45 & 4.46. Process which is shown in figure 4.46 is oxyclean process. Both processes are single step diffusion process.

4.8.1 Single step diffusion profiles

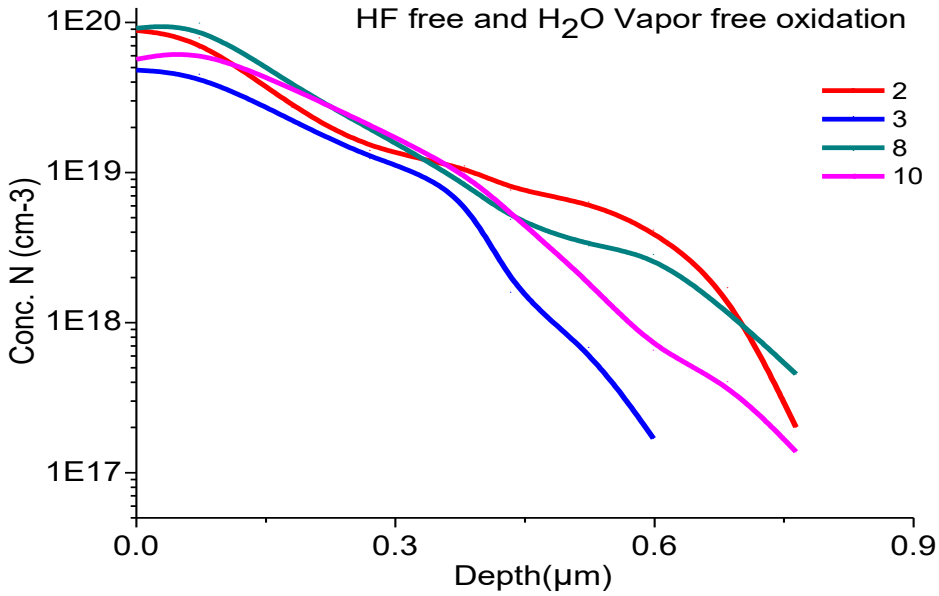


Figure 4.45 P diffusion profiles for emitter doped at 820 ºC with 30 minutes dry oxidation and 1 hour of drive-in, in nitrogen ambient, (Water free oxidation process, HF free process)

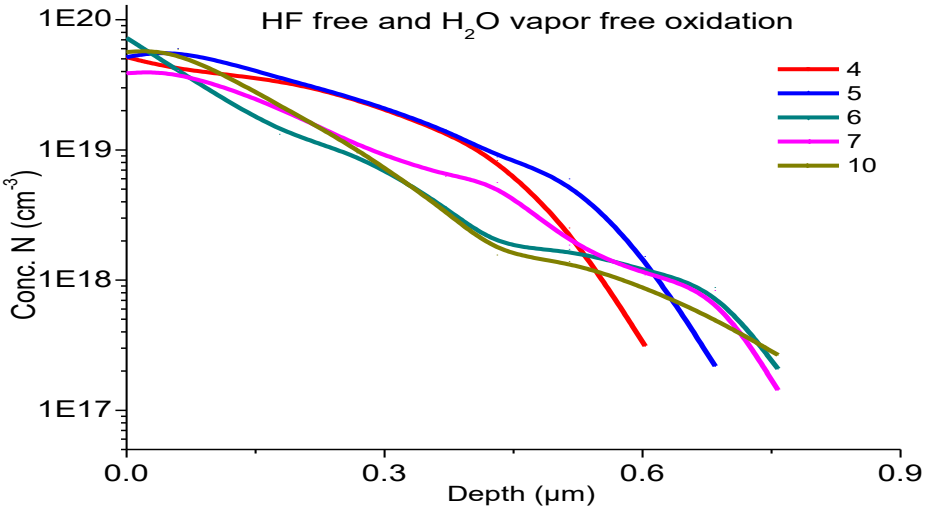
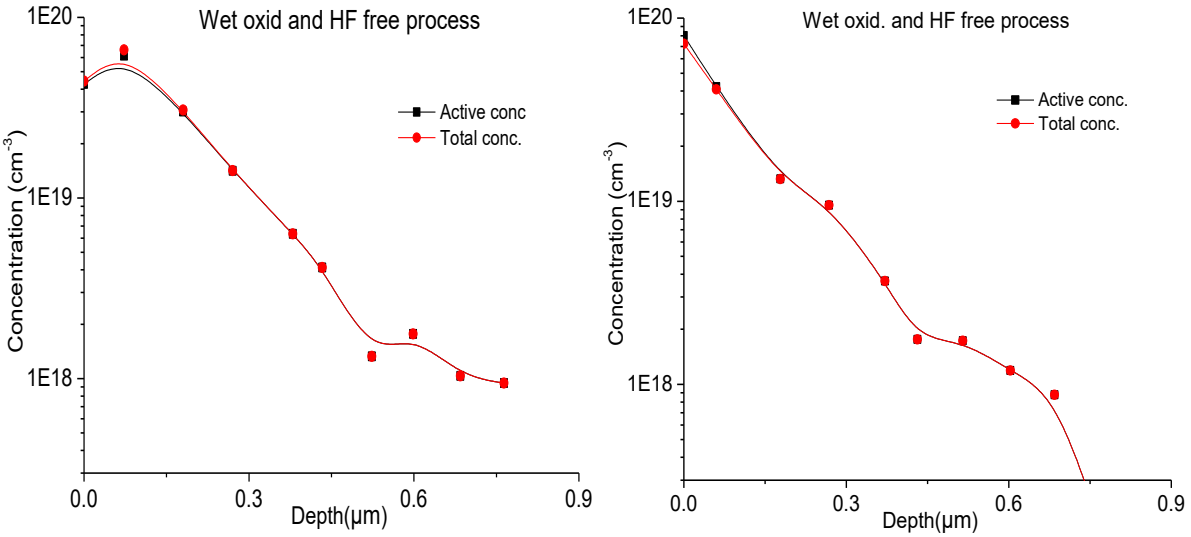


Figure 4.46 P diffusion profiles for emitter doped at 820 ºC with 30 minutes dry oxidation and 1 hour of drive-in, in oxyclean environment. (Water free and HF free process)

By using equation (4.23) derived from Fair and Tsai model [6], we have calculated total concentration of P diffusion in water free process and HF free process. Figures 4.47 a and b show the graphs of P Diffusion profiles of electrically active concentration and total concentration for HF free process and water free process**.** This total concentration includes both electrically active and inactive impurities. As it has been mentioned before this amount of inactive phosphorus correponds to the dead layer extent, which appear in the form of PSG.



a

P profile of the emitter doped at 820 ºC with electrically active and total concentration after 30 minutes dry oxidation with 1 hour of drive-in, in nitrogen ambient, (HF free process, Water free oxidation process)

b

P profile of the emitter doped at 820 ºC with electrically active and total concentration after 30 minutes dry oxidation with 1 hour of drive-in, in nitrogen ambient, (HF free process and Water free oxidation process)

Figure 4.47 P Diffusion profiles of electrically active concentration and total concentration, for HF free process and water free process (Single step diffusion process)

In single step diffusion process, concentration of P more than 97% is electrically active. From graph as shown in figure 4.47, it is clear that there is almost no difference in electrically active P and total concentration of P. Due to low temperature diffusion, dead layer which is produced due to electrically inactive P is vanished. Sheet resistance, concentration, Q and junction depth values of single step diffusion process is given in table 4.10. As it is described early in this chapter that our aim was to get softly, deep and passivated emitters. In this addition to this, our goal was to perform P diffusion in a single thermal process. We have used 820 ºC P difffusion as standard process due low temperature diffusion and reprduceability of P diffusion results. In our standard process,we have obtained surface concentration in range of 3-7x10^{19} cm^{-3} which is related to ~100 Ω/□ and around 0.60 µm junction depth. In these experiments, we have presented the incorporation of wet oxidation step (10-20 minutes) in between pre-deposition and drive-in, in order to the reduce electrically inactive phosphorus concentration, the dead layer extent. We have decreased the surface concentration below 1x10^{20} cm^{-3} with sheet resistance ~60-100 Ω/□.

Low temperature diffusion which is modificaiton of our standard process to get softly and deep emitters in a single thermal process (single step diffusion process). From experiments data of low temperature diffusion under different oxidation condtions, we have obtained some variation in results with respect to concentration and junction depth which we have obtained in standard process. As shown in graph in figure 4.48. Surface concentration of these lower temperature processes are lower than 8x10^{19} cm^{-3} with junction depth around $0.68 \pm 0.03\ \mu m$, which is more deeper than standard process.

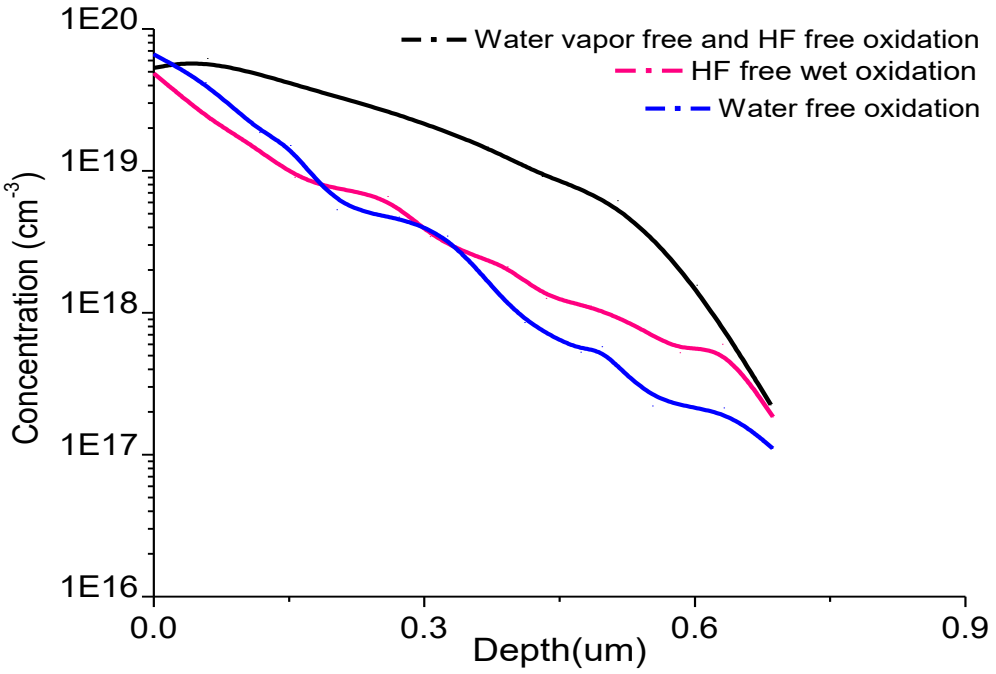


Figure 4.48 Diffusion profiles of low temperature process, doped at 820 ºC under variable process conditions.

Our process runs in oversaturation condition, It has some advantages in comparison to other processes with low Ns target that do not run in oversaturation condition. Each process of fabrication of emitters gives specific result in term of sheet resistance, surface

concentration and junction depth. Reliability of emitter is evaluated by the influence of passivation. For each emitter surface conditions, surface recombination velocities have been simulated by PC1D. results have been plotted against sheet resistance for corresponding to a conventional 0.2 and the current 0.7 µm junctions depth, in order to highlight the importance of having softy doped and deep junctions. Simulation results are shown in figures 4.49, 4.50 and 4.51. These simulations results show that deep emitters are better than superficial emitters and gives good passivation.

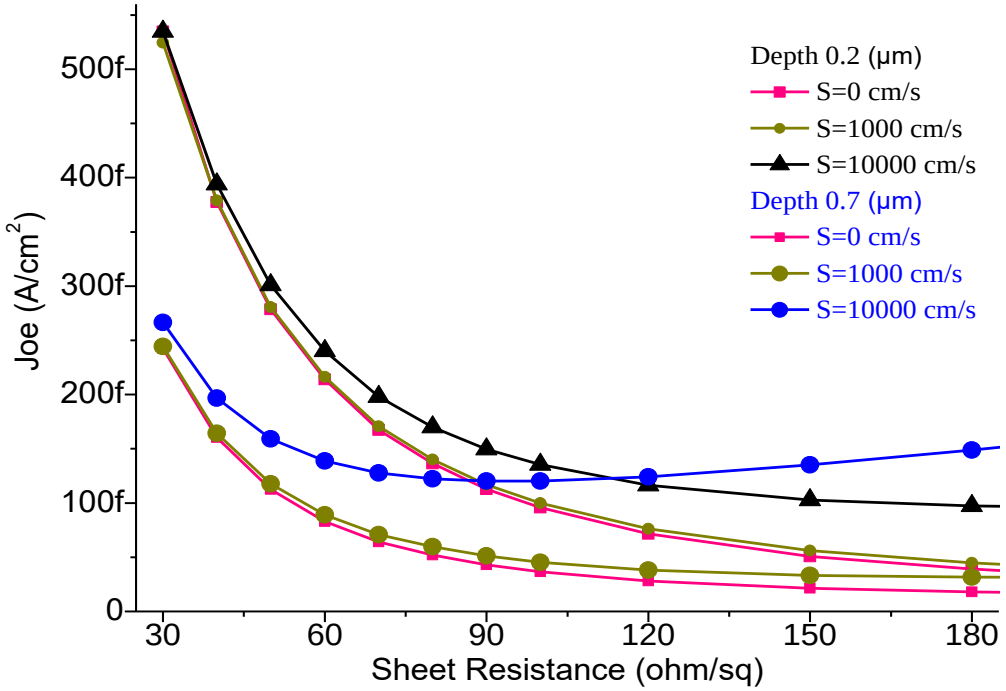


Figure 4.49 Saturation current of 0.2 and 0.7µm junction depth emitters resulted for several surface recombination velocities, values of S from 0 cm/s to 1000 and 10000 cm/s.

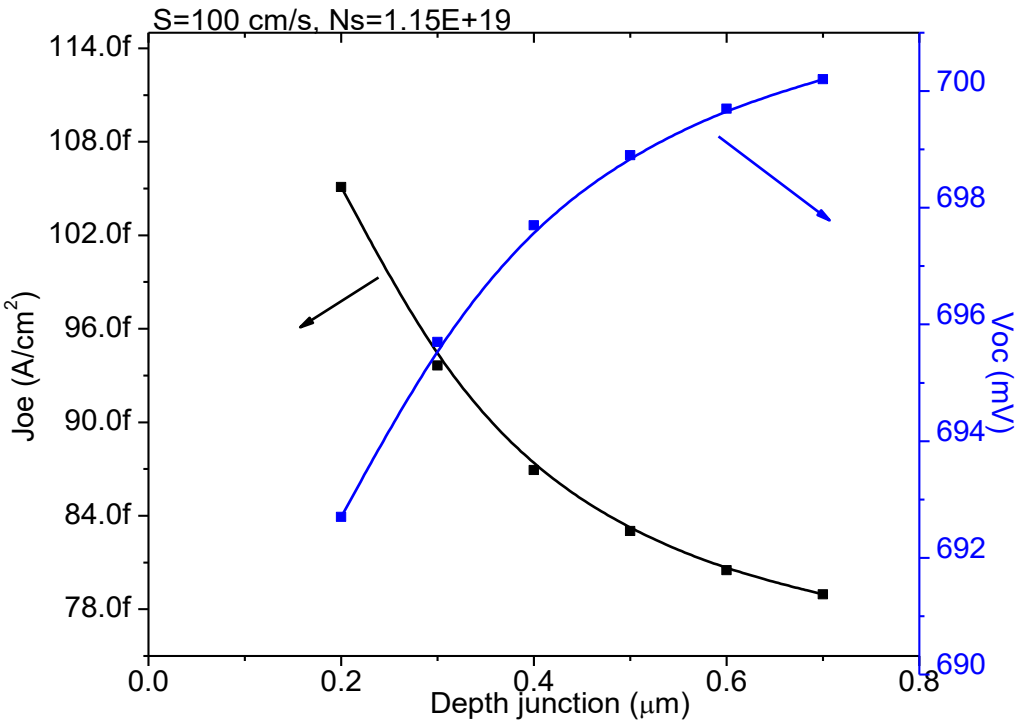


Figure 4.50 Saturation current density and Voc effect on junction depth emitters resulted from 100 cm/s surface recombination velocities

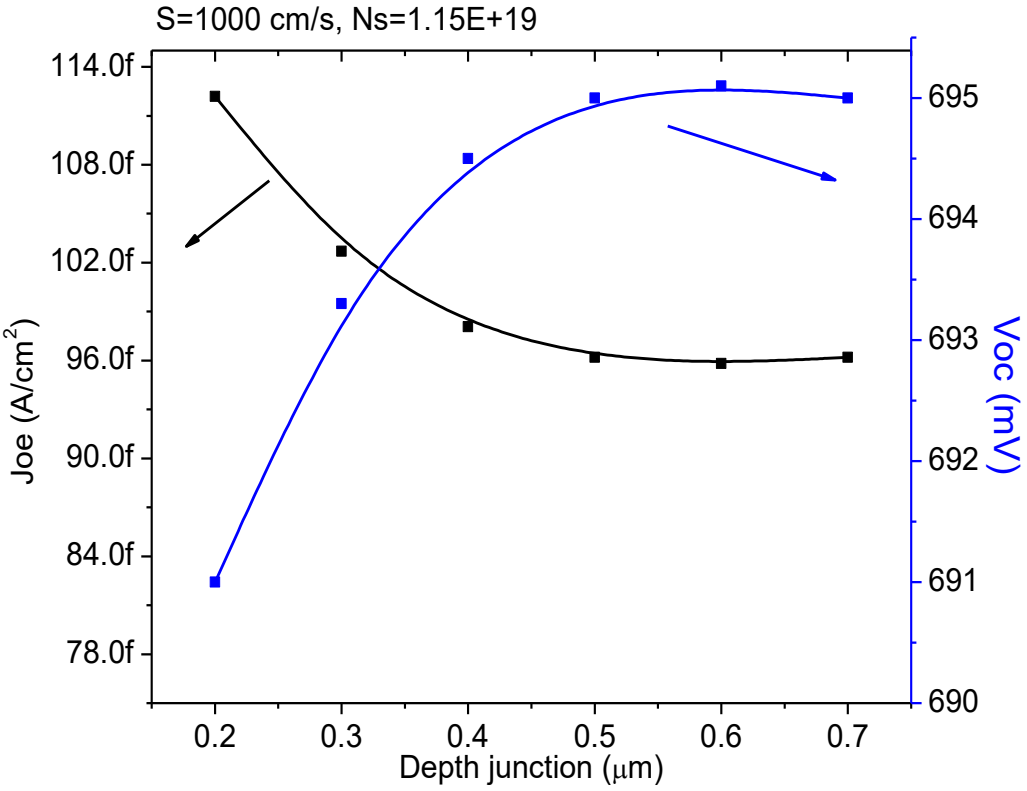


Figure 4.51Saturation current density and Voc effect on junction depth emitters resulted from 1000 cm/s surface recombination velocities

Besides the positive influence of having deep emitters in the Joe values, we have seen more influence of a good surface passivation for softly doped and deep emitters, moderate

sheet resistances, changing from 36 to 120 fA/cm^2, the advantages obtained from a lowly doped emitter has disappeared when junction depth is shallow. This figure 4.49 shows the influence of a good surface passivation for softly doped and deep emitters with moderate sheet resistances is changing from 58 to 130 fA/cm^2. This can be seen in the table 4.9 [34-35].

Table 4.9 Saturation current density (Joe) values for different values of surface recombination velocities

	J_{OE}(fA/cm^2)		
R_S (Ω/□)	S=0 cm/s	S=1000 cm/s	S=10000 cm/s
30	600	600	600
53	130	140	184
60	130	130	170
100	58	68	130

As I have mentioned early, some modification have been carried out in our standard process in order to achieve one thermal step process in the diffusion furnace, removing the intermediate chemical or wet oxidation steps. On this occasion, the impurity concentration in the surface increases significantly 7-8 x10^{19} cm^{-3} and the sheet resistance decreased. It can be observed that the charge of phosphorus impurity is the same, it seems that charges trapped in the oxide are very few, but the junction is deeper. Emitter deeper gives the chance of having less recombinant emitters. Results of above mentioned processes is summarized in table 4.10.

4.8.2 Summary of Low temperature diffusion

Overall results of low temperature P diffusion processes, including singe step diffusion process are given in table 4.10.

Table 4.10 Summary of Low temperature diffusion process (820 ºC)

Sheet Resistance R_S(Ω/□)	PC1D Conc. N (At/cm^3)	Q (cm^2/s)	Depth (µm)	Result
Diffusion at 820 ºC (with 20 min. wet oxidation)+ 1 hour of drive-in				
110	3.17E+19	4.32E+14	0.52	
129	1.89E+19	3.28E+14	0.62	
87	3.48E+19	5.8E+14	0.62	
59	6.05E+19	1.02E+15	0.62	
103	3.4E+19	5.9E+14	0.58	Average result
Diffusion at 820 ºC (with 20 min. wet oxidation) oxyclean process (HF free process)				
58	502E+19	8.9E+14	0.72	
62	4.0E+19	7.3E+14	0.82	
55	6.16E+19	9.27E+13	0.68	
66	4.33E+19	8.21E+14	0.68	
53.2	6.44E+19	1.2E+15	0.78	Average result
Diffusion at 820 ºC (with 20 min. wet oxidation) with drive-in (HF free process)				
69	7.21E+19	2.87E+14	0.48	

87	4.5E+19	5.78E+14	0.54	
79	5.9E+19	9.4E+19	0.48	
59	8.75E+19	9.77E+14	0.48	
32	1.3E+20	2.2E+15	0.64	
65	2.19+19	1.08E+15	0.53	Average Result
Diffusion at 820 ºC (water free oxidation process) +HF+ 20 dry oxidation with drive-in				
32	2.01E+20	2.13E+15	0.63	
81	8.18E+19	5.19E+14	0.5	
131	6.18E+19	3.62E+14	0.38	
37	1.31E+20	1.61E+15	0.77	
81	7.55E+19	3.85E+14	0.52	Average result
Diffusion at 820 ºC (water free and HF free process) + 30 dry oxidation with 1 hour drive-in Single step diffusion process				
61	5.25E+19	8.6E14	0.69	
55	6.06E19	9.3E14	0.69	
53	5.55E19	9.14E14	0.76	
49	6.18E19	9.01E14	0.76	
53	6.18E19	9.41E14	0.71	Average result

In addition to passivation, gettering effect in this single step diffusion process (Proposed process) is much higher than with conventional process. Getterging effect is evaluated by liftime measuremts. Results are given in Table 4.11 for comparison of gettering effect of our prosposed process with conventional process. For this purpose different kinds of wafers, including metallurgical grade silicon (MC) wafers has been used.

Table 4.11 Gettering effect on different kinds of wafers

Conventional process			Proposed process		
n-type wafer	p-type wafer	M.C wafers	n-type wafer	p-type wafer	M.C wafers
55µs 62µs	20µs 23µs	10µs	250µs 500µs	178µs 201µs	33µs

The improvment due to gettering by our proposed process is much higher than conventional process for the n and p-type wafers. In case of metalligical grade silicon wafers, by our proposed process improvement in lifetime is more than 3 times higher than conventional process. 33µs lifetime has achieved for metallurgical grade wafers by our process which is much higher than conventional gettering process. Emitters obtained by a single step thermal have concentration in range of 7-8 x10^{19} cm^{-3} with sheet resistance ~60 Ω/□ and junction depth is around 0.71 µm and saturation current of emitter is around 130 fA/cm^2.

4.9 Conclusion:

Phosphorus diffusions are used in solar cells fabrication process for all kinds of crystalline-silicon (c-Si) materials to form the *n*+ type emitter. Post diffusion oxidation is also common step in commercial fabrication sequence of crystalline solar cell. The quality of the emitter plays an important role for solar cell efficiency due to formation of P-N junction, which

is the core of the crystalline silicon (c-Si) solar cell. If the P surface concentration is high and exceeds the intrinsic charge-carrier concentration, have certain special features on electrical properties and conductivity [22-23].

The quality of emitters depends on diffusion temperature with flow of gases and doping time. At high temperature, concentration of phosphorus (P) exceed the solubility in Si ($10^{21}/cm^3$) which form a dead layer [24-25].which is electrically inactive and has effect on surface P concentration and junction depth. It produces recombination centers that increase Auger recombination that increase saturation current density (Joe) [26-27]. Moreover high surface P concentration increases the recombination (Auger recombination) which limits the lifetime and lowers the open circuit voltage (Voc) with overall solar cell efficiency [28]. Due to high P doping concentration, bandgap narrowing effect arises, which cause the absorption of photons in emitters region near the front surface. In addition to this, electrically inactive P also introduces defects in the crystalline lattice of silicon, Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure and also take part in efficiency loss due to high recombination (low lifetime). The amount of inactive phosphorus in term of surface concentration and depth junction can be improved by converting electrically inactive phosphorus into electrically active phosphorus by introducing a wet oxidation with drive in step after diffusion. When the extent of dead layer (electrically inactive) decrease emitter recombination probabilities also decrease which improves open circuit voltage (*Voc*), short circuit current density (*Jsc*) and efficiency of solar cell. [29-32]. In this work, we have performed several experiments in order to study the effect phosphorus diffusion on emitters under different temperature (800, 820,840 and 875 ^{0}C) with different conditions of wet oxidation and drive-in to get shallow and deep n+ emitters. The emitter saturation current which limits the open circuit voltage depends on active phosphorus concentration and junction depth. Concentration profile of phosphorus is determined by alkaline etching at 60^{0}C by using low conc. of NaOH (2%) to find the junction depth and doping concentration is determined by PCID simulation by using sheet resistance data.

The sheet resistance data is given in figure 4.18, 4.19 and 4.20 as well as in table 4.5. Sheet resistance data shows a non-uniformity of the P distribution at low temperature. It is observed that with increase of pre-deposition temperature increases the surface concentration (N_S) and makes the P distribution more uniform. But at high temperature, due to over solubility limit, P appears as in the form of dead layer, an electrically inactive layer of P. This electrically inactive P also introduces defects in the crystalline lattice of silicon, as a result Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure. High concentration of soluble P in Si increases the Auger recombination. These two types of recombination increases saturation current density, as a result cell *Voc* and *Jsc* decrease due to high recombination rate. At low temperature p diffusion, around 90% P is electrically active but at high temperature around 60% P is electrically active. The percentage of active P is calculated By Tsai Model [6]. Our results show that with increase of temperature, active P concentration decrease and vice versa. However we have introduced a wet oxidation step with drive in. it converts electrically inactive P into active P and decrease the recombination and improve surface quality for passivation. We have found a very thin surface region in which the surface concentration N may reach nearly 10^{20} atom/cc. However, this region is no more than 100 nm deep. Moreover PN junction depth can be control by drive in time but it also depends on pre-deposition condition (temperature, dopant and oxygen ratio). To get high efficiency and improve *Voc*, it is necessary to minimize the electrically inactive P in emitters. Our approach is removal of oxides grown during P pre-deposition by HF treatment. Next step is wet oxidation with drive-in which forces the precipitated P to diffuse into silicon and converts electrically inactive P into electrically active P.

By using PC1D simulation, we have simulated doping concentration of phosphorus diffusion data to predict efficiency of silicon solar cell. Results which are shown in graphs of figure 4.33 and 4.34 represent that moderate or low doped emitters give high efficiency. Due to this reason, we have planned to investigate low temperature diffusion for softly or moderate doped and deep emitters for silicon solar cell fabrication process to gain high efficiency. The result which we have obtained at 800 ºC is not uniform in out furnace system as compare to 820 ºC, we planned to proceed P diffusion at 820 ºC as standard process. In addition to this, doping concentration of P at 820 ºC is 95% electrically active as compare to high temperature diffusion. Due to this reason, there is lower probability to have recombination centers due to electrically inactive phosphorus.

The main goal of this investigation was to make a single step diffusion process in a furnace. We have conducted some experiments in order to achieve single step diffusion process for industrial solar cell fabrication. Prior to these experiments, we have investigated the effect of dry oxidation and HF free process to compare with wet oxidation. Process was started from pre-deposition step at 820 ºC followed by 20 minutes of oxidation with 70 minutes of drive-in at 950 ºC. Intermediate oxidation is water vapor free process. It has been observed that charges trapped in the oxide are very few, but the junction is deeper. Soft emitters have less chance of recombination in emitter region. Results of these emitters profiles are shown in figure 4.48 and summarized in table 4.10. Reliability of emitter is evaluated by the influence of passivation. For each emitter surface conditions, some surface recombination velocities have been simulated by PC1D. Results corresponding to a conventional 0.2 and the current 0.7 µm junction depths are plotted in graph. The influence of a good surface passivation for softly doped and deep emitters with moderate sheet resistances, is ranging from 58 to 130 fA/cm^2. Emitters obtained by a single thermal step have concentration in range of 7-8 x10^{19} cm^{-3} with sheet resistance ~60 Ω/□ and junction depth 0.71 µm and saturation current of emitter is 130 fA/cm^2. In addition to passivation, gettering effect in this single step diffusion process (Proposed process) is much higher than conventional process. Getterging effect is evaluated by liftime measuremts. In case of metalligical grade silicon wafers, by our proposed process (single step diffusion) improvement in lifetime is more than 3 times higher than conventional process. In case of P-type material, we have measured lifetime around 200 µs at high resistivity (5.4Ω.cm) wafers and on N-type low resistivity (0.8 Ω.cm) wafers around 505 µs by PCD technique. Improvement in lifetime is higher than conventional gettering processes.

4.10 References

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Chapter 5

5 Passivation and Selective Emitter Formation

5.1 Silicon passivation

Solar cell efficiency is limited by the recombination of electron hole pairs generated by photon. This recombination process occurs at the surface as well as at the interfaces. Lowering of recombination at the surface is accomplished by reducing the number of dangling bonds at the surface by deposition of passivating layer on surface. Solar cell industry usually replies on thermally grown silicon dioxide to passivate the dangling bonds. There are two ways to grow oxide layers either by thermal oxidation or by non-thermal oxidation (chemical vapor deposition). The presence of silicon dioxide helps to adjust the lattice constant of silicon and decrease density of voids and density of dangling bonds. Since silicon dioxide offers low cost production and scalability to large area implementation. There are many amorphous silicon based compounds used for surface passivation, which are given below;

Silicon dioxide (SiO_2)
Silicon nitride (Si_3N_4)
Silicon carbide (SiC)

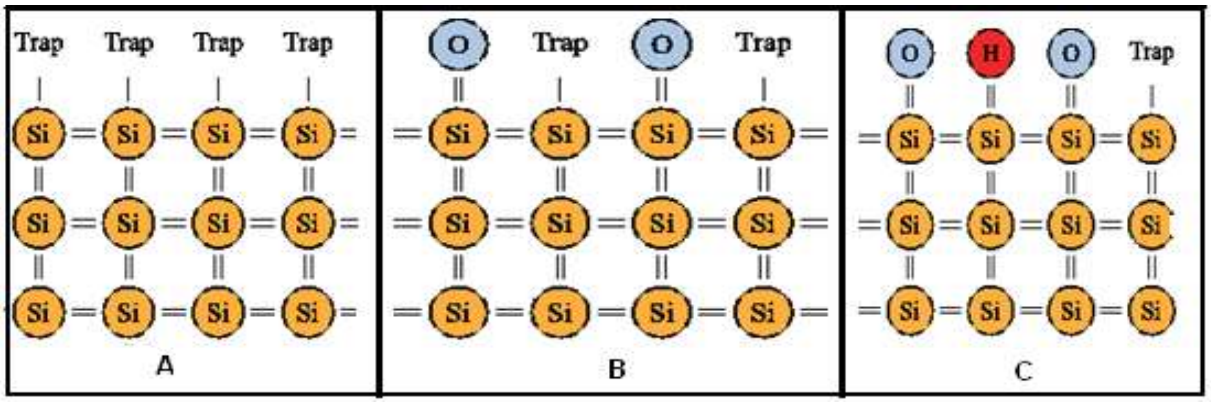


Figure 5.1 (A): At silicon surface, silicon atoms are missing and unpaired valence electrons are forming electrically active interface traps. (B) After oxidation most interface states are saturated with oxygen bonds. (C) After annealing the surface with a hydrogen related species the amount of interface defects is further decreased.

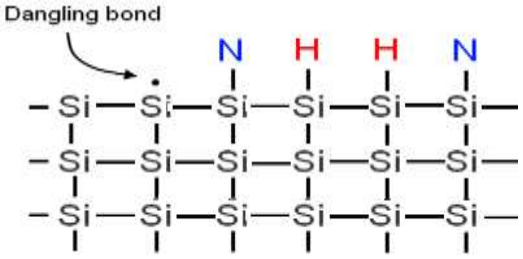


Figure 5.2. Silicon surface with unpassivated dangling bond and silicon surface atoms passivated with nitrogen and hydrogen atoms

Deposition condition and stoichiometric variations strongly effect on the optical and electronic properties. Surface with high content of silicon show a strong optical absorption in visible-ultraviolet range, with low conductivity as compare to crystalline silicon. When content of silicon is low, light absorption and conductivity decrease and exhibit transparency and dielectric properties [1].The methods which are used for passivation normally based on decomposition of hydrogenated gases. High content of hydrogen gas ensure to improve the surface passivation by saturating dangling bonds as shown in figure 5.2. This hydrogen is also beneficial for passivation of the defects in bulk of low quality grade silicon material. Oxygen content also improves surface passivation by saturating the dangling bonds.

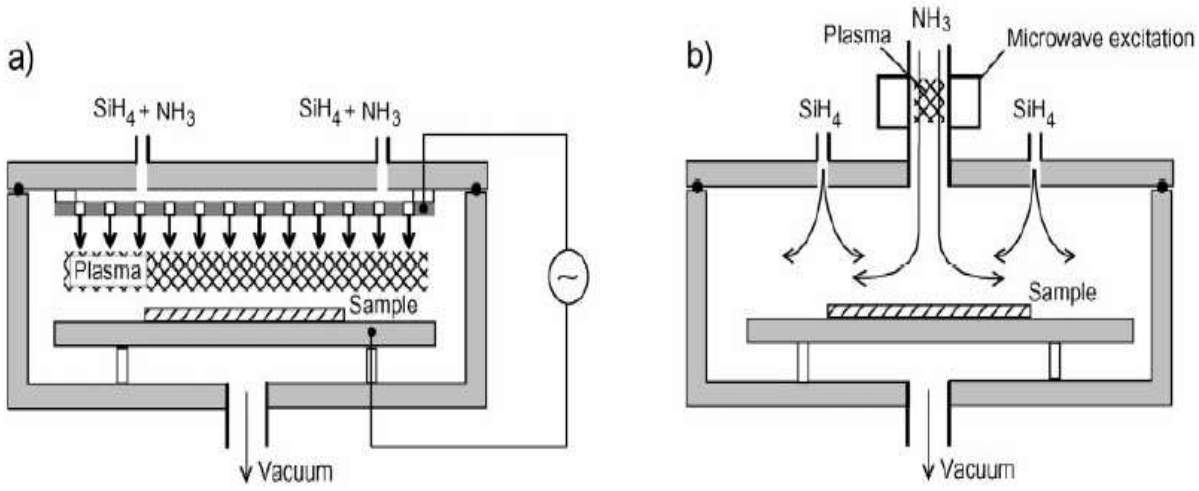


Figure 5.3. (a) Direct-plasma reactor excited through a RF source and (b) Remote-plasma reactor using microwave excitation process used to deposit SiNx. Extracted from reference [2]

5.2 Deposition Techniques:

Process of applying a thin film on a substrate is called deposition. There are many techniques which are used to deposit a thin film (layer) onto a substrate ranging from tenth of nanometer to micrometer scale. Deposition techniques are divided into two main categories:

1. Physical deposition techniques
2. Chemical deposition techniques

Deposition techniques are used in the fabrication of optics (reflective and antireflection layers) and electronics (as an insulating layer, semiconductor and conductors forms of integrated circuits as well as in solar cells fabrications). In physical deposition techniques, mechanical, electromechanical or thermodynamic means are used to produce a thin film. Commercially physical deposition system require a low pressure vapor environment that function properly, it is classified as physical vapor deposition (PVD). Electron beam evaporator is one of example, in which high energy beam is fired from electron gun to boil the material and deposited on the substrate after evaporation. Sputtering, molecular beam epitaxy, electro-spray and thermal evaporation are physical deposition techniques.

While in chemical deposition techniques, precursor reactants undergo a chemical change at substrate surface and leaving a solid layer. In chemical deposition technique, thin film produced from deposition tends to be conformal rather than directional

(deposition take place everywhere on the substrate). There are many techniques for chemical depositions Such as Hot wire chemical vapor deposition, spin coating, electroplating but in case of silicon solar cell, plasma enhanced chemical vapor deposition is considered as commercial techniques for fabrication.

There are some other techniques used for deposition of thin layer, such as sputtering and hot wire chemical vapor deposition (hotwire CVD). Sputtering is a physical deposition technique, which is based on bombardment of ions on solid silicon surface coming from plasma excited gases. This technique has advantages over PECVD, because no silane gas is used due to its explosive nature and also produces uniform film in composition and thickness in large area. While hotwire CVD is based on decomposition of gases by using high temperature (1600 ºC). No plasma and no voltage is applied inside the chamber, therefore is not chances of wafer damages due to ion bombardments.

5.2.1 Plasma Enhanced Chemical Vapor Deposition (PECVD):

PECVD is a technique used to deposit thin films from gas state (vapors) to solid state on a substrate. Chemical reaction which takes place after creation of plasma of reacting gases (vapors). Plasma is generally created by RF (radiofrequency) or DC discharge between two electrodes and space is filled with reacting gases. In silicon solar cell fabrication, PECVD technique is used to deposit antireflection layer of silicon nitride (SixNy). Silicon nitride layer not only acts as antireflection layer but also use for passivation of dangling bond.

Plasma enhanced chemical vapor deposition (PECVD) forms a thin film from precursor gaseous mixture, whose molecules are broken by using electric field. The gaseous excitation is used to produce plasma between two electrodes of electric field. The instrument can be divided into two types of configurations, first type in which wafer is places in contact with plasma directly is called direct configuration and second in which wafers and plasma are place separately in different chambers is called remote configuration. A schematic of both configurations are shown in figure 5.3 [2]. In case of silicon nitride deposition, this material is formed by the decomposition of silane and ammonia gases. In case of direct configuration, both gases are excited together while in case of remote configuration silane is introduced directly in the deposition chamber, where it reacts with decomposed atoms of nitrogen and hydrogen also come from excitation chamber. The plasma excitation frequency has a strong influence on electronic properties of resulting film silicon interface.

Surface damage is also observed during deposition; it is due to high frequency (so call plasma frequency <4MHz) ions which also follow the plasma excitation frequency and produces a strong surface bombardment which cause the surface damage. The film deposition with low frequency direct PECVD provide an intermediate quality surface passivation. This problem can be solved by using frequency higher than 4MHz with shorter acceleration period, in this way ions do not absorb significant amount of energy which could cause surface damage. Hence film fabricated by direct PECVD at high frequency (6-13MHz) provides a better quality surface passivation than film fabricated at low frequency. In addition to this, introduction of a remote chamber further improves quality of the surface passivation, because in this process no ion bombardment is produce and wafer is prevented for further damage.

5.2.2 Silicon nitride (Si_3N_4):

Silicon nitride is the state of art in surface passivation for crystalline silicon solar cell. Silicon nitride has been extensively used in research since last two decades**.** Silicon nitride film provides excellent surface passivation, transparency, antireflective properties and stability under ultraviolet light exposure and high thermal treatment. There are huge number of articles published in scientific journals, explain surface passivation properties of silicon nitride [3-4]. Preliminary studies on silicon nitride indicated that quality of surface passivation improved as fraction of silicon in silicon nitride film increased. High fraction of silicon also led to higher refractive indexes and higher extinction coefficient, with some absorption of light within film that does not contribute to the photocurrent. The introduction of nitrogen gas in plasma enhanced chemical vapor deposition system (apart from silane and ammonia) produced a transparent layer (film) with record low values of surface recombination velocity. For low resistivity p-type silicon wafers, by using this passivation, scheme was able to achieve surface recombination velocity lower than 10 cm/s with conventional PECVD in direct configuration.

At laboratory scale, to improve the quality of silicon nitride, remote PECVD is used in order to avoid ion bombardment but it is old technique. Direct PECVD technique is commercially available technique used to deposit SiNx. Another strategy which improves the quality of silicon nitride is thermal oxidation before the Si_3N_4 deposition. SiO_2 provides a low interface density and Si_3N_4 provides an extra field effect. Combination of such stacks of film provides effective recombination velocity lower than 3cm/s on p-type wafers with (1 Ω.cm) [5]. Hao et al also obtained similar results by using stacks of SiO_2/Si_3N_4 grown by LPCVD (low pressure CVD) at 775 ºC [6]. But without of SiO_2, silicon nitride deposited by LPCVD has given worse results due to serious irreversible bulk damage to silicon due to high temperature. Thin layer of SiO_2 helped to reduce the damage while thick layer of SiO_2 (about 50nm) completed eliminated the effect of bulk damage. On P-type wafer with high resistivity (100Ω.cm) S_{eff} value lower than 2 cm/s was achieved.

Passivation of silicon nitride with annealing after deposition of Si_3N_4 extensively has been studied in order to see the lifetime improvement. Effective lifetime verses annealing time curve usually reach a maximum point followed by decay and then saturate. With increase of process temperature, peak becomes narrower and located at shorter annealing time [3, 7]. It is useful for industrially screen printed solar cells, in which metal paste is printed on wafers to define the front and read contacts. After defining contacts, wafers are processed at high temperature 750-950 ºC for few seconds to 3 minutes. Since passivation layer (Si_3N_4) is deposited before Screen printing process and it is necessary to keep or enhance the properties after processing. Schmidt et al [8] has represented that layer with a reflective index =2.1 enhance the wafer effective lifetime after short treatment at 900 ºC. The reflective of index (silicon nitride) higher than 2.4 decreases the lifetime.

5.2.3 Instrumental description

Figure 5.4 Description of PECVD machine used deposit SiNx layer

1) Electrical connections control unit
2) Power supply (Power switch)
3) Computer (for process and deposition control)
4) Process Chamber
5) Loading chamber
6) Source plasma and microwave generator
7) Gases and water supply unit

Surface passivation is very important for silicon solar cells in order to reduce the recombination losses. In this work, we have investigated passivation properties of silicon nitride composition deposited by PECVD as well as passivation with silicon oxide. Varying composition of passivated layer of silicon nitride is studied by measuring lifetime and ellipsometric measurements.

5.3 Surface passivation:

Recombination process in silicon solar cells occurs though a number of simultaneous processes depending on intrinsic or extrinsic nature of material. Intrinsic processes (radiative and Auger recombination) are unavoidable processes while extrinsic processes related impurities concentration, defects and imperfections within crystals (SRH recombination).There are two types of surface passivation process to reduce the Surface recombination velocity of silicon solar cell.

- Chemical passivation
- Field effect passivation

Chemical passivation reduces the SRH recombination rate by decreasing density of interface traps D_{it} . It can be done by deposition of a passivating film (Si_3N_4 or SiO_2) on the surface by saturating the dangling bonds. Chemical passivation, SiN_x is obtained by

chemical reaction of silicon with nitrogen atoms. Passivated and unpassivated silicon dangling bond are shown in figure 5.2. For surface recombination, it is necessary to have electrons and holes on the surface. Surface recombination via defects as described by SRH theory, depends on the ratio of carriers concentration. Maximum recombination rate is observed when n=p. Recombination rate decreases rapidly when the concentrations of one type of carriers decrease. One way to decrease the carrier concentration is by introducing an electric field with fixed dielectric film which electrostatic repels one type of carriers. This method is used to decrease the SRV depending upon the polarity of film. This method is known as field effect passivation which is shown in figure 5.5.

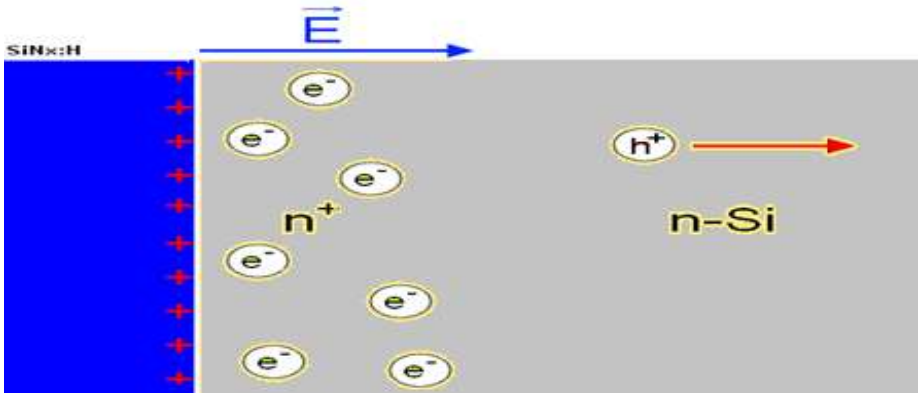


Figure 5.5 Field effect passivation by SiNx:H with fixed positive charges on n-type silicon substrate. Accumulation of electrons creates an electric field and repels the holes

5.4 The Lifetime Measurements

The effective lifetime is measured experimentally which sums of all recombination processes occur in silicon wafer. Lifetime is usually described by a single values parameters, it is complex concept and varies according to material quality, doping level, illumination level and injection of carries. The Lifetime of minority carriers is of particular interest is solar cells due to its effect on efficiency.

The decay of excess minority carriers due to recombination is called recombination lifetime and term lifetime is referred to the recombination lifetime of excessive minority carriers. As it is mentioned early in chapter 2, there are three recombination processes, which occur in silicon wafer, i.e. radiative recombination (band to band), Auger recombination Shockley-Read-Hall recombination (via traps within energy gap) in bulk and at the surface of wafer. Therefore effective lifetime is describes below in equation 5.1 and 5.2:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{auger}} + \frac{1}{\tau_s} \tag{5.1}$$

Radiative, Shockley-Read-Hall and Auger recombination are referred as bulk recombination. Thus effective lifetime is described as sum of lifetime in bulk and at surface.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \tag{5.2}$$

Auger lifetime can be calculated by using theoretical model by J. Schmidt et al [9].

$$Measured \text{ effective } lifetime = \frac{\Delta n}{\left(G - \left(\frac{d\Delta n}{dt}\right)\right)} \quad (5.3)$$

G is photo generation within wafer at time t, excessive carrier concentration Δn is calculated from photo conductance signal. However SRH lifetime depends on defects level in crystal lattice, it is more complicated to calculate theoretically. Bulk lifetime of extrinsic silicon can be calculated by using semi empirical models based on lifetime measurement of float zone silicon with low defect levels. The lifetime depends on the excess carriers and doping concentration, it is represented by M.J. Kerr et al [10] and more recent model is developed by A. Richter et al [11].

This equation describes general relationship for the lifetime of a wafer under any illumination. It depends on average carriers density and external generation. Equation 5.3 exist in the facts that all lifetime measurements methods are based on excessive carrier's density Δn. There are 3 different states of thermodynamics equilibrium, in which transient state (with no external generation) and quasi steady state (with almost constant generation) techniques are used to measure lifetime of silicon solar cells [10-11]

5.4.1 QSSPC technique

It is most common technique to measure passivation of this film deposited on crystalline silicon. In crystalline silicon solar cells both bulk and surface recombination mechanisms are involved. Bulk recombination is related to the quality of crystalline silicon material while surface recombination is determined by the passivation quality at the interfaces in the device. Any recombination U can be associated with characteristic lifetime.

$$\tau = \frac{\Delta n}{U} \quad (5.4)$$

While $\Delta n = n - n_0$ in the excess of minority carrier density (n_0 is carrier density under thermodynamics equilibrium). In the bulk of crystalline silicon wafers, lifetime is given by the effect of three main recombination processes; those are radiative, Auger and Shockley read Hall recombination:

$$U = U_{Rad} + U_{Aug} + U_{SRH} = \frac{\Delta n}{\tau_{rad}} + \frac{\Delta n}{\tau_{Auger}} + \frac{\Delta n}{\tau_{SRH}} = \frac{\Delta n}{\tau_b} \quad (5.5)$$

In radiative recombination an electron of conduction band neutralized by hole in a valence band emitting a photon with energy which corresponding to semiconductor band gap. Since silicon is indirect band gap material, this process is almost negligible compared to other one. In Auger recombination excess of band to band recombination is given to third carrier, either hole or electron. This mechanism is important at high injection level or in highly doped wafers. While in Shockley read Hall recombination take place through a defect in the band gap and excessive energy is released in the form of phonons. Recombination via defects is not intrinsic to the semiconductor. It can be minimized by perfect crystal growing process. In Photovoltaics low quality crystalline silicon material is used, therefore recombination via defects is dominant process in commercial crystalline silicon solar cells.

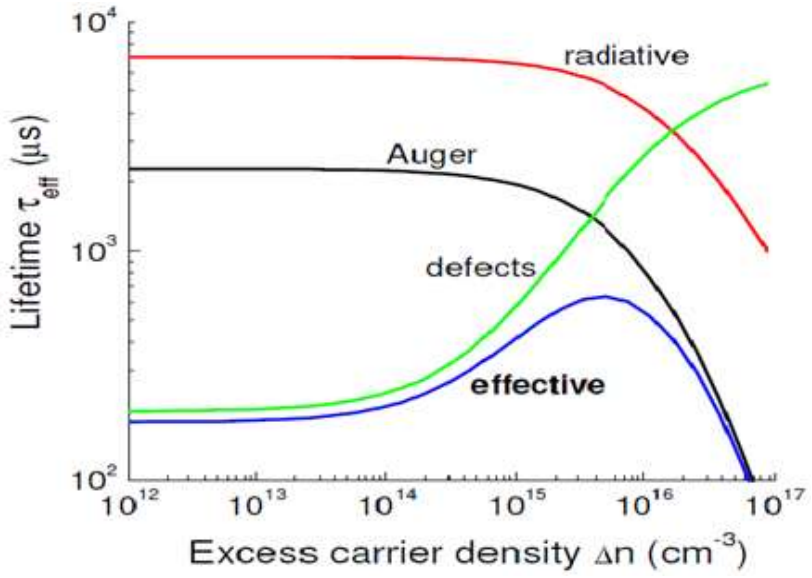


Figure 5.6 Fundamental recombination mechanism in the bulk of a silicon p-type wafer with at 300 K (n_i = 10^{10} cm^{-3}, N_A = 1 ohm.cm, τ_{n0} = 200µs, τ_{p0}= 6 ms).

It is clear that total recombination rate is sum of all recombination rates. In figure 5.6 effective lifetime of bulk, is given by the inverse sum of all lifetime processes. Figure 5.6 shows an example of recombination for p-type wafer with relatively low SRH lifetime.

5.4.2 QSSPC and surface recombination

At the surface of wafer, a high density is expected at the semiconductor surface due to loss of crystalline network. Defect density is mainly due to dangling bonds. In addition to this some defects are also appeared due to fabrication process. Unit of surface recombination is cm^{-2}/sec but it is usually expressed by surface recombination velocity with unit cm/s. The effective surface recombination velocity S_{eff} can as (reference)

$$U_s = S_{eff}.\Delta n \tag{5.6}$$

Δn is the excess minority carrier density at the limit of the space charge region created at the crystalline surface.

5.4.2.1 Measurement setup

The QSSPC technique was design and implemented first time by R.A Sinton and A. Cuevas in 1996 [12-14]. This technique allows the contactless characterization of silicon solar cell precursors. This technique is based on the RF (radio-frequency) bridge with an inductive coil that generates electromagnetic field within the wafer. Variation in conductivity of wafer modifies these fields leading to a variation in effective inductive values, which change the output voltage of the bridge. Block diagram is shown in the figure 5.7. Measuring system consists of a calibrated solar cell which is called reference solar cell along with silicon wafer (to be measured). This calibrated solar cell is used to measure light intensity, a digital oscilloscope (Tektronix TDS 220) and a flash lamp (quantum Q-flash Model X2) with filters. Two magnitudes are measured by this system.

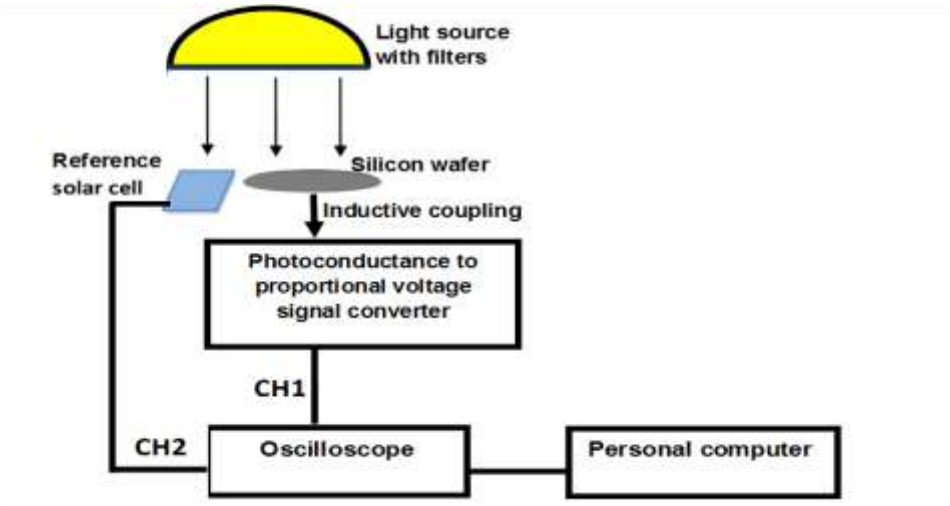


Figure 5.7 Block diagram for effective lifetime measurement (QSSPC)

Photo-conductance of sample $\Delta\sigma$ is a voltage signal proportional to the magnitude which is measured at CH1 in the oscilloscope. From photoconductance, Δn_{avg} can be estimated by using following equation 5.7:

$$\Delta\sigma = w.q(\mu_n + \mu_p)\Delta n_{avg} \tag{5.7}$$

Where *w* is the thickness of wafer, q is the elementary charge $\mu_n \; and \; \mu_p$ is mobility of electrons and hole. This magnitude is measured in Siemens (S), it is unit of electrical conductance (reciprocal of resistance).

The intensity of light which is voltage signal proportional to the short circuit current of the calibrated solar cell placed next to the crystalline silicon wafer measured at CH2. From this magnitude, electron hole pair generated (photo-generation) within the wafer $G_{ext}(t)$ can be estimated. For accurate estimation it is necessary to consider the effect of optical transmission factor. ($\mathbf{f_{opt}}$) which consider the losses due to reflection.

. When these magnitudes are known, the effective lifetime (τ_{eff}) can be calculated with following equation.

$$\tau_{eff} = \frac{w\Delta n_{av}(t)}{G_{ext}(t)} \tag{5.8}$$

In case of symmetric structure, both surfaces are similar (both sides have same structure), we can calculate effective surface recombination velocity S_{eff} applying following equation:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{w} \quad \rightarrow\rightarrow\rightarrow\rightarrow \quad S_{eff} \leq \frac{w}{2\tau_{eff}} \tag{5.9}$$

While τ_{bulk} is recombination lifetime of the bulk.

A typical τ_{eff} vs Δn_{av} curve measured by QSSPC is shown in figure.5.9 One advantage of this technique as compare to other techniques is the wide irradiance range from

($10^{13} to\ 10^{17}\ cm^{-3}$) that can be characterized only by changing the filter in the flash lamp. If high quality crystalline silicon substrate (FZ wafers) is used, the effective lifetime is actually limited by surface recombination ($\tau_{bulk} \gg \tau_{eff}$). In this case usually we obtain a good approximation of effective surface recombination velocity.

Furthermore this technique allows us to estimate the implicit open circuit voltage (implicit-*Voc*) of solar cell, typical example of measurement is shown in figure 5.8 [17-19].

$$V_{OC} = \frac{kT}{q} \ln \left[\frac{\Delta n (N_A + \Delta p)}{n_i^2} + 1 \right] \tag{5.10}$$

For high level injection, ($\Delta p = \Delta n$), the excess carrier densities can be considered equal to average excess carrier density measured by QSSPC.

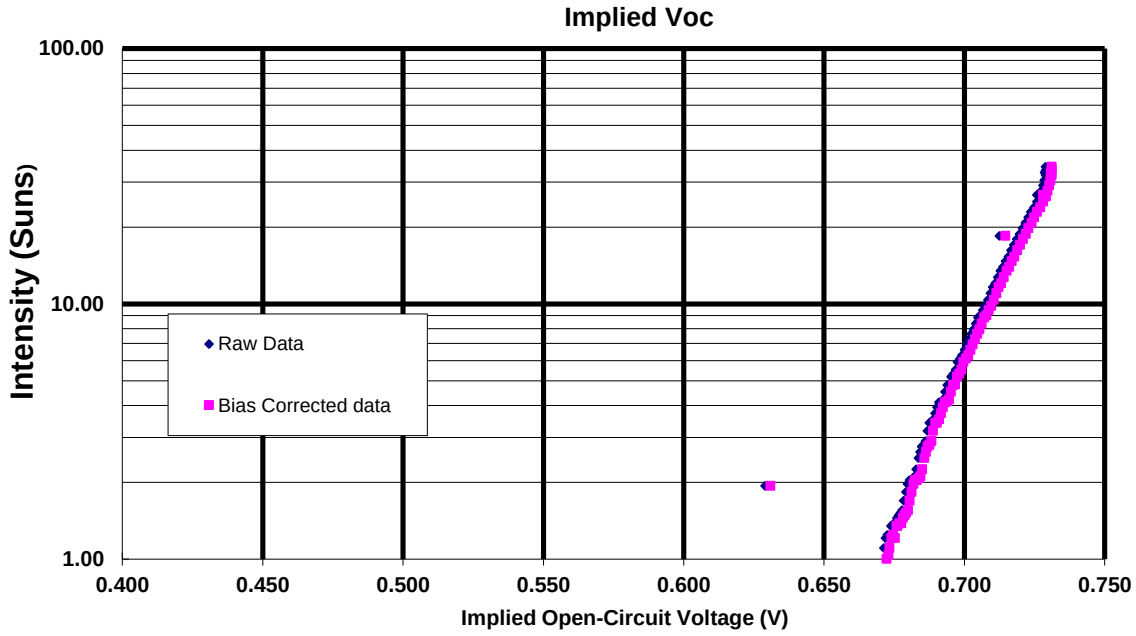


Figure 5.8 Estimation of implicit open circuit voltage (Voc) by QSSPC [17]

The error in the calculation of τ_{eff} can be consider lower than 15% taking into account non linearity between photoconductance and output signal by this technique due to maladjustment of optical factor (f_{opt}) or variation in flash spectrum.

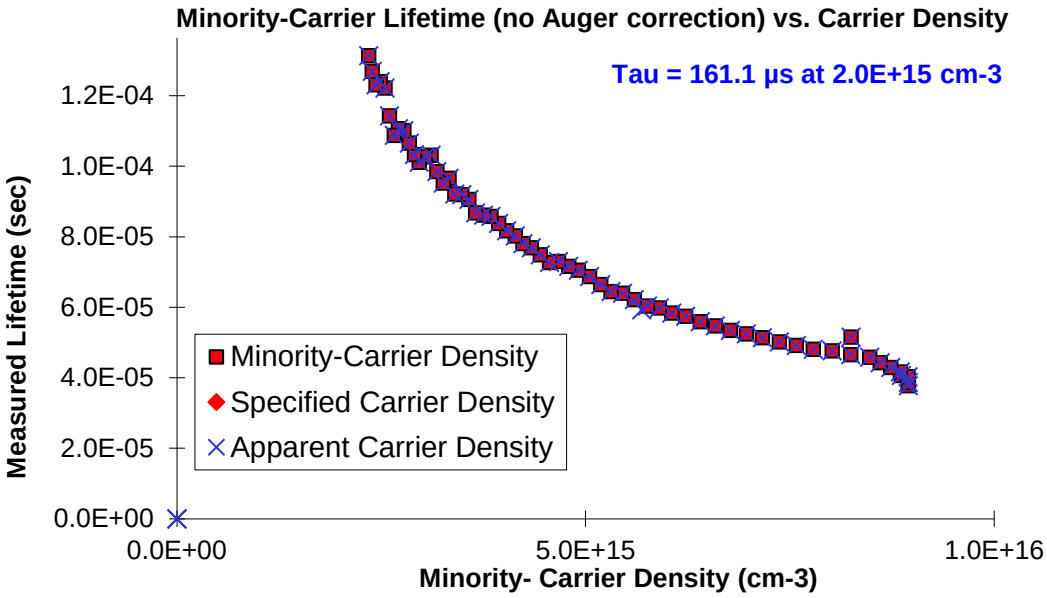


Figure 5.9 Minority carrier lifetime verses average excessive carrier density.

5.4.3 Transient photo conductance

In Transient lifetime measurements, lifetime depends on the decay of carriers over time, Carriers are generated by short pulse of light and decay of carrier's density with time is measured. Longer the minority carrier lifetime slower will be carriers decay. It is an alternative technique to determine excess carriers' lifetime which is based on the analysis of decaying of photo conductance transient after excess carriers have been created by a short light of pulse. [20]. Transient photo conductance is measured by using same hardware setup as for QSS-PC measurement technique. For transient photo conductance (TR-PC) measurement the excess photo conductance is measured by using an inductively coupled coil with a radio frequency (RT) circuit.

5.4.3.1 Measurement setup

For measuring the effective excess carrier lifetime, same hardware and setup is used as in QSSPC technique, although additional monitor cell can be omitted for the case of a transient photo conductance (TRPC) measurement. The main difference is the flash duration, flash duration is changed to a very short time constants, and it is presented in figure 5.10 where measurement signals for a typical TRPC measurement is shown. Due to fact that sample has to be in pure transient mode which means that excess carrier lifetime has to be small as compared to time constant of the flash lamp. Only sample with a high carrier lifetime can be reliable measured with this transient technique.

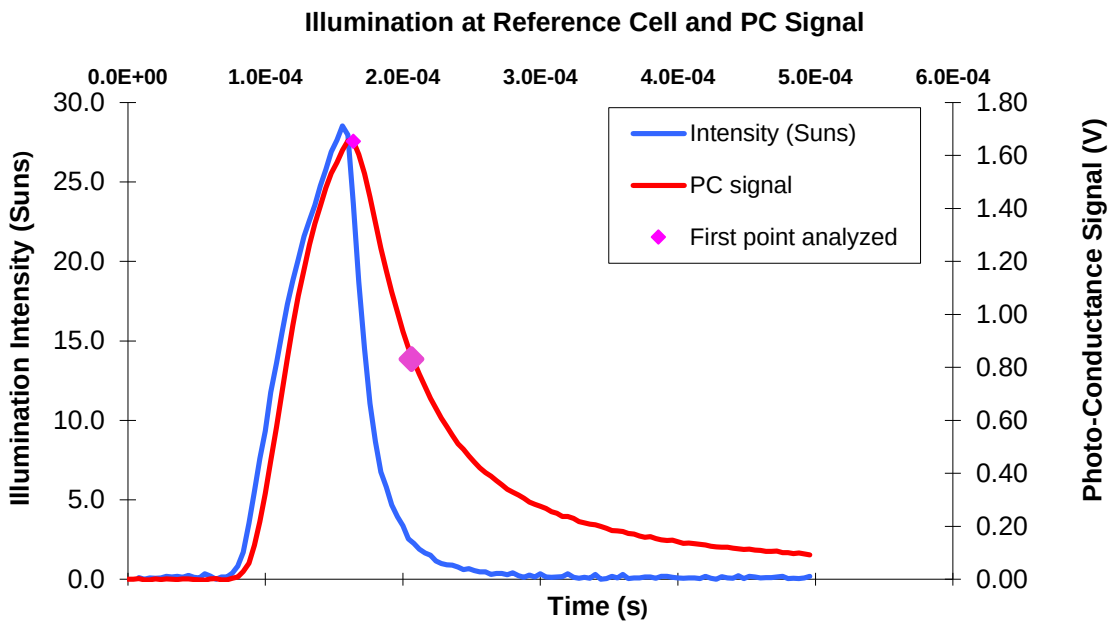


Figure 5.10 Typical measurement signal of a TRPC measurement. The time constant of the short flash pulse (blue) has to be small compared to the effective excess carrier lifetime of the sample in order to get reliable results.

Objective of this work was to improve quality of emitters through passivation. In previous batches we had observed very low lifetime due to bad passivation of emitters. In work, we have focused on passivation via oxidation process as well as with silicon nitride deposition or SiO_2/SiNx stack structure.

5.5 Passivation through oxidation Process

In this batch three different processes were designed with different degree of cleanliness. Additional cleaning was carried out by an ultra-clean process in addition to normal chemical polishing with CPX with RCA 1&2 cleaning process on-type float zone (FZ) wafers of resistivity 16.Ω.cm. For ultra-cleaning process, we have applied an efficient way which consists of phosphorus diffusion into silicon surface layers in which the gettered impurities have been trapped at high temperature. As we have expected, after removing the phosphorus-rich layer, the electrical properties of silicon wafers can be significantly improved. Gettering was performed, which cleaned bulk of silicon wafers by removing contaminations or defects from bulk and surface. After gettering, wafers were etched again with CPX and cleaned with RCA1 & 2 cleaning. We have also used test wafers in order to evaluate of our cleaning and etching process, we used our standard process (TiM process) for etching of wafers with NaOH. This wafer is used to compare the results with clean and ultra-clean process. These three processes only differ in degree of cleanliness prior to entering for oxidation stages for surface passivation. These three processes are given in scheme 1, 2 and 3.

Scheme 1: TiM Recipe used for fabrication of solar cell, (see figure 5.12b)
Scheme 2: Clean process via CPX etching (see figure 5.12a)
Scheme 3: Ultra-clean process through gettering via CPX etching, (see figure 5.11)

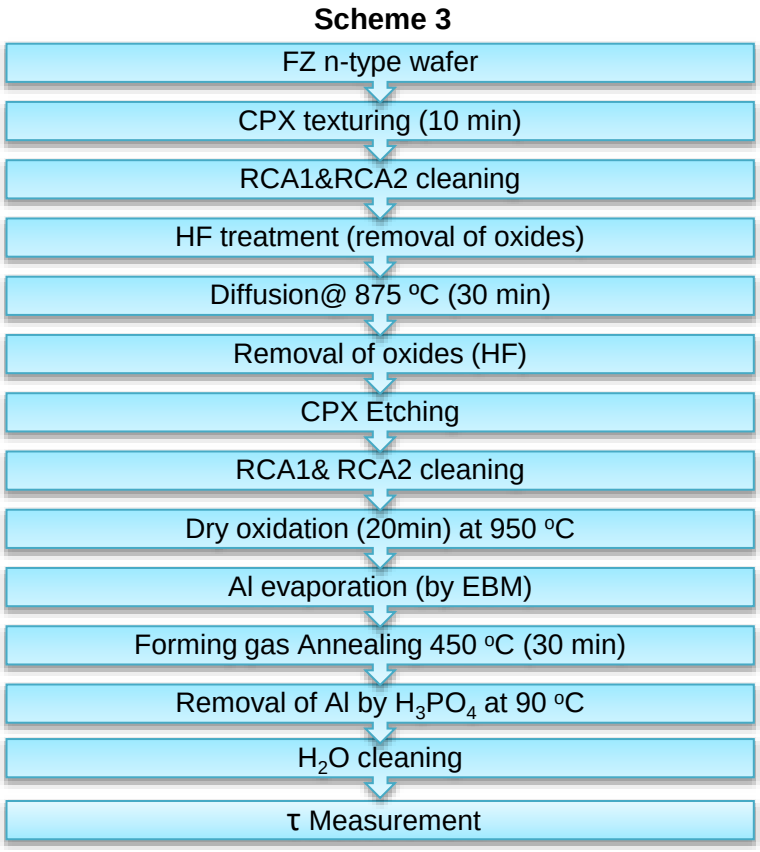
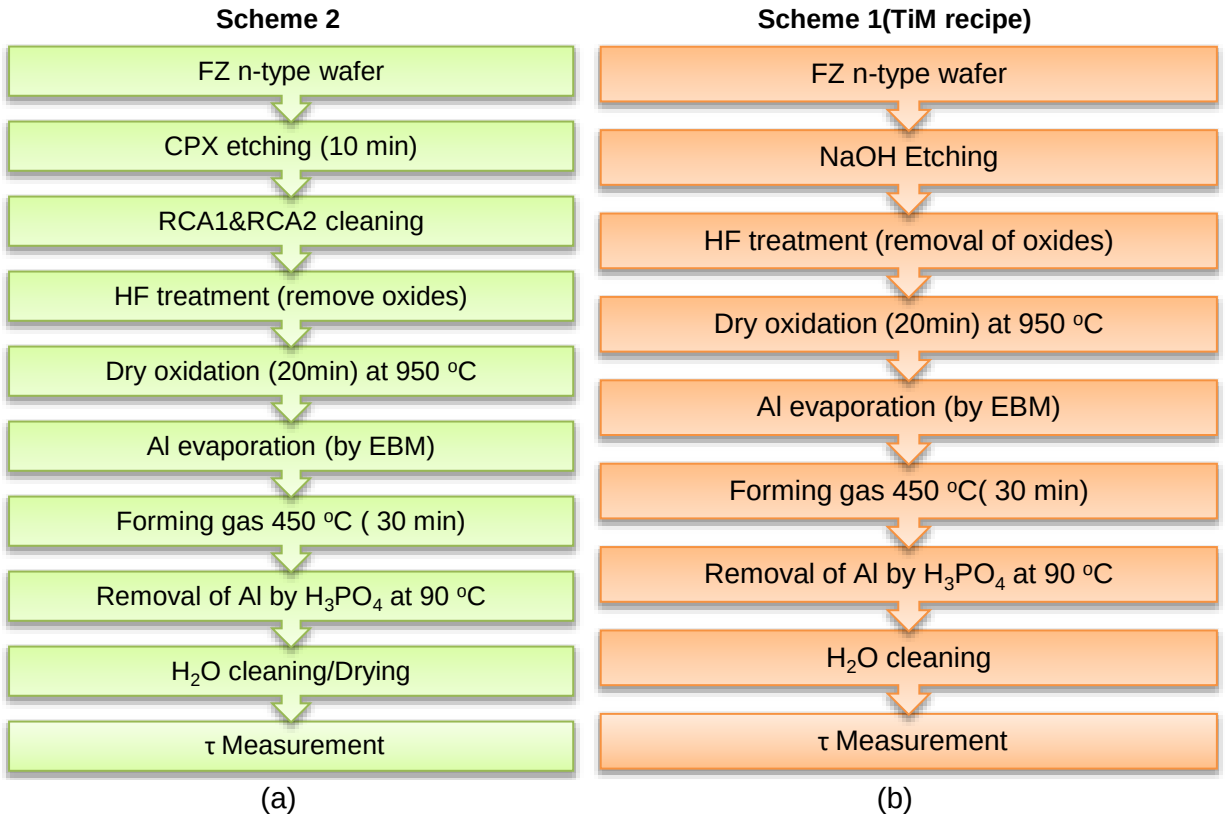


Figure 5.11 Fabrication process for silicon passivation through oxidation (Scheme 3)



(a) (b)

Figure 5.12 Fabrication process for silicon passivation through oxidation (Scheme a & b).

5.5.1 Results and characterization passivated surface

Dry oxidation was carried out under same conditions for all three scheme at 950 ºC for 20 minutes. According to previous experiments, a layer about 15nm of SiO_2 were produced on both side of wafer due dry oxidation. After this a thin layer about 50nm of Al was deposited on both side of wafers by EBM. SiO_2 and aluminum annealing (alnealing) at high temperature is used for surface passivation. Alneal was carried out on both side of oxidized wafers. For this purposed, wafers with caped layer of Al were annealed at 450 ºC for 30 minutes in forming gas. Finally Al layers were etched in H_3PO_4 at 90 ºC. During etching, a large amount of atomic hydrogen is generated due to reaction of Al with phosphoric acid. Atomic hydrogen which is generated within oxide layer passivate the dangling bonds at Si/SiO_2 interface. It is also found that Alnealing do not have effects on SiNx passivated surface [4, 21-23]. After cleaning with deionized water, wafers were dried.

After processing, these wafers were evaluated through lifetime measurements by PCD and QSSPC techniques. The results of lifetime measurements these 3 different processing schemes are given in figure 5.13. From these results it is clear that our recipe (TiM recipe) is destroying lifetimes of minority's carriers. In our opinion NaOH destroyed the lifetime by introducing impurities, possibly due to metallic etching bath. From ultra-clean process (scheme 3), It is clear lifetime is improved of ultra-clean process through gettering via P diffusion. We have performed same experiments which have applied for ultra-clean scheme excepting chemical etching process. CPX etching has given good result of passivation (lifetime measurement) but NaOH etching destroyed the lifetime of wafers.

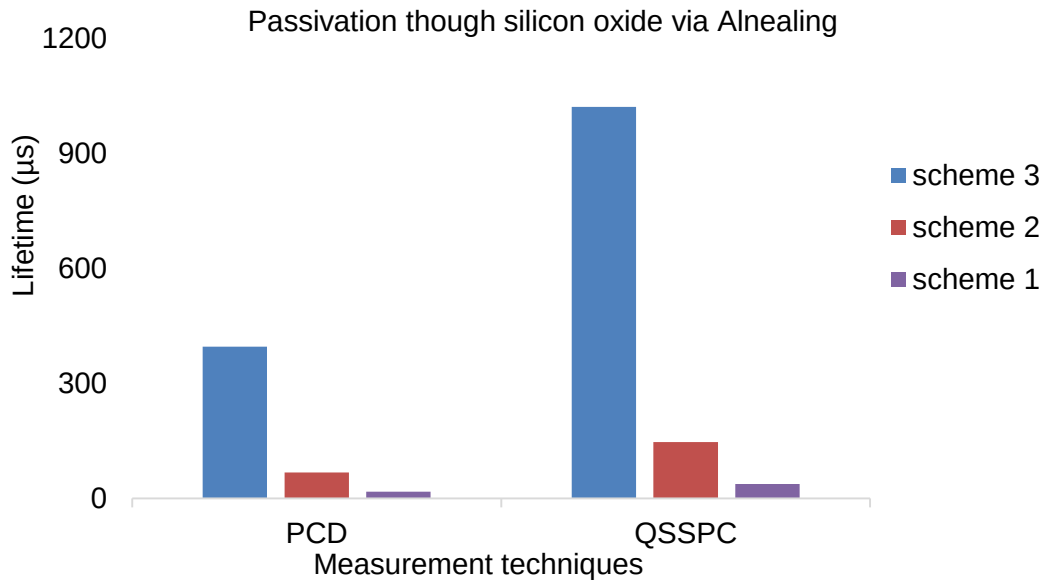


Figure 5.13 Lifetime measurement of different schemes (clean and ultra-clean process)

Although this process has given good results to improve passivation quality of silicon wafers and to decrease the surface recombination velocity but it is not compatible with industrial solar cell fabrication. Due to this reasons, we have concentrated to improve the passivation by using SiNx layer, by applying new recipes.

5.6 Passivation with stoichiometric SiNx Deposition (N-type wafer)

5.6.1 Objective:

In silicon solar cell fabrication different material has been used for antireflection coating as well as for passivation. Recently SiNx has found excellent material due to its dual properties of passivation as well ARC for high efficiency solar cells. On typical solar cell a layer of silicon nitride is deposited by PECVD and it also produces a positive charges at the interface of SiNx/Si, which helps the surface passivation.

Optical properties of Silicon nitride layer can be adjusted by controlling the composition of silicon nitride film. High concentration of silicon, non-stoichiometric film has high refractive index (>2.4) which has high absorption loss and low refractive index (<1.9) has low absorption loss. Typically on textured silicon wafer, a 75nm thick layer of SiNx is deposited for good results. An important issues for used of silicon nitride (SiNx) is its ability to passivate the impurities which kill the lifetime of minorities carriers, are present in silicon surface, It introduces H into surface layer and remove the damages.

The objective of this work is to find a good point (optimum point) for passivation by using silicon nitride as passivating layer on n-type Cz wafers of different thickness (Recipe for passivation). In order to find an optimal point for passivation, we have changed stoichiometry of silicon nitride. When we have optimized point, we have applied on selective emitter's passivation both n-type and p-type wafers. When the first objective is achieved, when optimal point for passivation by SiNx is found, we have applied these recipes for emitter's passivation.

There are number of ways, by which recombination process occurs in silicon solar cells and other semiconductors devices. These processes are intrinsic and extrinsic in nature. Intrinsic processes are unavoidable properties of material including radiative and Auger recombination. While extrinsic processes related to the defects of a materials like impurities and crystallographic defects within the material or at the surface of material including SRH bulk and surface recombination. All defects and extrinsic recombination processes can be reduced to minimum level. High recombination rates in silicon material decrease the lifetime of minority carriers. Extent of lifetime which can be achieved depends on quality of wafers and subsequent processing. Efficiency of silicon solar cells is limited by recombination lifetime of minority carriers. During fabrication process, devices undergo thermal step and minority carriers achieve high lifetime, thermal degradation and possible contamination must be avoid for high efficiency process. The objective of this work is get optimal point for passivation by using following recipe of SiNx by changing the gaseous flow in as given in table 5.1 (Recipe SiNx).

5.6.2 Experimental procedure:

Process is started from chemical etching process by using CPX mixture (acidic etching). N-type monocrystalline Cz-silicon wafers (ρ=0.8 Ω·cm; thickness = 200μm) have been taken for etching process. Wafers and etching mixture were taken in a Teflon tray and etching was carried out by shaking manually as shown in figure 5.15. Etching time varies from 10 to 20 minutes, in order to get to different wafers thicknesses. Thin wafers are in range of 135- 150μm and thick wafers are in range of 150-170 μm. After etching, RCA1&2 cleaning were performed to remove the all kind of impurities (inorganic and organics) and

treated with hydrofluoric acid before SiNx deposition. Description of process is given in figure 5.14.

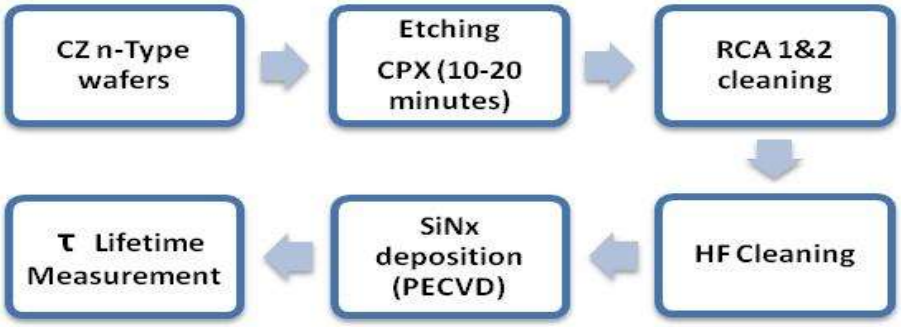


Figure 5.14Schematic representation of process to get optimum point for passivation.

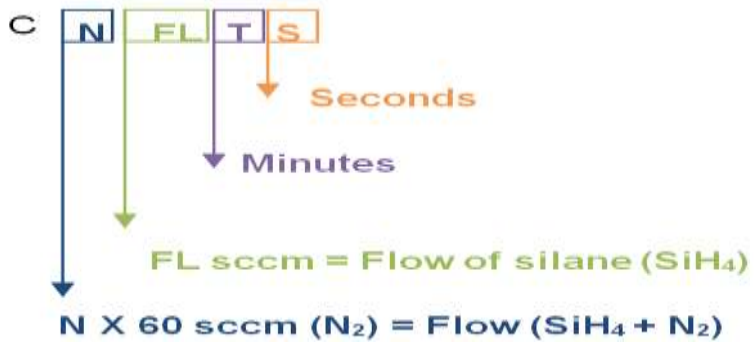
Figure 5.15 CPX manually etching process for silicon wafer.

5.6.3 Recipe of silicon nitride (SiNx) deposition

Table 5.1 Recipe of SiNx deposition

	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Ar (sccm)	Time	Temp. (^0C)	MW	Rf	Pressure
Start (Heat)					30 min	400			0.2 mb
Stabilization		60		40	90sec	400			0.2 mb
Pre Plasma		60		40	30 sec	400		300W 150V	0.2 mb
Cleaning				100	10 sec	400			0.2 mb
stabilization SiNx	5	60	55	40	30 sec	400			0.2 mb
Plasma	5	60	55		4 min	400	MW 2200	300W, 150V	0.2 mb

*Yellow color parameters are variables (we have to change these variables to get good passivation). SiH_4 and N_2 flow during stabilization of SiNx and SiH_4 with N_2 change with time during plasma deposition.



Experiments which we have performed to deposit SiNx by using above mentioned parameters (concentration) and their flow is given in table 5.2 under different temperature ranging from 300-400 ºC. We must keep in mind that we are looking for passivation with silicon nitride, at this moment, variation in thickness of SiNx layer is not important but we will try to have more or less in range of 80-90nm by changing the time of plasma deposition to get Blue color of SiNx layer. In this work, we have used CZ n-type with low resistivity wafers and SiNx deposition experiments were conducted in following orders as gaseous flow (concentration) is given in the table 5.2.

Table 2.2 Scheme for concentration of gaseous flow for SiNx deposition

N	FL	3	4.5	6	9	10	11	12
3		C3 3	C3 4.5	C3 6	C3 9	C 10	C311	C3 12
3.5		C3.5 3	C3.5 4.5	C3.5 6	C3.5 9	C3.5 10	C3.5 11	C3.5 12
4		C4 3	C4 4.5	C4 6	C4 9	C410	C4 11	C4 12
4.5		C4.5 3	C4.5 4.5	C4.5 9	C4.5 9	C4.5 10	C4.5 11	C4.5 12
4.9		C4.9 3	C4.9 4.5	C4.9 9	C4.9 9	C4.9 10	C4.9 11	C4.9 12

There are some values which are not possible due to minimum flow limit of SiNx deposition machine. E.g. FL (flow of silane) 3 is not possible to process due to low limit of silane flow. Total flow rate is given $\mathrm{C} = (\mathrm{N} \times 60) - \mathrm{FL}$. Ratio of nitrogen/silane is given in table 5.3.

Table 5.3 Nitrogen/silane ratio for SiNx deposition scheme

N	FL	3	4.5	6	9	10	11	12
3		59	39	29	19	17	15.3	14
3.5		69	45.6	34	22.3	20	18.1	16.5
4		79	52.3	39	25.6	23	20.8	19
4.5		89	59	44	29	26	23.5	21.5
4.9		97	64.3	48	31.6	28.4	25.7	23.5
5		99	65.6	49	32.3	29	26.2	24

As it is mention early, objective of this process is find an optimum point for passivation by SiNx deposition on CZ wafers. After achieving optimal point, we have applied these optimal points for emitter's passivation which we have planned for emitter passivation. Structure of n-type Cz wafer is shown in figure 5.16 after deposition of SiNx on both side of wafer.

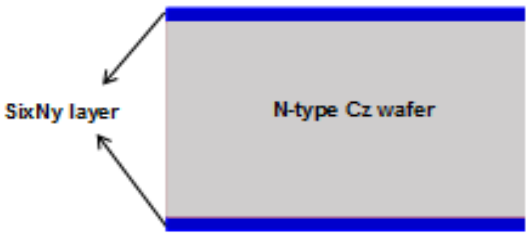


Figure 5.16 Structure of silicon wafers after silicon nitride deposition

Lifetime of SiNx layer deposited under different gaseous flow and variable time are given in figure 5.17. . In figure 5.17 graph, for plots we have used lifetime values which we have obtained by TPCD technique.

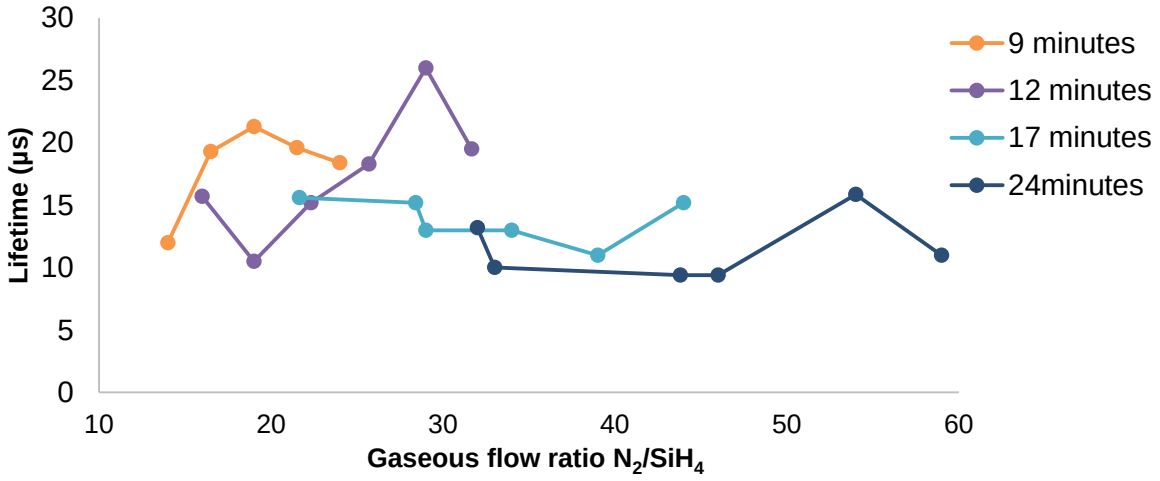


Figure 5.17 Lifetime measurements of different layer of SiNx deposited under different gaseous flow and variable time

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{w} \qquad (5.11)$$

Values of surface recombination velocities, which are calculated from lifetime measurements (TPCD) are given in the table 5.4.

Table 5.4 Comparison of Surface recombination velocities obtained after deposition SiNx by different ratio N_2/SiH_4

FL / N	4	6	7.5	9	10	12
3	900 1060	685 740		860 904		820 860
3.5		830 940		445 470		470 512
4	745 860	743 793		436 440		363 403
4.5		570 700		**310** **350**		400 430
4.9		636 840	568 607	**369** **419**	**390** **407**	465 549

We have used the optimal points, those have given the low values of surface recombination velocity or high lifetime of minority's carriers are applied to deposit the same recipes at low temperature. Lifetime measurements as well as surface recombination velocities of different Nitrogen/silane flow under different temperatures are given in figure 5.18 and 5.19.

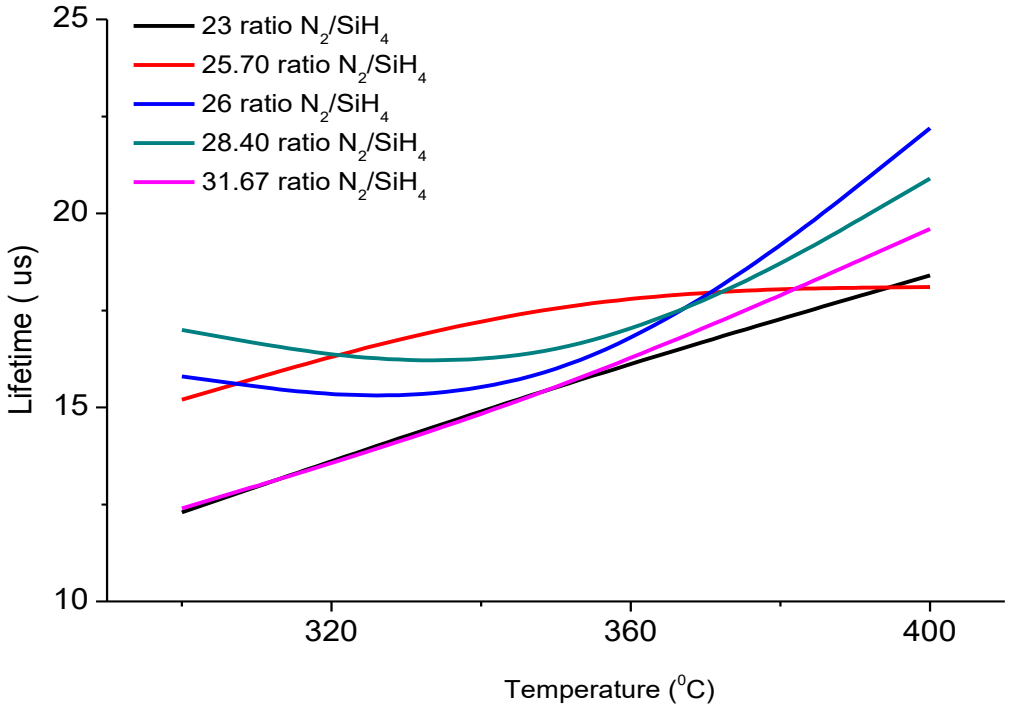


Figure 5.18 Lifetime measurements under different gaseous flow of N_2/SiH_4 at different temperature during SiNx layer deposition.

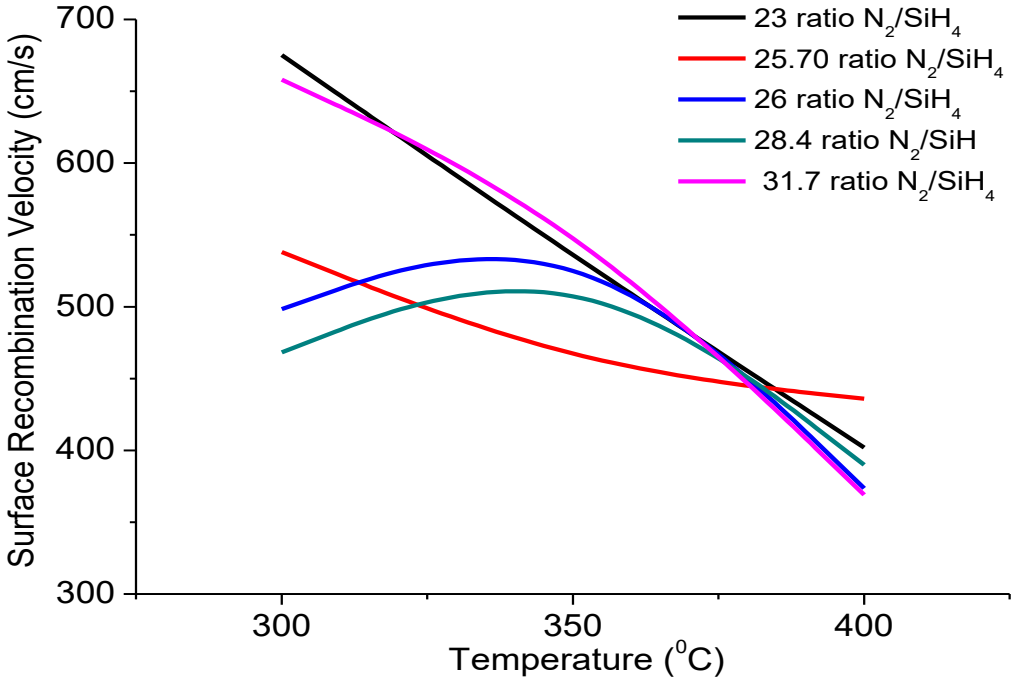


Figure 5.19 Surface recombination velocity calculations under different gaseous flow of N_2/SiH_4 at different temperature during SiNx layer deposition.

5.7 Passivation of emitters (N-type wafers)

Systemic fabrication process for passivation of emitters is shown in flow sheet diagram in figure 5.20(a). Process is started from chemical etching of wafers. N-type monocrystalline Cz-Silicon wafers (ρ = 0.8 Ω·cm; thickness = 150μm) with size 10x10 cm^2 has been taken for etching process, which was carried out by CPX solution, an etching solution used to etch silicon in acidic medium. RCA1&2 cleaning was performed to remove the all kind of impurities (inorganic and organics) and treated with hydrofluoric acid prior the wafer processing. "P" pre-deposition is carried out at 820 ^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under standard conditions. A dry oxidation was performed for 30 minutes with drive-in process. Drive in process was carried in oxidation furnace at 950^{0}C for 1 hour in nitrogen ambient. In addition to this experiment, a control experiments was performed in order to know the quality of passivation on silicon surface (without emitters). For this purpose, P diffusion was carried out at 820 ^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under standard conditions to perform gettering. Gettering process is used to remove impurities from bulk as well as from surface. After gettering, wafers were etched again with CPX to remove emitters as well as dead layer. Systematic fabrication process for emitter passivation is shown in figure 5.20(a). In figure 5.20(b), during CPX etching, wafers were divided into two thicknesses, half wafers were etched just for 5 minutes and half were etched for 10 minutes in order to get two thickness.

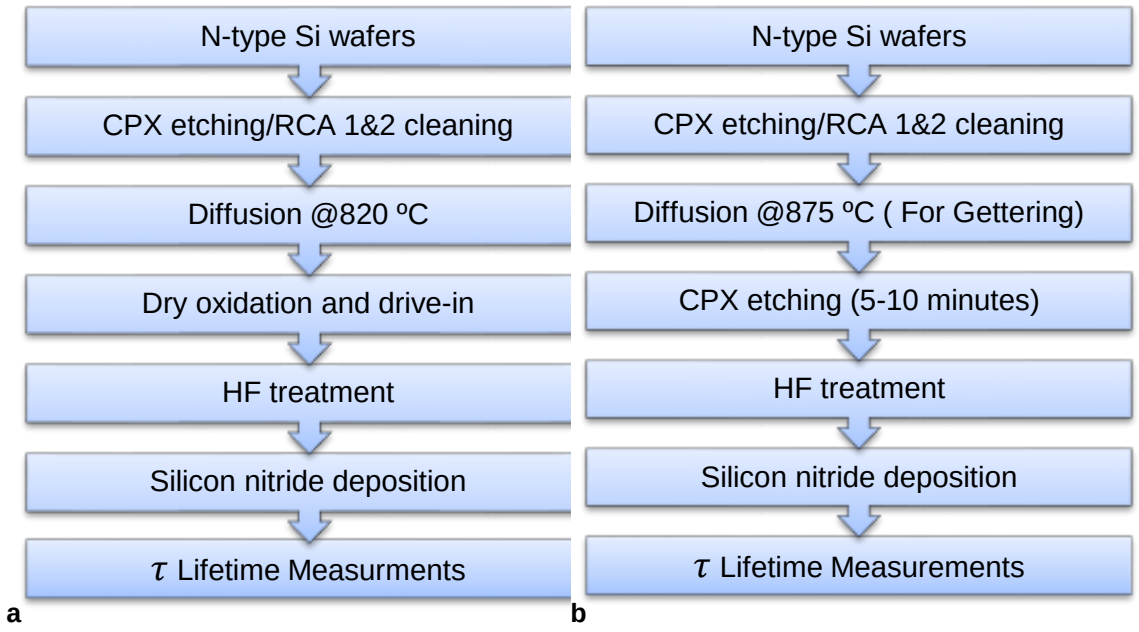
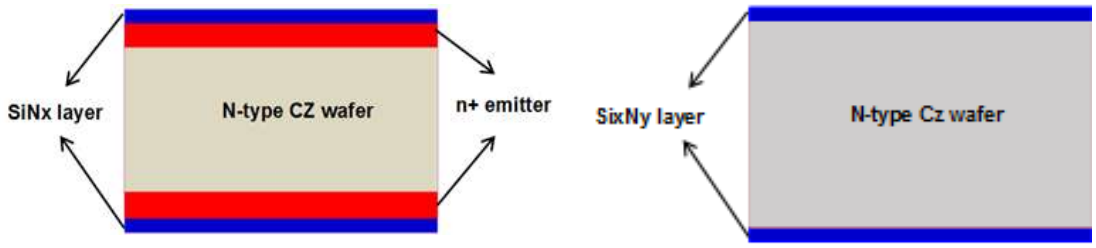


Figure 5.20 Fabrication process for passivation of emitters on n-type substrate (a), fabrication process for control experiment (b)

Both wafers were cleaned with HF in order to remove oxide layer, prior to SiN_X deposition. A layer of silicon nitride is deposited on both sides of wafer by plasma enhanced chemical vapor deposition (PECVD). We have used nitrogen/silane ratio, which has given the best results in SiNx optimization point for passivation. Structures of silicon wafers after processing are shown in figure 5.21.



a b

Figure 5.21 (a) Structure of of n-type wafer used for emitter passivation, (b) test wafer after SiNx deposition

After silicon nitride deposition (SiNx), lifetime of each wafers were measured at room temperature (17-20 ºC) for minority carrier's injection level in range of 10E13-E17/cm^3. Both quasi steady state (QSSPC) and transient photo conductance (TPCD) techniques were used to measure the lifetime of wafers. Lifetime measurement results are given in graph of figure 5.22 at different N_2/SiH_4 ratio which has given the best result for passivation. In figure 5.22, we have used lifetime values which we have obtained by TPCD technique for plots.

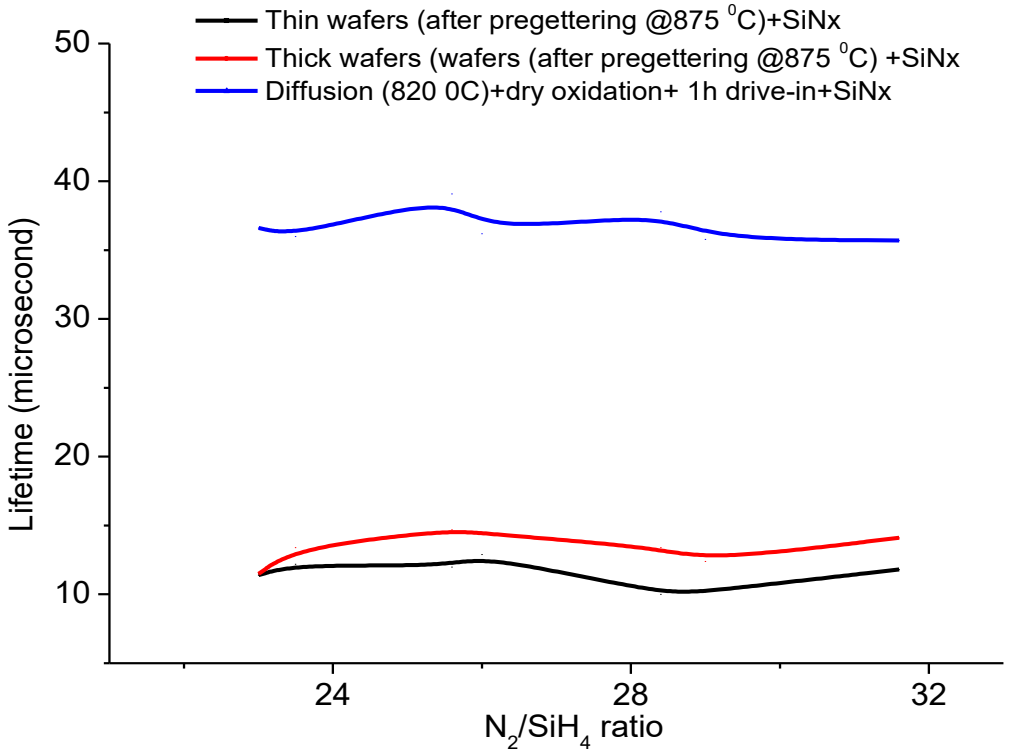


Figure 5.22 Effect of gaseous flow on lifetime of emitters and etched silicon wafers after SiNx deposition

A graph between SRV values and gaseous flow is given in figure 5.23, which is used to passivate emitters as well as ultra-clean silicon.

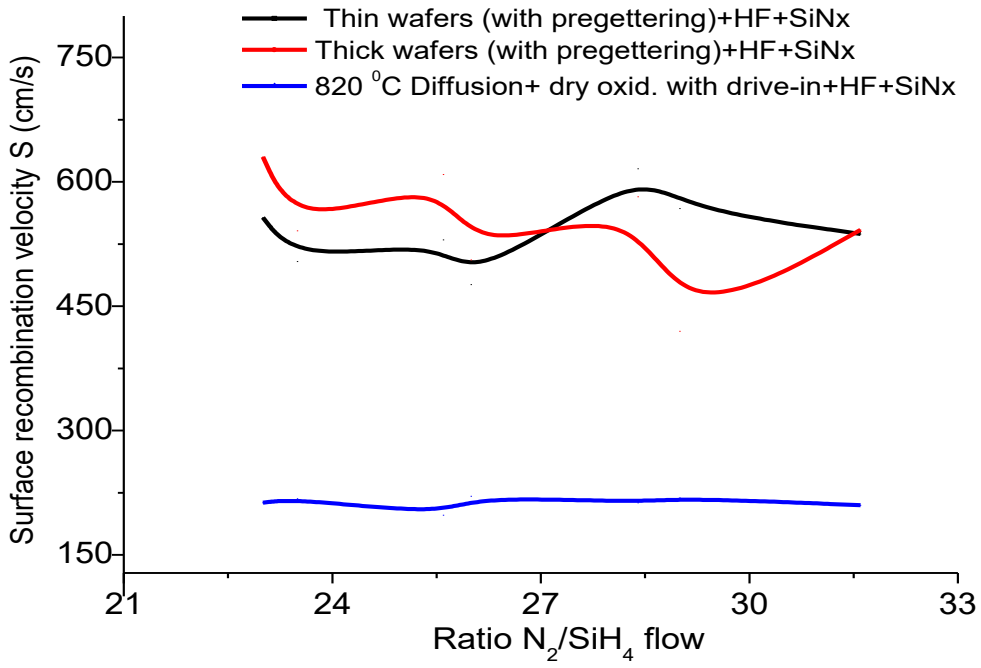


Figure 5.23 Effect of gaseous flow on surface recombination velocity of emitters and CPX etched emitters and silicon wafers after SiNx deposition.

From these results, we concluded that there is not much difference in lifetime or SRV values after changing the gaseous flow of N_2/SiH_4 in above experiments. We have chosen above gaseous flow on the basis of our experimental data on passivation of N- type wafers, after depositing a SiNx layer by changing gaseous flow. These values of gaseous flow were selected after series of experiments which we have conducted on n-type wafers in order to find optimal flow of gases for passivation (to get high lifetime).

5.7.1 Passivation of softly doped and high doped emitters (N-type substrate)

Systemic fabrication process of softly doped and highly dope emitters and their passivation scheme is shown in flow sheet diagram in figure 5.24. Process is started from chemical etching process of wafers. N-type monocrystalline Cz-Silicon wafers (ρ = 0.8 Ω·cm; thickness = 150µm) with size 10x10 cm^2 have been taken for etching process, which was carried out by CPX solution, an etching solution used to etch silicon wafers in acidic medium. RCA1&2 cleaning was carried out to remove the all kind of impurities (inorganic and organics) and cleaned with hydrofluoric acid (HF) prior to P diffusion. “P” pre-deposition is carried out at 820 ^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under standard conditions. A dry oxidation was performed for 30 minutes prior to drive-in process. Drive-in process was carried in oxidation furnace at 950^{0}C for 1 hour in nitrogen ambient. Wafers obtained after this process, have sheet resistance around 30-40 Ω/sq. Same process is repeated with high temperature P pre-deposition at 875 ºC for 30 minutes in order to get highly doped emitters. After P pre-deposition some wafers cleaned with HF in order to remove oxide layer prior to SiNx deposition as shown in figure 5.24(a). Rest of wafers were further processed. A dry oxidation was performed for 30 minutes prior to drive-in process except process which is shown in figure 5.24(b). Drive-in process was carried in oxidation furnace at 950^{0}C for 1 hour in nitrogen ambient. Wafers obtained after this process, have sheet resistance around 14-19 Ω/sq.

After dry oxidation with drive-in process, a layer of silicon nitride is deposited on both sides of wafer by plasma enhanced chemical vapor deposition (PECVD). We have used nitrogen/silane ratio, which has given the best results in SiNx optimization point for passivation Fabrication process which is shown in figure 5.24 (c) for lowly doped emitter's passivation is similar as it already mentioned in figure 5.21(a) but this process is HF free. Process which is shown in figure 5.24 (d), we have tried to convert high doped emitters into lowly doped emitters prior to passivation by chemical etching. During chemical etching, up to 50-100nm thick surface layer is removed in order to decrease the doping concentration. Wafers were cleaned with RCA1&2 and HF in order to remove oxide layer, prior to SiN_X deposition. A layer of silicon nitride is deposited on both sides of wafer by plasma enhanced chemical vapor deposition (PECVD).

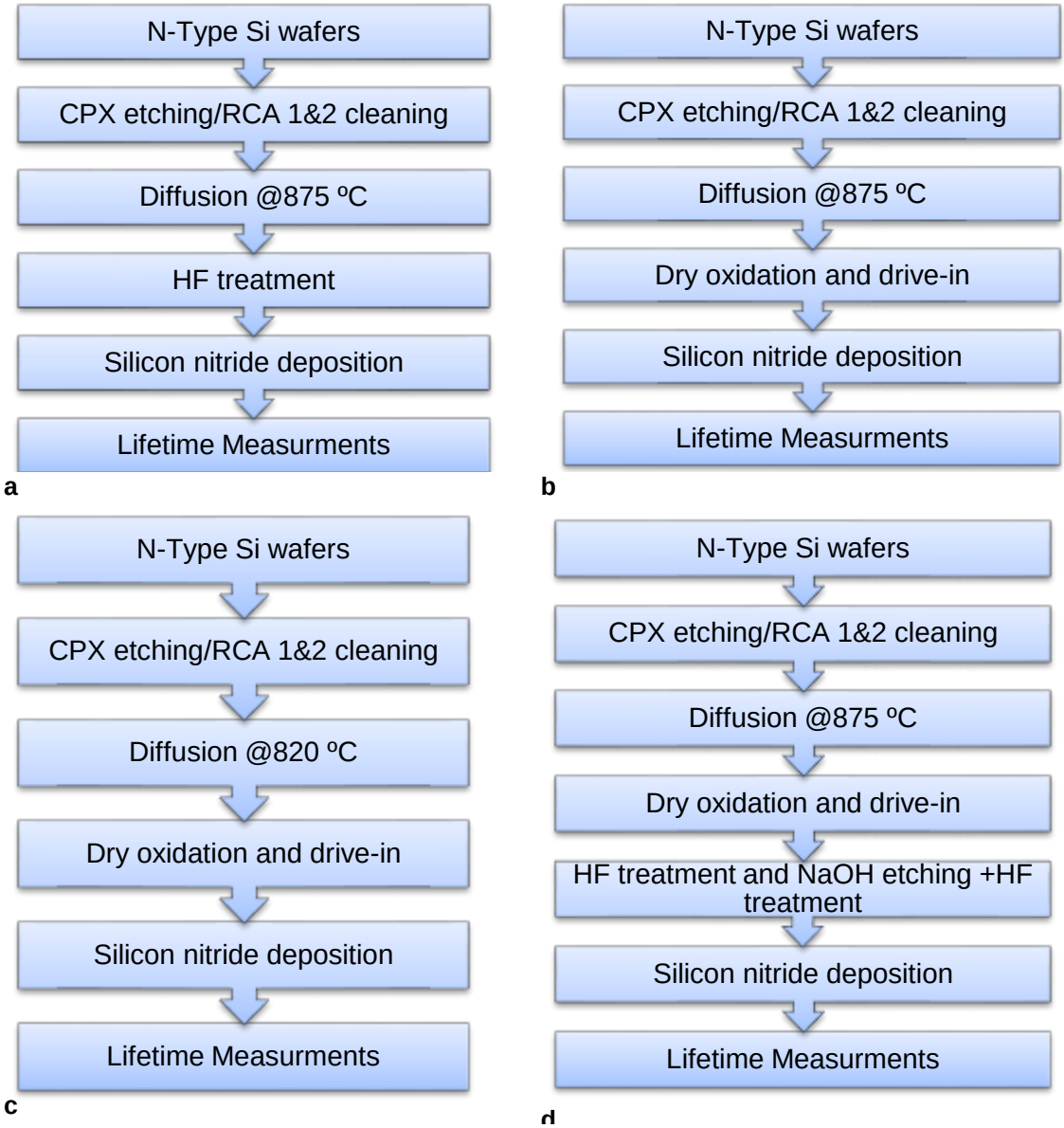


Figure 5.24 (a), Fabrication process for passivation of highly doped emitters on n-type substrate, (b) Fabrication process for passivation of highly doped emitters with drive-in on n-type substrate, (c) Fabrication process for passivation of lowly doped emitters on n-type substrate, HF free process (d) Fabrication process for passivation of highly doped emitters to lowly doped emitter on n-type substrate via NaOH etching.

After Silicon nitride deposition (SiNx), lifetime of each wafers were measured at room temperature (17-20ºC) for minority carriers injection level in range of 10E13-E17/cm^3. Both quasi steady state (QSSPC) and transient photo conductance (TPCD) techniques were used. Lifetime was measured after diffusion, after dry oxidation with drive-in and after SiNx deposition. Lifetime measurement results are given in graph in figure 5.25 and graph of SRV values is given in figure 5.25 for fabrication process of figure 5.24 (c).

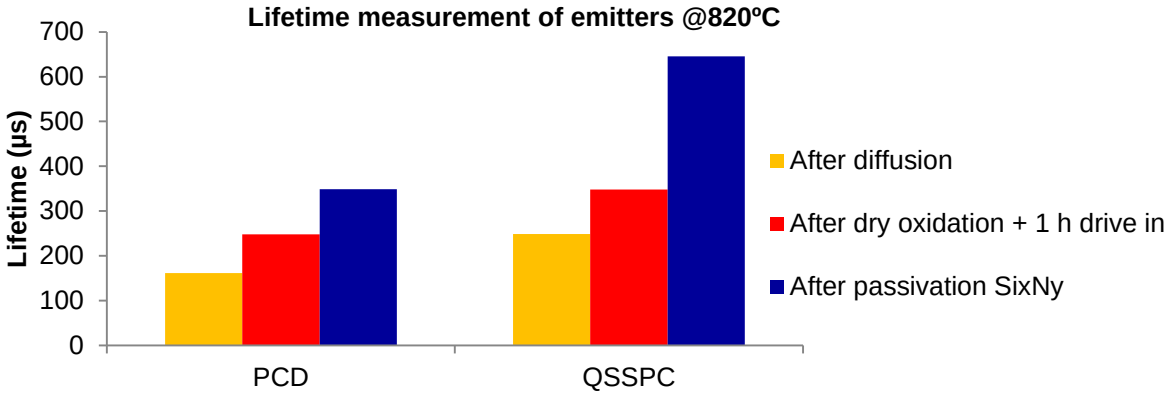


Figure 5.25 Lifetime measurement of fabrication process used for passivation of softly doped emitters on n-type substrate and HF free process

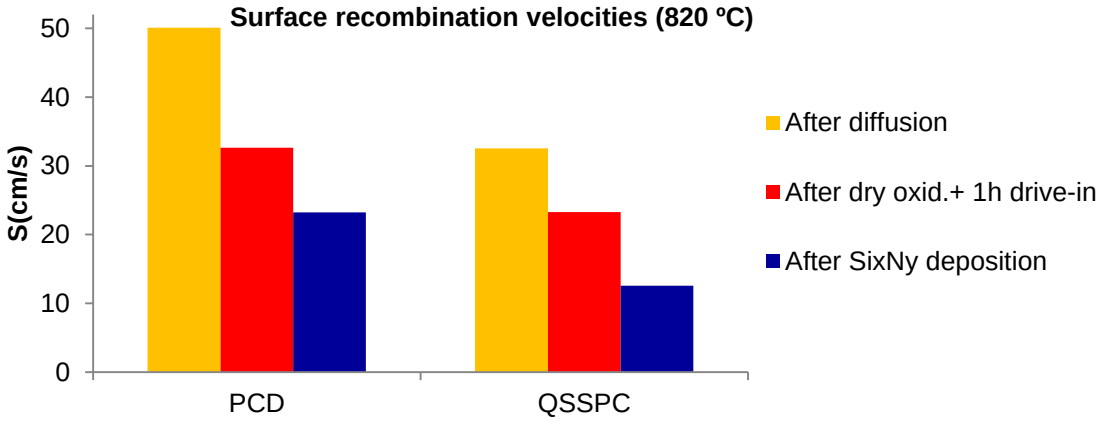


Figure 5.26 Surface recombination velocity of fabrication process used for passivation of softly doped emitters on n-type substrate and HF free process

Lifetime measurement results are given in graph of figure 5.27 and SRV values are given in graph figure 5.28 for fabrication process of figure 5.24(b). In both cases, 820 ºC P diffusion and 875 ºC P diffusion, passivation of wafers improved by dry oxidation. Passivation quality of surface of emitters is improved due to silicon oxide. Improvement of lifetime values due to dry oxidation is shown in figure 5.27 and SRV is given in figure 5.28 for 875 ºC P diffusion. These results show the compatibility of our recipe with oxide layer for high efficiency process. After Silicon nitride deposition (SiNx), lifetime of each wafers were measured at room temperature (17-20ºC) for minority carriers injection level in range of 10E13-E17/cm^3. Both quasi steady state (QSSPC) and transient photo conductance (TPCD) techniques were used. Lifetimes were measured after diffusion, after dry oxidation with drive-in and after SiNx deposition. Deposition of SiNx layer further improved the lifetime. It is clear that SiO_2/SiNx stack structure further improve the lifetime values of wafers.

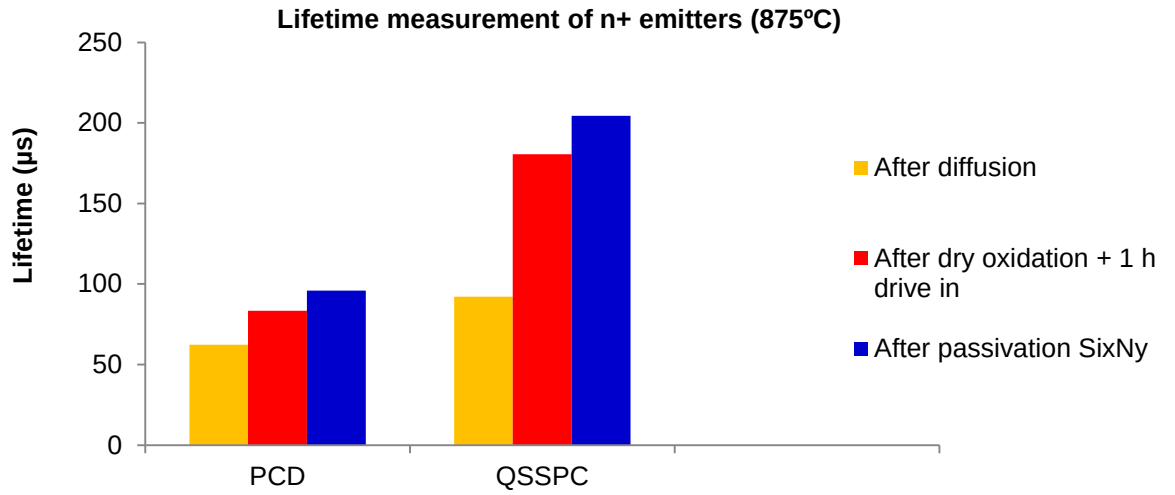


Figure 5.27 Lifetime measurement of fabrication process used for passivation of high doped emitters on n-type substrate and HF free process

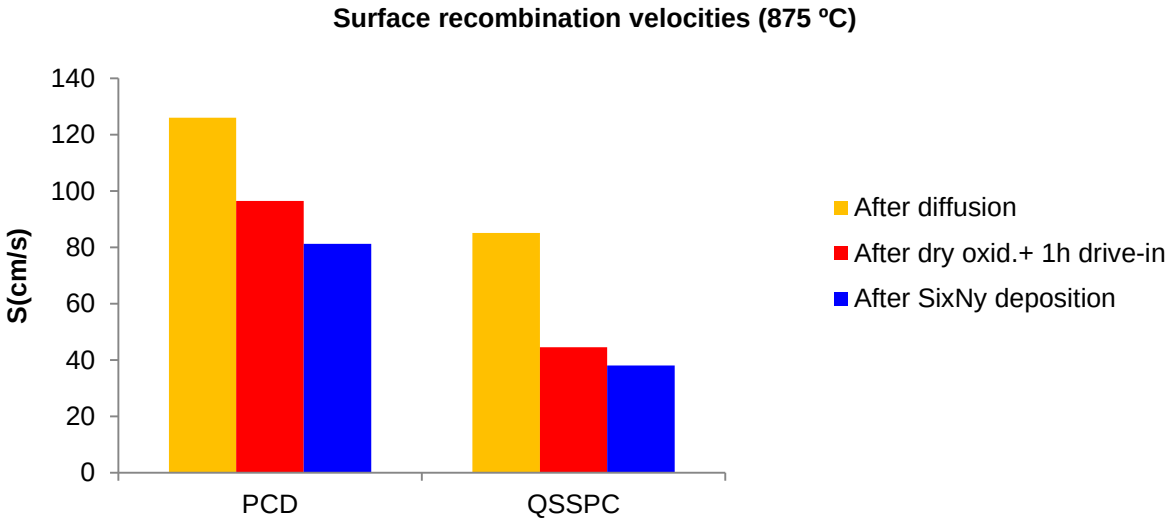


Figure 5.28 Surface recombination velocity of fabrication process used for passivation of softly doped emitters on n-type substrate and HF free process

For process 5.24(a), Lifetime was measured after diffusion, after HF treatment and after SiNx deposition. In this process, we have deposited SiNx layer by changing gaseous flow of nitrogen/silane (C4.59, C4.510, C4.910 and C4.99 see table 1 for detail of this chapter), in order to see the effect of nitrogen/silane concentration on lifetime measurement, Results are given in graph in figure 5.29 of fabrication process of figure 5.24(a). Prior to SiNx layer deposition on wafers with n+ emitter were cleaned by HF to remove the oxide layer on emitters. For process 5.24(a), it is also repeated by measuring the lifetime after each step, diffusion, dry oxidation, HF treatment and SiNx layer deposition. Results of lifetime measurements are given in figure 5.30. Flow of silane and nitrogen (in sccm) is given below for deposition of SiNx layer, C4.59 (SiH_4=9, N_2=261) SiNx (a), C4.510 (SiH_4=10, N_2=260) SiNx (b), C4.99 (SiH_4=9, N_2=285) SiNx(c) and C4.910 (SiH_4=9, N_2=285) SiNx (d). See table 5.2 for detail of gaseous flow and temperature.

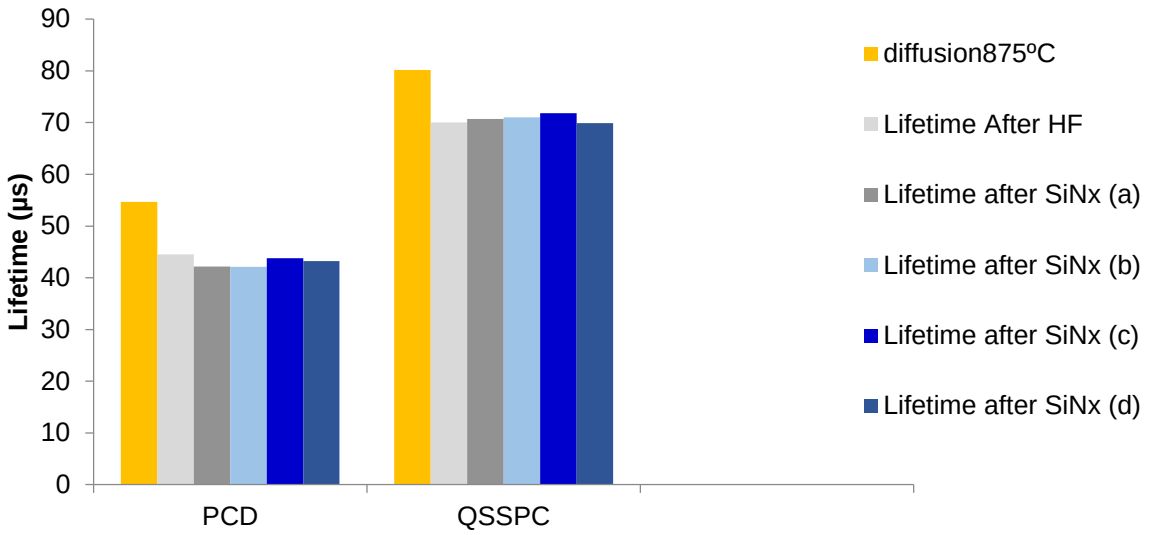


Figure 5.29 Lifetime measurement of fabrication process used for passivation of high doped emitters on n-type substrate, Lifetime is measured after phosphorus diffusion and after HF treatment, after deposition of SiNx by using different flow of N_2/SiH_4.

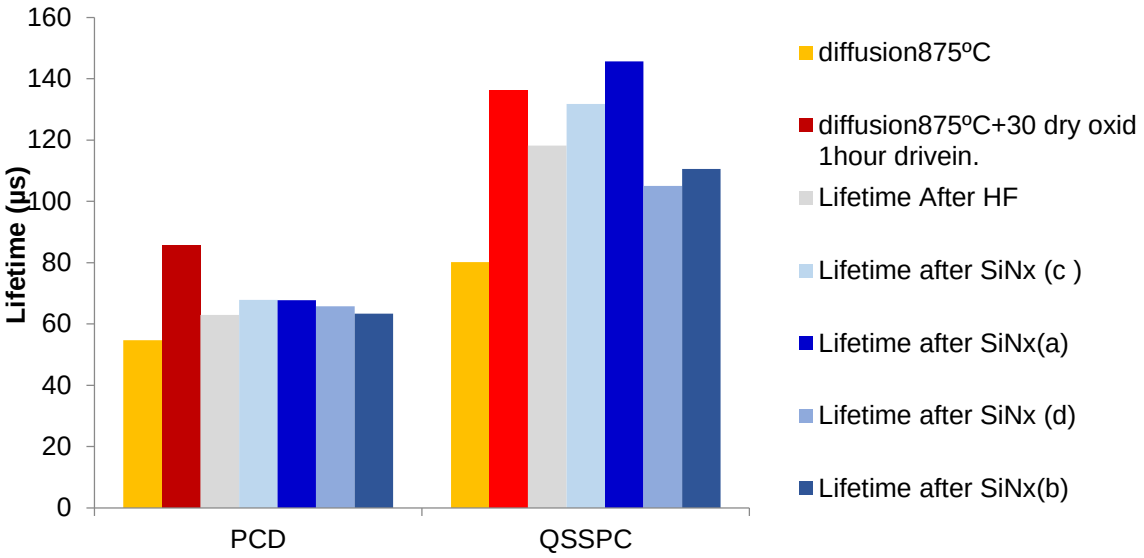


Figure 5.30 Lifetime measurement of fabrication process used for passivation of high doped emitters on n-type substrate, Lifetime is measured after phosphorus diffusion, after dry oxidation, after HF treatment, after deposition of SiNx layer.

Fabrication process which is shown in figure 5.24(d), we have tried to convert high doped emitters into lowly doped emitters prior to passivation by chemical etching. During chemical etching, up to 50-100nm thick surface layer is removed in order to decrease the doping concentration and to remove the dead layer. Wafers cleaned with RCA1&2 and HF in order to remove oxide layer, prior to SiN_X deposition. A layer of silicon nitride is deposited on both sides of wafer by plasma enhanced chemical vapor deposition (PECVD). We have used nitrogen/silane ratio, which has given the best results in SiNx optimization point for passivation. After Silicon nitride deposition (SiNx) on high doped emitters, lifetime of each wafers were measured at room temperature (17-20ºC) for minority carriers at injection level in range of 10E13-E17/cm^3. Both quasi steady state (QSSPC) and transient photo

conductance (TPCD) techniques were used. Lifetime was measured after diffusion, after HF treatment and after SiNx deposition. In this process, we have deposited SiNx layer by changing gaseous flow of nitrogen/silane (C4.59, C4.510, C4.910 and C4.99 see table 5.2 for detail), in order to see the effect of nitrogen/silane concentration on lifetime measurement, Results are given in graph in figure 5.31 of fabrication process of figure 5.24 (d). Flow of silane and nitrogen is in sccm (cubic centimeter/minute). C4.59 (SiH_4=9, N_2=261) SiNx (a), C4.510 (SiH_4=10, N_2=260) SiNx (b) and C4.99 (SiH_4=9, N_2=285) SiNx(c). See table 5.2 for detail of gaseous flow and temperature.

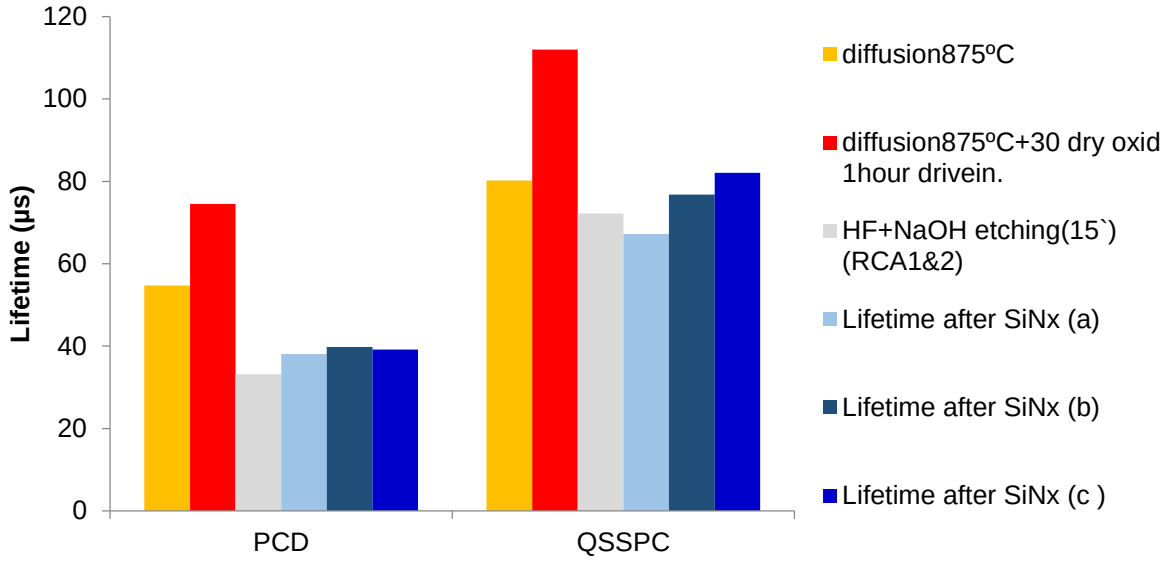


Figure 5.31 Lifetime measurement of fabrication process used for passivation of high doped to lowly emitters on n-type substrate, Lifetime is measured after phosphorus diffusion, after dry oxidation with drive-in, after etching by NaOH and cleaning, and after deposition of SiNx by using different flow of N2/SiH4 ratio.

5.8 Passivation of Softly doped emitters on P-type substrate

Process is started from chemical etching process of wafers. P-type monocrystalline Cz-Silicon wafers (ρ = 5.7 Ω·cm; thickness = 150µm) with size 10x10 cm^2 has been taken for etching process, which was carried out by CPX solution, an etching solution used to etch silicon in acidic medium. RCA1&2 cleaning was performed to remove the all kind of impurities (inorganic and organics) and treated with hydrofluoric acid prior to P diffusion. “P” pre-deposition is carried out at 820 ^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under standard conditions. A dry oxidation was carried out for 30 minutes with drive-in process. Drive in process was carried out in oxidation furnace at 950^{0}C for 1 hour in nitrogen ambient. A layer of silicon nitride is deposited on both sides of wafer by plasma enhanced chemical vapor deposition (PECVD). We have used nitrogen/silane ratio, which has given the best results in SiNx optimization point for passivation. After Silicon nitride deposition (SiNx), lifetime of each wafers were measured at room temperature (17-20ºC) for minority carriers injection level in range of 10E13-E17/cm^3. Both quasi steady state (QSSPC) and transient photo conductance (TPCD) techniques were used. Lifetime was measured after diffusion with dry oxidation and drive-in and after SiNx deposition. Fabrication scheme for passivation of n+ emitter is same as it is mentioned early

in figure 5.24(c) except p-type high resistivity wafers are used in this process. [23]. Structure of silicon wafers after emitter's formation and deposition of SiNx layer is shown in figure 5.32.

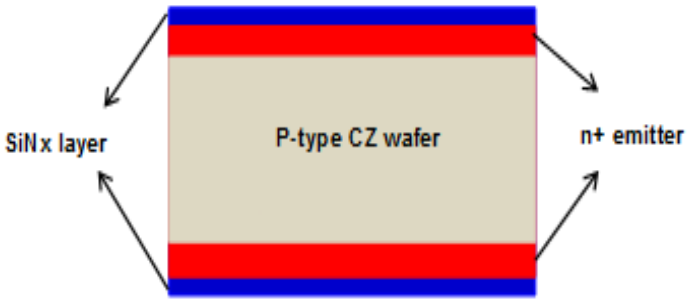


Figure 5.32 Structure of p-type wafer after n+ emitter formation and SiNx deposition

The effective lifetime of each cells were measured at 20 ºC with minority carrier injection level was in range of 1E13 to 1E17/cm^3. Both quasi-steady state (QSSPC) and transient photoconductance (PCD) techniques were used to measure effective lifetime. It is useful to use both techniques to determine the effective lifetime because both QSSPC and t-PCD are complementary to each other depending on system of calibration constants. Although measured lifetime by QSSPC is always higher than t-PCD but accuracy is low in case QSSPC. Lifetime measurement results of fabrication process used to passivate lowly doped n+ emitters on P-type substrate are given in figure 5.33 and effective recombination velocity obtained due to passivation is shown in figure 5.34.

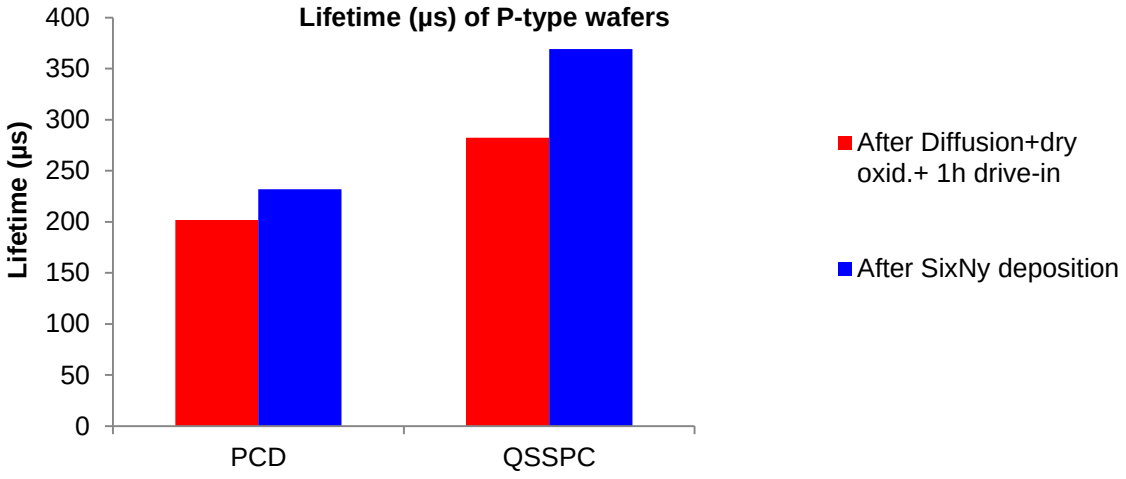


Figure 5.33 Lifetime measurement of fabrication process used for passivation of lowly doped n+ emitters on P-type substrate and HF free process

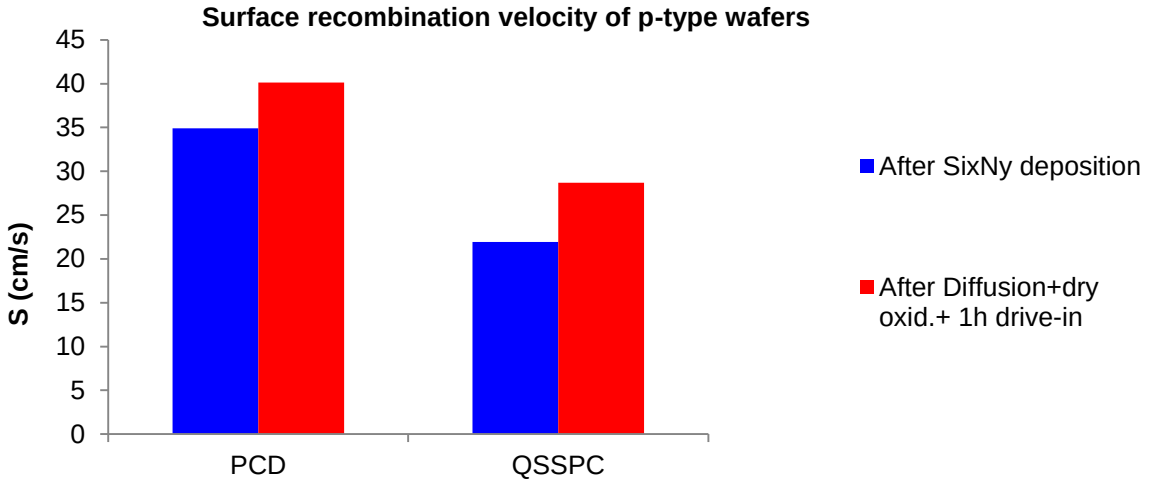


Figure 5.34 Surface recombination velocity of fabrication process used for passivation of lowly n+ doped emitters on P--type substrate

5.9 Selective emitters

In silicon solar cell fabrication, efficiency has been crossed over 19% by homogeneous full area emitter on p-type Cz wafers. Emitters' formation is basic step in fabrication of silicon solar cells and conversion efficiency of silicon solar cells depends on type and quality of emitters. There are two kinds of emitters which are currently used in fabrication process in both laboratory as well as industrial scale. Conventional homogeneous emitters are formed over full area of silicon wafer by using $POCl_3$ as a source of phosphorus at 800-875 ºC and nitrogen as a carrier gas in tube furnace under standard conditions. [24-27]. Second type of emitter is doped selectively with P either by using a tube furnace or other means such as laser, inkjet which are called selective emitters.

In case of p-type wafers, n^+ type homogenous emitters are formed by phosphorus diffusion. Highly doped emitters (sheet resistance 30-60Ω/sq) enabled to decrease contact resistivity between emitters and front metals contacts, but highly doped emitter increase the losses due to low short wavelength response, inactive phosphorus appears in the form of dead layer, which creates recombination centers, This electrically inactive P also introduces defects in the crystalline lattice of silicon, as a result Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure. High concentration of soluble P in Si increases the Auger recombination, as a result efficiency is seriously affected. In case of lowly doped emitters (sheet resistance 100-200 Ω/sq), it is difficult to make contacts between front metal (Ag) and lowly doped emitters, as a result contact resistivity increased which affects negatively on efficiency of solar cell [28]. For optimization of homogeneous emitters for industrial fabrication, there is one option to develop a new paste which can contact with lowly doped emitters (high sheet resistance emitters). Today in industrial fabrication, there is a compromise between emitters doping concentration and performance (moderate sheet resistance 50-80 Ω/sq) which has sufficiently low contact resistance in order to get good efficiency [29]. This comprise can be overcome by fabrication of selective emitters. Selective emitter have high doping concentration under metal contacts grid and low doping concentration under illumination area (area between the metal contacts). Selective emitter fabrication process helps to reduce contacts resistance as well as lower Auger and SRH recombination and improve the open circuit voltage.

There are many techniques which are mentioned in literature for fabrication of selective emitters. Röder et al, developed a process in which laser has been used to increase the doping concentration underneath the metal contacts from phosphorus glass silicate as a source of phosphorus. [29]. Lauermann et al, [30] used an etching resist (commercial available material) which is deposited by inkjet technique, with this mask, it is possible to etch back emitters between fingers area by chemical etching. Prior to this step, high doping was carried out to get highly doped emitters. In this process, extra steps of cleaning are necessary to remove the etch resist [30-32]. Fraunhofer ISE has developed an approach, which is based on simultaneous ablation of SiNx layer by laser and emitter layer underneath the ablated region by using a liquid (as P-source) laser beam is used for chemical processing (LCP) for selective emitter formation [33]. Similar was carried out by University of New South Wales (UNSW), they have deposited phosphoric acid as doping source on the wafer prior to laser doping. Roth & Rau are working on commercialization of this technique [34].

Institute of Physical Electronics (IPE), University of Stuttgart discover a process for industrial fabrication of selective emitters by using a pulsed Nd:YAG laser λ=532nm, 20kHz pulse repetition rate, and 65 nanosecond pulse duration having a Gaussian beam shape which melts the wafer surface locally and enables the fast incorporation of P atoms from the PSG-layer [35-37 and 30]. This process is patented, no more information is available. Up to 800nm deep selective emitter can obtained by using a pulse of long duration of few hundred nanoseconds. On cooling Si recrystallize epitxially and form a highly doped n+ selective emitters without any defect or damage.

Centrotherm (German solar cells company) also presented a selective emitter formation technology which is based on masked P diffusion by using a silicon oxide layer as a mask, which slows down P diffusion from surface into bulk underneath SiO_2. For selective diffusion, structure of SiO_2 was ablated by using a laser where the metals are formed afterward. A wet chemical etching step is used to remove the laser damages. After diffusion, heavily doped region results in 45Ω/sq sheet resistance while masked area in 110Ω/sq. This technology offers a certain degree of freedom in selective emitter formation and uses technologies already established in PV [38-39]. One of the objective of our work is also to get selective emitters for P/Al structure.

5.9.1 Fabrication of selective emitters

Fabrication process for selective emitter's formation is shown in figure 5.35. For P-type wafers, n^+ emitters are formed by phosphorus diffusion. Process is started from chemical etching and cleaning prior to P diffusion. For homogenous emitter's formation, P diffusion was carried at 820 ºC for 30 minutes. We have selected low temperature P diffusion for fabrication of selective emitters. Because highly doped emitter increase the losses due to low short wavelength response, inactive phosphorus appeared in the form of dead layer, which creates recombination centers, as a result Shockley-read-Hall recombination increased and efficiency is seriously affected. Although it is difficult to make contact with between front metal grids and lowly doped emitters but it can be overcome by introducing a second diffusion which increases the doping only underneath the metal grids [28]. In industrial fabrication, there is a compromised between emitters doping concentration and performance (moderate sheet resistance 50-80 Ω/sq) which has sufficiently low contact resistance in order to get good efficiency [29]. This compromise can be overcome by fabrication of selective emitters. Selective emitters have high doping concentration under

metal contacts grid and low doping concentration under illumination area (area between the metal contacts). Selective emitter fabrication process helps to reduce contacts resistance as well as lower Auger and SRH recombination and improve the open circuit voltage.

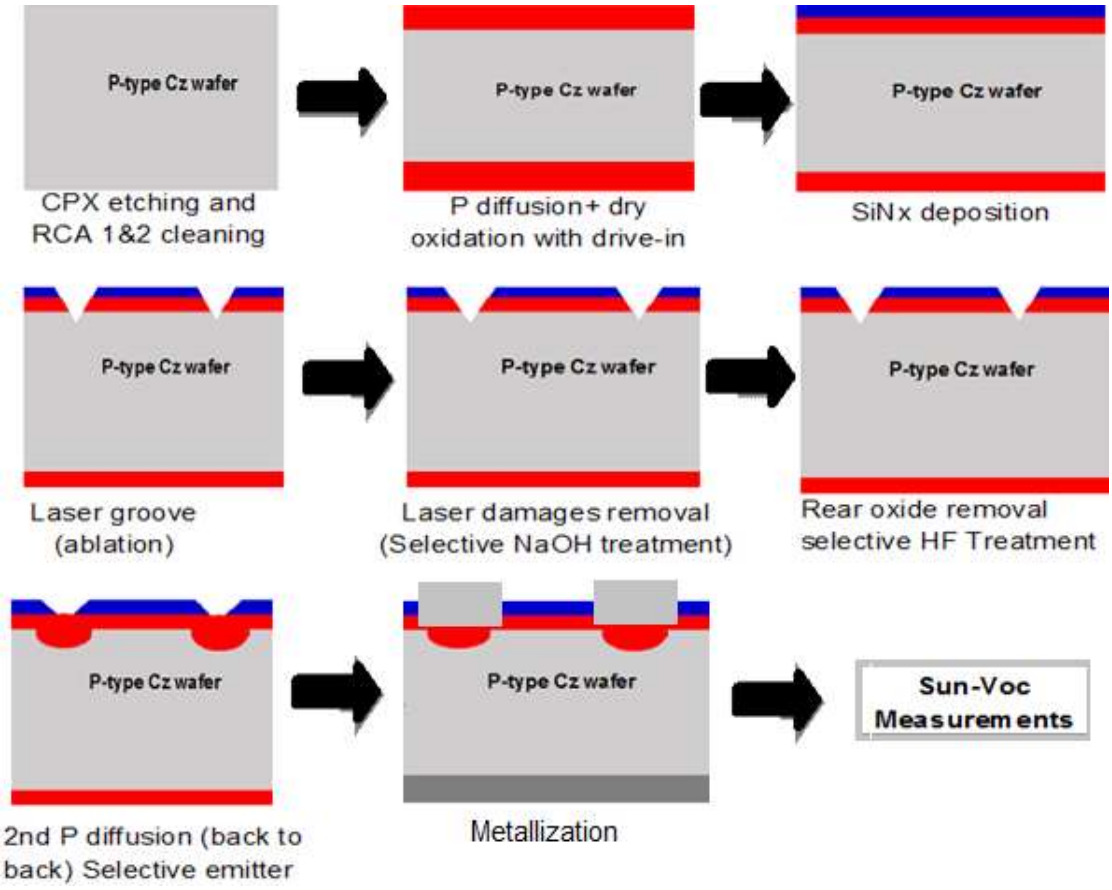


Figure 5.35 Fabrication process for selective emitters formation (p-type wafers)

We have fabricated selective emitter in two steps.

- Homogeneous emitter formation
- Selective emitter formation.

5.9.1.1 Homogeneous emitter formation

Homogeneous emitters are formed over full area of silicon wafer by using $POCl_3$ at different temperature ranging from 800 ºC to 875 ºC by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under standard conditions Fabrication process is started from chemical etching of both p-type monocrystalline silicon wafers obtained by Czochralski growth (Cz), a low quality wafers than float-zone wafers. Description of wafers are given below:

P-type monocrystalline silicon wafers (Cz)
Resistivity: 3-6 ohm.cm
Thickness: 200±10 µm (prior to etching)
Dopant: B
Conductivity: P type

We used CPX for etching of silicon wafers. Wafers about 200µm in thickness were taken for chemical etching CPX, (detail of CPX is given above) followed by RCA1 and RCA2 cleaning. For P diffusion p-type monocrystalline Cz-Silicon ($\rho = 5.4\,\Omega\cdot$

cm; thickness= $150 \pm 5\mu m$) with base doping N_{base} = 2.7E15 cm^{-3} and size $10\ cm \times 10\ cm$ has been taken for processing after chemical etching and cleaning. P pre-deposition is carried out at 820^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace under following conditions as shown in table 5.5. It is common to perform phosphorus diffusion in two-steps, pre-deposition and drive-in in second step. In this work we have introduced a single step P diffusion, P pre-deposition together with drive-in. In between P-pre-deposition and drive-in step, dry oxidation was carried out in order to passivate the emitters for 30 minutes. The emitters obtained by above mention procedure are homogeneous and uniform on the wafer's surface. They have almost similar sheet resistance values (doping concentration) on whole wafers surface. [27].

Table 5.5

P Pre-deposition		
Steps	Time in minutes (T in ºC)	Gases flow
wafers loading	5minutes at (750^{0}C)	N_2 6 *l*/min +O_2 0.1 *l*/min
Stabilization	5-10 (820^{0}C)	N_2 6*l*/min +O_2 0.1 *l*/min
Bubbler temperature and flow rate. 20 ^{0}C		240 cc/min N_2/$POCl_3$
Doping	30 minutes (820^{0}C)	N_2 6 *l*/min +O_2 0.1 *l*/min +
Oxidation	5 minutes (820^{0}C)	O_2 2 *l*/min
Annealing	5 minutes (820^{0}C)	N_2 2 *l*/min
Exit (wafers unloading) Optional	If we have to change the furnace	N_2 2 *l*/min
Dry oxidation and Drive-in		
Dry Oxidation	30 minutes (950 ^{0}C)	N_2 2 *l*/min+ O_2 2 *l*/min
Drive-in	1h=60 minutes (950 ^{0}C)	N_2 2 *l*/min
Exit (wafers unloading)	5 minutes (750^{0}C)	N_2 2 *l*/min

Gaseous flow of the process is given in table 5.5. Detail about diffusion process is given in chapter 4.

5.9.1.2 Silicon Nitride (SiNx) deposition on homogeneous emitters

After homogeneous emitter formation, SiNx layer was deposited by PECVD technique. Experiments which we have performed to deposit SiNx by using different parameters of PECVD technique are given below in table (recipe of SiNx) and gaseous flow of all gases used in deposition process are also given below in table. We have used 400 ºC temperature for SiNx deposition, due to previous results which we have obtained in passivation. We have found the best results at 400 ºC, instead of low temperature deposition (300 or 350 ºC). In this batch, we have used the recipe of SiNx which has given the best results in surface passivation of N-type wafers (table 5.6).

Table 5.6 Recipe of SiNx

	SiH_4 (sccm)	NH_3 sccm)	N_2 (sccm)	Ar (sccm)	Time	Temp. (^{0}C)	MW	Rf	Pressure
Start (Heat)					30 min	400			0.2 mb
Stabilization		60		40	1.3 min= 90sec	400			0.2 mb
Pre Plasma		60		40	30 sec	400		300W 150V	0.2 mb
Cleaning				100	10 sec	400			0.2 mb
stabilization SixNy	10	60	260	40	30 sec	400			0.2 mb
Plasma	10	60	260		3.15 mins	400	MW 2200	300W, 150V	0.2 mb

*Yellow color parameters are variables (we have to change these variables to get good passivation). SiH_4 and N_2 flow during stabilization of SiNx and SiH_4 with N_2 change with time during plasma.

C4.59 (SiH4=9, N2=261)
C4.510 (SiH4=10, N2=260)
C4.99 (SiH4=9, N2=285)
C4.910 (SiH4=9, N2=285)

After SiNx deposition, passivation properties were characterized by measuring lifetime of wafers by using PCD and QSSPC techniques. We have observed improvement lifetime after SiNx deposition. Values of lifetime also depends on oxide layer which is grown during dry oxidation process.

5.9.1.3 Lifetime measurement of homogeneous emitters:

After homogeneous emitter's formation, SiNx layer is deposited by PECVD technique by optimal point, which have got after SiNx layer optimization. Parameters of SiNx layer deposition is given above table. Passivation quality of these wafers were evaluated through lifetime measurements by PCD and QSSPC techniques before and after SiNx deposition is shown in figure 5.36. Surface recombination velocity is also calculated from lifetime measurements which plotted in figure 5.37.

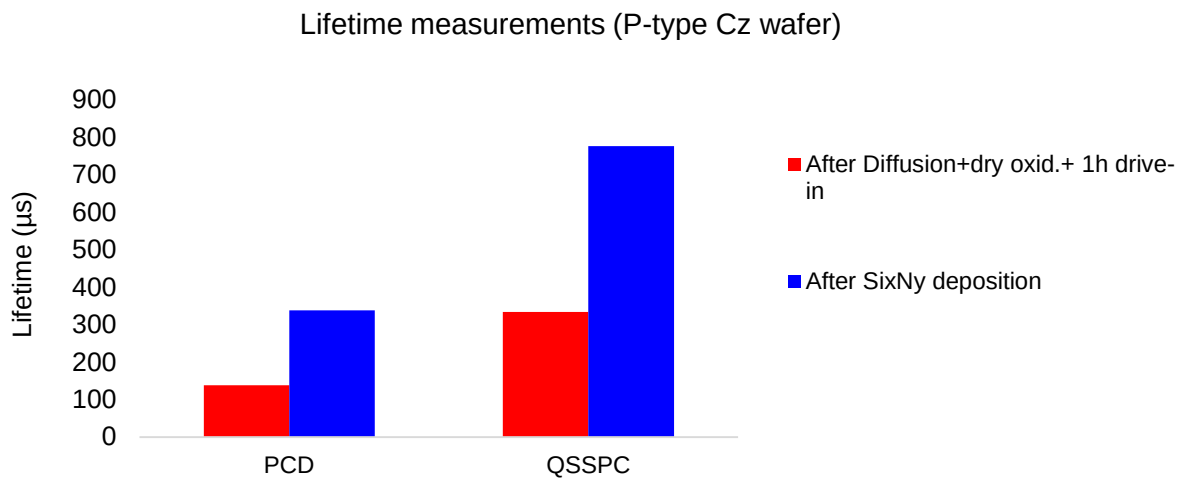


Figure 5.36 Lifetime measurement before and after SiNx deposition on P-tpe wafers by PCD and QSSPC technique

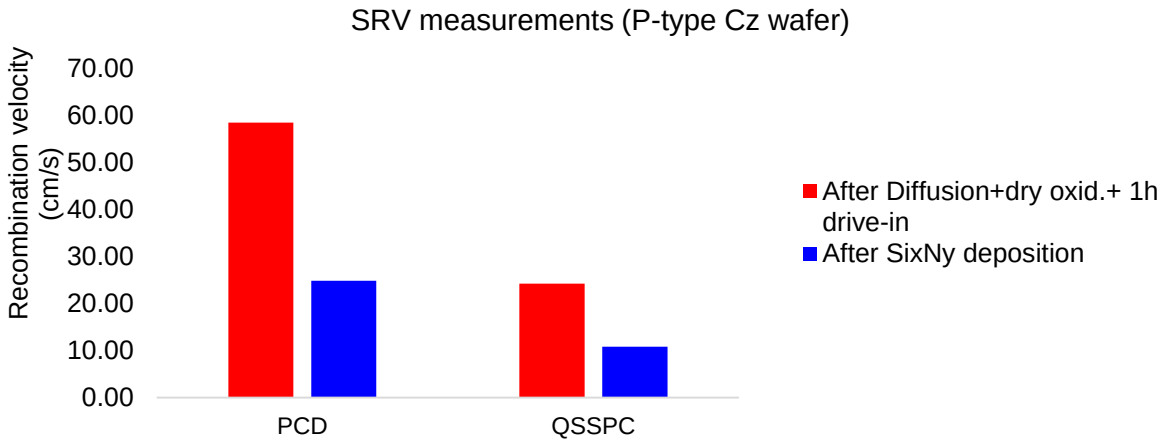


Figure 5.37 SRV of homogeneous emitters before and after SiNx deposition of P-Type wafers

5.9.1.4 Laser scribed grooves:

Laser micromachining processes being used in monocrystalline and polycrystalline solar cells include laser edge isolation, laser micro via drilling, laser fired contacts, and laser surface structuring as well cutting of wafers and . All of the above mentioned machining technologies have a guarantee for high efficiency of the complete solar cell at a minimum of materials damage and least material's loss. For selective emitter's formation and high efficiency achievement, we have used laser as a tool to scribe on wafers in specified manner to draw superficial grooves till 2-5 µm in depth and 25-30 µm in width, on cell area of $4.2 \times 3.2\ cm^2$. Each silicon wafer of $10.2 \times 10.2\ cm^2$ area has 4 cells on it as shown in figure 5.38. These grooves not only used for selective emitter's formation but also used to decrease emitter saturation current density to passivated emitters.

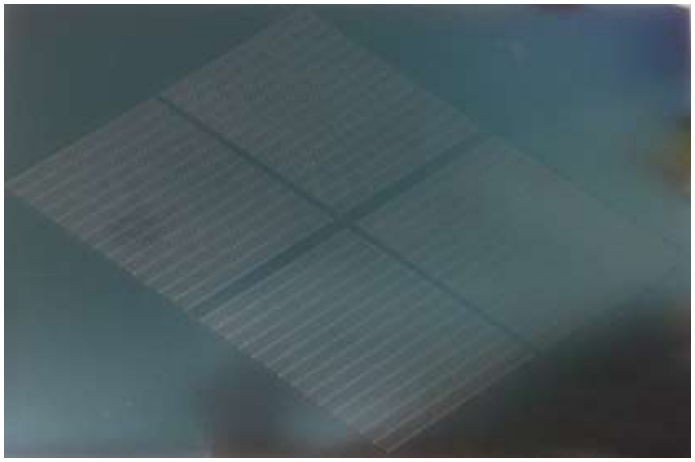


Figure 5.38. Laser scribed grooves on silicon wafer of 10.2X10.2cm^2 area

For proper use of laser, we used an Ast06 software to draw a sketch, which is used to define the point where laser beam scribe or ablate the surface. For proper observation, we used a pointer, which is used to indicate the laser scribing area on wafer surface and camera to see the scribing point or area of the wafer. We can adjust the platform manually or moving laser up and down for proper laser application [41-48]. Grooves are scribed on specified area of cells according to size of the cell. Approximately 48 lines are scribed of 4cm length and each line has 15 vertical mark about 45-50 µm in length on each line as shown in figure 5.39(b) as well as in the sketch figure 5.39(a).

In our lab, we have two kind of laser, one is green laser, which works in visible region and other works in IR region. Green laser of visible region has a wavelength 515nm use for scribing, cutting and edges isolation. The laser-system which is used in our experiments consists of a Q-switched fiber laser, which generates pulses of 10 ns duration, Gaussian beam, working at two wavelengths (infrared, IR, λ_1 = 1030 nm and green, GR, λ_2 = 515 nm).

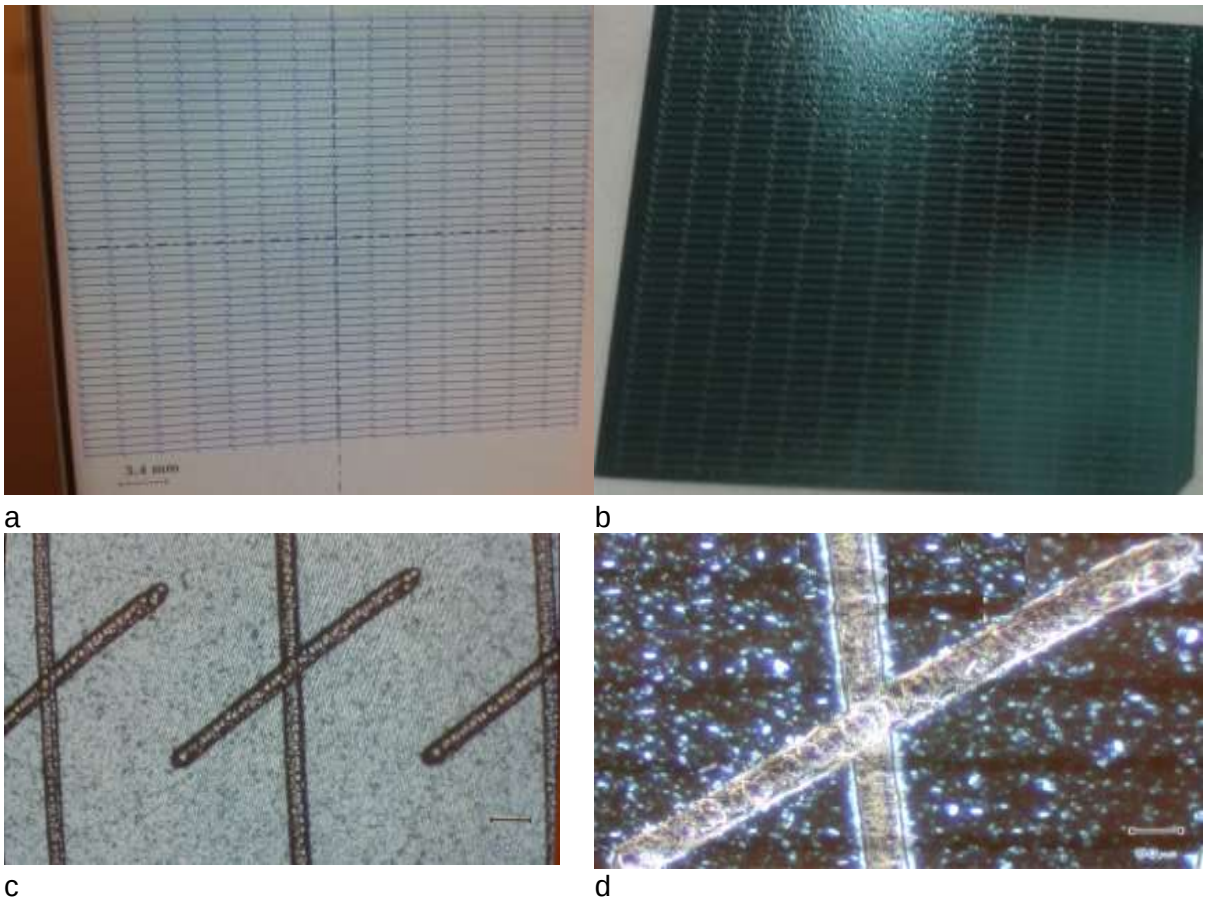
Silicon wafers are conventionally diced off by a thin diamond blade, currently green wavelength with milliseconds to nanosecond duration, low power pulsed fiber lasers and high beam quality continuous wave fiber lasers are being used to cut these materials. The cut quality is poor and micro cracking can occur due to excessive heat input, which can lead to failure of some components during process steps and associated reduction in yields. Due to this reason, post chemical treatment was carried out in order to remove laser induced damages [41-48].

5.9.1.5 Laser Description:

Lasers machine and its description are already shown in figures 3.40 (chapter 3). For operation we used a computer program Ast06. For proper functioning we have to adjust scanning speed which is from 20 to 3000mm/sec and pulse repetition frequency 10-200 kHz and power is variable under different conditions.

We have used following parameters for scribing groove on silicon wafer
Laser frequency: 50 kHz
Laser power: 34.2 A
Scanning velocity: 500 mm/sec
No of scan: 1

Although laser is advance and fast technique for processing and cutting but it has some disadvantages, in some cases we observed that due to melting of silicon by laser, silicon starts depositing on the edges of cells which cause in shunt conductance.



a b c d

Figure 5.39 a: Image of sketch which is used to define the scribing point/area by laser. Figure 5.41(b): Laser scribed grooves on silicon wafer surface. Figure 5.41(c&d): Microscopic images of grooves after laser processing

5.9.2 Selective emitter formation

After laser scribed grooves, silicon wafers were treated with 25% NaOH solution at 60 ºC in order to removed laser induced damages. NaOH not only removed the ablated material but also etch silicon to make the grooves deeper. In some cases backside were treated with HF in order to remove oxide layer. It is critical process, it was essential to protect the front AR coating (SiNx layer) from HF. HF not only etch the silicon oxide but also etch the silicon nitride.

For selective emitter's formation, 2nd P diffusion was carried out at 875 ºC for 30 minutes. This P diffusion was carried out under same gaseous flow and time except temperature. In this step, wafers were placed in furnace in such way that backside of one wafer is attached to backside of other wafer. In the boat (wafers carrier), two wafers were placed like a single wafer, their backsides were completely overlapped and looked like a single wafer (back to back). In this way phosphorus only diffuse on front side (surface). This step we called it back to back diffusion. In this step back surface of each wafer is protected from doping impurities. In order to confirm this protecting step, we have measured the sheet resistance of backside of wafers and sheet resistance values confirmed it that no P was diffused on backside.

In selective emitter formation, front surface is covered with silicon nitride. Silicon nitride layer acts as barrier for P diffusion. Phosphorus neither diffuse through silicon nitride inside nor outside. But in laser scribed grooves area, it is open to phosphorus diffusion and P can diffuse easily into silicon. During this 2nd diffusion step, doping concentration is increased only in grooves area. After phosphorus diffusion, we have evaluated surface of emitters through measuring the sheet resistance by removing SiNx layer of wafer. Sheet resistance values show that emitter under SiNx layer is not affected by 2nd diffusion. Low doping concentration of emitters is maintained underneath this silicon nitride layer. Now we have two areas on wafer surface with different doping concentrations. The process which is used to fabricate emitters with different concentrations are called selective emitters. Selective emitter have high doping concentration under metal contacts grid and low doping concentration under illumination area (area between the metal contacts). Selective emitter fabrication process helps to reduce contacts resistance as well as lower Auger and SRH recombination and improve the open circuit voltage [49].

5.9.2.1 Al-Deposition for Al-BSF

After 2nd phosphorus diffusion (for selective emitter formation), Wafers were cut/break manually by pressing at corner of wafers to isolate the solar cells, which were already marked by laser for cutting in order to separate cells. In this way, we have isolated cells from wafer just pressing cells area manually on the wafer surface. A thick layer of aluminum was deposited on backside of cells by screen printing technique in order create back surface field as well as back contact. For this purpose we have used Al paste (Al-5540 a commercially available Al paste supplied by Ferro electronics material) which was dried at 350ºC and was fired at different temperature from 875 to 950 ºC and at different speed of belt of furnace from 60 to 90 inches/minute for 2 to 3 minutes.

5.9.2.2 Sun-Voc Measurements and characterization (P-type wafers)

This measurement very similar to Voc measurement except Jsc, Suns-Voc uses a separate solar cell to monitor the illumination intensity of the solar cell instead of Jsc. Suns-Voc curve allows us to characterize lifetime of minorities carriers and its analysis also provides detailed information on the internal components of recombination in the solar cell. Sun-Voc measurements provide information of IV curves without the effect of series resistance of diode. Fitting of Sun-Voc curve is easier than illuminated curve since there is no dark current or series resistance. [50-51]. Detail of measurement of Sun-Voc and characterization process is given in chapter 3.

From Sun-Voc measurement, it is also possible to extract lifetime of base of solar cells by fitting the curves obtained by Sun-Voc measurements. In order to find out the lifetime of base of cell, we have to fix the values of J_{OE} and J_{OZ} for given solar cell and we have to adjust the values the Tau of base by changing its values in order to fit the curve with experimental curve, which is obtained from sun-Voc measurements. Lifetime obtained by fitting IV curve of Sun-Voc measurements are given in table 5.7.

Table 5.7 Fitted lifetime of base of different cells processed at different temperatures with Sun-Voc curve.

Speed	Rear surface	875 ºC	900 ºC	925 ºC
60 inch/min	Al-BSF with SiO_2	40µs 11µs	10 µs 20 µs	13µs 16 µs
	Al-BSF with Si (HF treatment)	13µs	15µs	30µs 20µs
70 inch/min	Al-BSF with SiO_2	8µs 10µs	13µs 17µs	20µs 13µs
	Al-BSF with Si (HF treatment)	20µs	21µs 11µs	13µs

From Sun-Voc measurement, it is also possible to extract solar cells parameters by fitting the curves obtained by Sun-Voc measurement such as J_{OE} and J_{OZ} for given solar cell. Solar cell parameters which are obtained after fitting the sun-Voc curve and measured Sun-Voc values for P-type wafers are given in the table 5.8:

Table 5.8 Sun-Voc and solar cell parameters of P-type silicon wafers (High resistivity wafers)

Cell ID	Tau base (µs)	Sun-Voc (mV)	Gsh	J_{OZ} (A/cm^2)	J_{OE} (A/cm^2)
Ob292560	20µs	576	5.00E-3	1.6E-7	2.82E-12
	200µs		5.00E-3	1.6E-7	3.20E12
Ob292560	20µs	568	6.00E-3	1.59E-7	2.26E-12
	200µs		6.00E-3	1.76E-7	4.76E-12
Ob187570	20µs	547	1.60E-2	1.59E-7	6.77E-12
	200µs		1.6E-2	1.59E-7	8.50E-12
Ob487570	20µs	567	4.00E-3	1.59E-7	4.37E-12
	200µs		4.00E-3	1.59E-7	7.89E-12
Ob287570sec	20µs	568	4.00E-3	1.59E-7	1.97E-12
	200µs		4.00E-3	1.59E-7	5.64E-12
Ob490070	20µs	583	8.00E-3	1.40E-7	8.40E-13
	200µs		8.00E-3	1.40E-7	2.82E-12
Ob490070	20µs	555	6.6E-3	1.59E-7	1.97E-12
	200µs		6.6E-3	1.59E-7	5.64E-12
Ob590070	20µs	386	2.5E-2	1.07E-7	1.41E-12
	200µs		2.5E-2	1.06E-7	2.92 E-12
Ob690070	20µs	544	2.2E-2	2.64E-7	2.54E-12
	200µs		2.2E-2	2.64E-7	5.07E-12
Ob492570	20µs	559	1.90E-2	1.59E-7	4.23E-12
	200µs		1.90E-2	1.59E-7	7.05E-12
Ob592570	20µs	566	2.0E-2	1.59E-7	1.97E-12
	200µs		2.0E-2	1.59E-7	3.37E-12
Ob192560	20µs	595	8.5E-3	9.7E-10	1.83E-12
	200µs		8.5E-3	9.7E-10	2.63E-12
Ob187560	20µs	562	1.15E-2	2.64E-7	2.54E-12
	200µs		1.15E-2	2.64E-7	5.27E-12

Ob287560	20µs	422	4.3E-2	1.59E-7	2.68E-13
	200µs		4.3E-2	1.59E-7	1.14E-12
Ob587560	20µs	569	6.7E-3	1.59E-7	2.31E-12
	200µs		6.7E-3	1.59E-7	5.07E-12
Ob190060	20µs	573	4.0E-3	1.59E-7	1.97E-12
	200µs		4.0E-3	1.59E-7	5.58E-12
Ob290060	20µs	583	6.00E-3	1.59E-7	1.30E-12
	200µs		4.0E-3	1.59E-7	1.97E-12

We have measured lifetime after laser damages removal by NaOH and high temperature P diffusion for selective emitter formation. Lifetime of the selective emitters is destroyed and emitter saturation current density is also increases which resulted low Sun-Voc values. Theoretically we were expecting Sun-Voc around 650mV, calculated from by using following equation. According to our opinion lifetime is destroyed either due to NaOH treatment or 2nd P diffusion for selective emitter formation. Another option was that NaOH bath has introduced impurities in laser scribed area and at high temperature, these impurities diffuse inside into base of silicon which destroyed the lifetime.

$$V_{oc} = \frac{kT}{q} \ln \left[\frac{nN_A}{n_i^2} \right] \quad = 650 \text{ mV}$$

"*n*" is minority carriers concentration at junction edge, n_i is intrinsic carrier concentration (9E9/cm^3) at 25 ºC. N_A is base doping of wafer and $\frac{kT}{q}$ is thermal voltage.

We have measured lifetime of wafers having laser scribed grooves with selective emitters and wafers with homogeneous emitters, we have found the lifetime is maintained surface which contain homogeneous emitters but lifetime is destroyed of wafer having selective emitters. The lifetime measurements area of wafer is shown in figure 5.41. The average values of Joe of selective emitters was high ranging from 1E-12 to 9E-12A/cm^2 in this batch. In addition to this shunt conductance was also high, we have obtained value of Sun-Voc around 583mV. In our opinion, lifetime is destroyed either by 2nd phosphorus diffusion or chemical treatments step which is used to remove laser damages. There is another option Al deposition and diffusion was not uniform and it is not creating BSF effect properly. We have also observed non-uniform surface of Al under microscope.

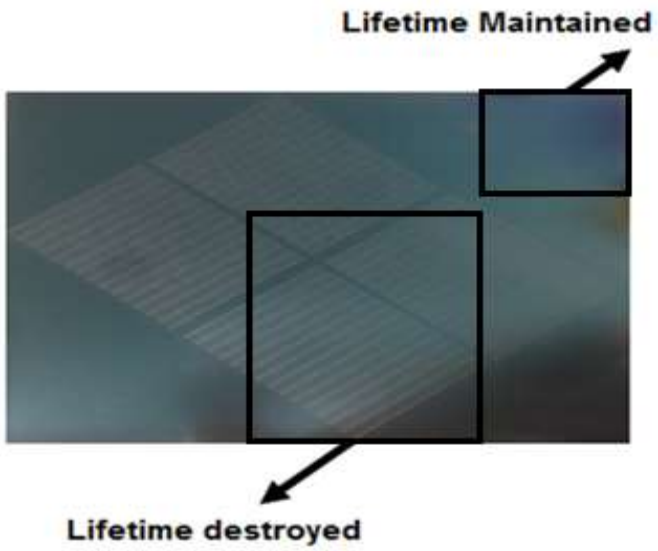


Figure 5.40 Characterization of wafer having area with selective emitters and are with homogeneous emitters

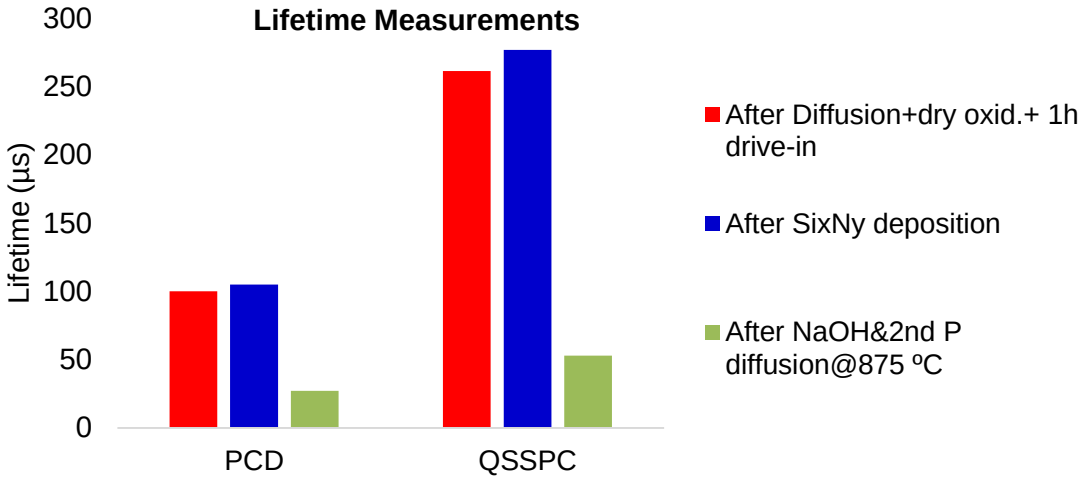


Figure 5.41 Lifetime measurement of wafers with selective emitters after different fabrication steps)

5.9.3 Selective emitter's formation on n-type wafers

Above mention process for selective emitter fabrication is repeated with N-type wafers of following characteristics ($\rho = 0.8\,\Omega \cdot cm\ with$ thickness= $150 \pm 5\mu m$) with base doping N_{base}= $2.4\text{E}15\ \text{cm}^{-3}$ and size$10\ cm \times 10\ cm$. Both n-type and p-type wafers were processed separately to get n+ emitters on both substrate. Systematic fabrication of selective emitters is given below in figure 5.42.

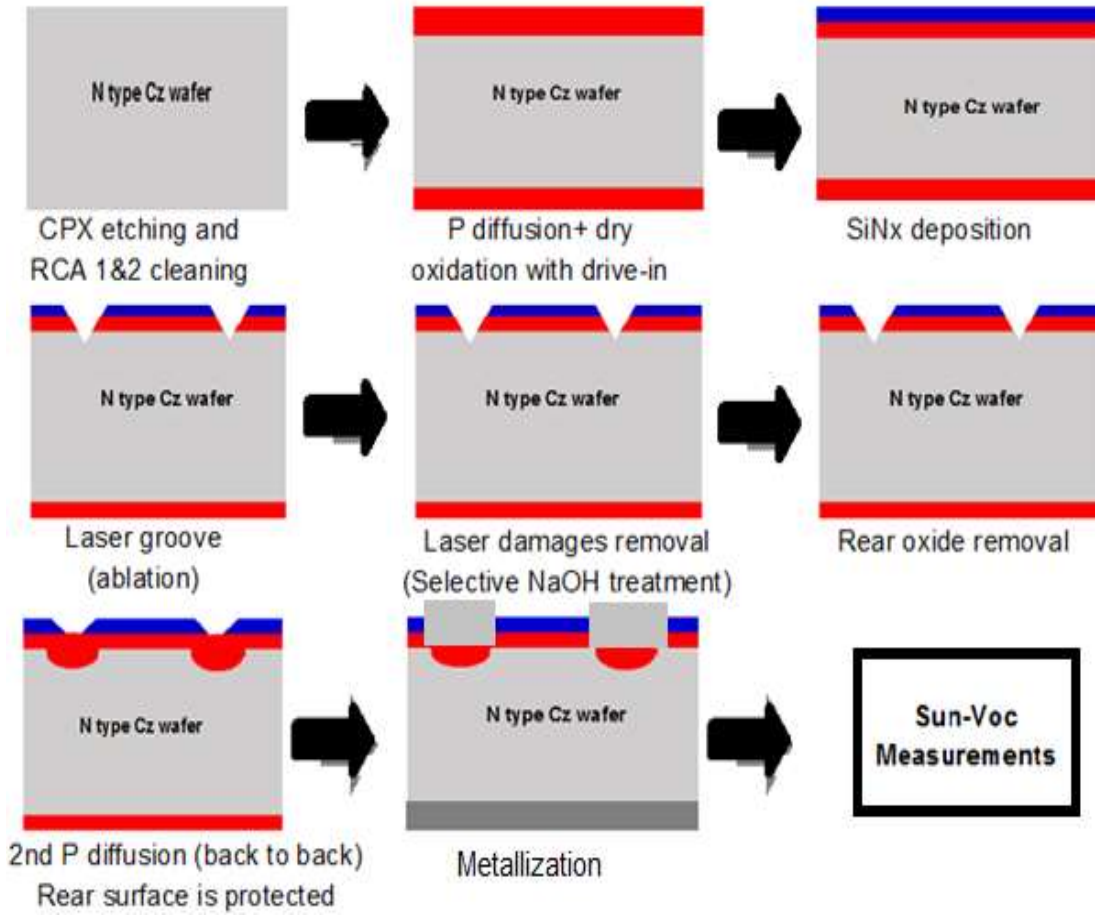


Figure 5.42 Fabrication process for selective emitter's formation (n-type wafers)

5.9.3.1 Lifetime Measurement of Homogeneous emitters (n-type wafers):

After homogeneous emitter's formation, SiNx layer is deposited by PECVD technique by optimal point, which have got after SiNx layer optimization. Parameters of SiNx layer deposition is given above table. Passivation quality of these wafers were evaluated through lifetime measurements by PCD and QSSPC techniques before and after SiNx deposition is shown in figure 5.43. In this batch, we have obtained passivated emitters with maximum lifetimes after dry oxidation as well as SiNx deposition. SRV was lower than 5 cm/s by QSSPC technique and lower than 18 cm/s by PCD technique which are given in figure 5.44.

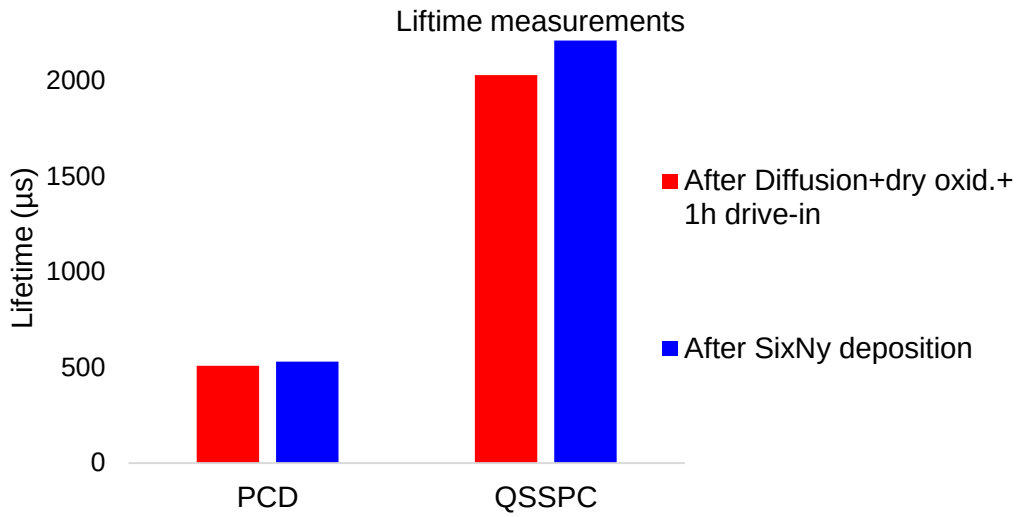


Figure 5.43 Lifetime measurement before and after SiNx deposition on n-type wafers by PCD and QSSPC technique

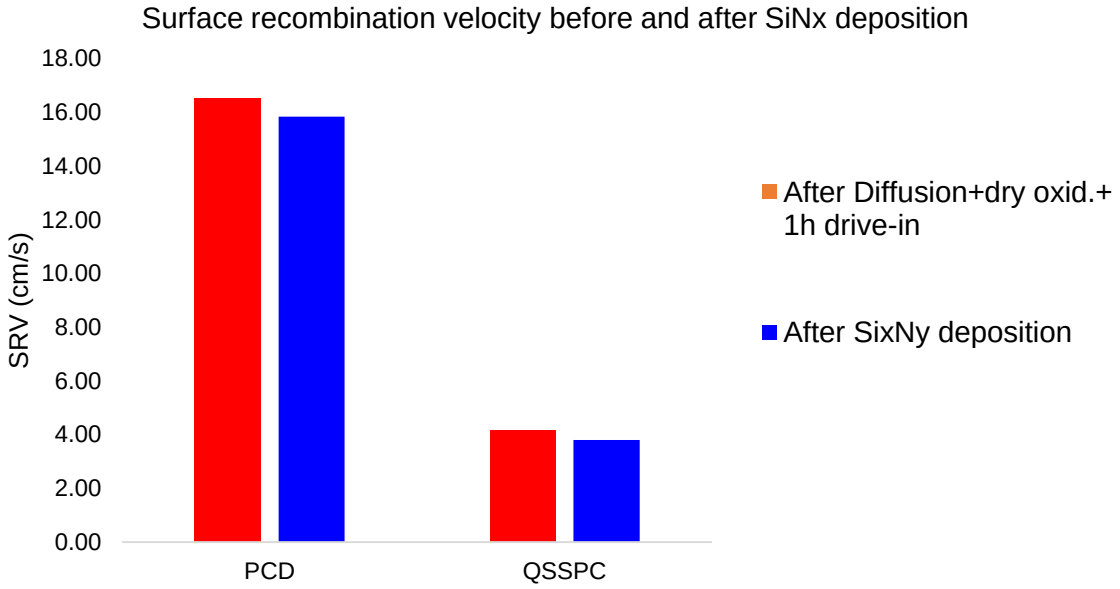


Figure 5.44 SRV measurements of homogeneous emitters before and after SiNx deposition on n-Type wafers

5.9.3.2 Sun-Voc Measurement of N-Type wafers

From Sun-Voc measurement, it is also possible to extract solar cells and diode parameters such as J_{OE} and J_{OZ}. These parameters which are obtained after fitting the sun-Voc curves and measured Sun-Voc values for N-type wafers are given in the table 5.9. N-Type Wafers have lifetime of base around (Tau base) 200µs.

Table 5.9 Sun-Voc and solar cell parameters of N-type silicon wafers

Cell ID	Sun-Voc (mV)	Gsh (ohm.cm^2)	JOZ (A/cm^2)	JOE (A/cm^2)
Ob2087560	273	1.00E-1	1.59E-6	1.3E-12
Ob2287570	313	1.00E-1	1.96E-7	7.53E-13
Ob2187570	511	4.8E-2	1.96E-7	5.13E-13
Ob2090070	558	4.88E-4	1.96E-7	5.13E-13
Ob2190070	614	2.00E-2	1.96E-7	5.13E-13
Ob2292570	564	4.20E-2	1.96E-7	6.84E-13
Ob2392570sec	272	1.30E-1	1.96E-7	6.84E-13
Ob2392570	266	1.30E-1	1.96E-7	6.84E-13
Ob2087560	458	5.2E-2	1.96E-7	6.84E-13
Ob2187560	516	3.3E-2	1.96E-7	1.03E-12
Ob2387560	485	4.50E-2	2.94E-8	1.20E-12
Ob2090060	602	2.5E-2	2.94E-8	6.84E-13
Ob2290060	626	3.00E-2	2.94E-8	5.13E-13
Ob2292560	618	4.00E-2	6.86E-10	6.84E-13
Ob2392560	493	7.60E-2	9.79E-10	6.84E-13

We have found the lifetime is maintained on wafer`s surface which contain homogeneous emitters but lifetime is destroyed of wafer having selective emitters. The average values of Joe of selective emitters was high ranging from 5.0 E-13 to 1.0E-12A/cm^2. Although shunt conductance is high, but still we have obtained a good value of Sun-Voc, the maximum was around 626 mV.

5.10 Selective emitter's formation (P-type wafers)

Above mention process for selective emitter fabrication is repeated with P-type wafers of following characteristics ($\rho = 5.7\ \Omega.cm$ withthickness$= 150 \pm 5\mu m$) with base doping N_{base}= $2.7\text{E}15\ \text{cm}^{-3}$ and size $10\ cm \times 10\ cm$ with little bit modification in rear surface of wafer. P-type wafers were processed to get n+ emitters in similar way as mentioned early in this chapter. Objective of this batch was to improve the quality of selective emitters which were destroyed in previous batch after 2nd P diffusion. Systematic fabrication process of selective emitters is given below in figure 5.45.

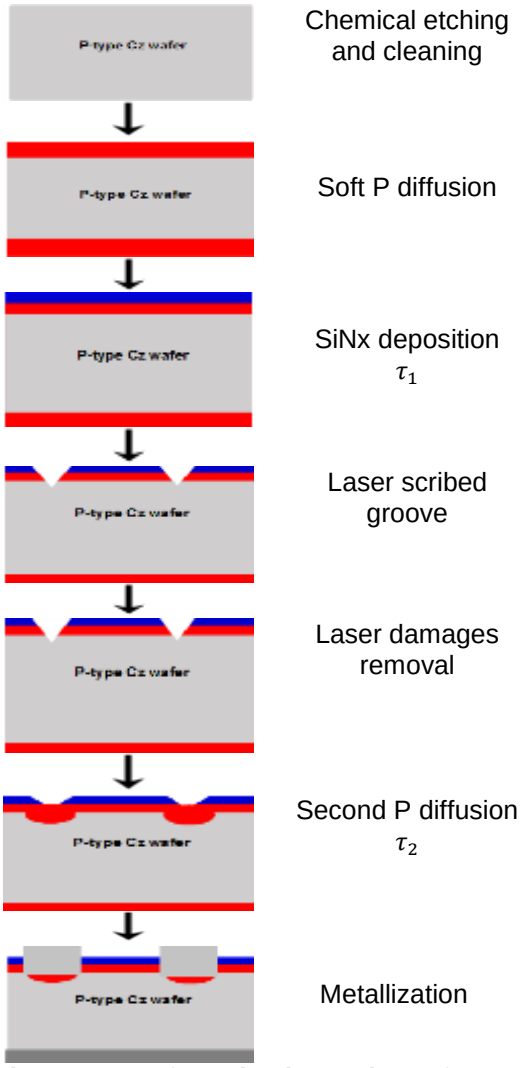


Figure 5.45 Fabrication process for selective emitters formation (p-type wafers)

As we had observd in previous batch, lifetime was destroyed, after NaOH treatment with 2nd Phosphorus diffusion. In order to confirm, process was repreated with NaOH as well as KOH treatment in order to remove the laser induced damages. In this batch we have used tefflon bath for NaOH and KOH treatment of wafers for laser damages removal for extra care of process. We have measured lifetime of wafers before and after NaOH treatment, detail of process and results is given in table 5.10. In addition to this, some wafers were also processed without NaOH treatment or without 2nd P diffusion in order to compare the results. Average lifetime of cells prior to laser processing was around 140 µs.

Table 5.10 Lifetime measurement of laser ablated wafers

Process	Lifetime	Result
Lifetime after Laser grooves, NaOH is used to remove damages + diffusion (875 ºC)	90.5µs 42.9 µs 72 µs	Lifetime decreased
Lifetime after Laser grooves + Diffusion (875 ºC)	139.5 µs 127.5 µs	Lifetime maintained
Lifetime after Laser groove (one line only) with NaOH to remove laser damages +diffusion(875ºC)	97.5	Lifetime is affected
Lifetime after Laser groove (one line only) + diffusion (875 ºC)	117 µs	Lifetime is affected

Lifetime is measured by transient technique.

From these measurements, it is clear lifetime is affected by NaOH, as a result emitter saturation current density is increased and open circuit voltage is decreased. After lifetime measurements and metallization, we also measured Sun-Voc of above cells, result of Sun-Voc is given in table 5.11.

Table 5.11 Sun-Voc measurements after 2nd Phosphorus diffusion, laser damages were removed by NaOH treatment

Belt speed	Rear structure	Sun-Voc values		
	Al-deposition	925 ºC (No laser)	925 ºC (laser1)	925 ºC (laser 2)
60 inches/min	Al-BSF with SiO_2 (a)	578 mV	613 mV 619 mV	614 mV 584 mV
	(b)	605 mV	578 mV 600 mV	600 mV 607 mV
70 inches/min	Al-BSF with SiO_2 (a)	591 mV	622mV 598 mV	608 mV 613 mV
	(b)	575 mV	598 mV 579 mV	613 mV 600 mV

Laser 1 has more number of laser scribed grooves than laser 2.

As we had observd in previous batch, lifetime was destroyed, after NaOH treatment with 2nd Phosphorus diffusion. In this batch we have treated cells with KOH in order to remove the laser induced damages. We have measured lifetime of wafers before and after KOH treatment, detail of process and results is given in table 5.12. In addition to this some wafers were also processed without KOH treatment or without 2nd P diffusion in order to compare the results. Average lifetime of cells prior to laser processing was around 140 µs. In this batch we have used tefflon bath for KOH treatment of wafers for laser damages removal for extra care of process.

Table 5.12 Lifetime measurement of laser ablated wafers

Process	Lifetime	Result
Lifetime after laser grooves with KOH to remove damages + diffusion (875 ºC)	93.5µs 83.9 µs 77 µs	Lifetime is affected
Lifetime after laser grooves with KOH to remove damages (No diffusion)	109 µs	Lifetime decreased
Lifetime after laser + Diffusion (875 ºC)	139.5 µs 127.5 µs	Lifetime maintained
Lifetime after laser (one line only) with KOH to remove damages + diffusion (875 ºC)	133 µs 125.1 µs	Lifetime is maintained
Lifetime after laser (one line only) + diffusion (875 ºC)	118 µs	Lifetime little bit decreased

Lifetime is measured by transient technique.

Although lifetime is also affected by KOH as we observed by using NaOH but loss of lifetime is not as high as we observed by using NaOH. In addition to this, high temperature diffusion is also affecting on lifetime but this loss is in few microseconds due deposition of solid inactive phosphorus. Sun-Voc measurement results of above cells after metallization are given in table 5.13.

Table 5.13 Sun-Voc measurements after 2nd Phosphorus diffusion, laser damages were removed by KOH treatment

Belt speed		Sun-Voc values		
	Al-deposition	925 ºC (No laser)	925 ºC (laser 1)	925 ºC (laser 2)
80 inches/min	Al-BSF with SiO_2	614 mV	599 mV 601 mV	620 mV 609 mV
		610 mV	613 mV	
70 inches/min	Al-BSF with SiO_2	614 mV	624 mV	612 mV
		623 mV 623 mV	620 mV 585 mV	610 mV

In our opinion, it is better to use KOH instead of NaOH to remove the laser induced damages in solar cells. For high efficiency process, we have to avoid NaOH based processes. According to simulations and theoretical calculation, it is important to maintain emitter saturation current density as low as possible for high efficiency process. Emitter saturation current densities and shunt conductance of solar cell are given in table 5.14 and table 5.15. Aluminum was deposited by screen printing technique which was dried at 350ºC and was fired at 925 ºC and at different speed of belt of furnace from 60 to 80 inches/minute.

Table 5.14 Solar cell parameters of P-type silicon wafers extracted by Sun-Voc measurements after metallization

Cell ID	Sun-Voc (mV)	Gsh (ohm.cm^2)	J_{OZ} (A/cm^2)	J_{OE} (A/cm^2)
Ob1NaOH L170	622 mV	1.5E-3	4.58E-8	7.52E-13
Ob1NaOH L270	6.8mV	5.0E-3	7.58E-8	1.02E-12
Ob2NaOH L170	598 mV	2.0E-3	1.38E-8	1.6E-12
Ob2NaOH L270	613 mV	7.1E-4	5.38E-8	1.1E-12
Ob4 L170	598 mV	2.0E-4	1.38E-7	1.07E-12
Ob4 L270	613 mV	3.0E-4	7.6E-8	1.07E-12
Ob5 L170	579 mV	5.0E-4	1.52E-7	4.07E-12
Ob5 L270	600 mV	6.0E-4	1.3E-7	1.9E-12
Ob12 a70	592 mV	5.0E-4	1.52E-7	6.2E-12
Ob12 Line b70	576 mV	5.0E-4	1.53E-7	6.4E-12
Ob1NaOH L160	613 mV	6.5E-4	7.58E-8	9.62E-13
Ob1NaOH L260	6 14 mV	2.0E-3	9.08E-8	8.52E-13
Ob2NaOH L160	578 mV	9.5E-3	1.58E-7	1.92E-12
Ob2NaOH L260	600 mV	1.5E-3	1.58E-7	1.42E-12
Ob11 NaOH Line a60	578 mV	1.5E-3	1.58E-7	3.42E-12
Ob11 NaOH Line b60	605 mV	1.5E-3	7.58E-7	1.72E-12
Ob4 L160	600mV	4.5E-4	1.58E-7	1.72E-12
Ob4 L260	607 mV	1.0E-3	4.58E-7	1.52E-12
Ob5 L160	619 mV	1.3E-3	7.58E-8	6.42E-13
Ob5 L260	607 mV	1.8E-4	2.28E-7	2.02E-12

L1: laser 1, L2 laser 2. (Laser 1 has more number of laser scribed grooves than laser 2).

After laser scribed grooves, prior to 2nd P diffusion, wafers were treated with KOH to remove the laser damages. Aluminum was deposited by screen printing technique which was dried at 350ºC and was fired at 925 ºC and at different speed of belt of furnace from 60 to 80 inches/minute for 2.45 minutes. Emitter saturation current densities and shunt conductance of solar cells are given in table 5.15.

Table 5.15 Solar cell parameters of P-type silicon wafers extracted by Sun-Voc measurements after metallization

Cell ID	Sun-Voc (mV)	Gsh (ohm.cm^2)	J_{OZ} (A/cm^2)	J_{OE} (A/cm^2)
Ob6KOH L1 70	623.4 mV	5.8E-4	9.28E-8	6.42E-13
Ob7KOH L1 70	620 mV	9.08E-4	1.12E-7	7.2E-13
Ob 8KOH L1 70	581 mV	1.8E-3	3.08E-7	1.9E-12
Ob6KOH L2 70	613 mV	9.08E-4	9.08E-8	8.6E-13
Ob7KOH L2 70	609 mV	2.08E-3	7.68E-8	1.02E-12
Ob 8KOH L2 70	585 mV	2.08E-3	1.28E-7	3.6E-12
Ob13 KOH Line a 70	615 mV	5.08E-4	1.28E-8	9.6E-13
Ob13KOH Lin b70	622 mV	9.18E-4	8.08E-8	6.7 E-13
Ob14 KOH line a 70	624 mV	2.08E-4	7.68E-8	7.5E-13
Ob14 KOH line b 70	616 mV	3.08E-4	7.08E-8	7.5E-13
Ob6KOH L1 80	599 mV	4.08E-3	2.28E-7	1.03E-12
Ob6KOH L2 80	613mV	1.08E-3	7.68E-8	9.65E-13
Ob7KOH L1 80	593 mV	1.58E-3	7.68E-8	3.15E-12
Ob7KOH L2 80	621 mV	1.5E-3	4.68E-8	7.5E-13
Ob 8KOH L1 80	601 mV	1.5E-3	9.18E-8	1.45E-12
Ob 8KOH L2 80	608mV	3.5E-4	9.88E-8	1.01E-12
Ob13 KOH Line a 80	614 mV	1.08E-3	6.28E-8	1.03 E-12
Ob13KOH line b 80	575 mV	4.18E-3	1.08E-7	6.07 E-12
Ob14 KOH line a 80	602 mV	4.08E-3	7.68E-7	1.45E-12
Ob14 KOH line b 80	610 mV	3.08E-3	7.68E-8	1.05E-12

L1: laser 1, L2 laser 2. (Laser 1 has more number of laser scribed grooves than laser 2).

After metallization, cells were evaluated by measuring Sun-Voc, in order to extract diode and electrical parameters of solar cells (Joe, Joz and Gsh) as well as open circuit voltage. From these measured we have found that after Al-deposition, emitter saturation current density (Joe) increased and we have Joe values ranging 6.7E-13 to 3.1E-12A/cm^2 and shunt conductance which were ranging from 2E-4 to 3.5E-3 ohm.cm^2 for p-type wafers. We have measured maximum Sun-Voc around 624 mV for p-type high resistivity wafers. It was theoretically expected 645mV from Joe 6.4 E-13 A/cm^2. Although emitter quality of selective emitters is affected by chemical treatment, which we have observed after lifetime measurements of selective emitters, we have found reduction in lifetime, what we had measured after SiNx layer deposition but lifetime is maintained under homogenous softly doped area. Destruction of lifetime is reduced when we have used teflon bath for chemical treatment. NaOH or KOH is used to remove laser damages prior to second P diffusion. By using KOH, reduction in lifetime is minor than NaOH.

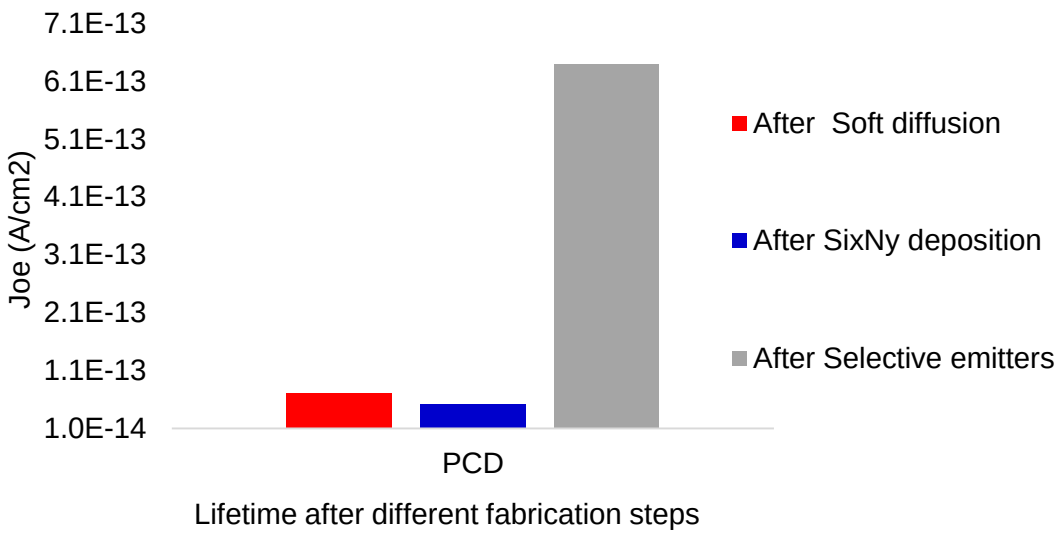


Figure 5.46 Effect of selective emitters on Joe before and after selective emitter formation

Emitter's saturation current density (Joe) which we have obtained after aluminum deposition is highly increased, it limits the open circuit voltage. This Joe value is due to Al-BSF (rear emitters). We have to optimize metallization process in order to measure real Joe of P/Al solar cells.

5.11 Aluminum optimization and Al-BSF

The purpose of Al-optimization is to optimize the temperature and speed of belt furnace to develop Al-BSF for fabrication of industrial thin films solar cells.

After 2nd phosphorus diffusion (for selective emitter formation), a layer aluminum was deposited on few wafers by EBM (by evaporation) in order to provide a uniform area on backside of the wafer by Al-deposition. After this process, we have 2 kind of wafers, some wafers have Al-layer on backside and some wafers do not have Al on backside prior to deposition of Al paste by screen printing. Wafers were cut manually by pressing at corner of wafers, which was already marked by laser for cutting in order to separate cells. In this way, we have isolated cells from wafer just pressing cells area manually on the wafer surface. It is not a recommend technique to isolate cells from processed wafers. A thick layer of aluminum was deposited on backside of cells by screen printing technique in order create back surface field as well as back contact. For this purpose we have used Al paste (Al-5540 a commercially available Al paste supplied by Ferro electronics material) which was dried at 350ºC and was fired at different temperature from 875 to 950 ºC and at different speed of belt of furnace from 60 to 90 inches/minute.

Screen printed alumiunum deposition on backside to create a Al-BSF is common technique used for back surface passivation as well as to create back contacts. Formation of Al-BSF by screen printing technique is two steps process, first deposition of Al-paste on back surface by screen printing, second a short time drying and annealing above the Al-Si eutectic temperature. Drying of A-paste is usually carried out at 300ºC to 350ºC and firing is performed at rapid thermal annealling temperature from 875ºC to 950ºC for short period of time (2.45 minutes). At high temperature Si is dissolve into Al-Si alloy melt. At cooling, silicon is rejected from melt and regrow on surface as an Al-doped or p+ BSF layer. Detail of this

step is also explained in chapter 3. In thin film solar cell when thickness of wafers decreases, back surface field (BSF) becomes more important in order to decrease the back surface recombination velocity and to increase the collection efficiency [52-58].

In order to optimize Al deposition for industrial solar cell fabrications, we have taken three different kind of wafers. All the wafers were processed till second P diffusion, as shown in figures (scheme for fabrication of selective emitters for P-type wafers and N-type wafers). In first process, oxide layer of rear n+ emitters was removed by HF treatment, and it is carried out manually as shown in figure 5.47.

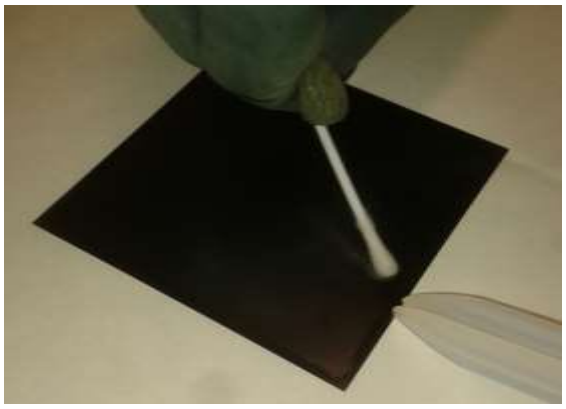


Figure 5.47 Selective manual process used to remove rear oxide (by protecting the front surface).

In second process, both silicon oxide as well as rear emitters were removed by selecting etching (HF treatment on rear side and NaOH etching) process prior to Al-deposition. SiNx layer on front side protects the emitters from NaOH etching. And in third process, Al layer was deposited on rear side of wafer containing silicon oxides layer and n+ emitter underneath Al-layer, this is deposited by EBM (evaporation). Aluminum paste which was deposited on backside of all cells, were dried at 350ºC at 72 inches/minutes for 1.5 minutes but firing was carried at different temperature ranging from 875ºC to 925ºC for 2.15 to 3 minutes. [52-58]. For Al-optimization we have used both P-type (high resistivity) and N-type (low resistivity). Structure of wafers which is shown in figure 5.48, represents wafers are ready for Al-deposition.

Figure 5.48 Different rear structures of solar cells used for Al-optimization process.

Characterization of Al-optimization was carried out by measuring Sun-Voc, Matrix has been made in order to see the the effect of temperature, speed of belt furnace and quality of back surface field on open circuit voltage and cell performance. Thickness of BSF is

measured by microscopic studies by focussing at top of surface as well as base of surface. From Sun-Voc we can extract all solar cell parameters Joe, Joz Gsh and series resistance even lifetime of bulk, which are used to characterize the performance of solar cell.

Suns-Voc curve allows us to characterize lifetime of minority's carriers and its analysis also provides detailed information on the internal components of recombination in the solar cell. Sun-Voc measurements provide information of IV curves without the effect of series resistance of diode. Fitting of Sun-Voc curve is easier than illuminated curve since there is no dark current or series resistance. [50-51]. Detail of measurement of Sun-Voc and characterization process is given in chapter 3. Solar cells parameters which are extracted from Sun-Voc curves are given above. Sun-Voc values which are obtained after metallization are given in table 5.15

Table 5.16 Matrix for Al optimization (Al-BSF) (P-type wafers)

Belt speed	Rear structure of S. emtters	**Sun-Voc (mV)**		
		875 ºC	900 ºC	925 ºC
60 inches/min.	Al-BSF with SiO_2 (HF free)	422 569	573 583	568 584
	Al-BSF with Si (HF treatment)	562	567	595 576
70 inches/min.	Al-BSF with SiO_2 (HF free)	568	568 544	559 566
	Al-BSF with Si (HF treatment)	547 567	583 555	565
80 inches/min.	Al-BSF with SiO_2		601	614
60 inches/min	Al-BSF with Si		580 574	584
	Al-BSF with Si (double layer of Al)			575
	Al-BSF with SiO_2 (Double layer of Al)		590	
	Al-BSF with Si		564	568
	Al-BSF with Si (double layer of Al)		558	558
80 inches/min.	Al-BSF with SiO_2		614	623 601
	Al-BSF with SiO_2		614	624

In this both case, SiO_2 and Si have rear n+ emitters prior to Al-deposition.

After second P diffusion, a layer aluminum was deposited on few wafers by EBM (by evaporation) in order to provide a uniform area on backside of the wafer by Al-deposition. we have 2 kind of wafers, some wafers have Al-layer on backside and some wafers do not have Al on backside prior to deposition of Al paste by screen printing. In case of SiO_2, rear surface has oxide layer with n+ emitters on rear surface, prior to Al-deposition. In case of Si, surface has base doping (rear n+ emitter was removed). In case of double layer, first layer is deposited by EBM and second layer is deposited by screen printing technique.

From these results, it is concluded that maximum Sun-Voc can be obtained by depositing Al-layer on silicon oxide surface (Al- BSF with SiO_2) for high resistivity p-type wafers. However there is not a big difference in sun-voc values obtained from Al-BSF having oxide free surface or surface with base doping. Variation in emitter saturation current density is not very high for n-type wafers. Although we have low sun-Voc values due high shunt conductance, theoretically we have calculated around 650 mV from emitter saturation current density 0.67 E-12 A/cm^2, which we have obtained after Al-optimization.

$$V_{oc} = \frac{kT}{q} \ln \left[\frac{nN_A}{n_i^2} \right] \quad = 650 \text{ mV}$$

"n" is minority carriers concentration at junction edge, n_i is intrinsic carrier concentration (9E9/cm^3) at 25 ºC. N_A is base doping of wafer and $\frac{kT}{q}$ is thermal voltage.

$$J_{SC} = J_0 \exp \left[\frac{qV_{OC}}{mkT} \right] \quad = 40\text{mA}$$

J_{SC} is short circuit current.

Optimal temperature for Al-deposition firing is 925 ºC at 60inches/min belt furnace speed for good firing and p+ BSF formation. In addition to this rear structure with SiO_2 surface (structure of figure 5.48(1)) of selective emitters have given the maximum voltage and good emitters saturation current density values than selective emitters with rear P emitter free surface. Emitter's saturation current density (Joe) which we have obtained after aluminum deposition is highly increased, it limits the open circuit voltage. This Joe value is due to Al-BSF (rear emitters). We have to optimize metallization process in order to measure real Joe of P/Al solar cells.

5.12 Conclusion:

In this work, we have developed a new recipe for passivation of emitters. A large of number of experiments were performed in order to find the optimal points for passivation by changing flow of nitrogen and silane under different condition of time and temperature. SiNx deposition was carried out by PECVD technique on CPX etched n-type low resistivity (0.5-2Ω.cm) wafers in order to find the optimal point for passivation.

Optimization experiments which we have performed to deposit SiNx layer by changing nitrogen to silane (N_2/SiH_4) ratio were ranging from 16 to 99 for stoichiometric layer at temperature 300-400 ºC under variable time 3 to 24 minutes. At this moment, variation in thickness of SiNx layer was not important but we tried to have more or less 80-90nm by changing the time of plasma deposition to get Blue color of SiNx layer. The bulk lifetime of n-type wafers were determined by using thickness variation methods as described by Eades, which was about 200 µs. The best values of lifetime measurements which we have found on 145 µm thick n-type wafer was around 22 µs by PCD technique which corresponding to 310cm/s effective surface recombination velocity (SRV). The gaseous flows which gave the best results are from 29(N_2=261, SiH_4=9) to 31.6(N_2=285, SiH_4=9) ratio of N_2/SiH_4 at 400 ºC. This optimal point of new recipe was applied for emitter's passivation through SiNx deposition on both n-type and p-type silicon wafers. This recipe does not give good results of passivation, if emitter's surface is free from oxide layer (wafers were cleaned with HF prior to

SiNx deposition), however the best results were obtained on stack structure SiO_2/SiNx and SiNx deposition time was 3.15minutes on emitter surface with silicon oxide layer.

The maximum lifetime which we measured on stack structure SiO_2/SiNx for passivated emitter was 334 µs by PCD technique and 780 µs by QSSPC technique of high resistivity (3 - 5.4Ω.cm) p-type wafers which corresponds to an effective SRV10 cm/s for QSSPC technique and 24cm/s by PCD technique for p-type wafers. In case of N-type wafers, the maximum lifetime on stack structure SiO_2/SiNx for passivated emitter was 1263µs by PCD technique and 2209 µs by QSSPC technique on low resistivity (0.8-3Ω.cm) wafers which corresponds to an effective SRV 3.8 cm/s for QSSPC technique and 15cm/s by PCD technique. Average lifetime of stack structure SiO_2/SiNx on n-type low resistivity wafers were around 530-702 µs by PCD technique and 850-1250 µs by QSSPC technique, when SiNx was deposited only on front surface. Emitter's saturation current density (Joe) further decrease due to passivation effect of SiNx, which were around 5E-14 to 2.3E-14 for p-types wafers.

In case of softly(lowly) doped emitters (sheet resistance 90-150 Ω/sq), it is difficult to make contacts between front metal and softly doped emitters, as a result contact resistivity increases which affects negatively on efficiency of solar cell. Today in industrial fabrication, there is a compromise between doping concentration of emitters and performance (moderate sheet resistance 50-80 Ω/sq) which has sufficiently low contact resistance in order to get good efficiency [29]. This compromise can be overcome by fabrication of selective emitter. Selective emitters have high doping concentration under metal contacts grid and low doping concentration under illumination area. Selective emitter fabrication helps to reduce contacts resistance as well as lower Auger and SRH recombination and improve the open circuit voltage. After passivation of homogeneous emitters, for selective emitter's formation we have used laser as a tool to scribe on wafers in specified manner to draw superficial grooves till 2-5 µm in depth and 25-30 µm in width, on cell area of $4.2 \times 3.2\ cm^2$. Damages of laser were removed by alkaline selective etching, by protecting backside as well as emitters under SiNx layer. Second P diffusion was carried out at 875 ºC for 30 minutes under same gaseous flow as for standard process. After this diffusion, we have two areas on front surface with different doping concentrations, the process which is used to fabricate emitters with different concentrations are called selective emitters formation.

After Isolation of cells from wafer, a thick layer of aluminum was deposited on backside of cells by screen printing technique in order create back surface field (BSF) as well as back contact. During this step, optimization of Al deposition for industrial solar cell fabrication was carried out on three different of kind of rear surface structures(rear emitters free surface (surface with base doping), emitters with oxidize layer and oxide layer free rear emitter) having similar front surfaces. Aluminum paste which was deposited on backside of all cells, were dried at 350ºC at 70 inches/minutes for 2.5 minutes but firing was carried at different temperature ranging from 875ºC to 925ºC for 2.15 to 3 minutes. Optimal temperature for Al-deposition is 925 ºC at 60inches/min belt furnace speed for good firing and p+ BSF effect formation with rear emitter with silicon oxide (SiO_2) has low emitters saturation current density was observed after Al deposition and firing. Although Joe (emitter saturation current density) it was high values what we had after homogenous emitter's formation. The best values which we had obtained on n-type wafers around 6.8E-13 A/cm^2 and 6.4 E-13 A/cm^2 for p-type wafers.

After back contacts formation, we have measured Sun-Voc of cells to get electrical parameters of solar cells, we have found that emitter saturation current density (Joe) of cells increased which were in range from 6.45E-13 to 3.1E-12A/cm^2 and shunt conductance was

in range from 2E-4 to 3.5E-3 ohm.cm^2. This Joe is due to rear emitters (Al-BSF), we have to optimize some parameters for appropriate metallization such as metallization paste in order to measure the real low Joe of the cells. Quality of selective emitters is affected by chemical treatment, this phenomena was observed after lifetime measurements of selective emitters, we have found reduction in lifetime, what we had measured after SiNx layer deposition but lifetime is maintained under homogenous softly doped area. Destruction of lifetime is reduced when we have used teflon bath for chemical treatment. NaOH or KOH is used to remove laser damages prior to 2nd P diffusion. By using KOH, reduction in lifetime is minor than NaOH.

We have measured maximum Sun-Voc around 624 mV for p-type high resistivity wafers and 626mV for low resistivity n-type wafers. Final behavior of P/Al solar cell is due to Al-BSF, it can be further improved and theoretically expected Sun-Voc is around 650 mV. Process which is used to fabricate selective emitter is feasible to apply for industrial fabrication of P/Al silicon solar cells with selective emitters with expected efficiency around 20%.

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Chapter 6

6 Conclusion and future plan

6.1 Conclusion:

The objective of this research work was to increase competitiveness of photovoltaics by improving the technology for high efficiency process and to decrease cost.

High efficiency P/Al technology was developed in the mid of 1980s by theoretical and experimental studies of A. Cuevas and M. Balbuena at IES-UPM. They have concluded that it is possible to obtain high efficiency with softly doped deep phosphorus emitters and aluminum back surface field, P/Al (P emitters- Al BSF). They have obtained efficiency above 19% by using high quality FZ monocrystalline silicon wafers. In fact when P/Al technology was described at that time, efficiency achievement was remarkable and among the best silicon solar efficiency reported in the world. The main objective of this work was to improve high efficiency P/Al technology by using low grade silicon thin wafers for solar cells for industrial application.

Fabrication process is started from chemical etching and texturing of P-type monocrystalline (Cz) wafers with resistivity 0.5-2 Ω.cm and thickness 160µm. Phosphorus pre-deposition was carried out at 825 ^{0}C by using $POCl_3$ as a source of phosphorus and nitrogen as a carrier gas in tube furnace. 1µm thick layer of Al is deposited on backside of wafers by electron beam machine (EBM), diffused in quartz furnace simultaneously with phosphorus for 3 hours at 1050ºC in nitrogen ambient. Diffusion profile of P has been made to get doping concentration which is around $1 \times E19\ cm^{-3}$ with junction depth 1.05µm. Doping profile of Al is made, which represents the doping concentration of Al in Si is around $1 \times E19\ cm^{-3}$ with junction depth around 3.5 µm on rear side of wafers. Simultaneous drive-in of P and Al in P/Al technology resulted a n^+pp^+ structure. Silicon nitride layer is deposited by PECVD on front side of wafers in order to achieve passivation, this layer also acts as an antireflection layer. Fronts contacts are defined by evaporation of metals (Ti/Pd/Ag) by EBM by using photolithographic technique and for back contacts, layers of Al/Ag are also deposited by using EMB100/150nm thick respectively on backside of wafer. Final structure of P/Al technology (n^+pp^+) was annealed at low temperature in a forming gas atmosphere in order to produce a good alloy between different metals which reduces series resistance and recover the damages produced by EBM. By applying P/Al technology, we have fabricated 2 different batches of $n^+p\,p^+$ (P/Al) solar cells, their characterization were carried out by Sun-Voc and lifetime measurements during fabrication steps and IV characteristics were measured under dark and illumination at the end of fabrication process.

The best results which we have obtained in batch 1 has efficiency around 14.75% with open circuit voltage around 603mV, short circuit current 37mA/cm^2. Although shunt conductance is high but still we have a good efficiency. In this batch emitters are poorly passivated, we have observed high emitter saturation current density which limit the open circuit voltage and efficiency of solar cell. While in second batch, the maximum efficiency which we have obtained was around 16.5% with open circuit voltage 600mV and Sun-Voc

around 605mV with short circuit current 39mA/cm^2. Fill factor is low due to series resistance which is around 70. IV curves data of all batches are further processed by using Multiv fitting program in order to extract all information of diodes and electrical parameters of solar cell (Joe, Joz Gsh and Rs). Sun-Voc measurements also provided information of diode parameters of solar cell (Joe, Joz and Gsh) without the effect of series resistance. From PC1D simulations, it is clear that it is possible to get efficiency around 19% by P/Al technology. Simulations results are given in chapter 3 (PC1D simulations).

In fabrication process of P/Al silicon solar cells we have obtained emitter saturation current density for worse emitters are in range of 1E-11A/cm^2 and good emitters is around 5E-13 A/cm^2. The quality of emitters play important role in the performance of silicon solar cells. Passivation quality of emitters depends on diffusion temperature with flow of gases and doping time. At high temperature, concentration of phosphorus (P) exceed the solubility in Si (10^{21}/cm^3) which form a dead layer which is electrically inactive and has effect on surface P concentration and junction depth. Moreover high surface P concentration reduced the passivation effect which lowers the open circuit voltage (Voc) and overall solar cell efficiency. It is observed that at high temperature, phosphorus is precipitated in the form of dead layer due over solid solubility limit. Due to over solubility limit, P appears as in the form of dead layer, an electrically inactive layer of P. This electrically inactive P also introduces defects in the crystalline lattice of silicon, as a result Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure. High concentration of soluble P in Si increases the Auger recombination. These two types of recombination increase saturation current density (Joe), as a result cell *Voc* and *Jsc* decrease due to high recombination rate.

There are some technological steps, involve in fabrication process which are source of impurities are almost inevitable. Those are identified as transitions metals which are common source of contaminating impurities. These contaminating impurities have negative impact on the lifetime of minority's carries which supposed to degrade the performance or efficiency of solar cells. There are two strategies which are pursued in complementary form to alleviate effect of contaminations. On one hand high cleanliness of process including wafer cleaning after etching and texturing process by RCA1&2 cleaning and second cleaning by integrating gettering process by P or Al during diffusion process. These two processes are used to reduce the concentration of contaminating impurities of active area of the device.

There are various techniques which are used to characterize the impurities, some of them are used to measure the concentration of impurities and some of them are used to measure its effects. In particular lifetime measurement techniques by photoconductivity decay which in term of surface passivation is used to measure impact of impurities on surface and in the bulk are reliable measurement techniques. We have measured lifetime of P/Al solar cell structure after each thermal step. Due to high temperature and impurities, lifetime was destroyed. After diffusion and P/Al drive-in process, we tried to measure lifetime but it was difficult to measure due to low values. After SixNy deposited by PECVD, which is used to passivate the surface, we had measured lifetime of solar cells around 20µs by PCD (transient photo-conductance decay) and 40 µs By QSSPC technique (quasi steady state photo-conductance decay). In this P/Al fabrication process, we did not observe improvement in of lifetime after Al-gettering step during drive-in. Although some researchers have observed improvement in lifetime after gettering by P/Al but they have used FZ wafers in fabrication process. In some cases improvement in lifetime was observed, when they used

phosphorus pre-gettering or pre-oxidation step prior to fabrication on Cz or multicrystalline material. According to theoretical knowledge, lifetime of the silicon wafers should be improved due to gettering step by aluminum. The gettering effect is due to solubility of metallic impurities, which is higher in liquid aluminum silicon (Al-Si) due to high temperature as compare to solid silicon. This may be because most of the impurities present in the substrate are trapped in crystal defects (dislocations and grain boundaries) or to occupy substitutional positions within the network, which makes difficult its removal by aluminum.

Low quality emitters produce the recombination centers due poor passivation which decrease the lifetime of the solar cell, as a result effective surface recombination velocity increased. In P/Al silicon solar cell fabrication process we have calculated effective surface recombination velocity around 500cm/s. PC1D simulation showed that efficiency of silicon solar cells is higher at low surface recombination rate. Higher surface recombination velocity decrease the efficiency. Efficiency of P/Al structure will be around 19%, if we will have passivated emitters as shown by PC1D simulations.

Due to low solar cell efficiency than expected, poor quality of emitter's passivation, we have planned to investigate P diffusion deeply in order to get softly doped and deep emitters along with passivation by deposition of plasma layer (SiNx) in detail in order to get fully passivated emitters.

The quality of the emitter plays an important role for solar cell efficiency due to formation of P-N junction, which is the core of the crystalline silicon (c-Si) solar cell. If the P surface concentration is high and exceeds the intrinsic charge-carrier concentration, have certain special features on electrical properties and conductivity. The quality of emitters depends on diffusion temperature with flow of gases and doping time. At high temperature, concentration of phosphorus (P) exceed the solubility in Si ($10^{21}/cm^3$) which form a dead layer, which is electrically inactive and has effect on surface P concentration and junction depth. Due to over solubility limit, P appears as in the form of dead layer, an electrically inactive layer of P. This electrically inactive P also introduces defects in the crystalline lattice of silicon, as a result Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure. High concentration of soluble P in Si increases the Auger recombination, which limits the lifetime and lowers the open circuit voltage (*Voc*) with overall solar cell efficiency. Due to high P doping concentration, bandgap narrowing effect arises, which cause the absorption of photons in emitters region near the front surface. In addition to this, electrically inactive P also introduces defects in the crystalline lattice of silicon, Shockley Read Hall (SRH) recombination appears due to defects in crystalline structure and also take part in efficiency loss due to high recombination (low lifetime). The amount of inactive phosphorus in term of surface concentration and depth junction can be improved by converting electrically inactive phosphorus into electrically active phosphorus by introducing a wet oxidation with drive in step after diffusion. When the extent of dead layer (electrically inactive) decrease emitter recombination probabilities also decrease which improves open circuit voltage (*Voc*), short circuit current density (*Jsc*) and efficiency of solar cell. In this work, during P diffusion, we have performed several experiments in order to study the effect of phosphorus diffusion on quality of emitters at different temperature (800, 820,840 and 875 ^{0}C) with different conditions of wet oxidation and drive-in to get shallow and deep n+ emitters. Profile of P diffusion for different temperature is shown in figure 6.1. Concentration profile of phosphorus is determined by alkaline etching at 60^{0}C by using low conc. of NaOH (2%) to find the junction depth and doping concentration is determined by PCID simulation by using sheet resistance data.

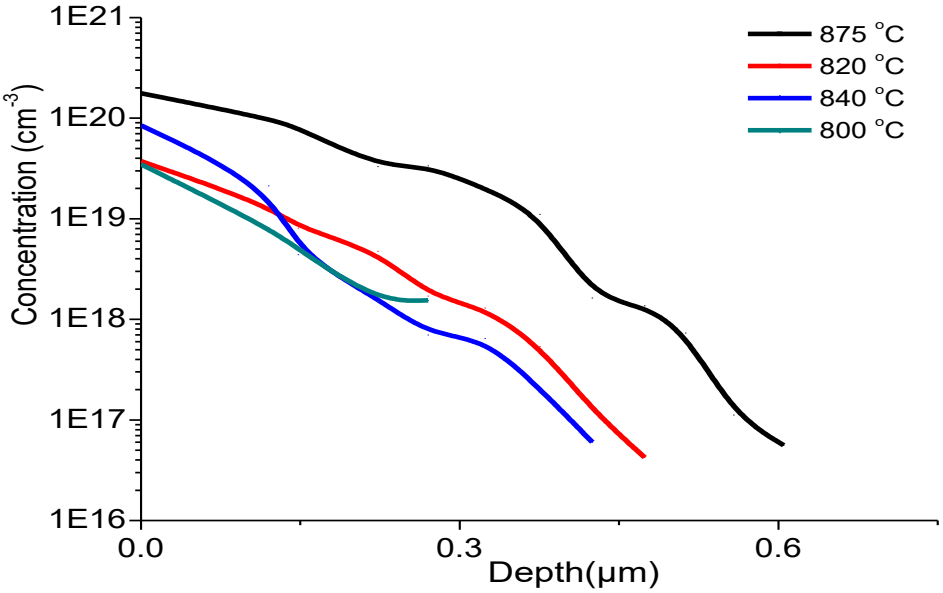


Figure 6.1 Phosphorus Diffusion profiles at different temperature.

Sheet resistance data shows a non-uniformity of the P distribution at low temperature. It is observed that increase of P pre-deposition temperature, increase the surface concentration (N_S) and makes the P distribution more uniform. But at high temperature, phosphorus precipitated in the form of dead layer due to over solubility limit. Due to this layer recombination centers appear, as a result SRH recombination increase. These recombination centers increase emitter's saturation current density, as a result *Voc* and *Jsc* decrease due to high recombination rate. At low temperature P diffusion, about 90-95% P is active but at high temperature around 60% P is electrically active. The percentage of active P is calculated By Tsai Model. Our results show that with increase of temperature, active P concentration decrease and vice versa. However we have introduced a wet oxidation step with drive in. it converts electrically inactive P into active P and decrease the recombination and improve surface quality for passivation. We have found a very thin surface region in which the surface concentration (N) may reach nearly 10^{20} atom/cc. However, this region is no more than 50-100 nm deep. Moreover PN junction depth can be control by drive in time but it also depends on pre-deposition condition (temperature, dopant and oxygen ratio). Low level of oxygen increases the junction depth in P pre-deposition. To get high efficiency and improve *Voc*, it is necessary to minimize the electrically inactive P in emitters. Our approach is removal of oxides grown during P pre-deposition by HF treatment, which remove the dead layer. Next step is wet oxidation with drive-in which forces the precipitated P to diffuse into silicon.

By using PC1D simulation, we have simulated doping concentration of phosphorus diffusion data to predict efficiency of silicon solar cell. Results shows that moderate or softy (lowly) doped emitters give high efficiency. Due to this reason, we have planned to investigate low temperature diffusion for softly or moderate doped and deep emitters for silicon solar cell fabrication process to gain high efficiency. The results which we have obtained at 800 ºC is not uniform as compare to 820 ºC, we preferred to proceed P diffusion at 820 ºC as a standard process. In addition to this, doping concentration of P at 820 ºC is

95% electrically active as compare to high temperature diffusion. Due to this reason, there is less probability to have recombination centers due to electrically inactive phosphorus.

One of our goal of this work was to make a single step diffusion process in a furnace. We have conducted some experiments in order to achieve single step diffusion process for industrial solar cell fabrication. Prior to this experiment, we have investigated the effect of dry oxidation and HF free process to compare with wet oxidation. Our single step diffusions process was started from pre-deposition step at 820 ºC followed by 20 minutes of dry oxidation with 70 minutes of drive-in at 950 ºC. It has been observed that charges trapped in the oxide are very few, but the junction is deeper. A deeper junction gives the chance of having less recombination centers in emitters. Reliability of emitter is evaluated by the influence of passivation. For each emitter surface conditions, surface recombination velocities have been simulated by PC1D. Results corresponding to a conventional 0.2 µm and current 0.7 µm shows that deep emitters junction depth give low values of emitter saturation current density (Joe) as compare to conventional junction depth. The influence of a good surface passivation for softly doped and deep emitters with moderate sheet resistances, is ranging from 58 to 130 fA/cm^2. Emitters obtained by a single thermal step are in range of 7-8 x10^{19} cm^{-3} with sheet resistance ~60 Ω/□ and junction depth 0.71 µm and saturation current of emitter is 130 fA/cm^2. In addition to passivation, gettering effect in this single step diffusion process (Proposed process) is much higher than conventional process.

We have applied our single step diffusion standard process for fabrication of emitters on both types of substrates (N-type and P-type wafers). In both cases wafers were etched by CPX (acidic etching) and cleaned by RCA1&2 prior to P diffusion and drive-in. After processing, we have measured lifetime by using PCD and QSSPC techniques. In case of P-type material, we have measured lifetime around 201 µs by PCD technique and 282 µs by QSSPC technique of high resistivity (5.4Ω.cm) wafers. Process is repeated many times in order to check the reproducibility, average lifetime of this single step diffusion process on high resistivity p-type wafers were in range of 130 to150 µs by PCD technique and 200-300 µs by QSSPC technique. In case of N-type wafers, we have measured maximum values around 509 µs by PCD technique and 2029 µs by QSSPC technique on low resistivity (0.8-3Ω.cm) wafers. Average lifetime of this single step diffusion process on N-type low resistivity wafers were in range of 250-350 µs by PCD technique and 500-800 µs by QSSPC technique on planar structures. Emitter's saturation current density of were around 9E-14 to 7E-14 for p-types wafers concluded by teffsim adjustments. In addition to passivation, gettering effect in this single step diffusion process is much higher than conventional process. Getterging effect is evaluated by liftime measuremts. In case of metalligical grade silicon wafers, by our proposed process (single step diffusion), improvement in lifetime is 3 times higher than conventional process. In case of P-type material, we have measured lifetime around 200 µs at high resistivity (5.4Ω.cm) wafers and on N-type low resistivity (0.8 Ω.cm) wafers around 505 µs by PCD technique. Improvement in lifetime is much higher than conventional gettering processes.

Further passivation quality of emitters were improved by deposition of silicon nitride layer (SiNx). SiNx is an excellent material due to its dual properties of passivation as well as ARC (anti-reflection coating) for high efficiency solar cells. In this work, we have developed a new recipe for passivation of emitters. A large number of experiments were performed in order to find the optimal points of passivation by changing flow of nitrogen and silane under different condition of time and temperature. SiNx deposition was carried out by PECVD technique on CPX etched n-type low resistivity (0.5-2Ω.cm) wafers. Optimization experiments which we have performed to deposit SiNx layer by changing nitrogen to silane (N_2/SiH_4) ratio ranging

from 16 to 99 for stoichiometric layer at temperature 300-400 ºC. At this moment, variation in thickness of SiNx layer was not important but we tried to have more or less 80-90nm by changing the time of plasma deposition to get blue color of SiNx layer. The bulk lifetime of n-type wafers were determined by using thickness variation methods as described by Eades, was around 200 µs. The best values of lifetime measurements which we have found on 145 µm thick n-type wafer was around 22 µs which corresponding to 310cm/s effective surface recombination velocity (SRV). The gaseous flow which gave the best results is from 29(N_2=261, SiH_4=9) to 31.6(N_2=285, SiH_4=9) ratio of N_2/SiH_4 at 400 ºC. This optimal point of new recipe was applied for emitter's passivation through SiNx deposition on both n-type and p-type silicon wafers. This recipe does not give good results of passivation, if emitters surface is free from oxide layer (surface were treatment with HF prior to SiNx deposition), however the best results were obtained on stack structure SiO_2/SiNx.

The maximum lifetime which we measured on stack structure SiO_2/SiNx for passivated emitter was 334 µs by PCD technique and 780 µs by QSSPC technique of high resistivity (5.4Ω.cm) p-type wafers which corresponds to an effective SRV10 cm/s for QSSPC technique and 24cm/s by PCD technique for p-type wafers. In case of N-type wafers, the maximum lifetime on stack structure SiO_2/SiNx for passivated emitter was 1263µs by PCD technique and 2209 µs by QSSPC technique on low resistivity (0.8-3Ω.cm) wafers which corresponds to an effective SRV 3.8 cm/s for QSSPC technique and 15cm/s by PCD. Average lifetime of stack structure SiO_2/SiNx on n-type low resistivity wafers were around 530-702 µs by PCD technique and 850-1250 µs by QSSPC technique and SiNx was deposited only on front surface. Emitter's saturation current density (Joe) further decreased due to passivation effect of SiNx, which were around 5E-14 to 3.0E-14 for p-types wafers.

In case of softly(lowly) doped emitters (sheet resistance 90-150 Ω/sq), it is difficult to make contacts between front metal and softly doped emitters, as a result contact resistivity increased which affect negatively on efficiency of solar cell. Today in industrial fabrication, there is a compromise between doping concentration of emitters and performance (moderate sheet resistance 50-80 Ω/sq) which has sufficiently low contact resistance in order to get good efficiency. This compromise can be overcome by fabrication of selective emitters. Selective emitter have high doping concentration under metal contacts grid and low doping concentration under illumination area. Selective emitter fabrication helps to reduce contacts resistance as well as lower Auger and SRH recombination and improve the open circuit voltage. For selective emitter's formation, we have used laser as a tool to scribe on wafers in specified manner to draw superficial grooves till 2-5 µm in depth and 25-30 µm in width, on cell area of $4.2 \times 3.2\ cm^2$. Damages of laser were removed by alkaline selective etching, by protecting backside as well as emitters under SiNx layer. Second P diffusion was carried out at 875 ºC for 30 minutes under same gaseous flow as for standard process. We have two areas on front surface with different doping concentrations, the process which is used to fabricate emitters with different concentrations are called selective emitters formation. After Isolation of cells from wafer, a thick layer of aluminum was deposited on backside of cells by screen printing technique in order create back surface field (BSF) as well as back contact. During this step, optimization of Al for industrial solar cell fabrication was carried out on three different of kind of rear surface structures (rear emitters free surface (base doped)), emitters with oxidize layer and oxide layer free rear emitter) having similar front surface. Aluminum paste which was deposited on backside of all cells, were dried at 350ºC at 72 inches/minutes for 2.5 minutes but firing was carried at different temperature ranging from 875ºC to 925ºC for 2.15 to 3 minutes. Optimal temperature for Al-deposition is 925 ºC at 60inches/min belt furnace speed for good firing and p+ BSF effect formation In this process, Al- layer deposited at rear emitter with silicon oxide (SiO_2) have the highest open

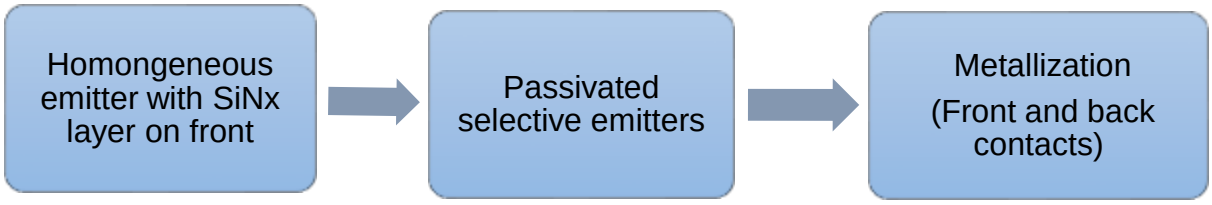
circuit voltage and lower emitter saturation current density in Al optimization process as compare to other rear structure.

After back contacts formation, we have measured Sun-Voc of cells to get electrical parameters of solar cells, we have found that emitter saturation current density (Joe) of cells increased which were in range from 6.45E-13 to 3.1E-12A/cm^2 and shunt conductance was in range from 2E-4 to 3.5E-3 ohm.cm^2. This Joe is due to rear emitters (Al-BSF), we have to optimize some parameters for appropriate metallization such as metallization paste in order to measure the real low Joe values of the cells. Quality of selective emitters is affected by chemical treatment, this phenomena was observed after lifetime measurements of selective emitters, we have found reduction in lifetime, what we had measured after SiNx layer deposition but lifetime is maintained under homogenous softly doped area. Destruction of lifetime is reduced when we have used teflon bath for chemical treatment. NaOH or KOH is used to remove laser damages prior to 2nd P diffusion. By using KOH, reduction in lifetime is minor than NaOH.

We have measured maximum Sun-Voc around 624 mV for p-type high resistivity wafers and 626mV for low resistivity n-type wafers. Final behavior of P/Al solar cell is due to Al-BSF, it can be further improved and theoretically expected is around 650 mV. Process which is used to fabricate selective emitter is feasible to apply for industrial fabrication of P/Al silicon solar cells with selective emitters with expected high efficiency.

6.2 Future Plan:

Up till now we have fabricated selective emitters via second P diffusion. In future we will focus on the passivation to get passivated selective emitters, prior to complete fabrication process of P/Al solar cells. We will further investigate passivation of selective emitters, in order to get high efficiency for industrial solar cells fabrication. There are two options to have passivated selective emitters. There is one option, we will try to maintain lifetime which we have obtained after homogeneous emitter formation, or we will try to passivate selective emitters after second phosphorus diffusion. When we will have passivated selective emitters, we will complete metallization process by screen printing. We will apply this P/Al technology for fabrication of industrial solar cells with selective emitters. Plan for fabrication is shown in flow sheet below:



The process which is mentioned above for selective emitter's formation, we will continue this process to complete fabrication of P/Al solar cell structure with selective emitters. For metallization we will use screen printing technique to create front and back metal contacts. Proposed structure of P/Al silicon solar cell with selective emitter is shown in figure 6.2.

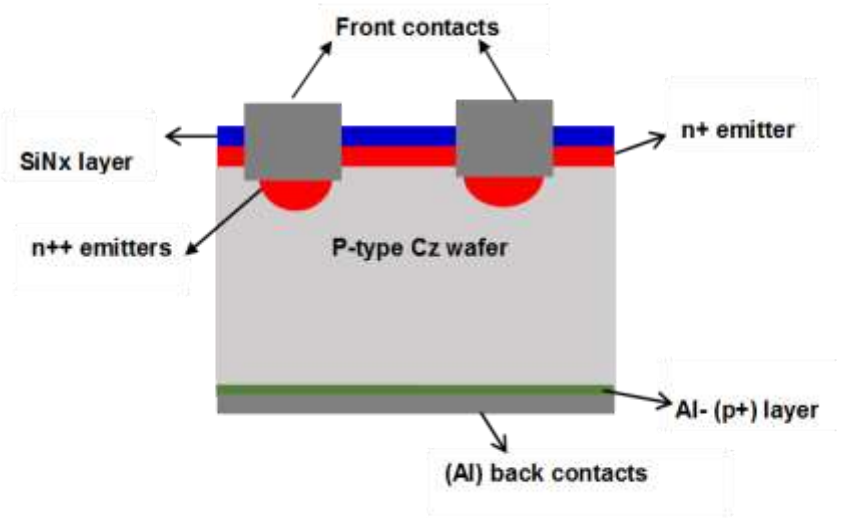


Figure 6.2 Proposed structure of P/Al solar cell with selective emitters

Selective emitters have high doping concentration under metal contacts grid and low doping concentration under illumination area (area between the metal contacts). Selective emitter fabrication process helps to reduce contacts resistance as well as lower Auger and SRH recombination and improve the open circuit voltage.

During selective emitter's formation, we have concluded that lifetime is affected seriously either due to chemical etching with high temperature second P diffusion for selective emitter's formation. Emitter saturation current density (Joe) is highly increased during fabrication process to create selectivity in emitter's area. In my opinion, there is one option to maintain passivation is by deposition of second layer of SiNx or to carry out a dry oxidation for 30 minutes at high temperature. As we are expecting to get passivated selective emitters after second phosphorus diffusion (process is shown in figure 5.35 in selective emitter formation). After passivated selective emitter's achievement, we will continue to finish fabrication process by creating front and back contacts by using screen printing an industrial technique used to create contacts.

Emitter's saturation current density (Joe) which we have obtained after aluminum deposition is highly increased, it limits the open circuit voltage. This Joe value is due to Al-BSF (rear emitters). We have to optimize metallization process in order to measure real Joe of P/Al solar cells.

As it is mentioned early we have to maintain high doping concentration underneath the front metal contacts grids for selective emitters, there is another way to maintain high doping concentration underneath front contacts grids is by spraying of H_3PO_4/P_2O_5 poly-phosphoric acid in laser scribed groove areas with drive-in process, if the technique of selective emitter formation via second P diffusion will not give desirable results. Prior to front metallization, a layer of Al (Al-BSF) will be deposited in order to measure Sun-*Voc* to extract electrical parameters of solar cells to know performance of solar cell.

Appendixes

Appendix A:

Etching characteristics of sodium hydroxide (NaOH) for silicon, silicon dioxide and silicon nitride with Arrhenius plots

Etching is micro-fabrication process which is used to remove layers from surface of a wafer by physically or chemically. The term etching is used to describe technique by which material can be uniformly removed from the surface of wafer as in case of polishing wafers or locally removed as in case of delineation of pattern for microcircuit. Every wafer under goes many etching steps before completion. In case of many steps etching, some parts of wafer surface are protected from etchant by “masking” materials which resists etching. In some cases, masking material is a photoresist, which has been pattern by using photolithography. Silicon nitride is also act as mask up to some extent in solar cell fabrication by using photolithographic technique [1]. Silicon wafer etching process is used in the fabrication of microelectronics devices or solar cells. The etching process occurs many times during wafer processing, so it is important to maintain accuracy in fabrication. The depth and shape of wafer surface can be monitored by etching time and choice of etching material.

There are two types of etching process.

- Dry etching
- Wet etching (chemical etching)

Dry etching:

In dry etching, plasma or etchant gases remove the substrate material, the removal of substrate take place either by utilizing high energy beam particle or by chemical reaction. In physical dry etching high energy particle or beam (electron, ions or photons) knock out the atoms from substrate surface. In this case no chemical reaction take place and only unmasked material is removed.

In dry chemical etching, material or surface to be etched is exposed directly to bombardment of ions (plasma of reactive gases such as fluorocarbons, oxygen, chlorine, and boron trichloride with addition of nitrogen or argon or helium) which dislodge the portion of material from exposed surface. In this process, plasma generates volatile etch products at room temperature from chemical reactions between elements of material with reactive species of plasma. Sometime plasma modifies the physical propertied of target surface. Common type of dry etching is reactive ion etching. In this thesis, we have used only wet chemical etching process.

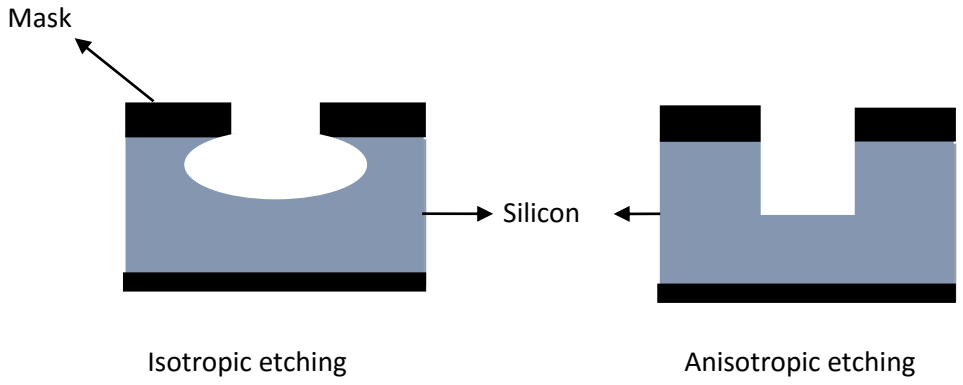
Wet etching:

Wet etching process for reducing the thickness of silicon wafers have been gaining popularity over traditional methods of thinning wafers such as physical grinding or plasma etching. Wet chemical etching process for thinning of wafers is quick, instrument free, cost effective process and widely used in industrial fabrication of solar cell. The wet chemical etching process for any material usually consist of three steps: transport of reactant to

surface of wafer, reaction at the surface of wafer and movement of reaction products into the volume of etchant solution. An etching process which is limited by rate of surface reaction usually tend to enhance surface roughness and promote faceting. Since surface reactivity is function of localized defects and crystallographic orientation. On the hand etching can be limited by rate of diffusion of etchant through a stagnant layer at the surface. This changes polished wafer into rough surface with protuberances and facets will tend to become smooth in this process.

In wet chemical etching process, etch rate can be improved by rapid stirring in order to remove reaction product and gas bubbles or it can be increased by increasing the temperature of etching solution. Typically etching rate is doubled with every increase of 10^0C of temperature. So temperature dependent etching characteristics can be used to take advantage in situations where it is necessary to keep wafer surface free from contamination.

In case of single crystal silicon material, their etching process can be either isotropic or anisotropic in character. Isotropic etching is uniform process and removes the material in all direction at same rate both in vertical and horizontal direction. While in anisotropic etching remove the material in selective direction. Anisotropic etching uses chemical that remove crystalline materials at different rate depending on density and orientation. Figure A.1, shows the isotropic and anisotropic etching process, both have different selectivity properties on different materials which leads to different wet etching processes.



Isotropic etching equally etching in all direction
Anisotropic etching higher rate in vertical than horizontal direction

Figure A.1 Isotropic and anisotropic etching

Etching chemistry relies on oxidation reaction, followed by the dissolution of oxides. This reaction represents the main process of chemical etching by which silicon material is oxidized and susceptible to dissolution. Typically wet etchants have an oxidizer to facilitate the chemical reaction, a solvent to dissolve the reaction products. Wet chemical etching is typically selective process in nature, which has advantages in processing and is simple to carry out than dry etching. The etchant can be mixed with other etching solvent or diluted with water to change the rate of the reaction, and hence the etch rate, but in most cases, wet etch processes are isotropic, removing material horizontally and vertically. Certain mixes of etchants can provide a degree of orientation of the etch direction based on the crystal orientation of the silicon that they react with.

There are two type of wet chemical etching:

- Acidic etching
- Alkaline etching

In case of acidic etching a mixture of nitric acid, hydrofluoric acid and acetic acid is used. A water solution of above three acids is typically used as an isotropic etchant. Mixture of above acids produce nitrogen peroxide (NO_2) and protons (holes) which react with silicon and produce silicon dioxide (SiO_2) which is dissolved by hydrofluoric acid. Following series of chemical reaction take place which is given below: [1]

$$H_2O \quad \rightleftarrows \quad OH^- + H^+$$

$$HNO_3 + H_2O \quad \rightarrow\rightarrow\rightarrow \quad NO_3^- + H_3O^+$$

$$Si + 2H^+ \rightarrow\rightarrow\rightarrow\rightarrow Si^{2+} + H_2 \qquad \text{(A.1)}$$

$$2Si^{2+} + 4OH^- \rightarrow\rightarrow 2Si(OH)_2 \rightarrow\rightarrow 2SiO_2 + 2H_2$$

$$SiO_2 + 6HF \rightarrow\rightarrow\rightarrow\rightarrow H_2SiF_6 + 2H_2O$$

Overall etching reaction

$$HNO_3 + Si + 6HF \rightarrow\rightarrow H_2SiF_6 + H_2O + HNO_2 + H_2$$

Etching rate of silicon depends on the concentration ratio of etchants and dilution of etchants, details of concentration ratios with dilution is given in the literature. [4-7].

Etching of silicon (Anisotropic etching)

Although etch characteristics of silicon with wet etchants are well documents, but the best results for various micromachining structure are obtained by trial and error methods. [2-3, 8-9]. Silicon is an element which belongs to metalloid family of periodic table. It is denoted by symbol Si which has atomic 14 and atomic weight 28.085. It is tetravalent element with electronic configuration $1s^2$, $2s^2$, $2p^6$, $3s^2$, $3p^2$. Electronic structure is shown in figure A.2.

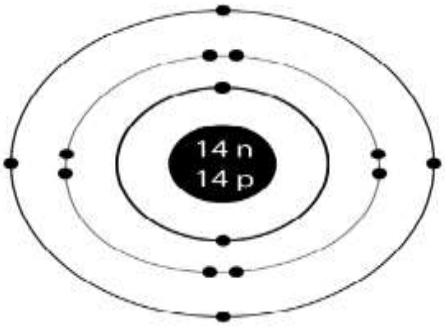


Figure A.2 Electronic structure of silicon

Silicon ingot which is obtained by Czochralski (CZ) crystal growth process can by pulled in a defined orientation (100). There is one big economic advantage of this process is that during solar cell process, we can use this crystallographic plane for homogeneous texturing with cost effective wet chemical etching process. During anisotropic etching, the surface

structure with random pyramids is built that enhance the absorption of incoming light effectively into solar cell. As a result, overall efficiency of silicon solar cell increases. Different crystallographic planes of silicon are shown in figures. A.3

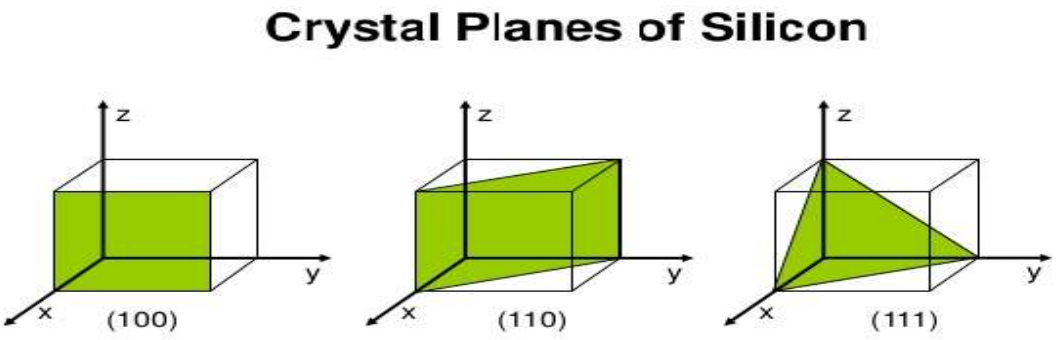


Figure A.3 Crystallographic planes of silicon

During Ingot cutting to get wafers, silicon wafers at the surface contain saw-damaged layer which is important to remove at the beginning of the process. Thickness of damage depends on techniques used for cutting of the ingot, usually 20-30 µm thickness from both sides of wafer is sufficient to get damaged free wafer. This damage is removed by chemical etching. There are many chemicals which are used for silicon etching, among them are tetra methyl ammonium hydroxide (TMAH), ethylene diamine in pyrocatechol solution, hydrazine (N_2H_4), and hydroxides of alkali metals (LiOH, NaOH, KOH, CsOH) solution. [2-3]. In chemical etching, alkaline etching is considered to be the best etching for saw-damaged wafers.

The etching rate of silicon depends on crystal planes and was determined as a function of temperature, crystal orientation and etchant concentration. A correlation was found between energy of activation and etching rate, it was observed that slowly etching crystal surface (plane) exhibiting higher energy of activation. It also observed that with increasing concentration of etchant solution, etching rate was also decreased till 40% of Alkali solution. But etching rate was decreased when concentration of alkali solution crossed the 44%. Anisotropic etching behavior of silicon by alkali solutions was described by an electrochemical model by Seidel et al. [2-3]. In oxidation step $4OH^-$ ions react with silicon atoms at surface, which injects 4 electrons into conduction band, and stay there near crystal surface due to presence of space charge layer. This reaction is accompanied by the breaking of the back bonds by thermal excitation of respective surface state electrons into the conduction band. This step of reaction is rate limiting step. In next step, injected electrons react with water to form new hydroxides ions and hydrogen. According to Seidel et al, monosilicic acid $Si(OH)_4$ is the first product of chemical reaction which is formed in all anisotropic silicon etchants. The chemical reaction and mechanism is shown in equation A.2.

$$Si + 4OH^- \rightarrow\rightarrow Si(OH)_4 + 4e^-_{cond.} \quad \text{(A.2)}$$

$$2H_2O + 4e^-_{cond.} \rightarrow\rightarrow 4OH^- + 2H_2$$

The overall reaction of anisotropic silicon etching in given below in equation A.3

$$Si + 2NaOH + 2H_2O \rightarrow\rightarrow Na_2SiO_2(OH)_2 + 2H_2 \quad \text{(A.3)}$$

Table A.1 Etching rates at different concentration of potassium hydroxide concentration in (µm/min). [10]

Crystallographic orientation	Etching Rates at different Concentration of KOH in (µm/min)		
	30%	**40%**	**50%**
(100)	0.797	0.599	0.539
(110)	1.455	1.294	0.870
(210)	1.561	1.23	0.959
(111)	0.005	0.009	0.009

Anisotropic wet etching is an important technology for fabrication of microstructure onto single crystals silicon wafers. Many studies related to etching rate have been done to control to etched shape and to gain the desire thickness of wafers. Seidel et al, [2-3] investigated etching mechanism of crystalline silicon wafers and studied concentration and temperature dependence of etching rate at different oriented planes in alkali solutions. In this work, we have investigated influence of concentration and temperature of etchant and sodium hydroxide is used as an etchant.

Sodium hydroxide (NaOH) solution preparation

NaOH solution was prepared by dissolving 1.08, 2.04, 3.00 Kg of sodium hydroxide (for 9%, 17% and 25% NaOH solution approximately) in 12 liters of de-ionized water by continuously stirring with a glass rod. Etching experiments were carried at different temperatures (45^{0}C, 61^{0}C and 90 ^{0}C) for each concentration. The solution was heated to get the desire temperature and allowed to stand for 10 minutes in order to get homogeneous temperature inside etching bath. The temperature was precisely controlled by automatic system with ± 2 ^{0}C. All experiments were performed under fuming hood.

Experimental Procedure:

In our experimental work, we have used polished single crystal silicon wafers with (100) orientation. We have taken p-type wafers with resistivity 1-1.5 ohm.cm and 102x102 mm in size and 200µm in thickness. In case of etching profile we have sodium hydroxide (Merck Germany) as an etchant. For this purpose we have prepared solution of sodium hydroxide with different concentrations (9%, 17% and 25%) and silicon etching experiments was carried at three different temperatures (45^{0}C, 61^{0}C and 90 ^{0}C). Before dipping the wafers in etching solution, thickness and weight of silicon wafers were noted. It was also made sure that wafers were clean and oxides free (native oxides was removed in HF solution followed by rinsing in de-ionized (DI) water). For better results and uniformity, wafers were places in vertically in etching bath.

Appendix A1: Etching rate of silicon

Dependence of Si (100) etching rate for different NaOH concentration at different temperature is shown in figure A1.1. Maximum etching rate was observed in all case from 2-

3.5 µm/min at 90 ^{0}C at all concentration. Etch rate increased with increasing temperature. According to literature maximum etching rate was observed near the boiling point of solution (4.5µm/min was observed for Si (100) orientation at 100 ^{0}C). Operating at higher temperature helps to remove hydrogen bubbles rapidly, since the viscosity of the etchant decrease at higher temperature, which allows the bubbles to dislodge easily from surface and increase the etching rate. Decrease in thickness was measured by instrument and also estimated by decreased in weight of wafers. [10-21]

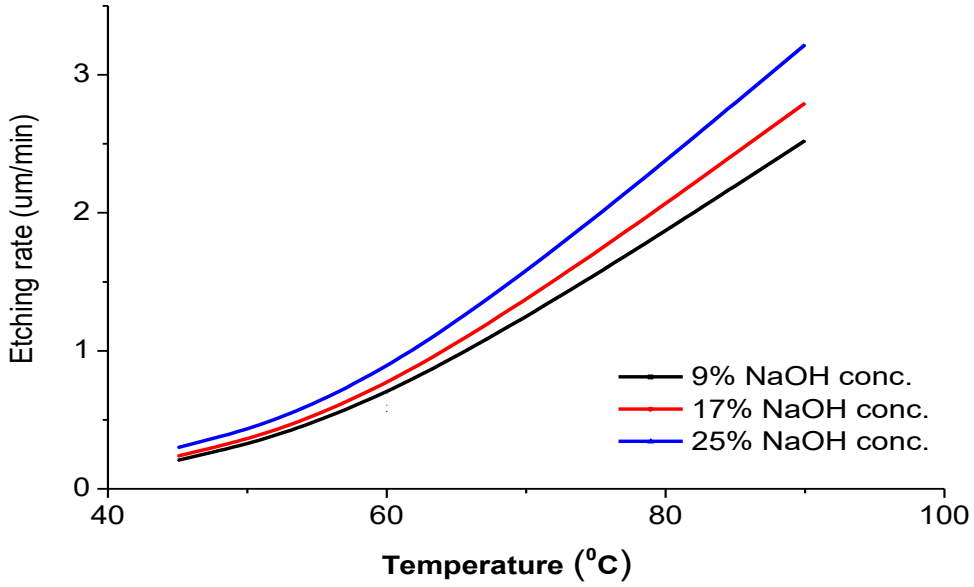


Figure A1.1 Si (100) etch rate in NaOH solution

Activation Energy

We can determine the energy of activation and pre exponential factor (R_0) by using Arrhenius equation A1.1

$$R = R_0\, Exp(-\frac{E_a}{kT}) \qquad \text{A1.1}$$

Where T in temperature in Kelvin
k is Boltzmann´s constant

Figure A1.2 shows the Arrhenius plot of etch rates of Si (100) in NaOH solution. We calculated energy of activation for pre exponential factor from Arrhenius plots.

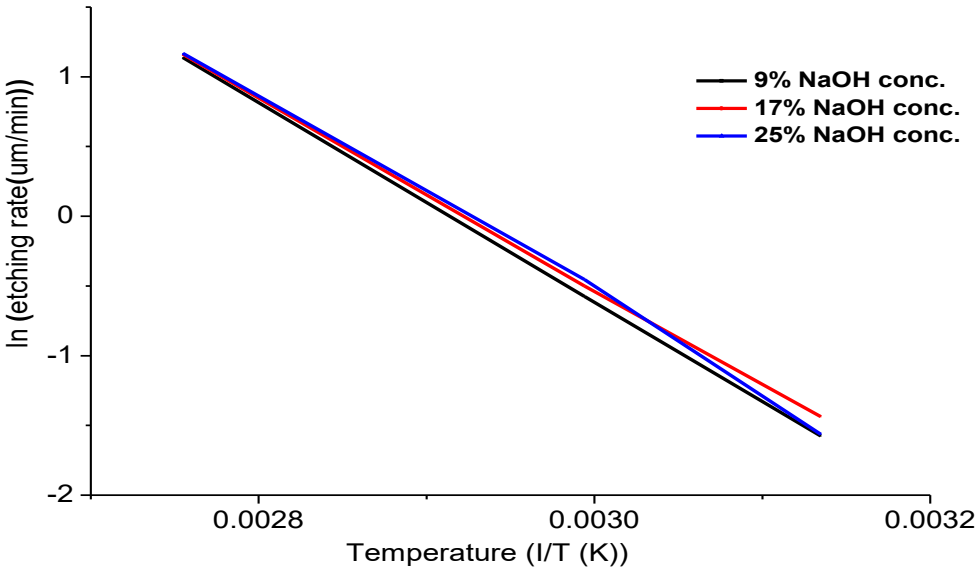


Figure A1.2 Arrhenius plot of Si (100) etch rate in NaOH solution

Activation energy of Si (100) wafer is found in this range. 0.59-0.61eV whereas pre-exponential factor is in range of 8.5×10^8 - 1×10^9 µm/min. This is almost similar which is already published in literature. [2-3]. Figure A1.3 & A1.4 shows the energy of activation and pre-exponential factor of silicon (100) calculated at different concentration of NaOH solution [10-15].

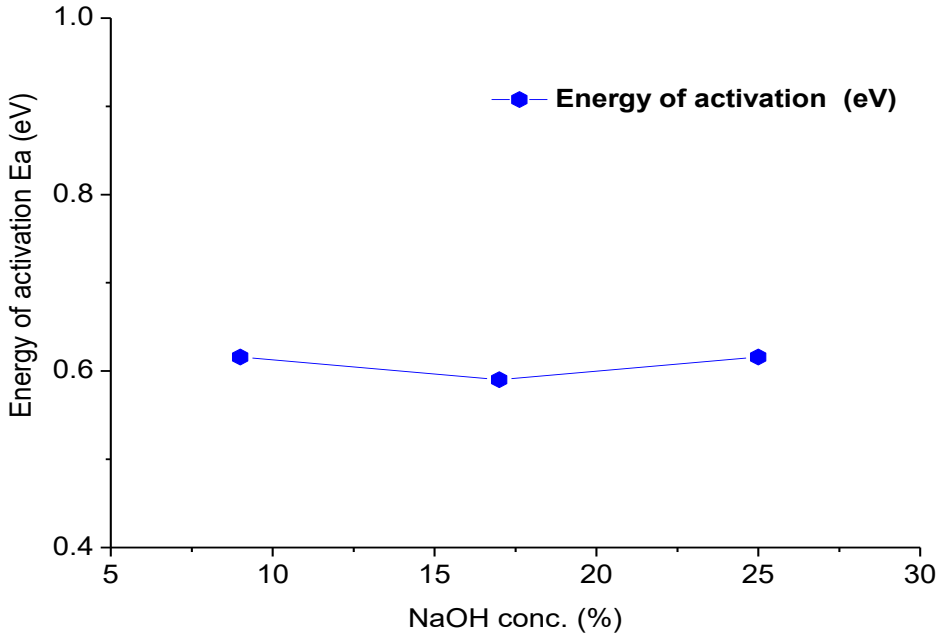


Figure A1.3 Dependence of energy of activation on NaOH solution

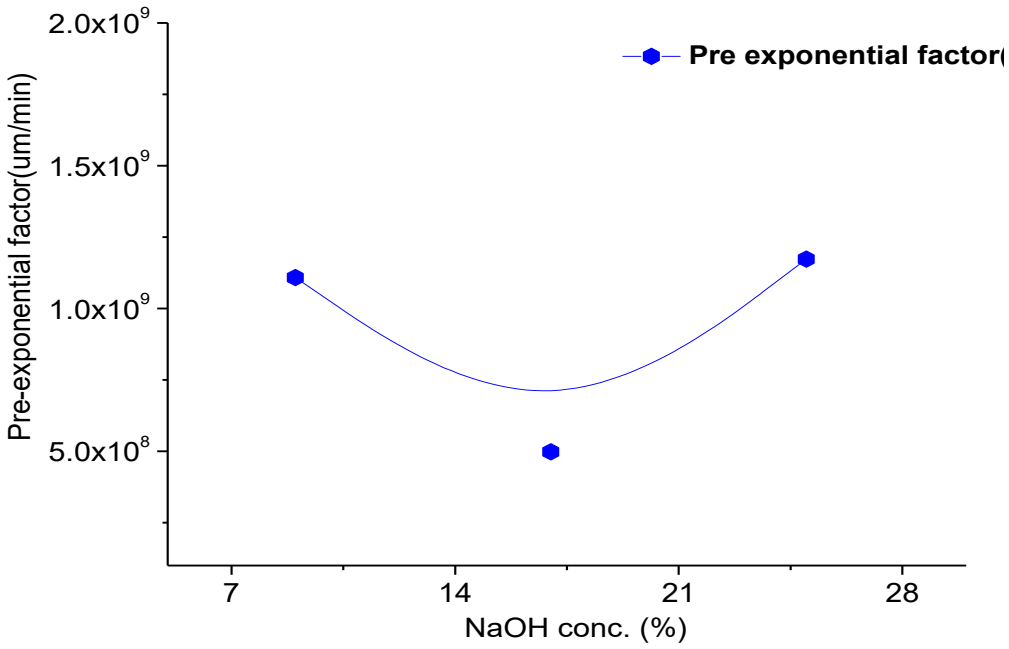


Figure A1.4 Dependence of pre exponential factor on NaOH concentration

From above and plots, we have found that There are two main factors which effect on etching rate of single crystalline silicon, which are as follows:

- Concentration
- Temperature

Concentration Base dopant also affects the etching rate of silicon, it is found that etch rate of silicon decreases with the increase of base doping concentration. [2-3]

Appendix A2: Etching rate of silicon dioxide

Silicon dioxide is most important material in silicon technology than silicon itself. It has functions like a capacity dielectric and isolation material, in which oxides form a part of finished device. But sometime oxides are used intermittently in many cases during silicon processing as a masking material for diffusion or etching and as a cleaning method to reclaim perfect silicon surface. Silicon dioxide etching experiments, phosphorus doped (n-type emitters) wafers, diffused under different temperature (800-875^{0}C) were taken to grow oxides film by thermal Oxidation. Thermal oxidation was carried both in wet and dry environment for 10-25 minutes followed by the drive in of 1 hour at 950^{0}C. The thickness of oxides which we have obtained experimentally are already is shown in graphs of figures 4.16 and 4.17 (wet and dry oxidation in chapter 4). [22-23].

Procedure for silicon dioxide etching is similar as we have already explained above for silicon etching. Etch rate for silicon dioxide was determined at same temperature and concentration. Dependence of SiO_2 etching rate for different NaOH concentration at different temperature is shown in figure A2.1. Maximum etching rate was observed in all case 8-20 nm/min at 90 ^{0}C for all concentration. [1-3]

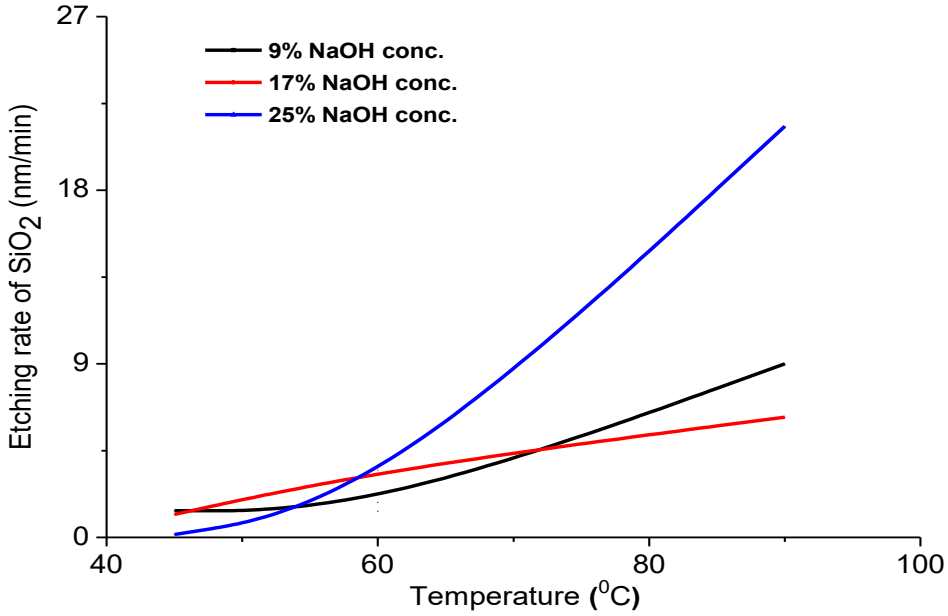


Figure A2.1 SiO_2 etch rate in NaOH solution

Activation Energy

We can calculate the energy of activation and pre exponential factor (R_0) by using Arrhenius equation A1.1 for silicon dioxide. Figure A2.2 shows the Arrhenius plot of etch rates of SiO_2 in NaOH solution. We have calculated energy of activation for pre exponential factor from Arrhenius plots for different concentration of NaOH. [1-3]

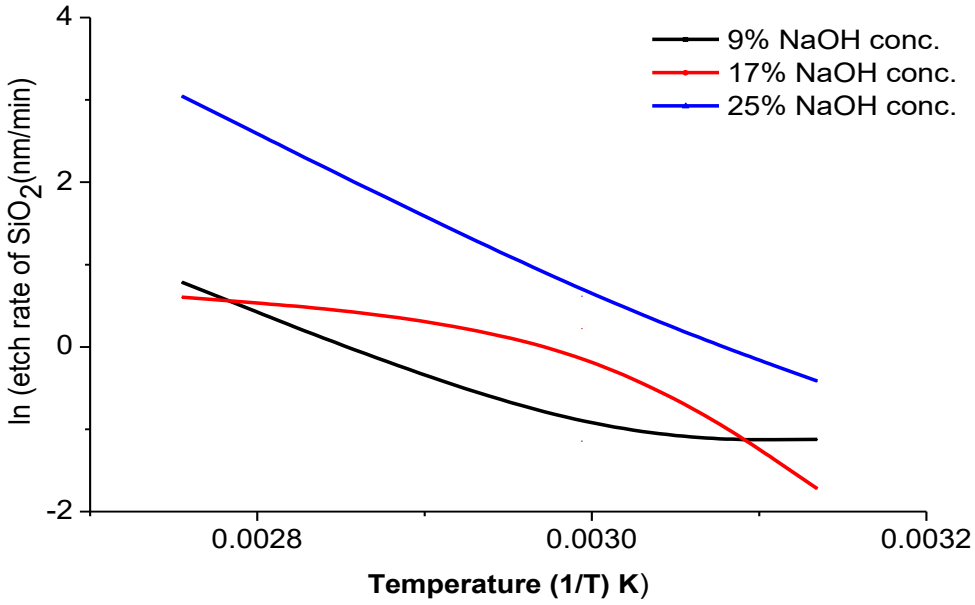


Figure A2.2 Arrhenius plot of SiO_2 etch rate in NaOH solution

Activation energy of SiO_2 wafer is found in this range 0.40-0.80 eV, whereas pre-exponential factor is in range of 1×10^7 - 1×10^{12} nm/min. This is almost similar which is already published in literature. [2-3]. Figure A2.3 & A2.4 show the energy of activation and pre-exponential factor of silicon dioxide calculated at different concentration of NaOH solution.

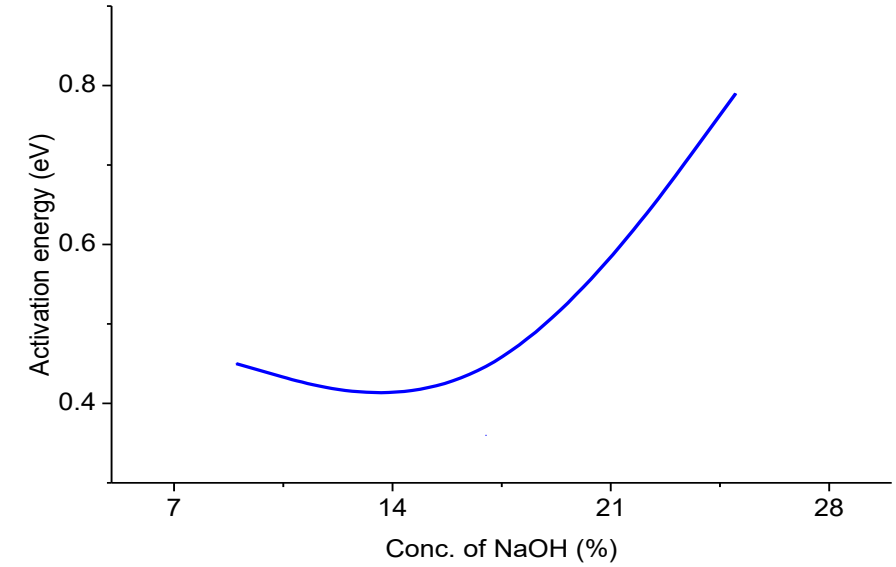


Figure A2.3 Dependence of energy of activation of SiO_2 on NaOH solution

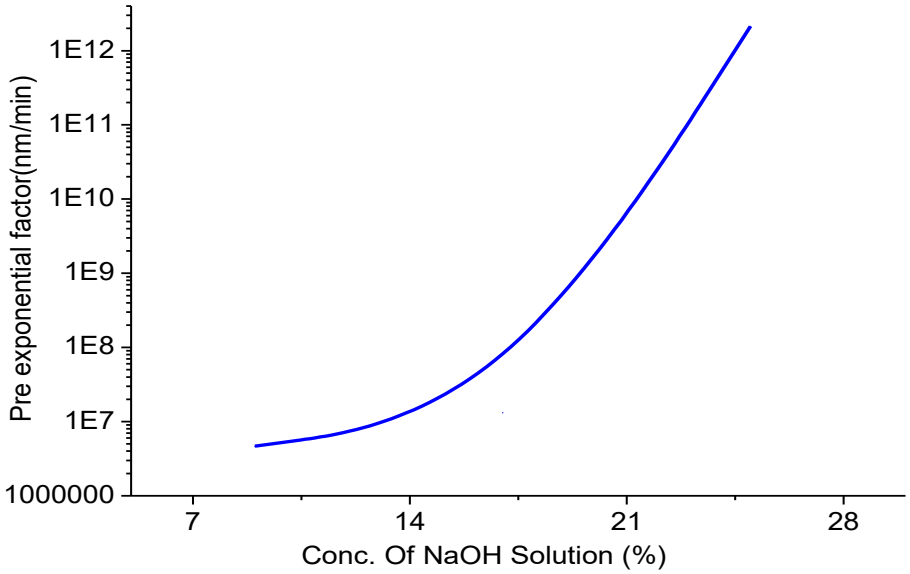


Figure A2.4 Dependence of pre exponential factor of SiO_2 on NaOH concentration

Appendix A3: Etching rate of silicon nitride

For silicon nitride (Si_3N_4) etching, a layer of silicon nitride is deposited by plasma enhanced chemical vapor deposition (PECVD) [24]. Etching rate of silicon nitride in NaOH solution for all concentrations is less than 1 nm/5min (unable measure) as shown in figure A3.1. In our experiments, we could not measure etch rate for silicon nitride correctly by using ellipsometry or weight loss technique. For practical application silicon nitride can be used as perfect masking material [2].

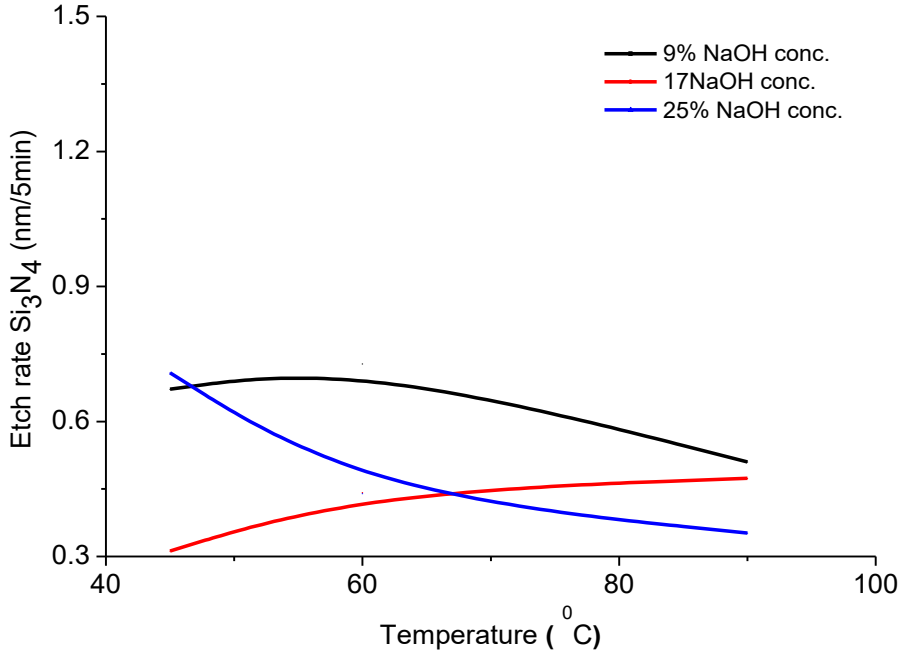


Figure A3.1 Etch rate of Silicon nitride in NaOH solution

In case of silicon nitride, we have doubt that we have observed weight loss during etching process is due to edges of wafers (which may not have silicon nitride layer).

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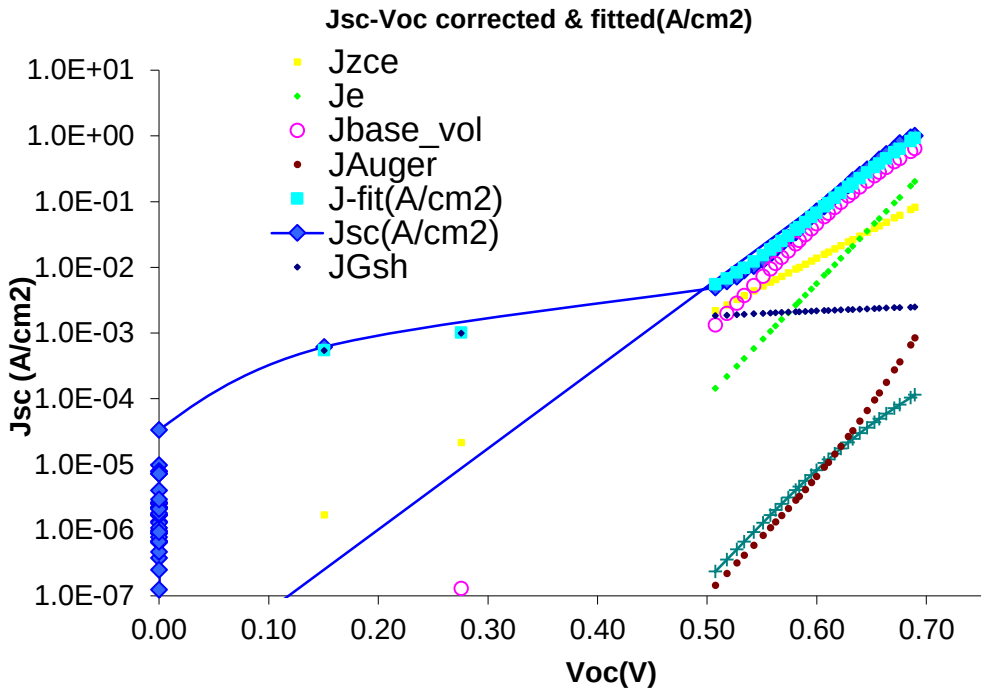
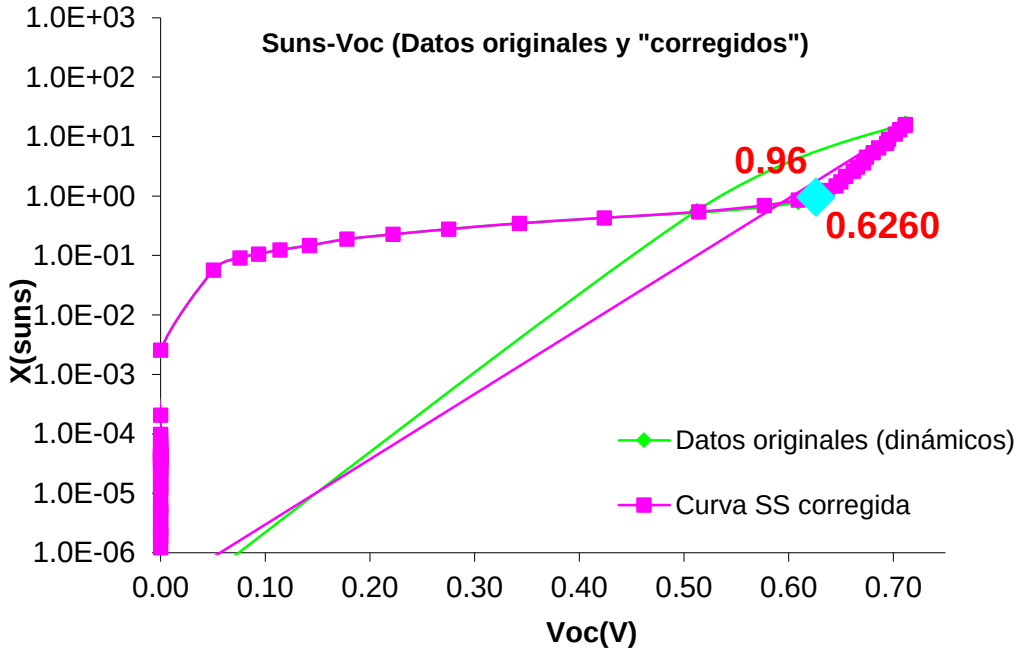
Appendix B

Sun-Voc Measurement of the best wafer.





List of abbreviations used

PV	Photovoltaics
Si	Silicon
FZ	Float-zone
Cz	Czochralski
a-Si	Amorphous silicon
L	Carrier diffusion length
D	Carrier diffusivity
μ	Carrier mobility
N_A	Acceptor concentration
SRH	Shockley-read-hall
τ	Minority carrier Lifetime
τ_{eff}	Effective minority carrier lifetime
τ_{Bulk}	Bulk minority carrier lifetime
τ_{n0}	Electron lifetime
τ_{p0}	Hole lifetime
N_D	Donor concentration
q	Electron charge
V_T	Thermal voltage
v_{th}	Thermal velocity
I	Current
V	Voltage
J_{SC} (I_{SC})	Short-circuit current density
V_{OC}	Open-circuit current density
FF	Fill factor
Rs	Series resistance
R_{Shunt}	Shunt resistance
V_j	Voltage across the diode as well as resistor R_{SH}
J	Current density (Ampere/cm^2)
J_0	Reverse current density (Ampere/cm^2)
J_L	Light generated current density (Ampere/cm^2)
r_S	Specific series resistance (Ω-cm^2)
$\boldsymbol{r_{SH}}$	Specific shunt resistance (Ω-cm^2)
σ_N	Electron capture cross-section
σ_P	Hole capture cross-section
N_T	Trap density
S or SRV	Surface recombination velocity
BSR	Back surface reflector
R_B	Back surface reflectance
J_0	Saturation current density (A/cm^2)
J_{0E}	Saturation current density on emitter side of depletion region

J_{01}	Saturation current density of 1st diode in two diode model of a solar cell
J_{02}	Saturation current density of 2nd diode in two diode model of a solar cell
n_1	Ideality factor of 1st diode in two diode model of a solar cell
n_2	Ideality factor of 2nd diode in two diode model of a solar cell
n	Ideality factor in single-diode model
PECVD	Plasma enhanced chemical vapor deposition
SP	Screen Printed or Screen-Printing
PL	Photolithography
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectroscopy

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