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Common-Mode Voltage Elimination in Multilevel Power Inverter-Based Motor Drive Applications

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ABSTRACT The industry and academia are focusing their efforts on finding more efficient and reliable electrical machines and motor drives. However, many of the motors driven by pulse-width modulated converters face the recurring problem of common-mode voltage (CMV). In fact, this voltage leads to other problems such as bearing breakdown, deterioration of the stator winding insulation and electromagnetic interferences (EMI) that can affect the lifespan and correct operation of the motors. In this sense, multilevel converters have proven to be a useful tool for solving these problems and mitigating CMV over the past few decades. Among other reasons, because they provide additional degrees of freedom when comparing with two-level converters. However, although there are several proposals in the scientific literature on this topic, no complete information has been reviewed about the CMV issues and the different multilevel alternatives that can be used to solve it. In this context, the objective of this work is to determine how multilevel power converters provide additional degrees of freedom to make the reduction of the CMV possible by using specific modulation techniques, making it easier for engineers and scientists in this field to find solutions to this problem. This document consists of a descriptive study that collects the strengths and weaknesses of most important multilevel power converters, with special emphasis on how CMV affects each of them. In addition, the differences of modulation techniques aimed to the CMV reduction are explained in terms of output voltage, operating linear range, and generated CMV. Considering this last, it is recommended to use those modulation techniques that allow the generation of CMV levels of 0 V in order to be able to completely eliminate said voltage.

INDEX TERMS Electric drives, common-mode voltage, power conversion topologies, inverter, multilevel, modulation, PWM.

I. INTRODUCTION

Most commercial electric drives are constituted by an electrical machine and a power converter that conditions the input power to that required by the machine. In general, this converter allows to regulate the speed of the machine, as well as the torque or the position [1]–[3]. In this context, the power converter characteristics (efficiency, robustness, etc.) are as important as those of the electric machine. For this reason, the power converter-based variable frequency drives market has focused its efforts in both the converter and the electric machine, achieving an efficiency increase in the overall drive system [4]–[6]. This fact is illustrated in Fig. 1, where the main strategies to reduce the energy consumption in electric drives are represented, including [7]:

1) The reduction of the power losses in the energy conversion process (drive efficiency increase).
2) The reduction of load power by means of friction/losses processes reduction and speed adjustment.

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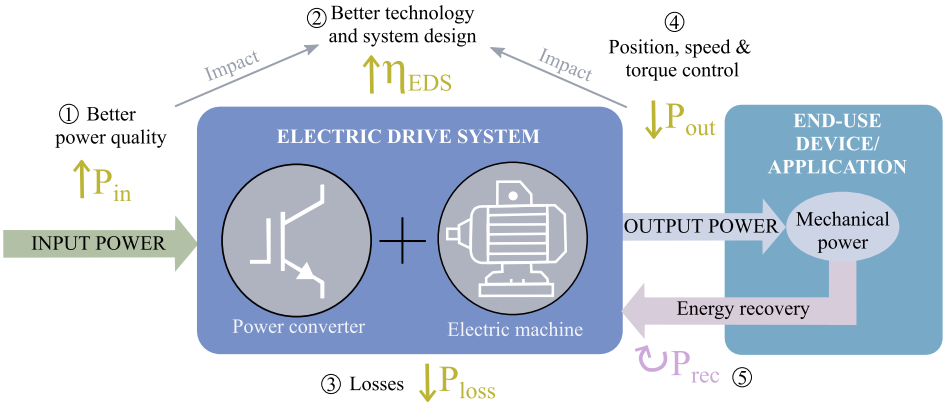


FIGURE 1. Energy consumption reduction in drives without affecting provided useful energy (adapted from [7]).

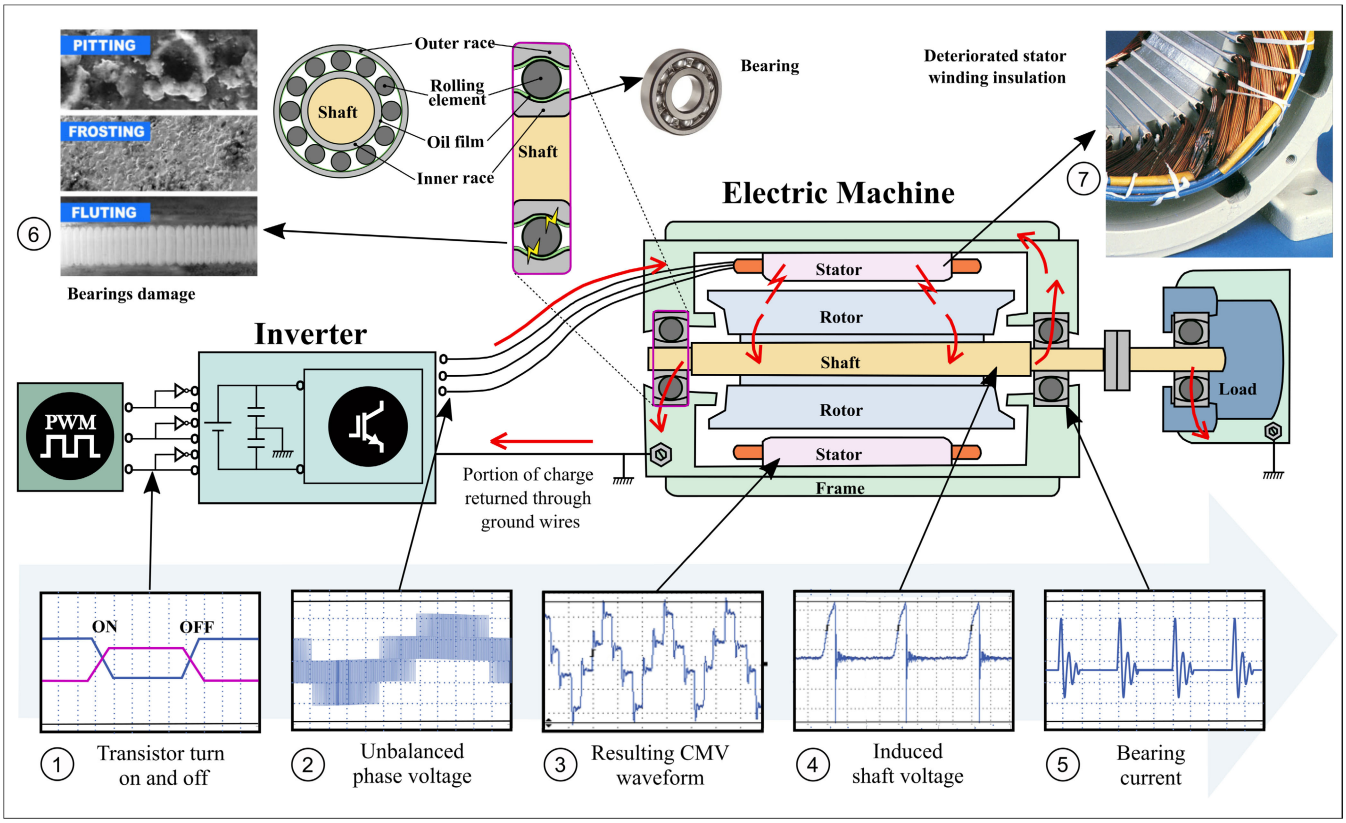


FIGURE 2. Problems caused by common-mode voltage in electric drive systems [8].

3) The reuse of stored kinetic and/or gravitational potential energy (electrical energy regeneration for direct use in other drives, injection into the AC grid and/or common DC bus, and/or energy storage in supercapacitors or batteries).

Despite the search for more efficient systems through the improvement of power converters, the increasing use of these converters in electric drive systems has renewed concerns about one of the main problems of these systems: the common-mode voltage (CMV) [9]–[11]. The high switching frequencies of the semiconductor devices produce high common-mode leakage currents. As a consequence of the existence of several stray common-mode impedance paths between the inverter and the motor frame, this leakage current flows through them every CMV variation (Fig.2) [12]–[15]. This currents lead to motor bearing failures [16]–[18], in addition to electromagnetic interferences (EMI) [19]–[21] or motor stator insulation deterioration (Fig.2) [22]–[24]. Moreover, due to the inherent advantages

of the new wide-bandgap materials (especially silicon carbide and gallium nitride), converters based on semiconductors of these materials are expected to be increasingly employed [22], [25]–[28]. Although, these converters are more efficient than silicon-based converters, their high switching frequencies and high dv/dt worsen the aforementioned CMV problem [14], [29]–[31].

Even though the two-level three-phase voltage source inverter (VSI) is the most widely extended power converter [32]–[34], it is well known that it exhibits poor CMV characteristics [35]–[38]. Conversely, other converters with higher number of voltage levels, called 'multilevel' converters, exhibit additional degrees of freedom that can be used to reduce this stray CMV. In addition, they divide the bus voltage into smaller sections, thus lowering the maximum voltage that each semiconductor device must withstand [39]–[42]. Last, multilevel converters present also other benefits such as improved output waveform quality, i.e. lower total harmonic distortion of the output current (THD_i), reduced EMI and better fault tolerance [43], [44].

Multilevel converters are shown in Fig. 3 together with other converter topologies that have been proposed in the scientific literature as suitable solutions to fix CMV derived problems. In previous works [8], [45], the authors have already reviewed two-level three-phase and multiphase topologies directly aimed at CMV reduction. Due to the large number of available alternatives, this work is only focused on multilevel topologies, leaving aside multiphase topologies. Such converters are widely used in many medium- or high-power industrial applications,[1] such as industrial electric motor driven systems (EMDS) (fans, pumps, conveyors, etc. [42]), flexible AC transmission systems (FACTS) [43], high-voltage DC (HVDC) transmission systems [46], renewable energy sources (RES) [47], [48], as well as electric transportation applications, including more electric aircrafts (MEA) [49] and hybrid and fully electric vehicles (HEV/EVs) [50]). Moreover, as a consequence of their benefits, it is expected that more and more multilevel converters will be used, especially since renewable energies are becoming the main source of electrical energy and the transport sector is moving towards a 100 % electric future.

In the particular case of road transport, which currently accounts for approximately 75 % of transport greenhouse gas emissions [51], regulations and policies on emissions are increasingly strict. This last means that the road transport sector is one of the sectors that will change most rapidly, since emissions can be either reduced or eliminated by an hybrid or fully electric transportation, which implies that, ultimately, the electric vehicle fleet will grow considerably in the coming years [25], [51].[2] In addition, an increase in the number of vehicles will be accompanied by a change in trend that is also beginning to replace the nominal voltages of the battery from 400 V to 800 V [53]–[57]. So it can be expected that the number of multilevel inverters may be increased with the increase in the number of vehicles expected for the next few years [58], without forgetting that the multilevel inverters will also continue to be used in the other applications.

Considering all the above, it is important to understand the operation of the main multilevel converters in electric drive systems and their relationship with the CMV. Therefore, this work aims to make a complete review of these converters, as well as their relationship with the CMV and how to eliminate it. In this sense, first of all, section II explains how CMV is originated in two-level converters, emphasizing how the number of phases affects this voltage and also extrapolating the results for multiphase converters. In addition, figures-of-merit that allow comparing the different CMV waveforms are defined. Then, in section III, the main topologies of multilevel converters and the CMV values they generate are reviewed. Section IV reviews the various modulation techniques that can be used to reduce/eliminate CMV. Finally, Section V summarizes the main conclusions of this review work.

II. INFLUENCE OF THE NUMBER OF PHASES ON THE COMMON-MODE VOLTAGE IN ELECTRIC DRIVES

In [8] the analytical expression for CMV is presented by the authors. However, it is common to see in the scientific literature the equivalence between the electrical machine neutral to ground voltage and the common mode voltage [14], [59]. Although this is not strictly true, it is ideally a good approximation since the CMV waveform will be proportional and very close to neutral to ground voltage. This is reflected in Fig. 4a where the CMV instead of the neutral-ground voltage of the electrical machine is represented in purple. Fig. 4 represents a generalized VSI for any number of phases and connected to an inductive load with a star connection that presents, in its simplest form, the model of an electrical machine. Considering this figure, it can be stated that the CMV levels generated by each switching state of this converter are obtained as:

$$v_{CM}(t) = \frac{1}{m}\sum_{i=1}^{m} v_{i0} \approx v_{NO}(t), \tag{1}$$

where m is the number of phases/legs and v_{i0} is the i-th inverter output phase-to-ground voltage. Also, simplifying (1) for a three-phase converter, CMV is defined as:

$$v_{CM}(t) = \frac{v_{10} + v_{20} + v_{30}}{3}. \tag{2}$$

[1] In order to reach such power levels, an accepted solution is to increase the converter operating voltage. In this sense, the use of multilevel topologies facilitates this task, since it is possible to manage a bus voltage much higher than that established by the blocking voltage of the semiconductor. This is because in a multilevel converter, each of the devices blocks a fraction of the bus voltage.

[2] Regarding electric vehicle sales, the International Energy Agency estimates that the global stock of electric vehicles can reach 140 million by 2030 with stated policy scenarios, and if ambitious sustainable development scenarios are implemented, it would reach 245 million units [52].

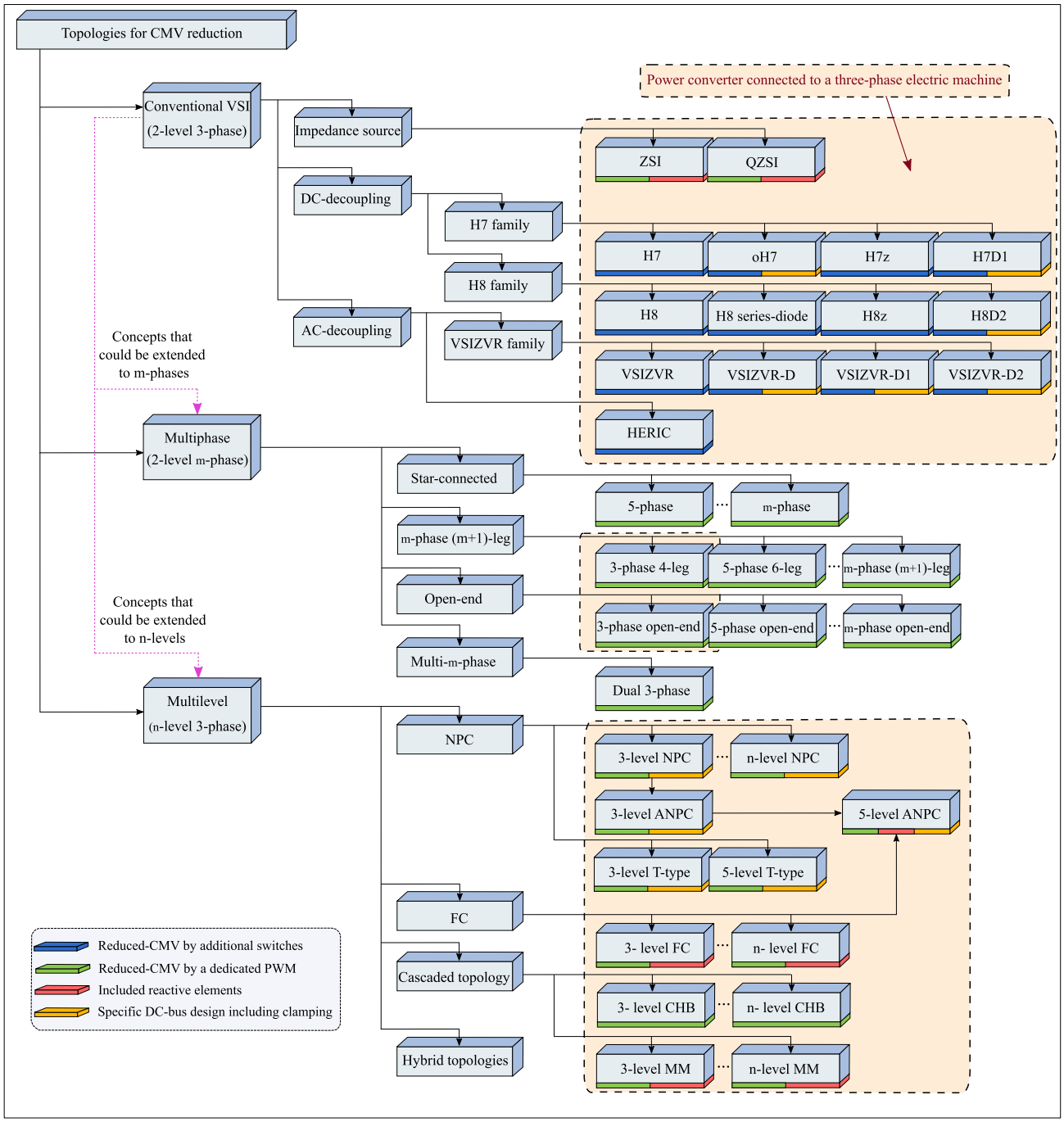
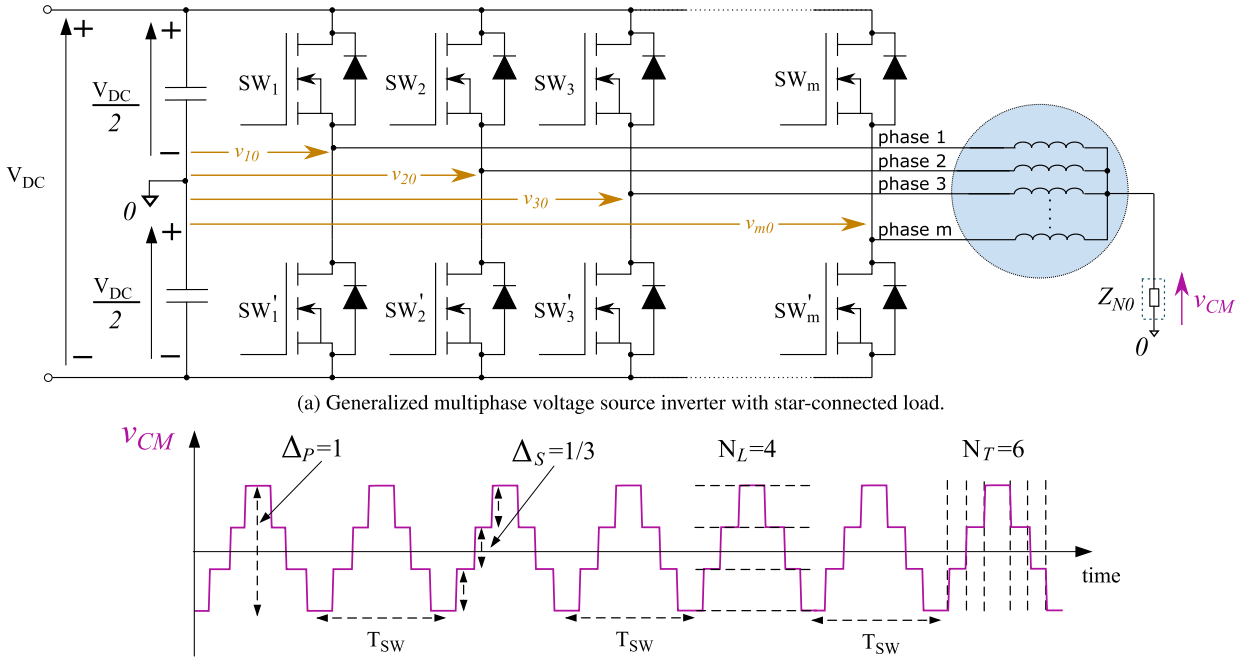


FIGURE 3. Most important inverter topologies for CMV reduction in electric drive systems.

Fig. 4b represents the CMV waveform when the converter is a three-phase inverter. In this sense, the CMV waveform voltage levels of each switching state is shown in Table 1. At the same time, as each converter topology and modulation technique provides a different CMV waveform, CMV-related particularities are best captured by the following 'the lower the better' figures-of-merit, which will be helpful to understand and compare the CMV waveforms to be presented in this work:

1) $\Delta_P \in [0, 1]$ — Waveform peak-to-peak value, relative to V_{DC}.
2) $\Delta_S \in [0, \Delta_P]$ — Height of the largest CMV step, also relative to V_{DC}.
3) N_L — Number of different levels per T_{sw}.
4) N_T — Number of transitions (step shifts) per T_{sw}.

Fig. 4b also shows these figures-of-merit, where, in a conventional three-phase two-level VSI using traditional Space vector PWM (SV-PWM) technique, they correspond



(a) Generalized multiphase voltage source inverter with star-connected load.

(b) CMV waveform when 3-phase inverter is used and a conventional PWM is applied.

FIGURE 4. Representation of the common-mode voltage: (a) Multiphase voltage source inverter with star-connected load. (b) Traditional CMV waveform in a three-phase inverter.

TABLE 1. CMV of traditional VSI converter according to the switching states and their associated space vectors.

Voltage vector (switching state)	Device switching state SW_1	SW_2	SW_3	CMV [V]
$\mathbf{V_0}$ (000)	OFF	OFF	OFF	$-V_{DC}/2$
$\mathbf{V_1}$ (100)	ON	OFF	OFF	$-V_{DC}/6$
$\mathbf{V_2}$ (110)	ON	ON	OFF	$V_{DC}/6$
$\mathbf{V_3}$ (010)	OFF	ON	OFF	$-V_{DC}/6$
$\mathbf{V_4}$ (011)	OFF	ON	ON	$V_{DC}/6$
$\mathbf{V_5}$ (010)	OFF	OFF	ON	$-V_{DC}/6$
$\mathbf{V_6}$ (101)	ON	ON	OFF	$V_{DC}/6$
$\mathbf{V_7}$ (111)	ON	ON	ON	$V_{DC}/2$

to $\Delta_P = 1$, $\Delta_S = 1/3$, $N_L = 4$, and $N_T = 6$, which are poor values, as indicated in [8]. Indeed, these indicators can be improved (lowered) by using alternative modulation techniques in multilevel converters. Therefore, these topics will be covered in the next sections, where the most relevant multilevel converter topologies and modulation techniques are reviewed (sections III and IV, respectively).

III. COMMON-MODE VOLTAGE IN MULTILEVEL INVERTER TOPOLOGIES

For more than fifty years, researchers have been focused on developing new multilevel power converters for medium-voltage and high-power operation [43]. Some of these architectures have been presented, first in the academia and, finally, as commercial products for applications such as EMDSs [60], [61], FACTS [62], HVDC [41], [46] or RES [63]–[66]. In this context, the most well-known multilevel converter structures are the Neutral-point-clamped (NPC) [67], the Flying capacitor (FC) [68] and the Cascaded H-bridge (CHB) [69]. Topologies that include a clamping circuit in addition to the NPC, as the Active neutral-point-clamped (ANPC) and the T-type NPC are also interesting options [70], [71]. The Modular multilevel (MM) converter has also been extensively investigated in the last decade [40], [42], [72] and, likewise and although they are not analyzed in this work, other hybrid architectures which consist on a combination of the previous ones have also been proposed [73], [74].

All these multilevel topologies can be used to reduce the CMV due to their additional degrees of freedom, since, in accordance with (2), the CMV is directly related to the converter output phase voltages. In general, incorporating additional hardware in these converters to improve the CMV is not interesting, because these architectures are already complex from the hardware point of view. Thus, a better solution is to achieve the CMV reduction through advanced modulation algorithms [75]–[77]. In this sense, the relationship between the switching states of the power converter devices and the vector representation of a SV-based modulation helps to better understand CMV. Hence, considering conventional SV-PWM modulation, the most important characteristics of the above-mentioned converters and their relationship with CMV are presented below.

A. MOST RELEVANT MULTILEVEL CONVERTERS

1) NEUTRAL-POINT-CLAMPED (NPC) CONVERTER

This converter was introduced by Nabae in 1981 [67] and it is possibly the first worldwide commercialized multilevel

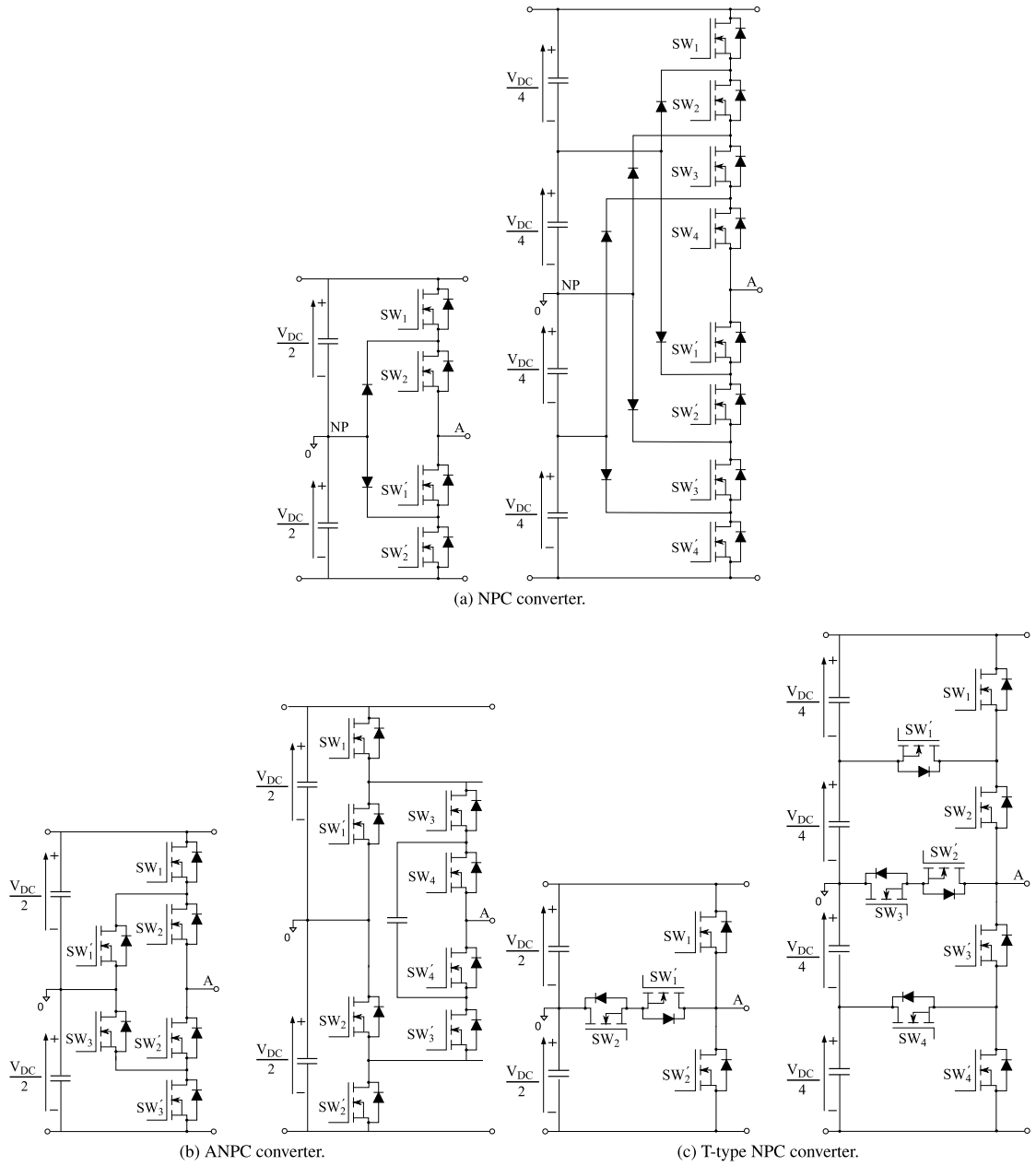


FIGURE 5. Conventional multilevel inverter topologies for three and five levels (only one leg is shown) - (1).

architecture. This converter uses diodes to connect the midpoint of the upper and lower legs with the DC bus midpoint (*NP*) (see Fig. 5a). In its simplest configuration it provides three voltage levels at the output of each phase. Likewise, in order to increase the number of output voltage levels, the number of diodes and switches can be increased too. The possibility of multiple output voltage levels make this topology appropriate for medium and high power applications, such as RES [63] or industrial drives [60].

The NPC converter exhibits some interesting advantages. From the hardware point of view and compared to other multilevel converters, despite some clamping diodes are employed, few capacitors are needed, thus reducing the system cost while reducing the converter size and increasing the system power density. In addition, the NPC converter (as well as the FC converter) requires a just one DC source. This is an advantage over the CHB converter, which requires various independent DC sources. Moreover, when comparing any multilevel converter over the two-level traditional architecture, they exhibit a lower THD_i, due to the multiple level output, and the reduction of the voltage stress on each switching device [78].

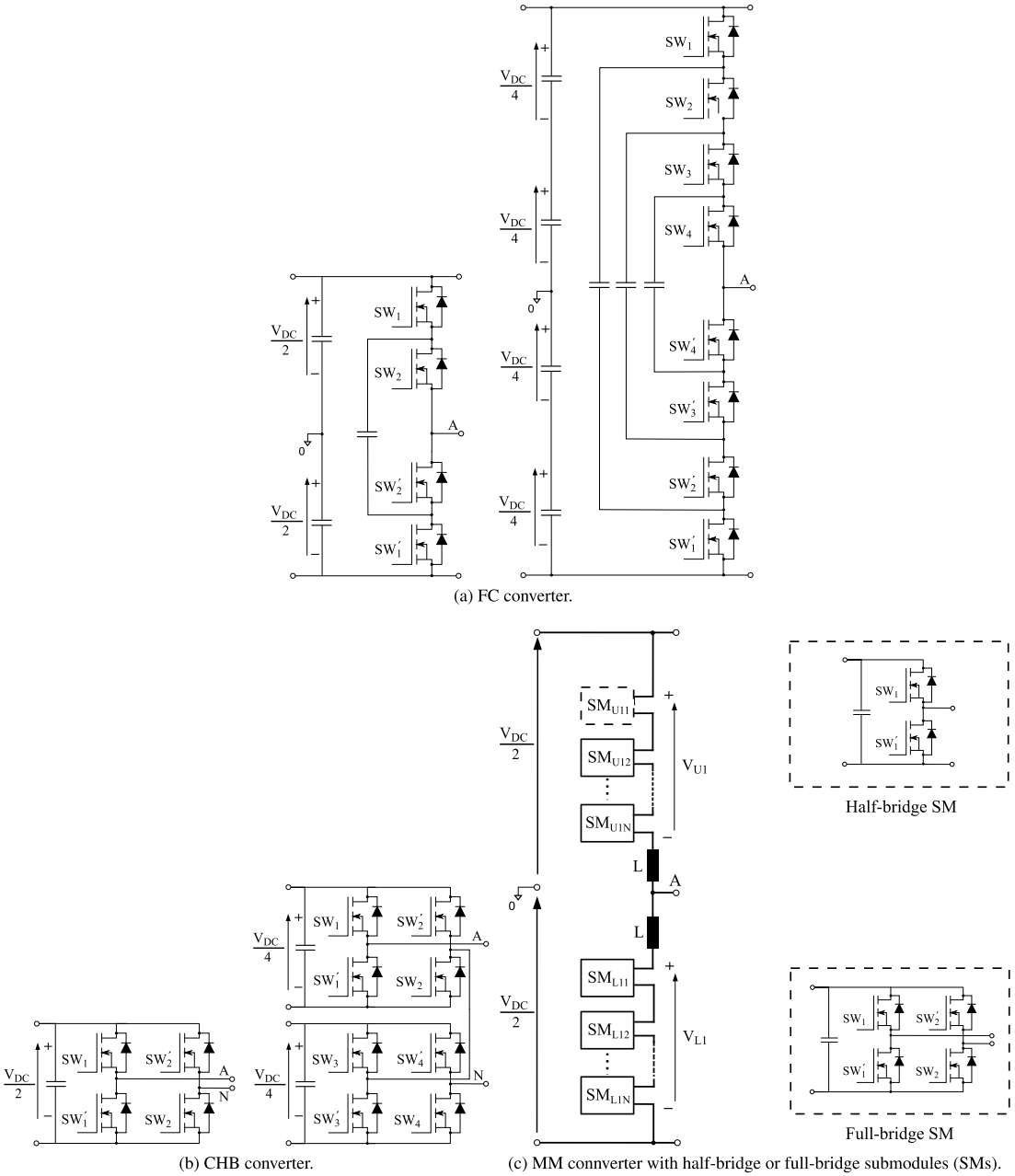


FIGURE 6. **Conventional multilevel inverter topologies for three and five levels (only one leg is shown) - (2).**

Conversely, as the number of output levels increases, so does the complexity of the converter due to the voltage unbalance between the DC-bus capacitors and the need of high number of series connected clamping diodes. Furthermore, these clamping diodes withstand a high voltage stress equal to $V_{DC}\dfrac{(n-2)}{(n-1)}$ for an n-level converter, which is a disadvantage for a converter with a high number of levels. Likewise, NPC converters suffer from unequal share of commutation losses among switches due to the unequal number of commutations [39]. In addition, low-frequency voltage ripple appears in *NP* for high modulation rates and low power factors, resulting in low-frequency distortion on the AC output. For these reasons, it is not common to see NPC converters with more than five levels, as the disadvantages outweigh the advantages.

2) ACTIVE NPC (ANPC) CONVERTER

The ANPC was introduced by Brückner in 2001, replacing the diodes of the three-level NPC converter by active devices [79], [80]. Likewise, its five-level implementation

combining both NPC and FC converter concepts was proposed by Barbosa in 2005 [81]. Regardless of the number of levels, the ANPC architecture (see Fig. 5b) is an appropriate candidate for high-power EMDS applications and has received attention in recent years [70], [82]. In industry, an example is ABB, which has upgraded its HVDC Light converter by using a three-level active-NPC structure [43]. In addition, the ABB's five-level ACS2000 is used in diverse fields of application for various industries within the general purpose drives' market as fans, pumps or compressors [83].

The main advantage of the three-level ANPC converter is that it is possible to control the loss distribution among the switching devices [70], [80]. For example, in [80] a loss-balancing scheme is proposed, which can significantly increase the converter output power. On the other hand, as an additional advantage, the five-level ANPC features redundant switching states [81], which provide additional degrees of freedom and, consequently, open-phase fault tolerance control [84], [85]. In addition, compared with the NPC, the five-level ANPC converter has simpler voltage-balancing control of the NP, more flexibility on the output voltage value and higher reliability [86]. It can be said that the five-level ANPC combines the flexibility of the FC converter with the robustness of industrial NPC converters to generate the multilevel voltages [81].

As far as disadvantages are concerned, for the three-level structure, the main drawback is that it needs to control a greater number of active devices. Further, the extension of three levels to a higher number of levels is not straightforward in this converter. To increase the number of levels, while respecting the operation of the converter architecture, a hybrid solution that combines the NPC and FC structures is necessary.

3) T-TYPE NPC CONVERTER

This converter was introduced in 2010 by Schweizer in [87]. Compared to the three-level NPC topology, the T-type incorporates an active bidirectional switch to clamp the DC bus midpoint, thus using two diodes less per bridge leg; see Fig. 5c. Moreover, when increasing to five levels there are two variants of the converter: the dual three-level T-type and the five-level T-type (Fig. 5c), both introduced by Salem in 2013 [71], [88]. In addition to their multilevel nature, the former can also be considered multiphase. In any case, the T-type NPC converter has been extensively investigated in the last decade for RES applications [64], [89], [90], as well as EMDSs [61], [88].

The T-type converter basically combines the advantages of the two-level structure such as low conduction losses, reduced part count and a simple operation, with the advantages of the three-level architecture such as low switching losses and superior output voltage quality [71]. Likewise, in a T-type inverter, fault-tolerant operation can be performed when open-switch fault occurs without adding extra devices [90].

Among its disadvantages, the *NP* of three-level T-type is similar to the NPC converter, because it needs to be controlled in order to keep equal the voltages of the DC bus capacitors [71]. However, unlike the NPC, its most significant drawback is that the devices must block all DC bus voltage [71].

4) FLYING CAPACITOR (FC) CONVERTER

The FC was introduced by Meynard and Foch in 1992 [68]. Here, an n-level FC converter links the midpoint of upper legs with the midpoint of their respective lower legs by means of $3(n-2)$ capacitors (Fig. 6a). In addition, these capacitors are to be precharged in order to produce the correct phase-to-ground output voltage [62]. The hardware structure of the FC converter makes this topology suitable for photovoltaic (PV) applications [65] and wind turbines [66]. In addition, this topology has also been employed in drive systems as in the case of induction motor drives [91].

The main advantage of the FC architecture is that it is able to generate the same output voltage employing different switch on/off configurations, that is, the FC converter has redundant switching states. Due to this fact, currents may flow with different polarity through the flying capacitors in order to charge or discharge them as needed. In addition, this vector redundancy allows distributing the switching stress equally between the semiconductors [92]. And finally, unlike the NPC structure, low frequency ripple does not appear in the capacitors [93].

In return, the increment of levels reduces the accurate charging and discharging control of flying capacitors [62]. Moreover, as the number of required capacitors is high, especially in inverters with more than five levels, the inverter becomes bulky, expensive and its modularity is reduced [94]. In addition, the voltage of its capacitors must be measured, but regardless of the number of levels a per-phase single sensor is sufficient [95].

5) CASCADED H-BRIDGE (CHB) CONVERTER

This converter was introduced by Marchesoni in 1990 [69]. The structure of the CHB is based on submodules (SM), each of which contains a full-bridge, a DC-link capacitor and an independent voltage source provided by transformers or batteries (Fig. 6b). Since adding more SMs and increasing the number of levels is easy, this converter has been used in a wide variety of high-voltage applications, including EMDSs [96], FACTS such as static synchronous compensators (STATCOM) [43], and HVDC applications [41].

CHB architectures can reach high output voltage values by connecting various inverters in series. Since each inverter can be considered as an independent SM, in case of a fault in one of them, it can be easily replaced without nearly affecting the converter performance. Consequently, one of the main advantages of this topology is its modularity and fault tolerance. Moreover, this topology features redundant switching states as the FC structure, thus allowing equal distribution of switching stress between the semiconductors and reducing the switching losses [97]. The latter is a particularly interesting feature in applications where efficiency is one of the major objectives, such as in HEV/EVs [98].

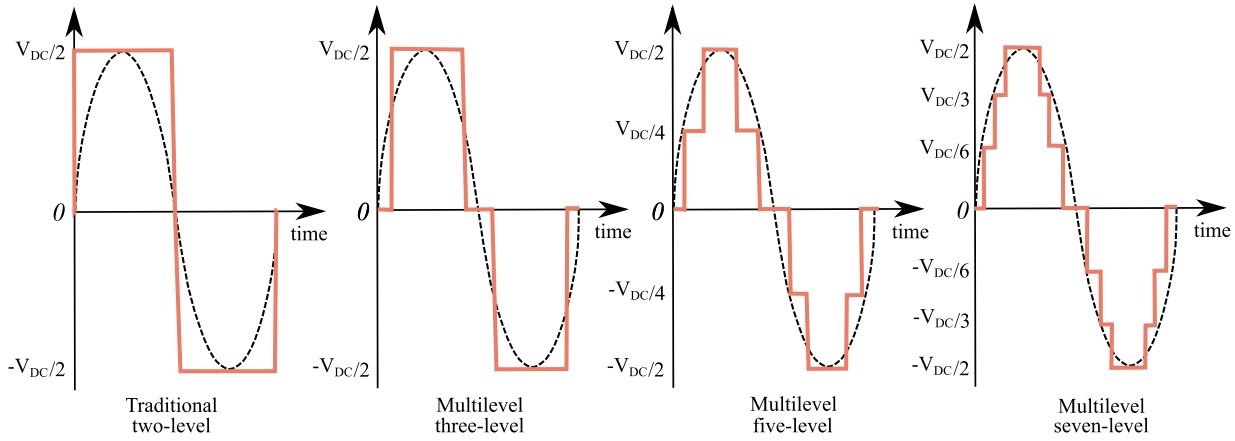


FIGURE 7. Output phase-ground voltage waveforms as a function of the number of levels, synthesized with independence of the multilevel architecture.

TABLE 2. One phase switching states of the devices of multilevel converters of three and five levels and phase-to-earth output voltage generated.

No. levels	Switching state(1)					Output phase voltage [V] for various topologies(4)				
						NPC topologies			FC	CHB
	Identifier	SW_1 (2)	SW_2	SW_3	SW_4	NPC	ANPC	T-type		
Three	-1	OFF	OFF	✗(3)	✗	$-V_{DC}/2$	✗	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$
	0	OFF	ON	✗	✗	0	✗	0	0	0
	0	ON	OFF	✗	✗	✗	✗	✗	0	0
	1	ON	ON	✗	✗	$V_{DC}/2$	✗	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$
Three	-1	OFF	OFF	OFF	✗	✗	$-V_{DC}/2$	✗	✗	✗
	0	OFF	OFF	ON	✗	✗	0	✗	✗	✗
	0	OFF	ON	OFF	✗	✗	0	✗	✗	✗
	0	OFF	ON	ON	✗	✗	0	✗	✗	✗
	-1	ON	OFF	OFF	✗	✗	$-V_{DC}/2$	✗	✗	✗
	0	ON	OFF	ON	✗	✗	0	✗	✗	✗
	1	ON	ON	OFF	✗	✗	$V_{DC}/2$	✗	✗	✗
	1	ON	ON	ON	✗	✗	$V_{DC}/2$	✗	✗	✗
Five	-2	OFF	OFF	OFF	OFF	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$
	-1	OFF	OFF	OFF	ON	$-V_{DC}/4$	$-V_{DC}/4$	$-V_{DC}/4$	$-V_{DC}/4$	$-V_{DC}/4$
	-1 or 0	OFF	OFF	ON	OFF	✗	$-V_{DC}/4$	0	$-V_{DC}/4$	$-V_{DC}/4$
	0	OFF	OFF	ON	ON	0	0	0	0	0
	-1 or 0	OFF	ON	OFF	OFF	✗	0	✗	$-V_{DC}/4$	$-V_{DC}/4$
	0 or 1	OFF	ON	OFF	ON	✗	$V_{DC}/4$	✗	0	0
	-1, 0 or 1	OFF	ON	ON	OFF	✗	$-V_{DC}/4$	$V_{DC}/4$	0	0
	0 or 1	OFF	ON	ON	ON	$V_{DC}/4$	0	$V_{DC}/4$	$V_{DC}/4$	$V_{DC}/4$
	-2 or -1	ON	OFF	OFF	OFF	✗	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/4$	$-V_{DC}/4$
	-1 or 0	ON	OFF	OFF	ON	✗	$-V_{DC}/4$	$-V_{DC}/4$	0	0
	0 or 1	ON	OFF	ON	OFF	✗	$V_{DC}/4$	0	0	0
	0, 1 or 2	ON	OFF	ON	ON	✗	$V_{DC}/2$	0	$V_{DC}/4$	$V_{DC}/4$
	0	ON	ON	OFF	OFF	✗	0	✗	0	0
	1 or 2	ON	ON	ON	OFF	✗	$V_{DC}/4$	$V_{DC}/2$	$V_{DC}/4$	$V_{DC}/4$
	1	ON	ON	OFF	ON	✗	$V_{DC}/4$	✗	$V_{DC}/4$	$V_{DC}/4$
	2	ON	ON	ON	ON	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$

Notes:
(1) The output phase voltage depends on the switching state; e.g. in five-level converters when the switching state is -2, -1, 0, 1 or 2, the phase voltage will be $-V_{DC}/2$, $-V_{DC}/4$, 0, $V_{DC}/4$ or $V_{DC}/2$, respectively.
(2) The representation of each switch for all these topologies is seen in Figs. 5 and 6.
(3) The ✗ represents a non existing switch or a switching sequence that can not be produced.
(4) The MM converter is not included in the table because the number of switches depends on the used submodules.

As a disadvantage, a high number of independent DC sources are needed, one for each SM. Therefore, CHB architectures are mainly used in PV applications, where each half-bridge can be feed by means of an isolated PV panel. Likewise, independent batteries or fuel cells can be also employed as isolated DC sources [99], thus making the converter suitable for off-grid drive systems.

6) MODULAR MULTILEVEL (MM) CONVERTER

This converter was introduced by Lesnicar in 2003 [100]. Fig. 6c depicts its structure, where, in its most simple version, each SM is constituted by half-bridge or full-bridge converters. However, various SM architectures have been proposed to improve the inverter performance, among which the MM-NPC and the MM-FC converters stand out [101],

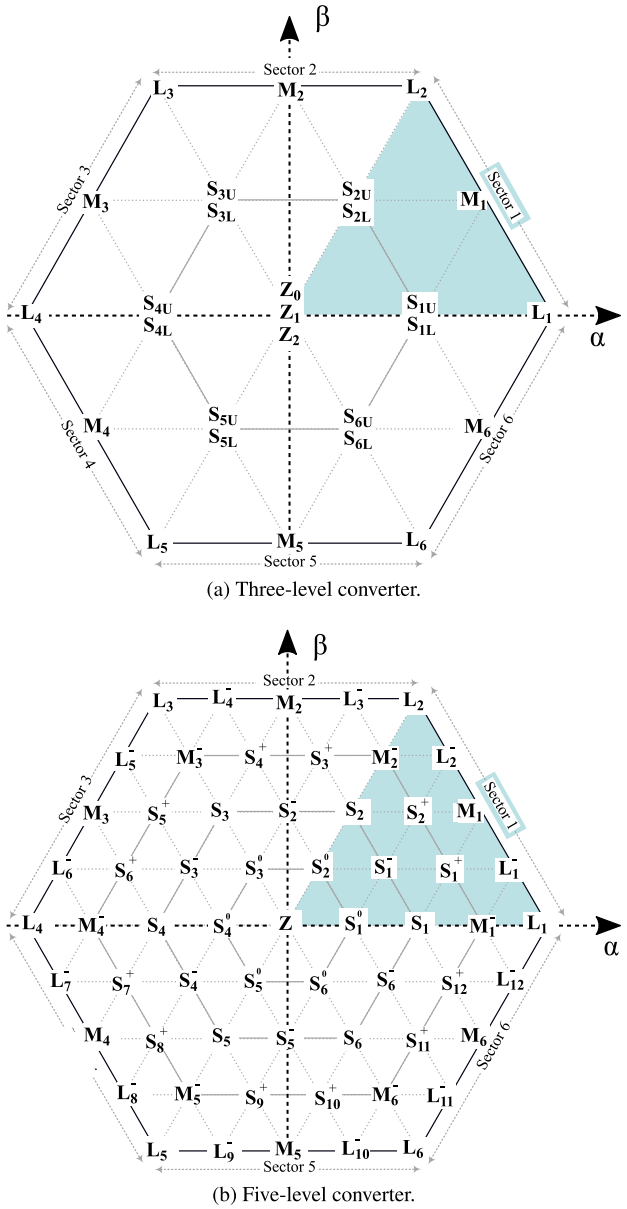
TABLE 3. CMV of three- and five-level multilevel converters produced by each voltage vector.

Three-level inverter		
Vector type	**Voltage vectors (switching states)**	**CMV value [V]**
Zero	$\mathbf{Z_0}$ (-1,-1,-1)	$-V_{DC}/2$
Small	$\mathbf{S_{1L}}$ (0,-1,-1), $\mathbf{S_{3L}}$ (-1,0,-1), $\mathbf{S_{5L}}$ (-1,-1,0)	$-V_{DC}/3$
	$\mathbf{S_{2L}}$ (0,0,-1), $\mathbf{S_{4L}}$ (-1,0,0), $\mathbf{S_{6L}}$ (0,-1,0)	$-V_{DC}/6$
Large	$\mathbf{L_1}$ (1,-1,-1), $\mathbf{L_3}$ (-1,1,-1), $\mathbf{L_5}$ (-1,-1,1)	
Zero	$\mathbf{Z_1}$ (0,0,0),	0
Medium	$\mathbf{M_1}$ (1,0,-1), $\mathbf{M_2}$ (0,1,-1), $\mathbf{M_3}$ (-1,1,0), $\mathbf{M_4}$ (-1,0,1), $\mathbf{M_5}$ (0,-1,1), $\mathbf{M_6}$ (1,-1,0)	
Large	$\mathbf{L_2}$ (1,1,-1), $\mathbf{L_4}$ (-1,1,1), $\mathbf{L_6}$ (1,-1,1)	$V_{DC}/6$
Small	$\mathbf{S_{1U}}$ (1,0,0), $\mathbf{S_{3U}}$ (0,1,0), $\mathbf{S_{5U}}$ (0,0,1)	
	$\mathbf{S_{2U}}$ (1,1,0), $\mathbf{S_{4U}}$ (0,1,1), $\mathbf{S_{6U}}$ (1,0,1)	$V_{DC}/3$
Zero	$\mathbf{Z_2}$ (1,1,1)	$V_{DC}/2$
Five-level inverter		
Vector type	**Voltage vectors (switching states)**	**CMV value [V]**
Zero	$\mathbf{Z}$	$-V_{DC}/2$
Extremely small	$\mathbf{S_1^0\ S_3^0\ S_5^0}$	$-5V_{DC}/12$
Extremely small	$\mathbf{S_2^0\ S_4^0\ S_6^0}$	$-V_{DC}/3$
Small	$\mathbf{S_1\ S_3\ S_5}$	
Zero	$\mathbf{Z}$	$-V_{DC}/4$
Lower small	$\mathbf{S_1^-\ S_2^-\ S_3^-\ S_4^-\ S_5^-\ S_6^-}$	
Lower median	$\mathbf{M_1^-\ M_3^-\ M_5^-}$	
Extremely small	$\mathbf{S_1^0\ S_3^0\ S_5^0}$	$-V_{DC}/6$
Small	$\mathbf{S_2\ S_4\ S_6}$	
Higher small	$\mathbf{S_1^+\ S_4^+\ S_5^+\ S_8^+\ S_9^+\ S_{12}^+}$	
Large	$\mathbf{L_1\ L_3\ L_5}$	
Extremely small	$\mathbf{S_2^0\ S_4^0\ S_6^0}$	$-V_{DC}/12$
Small	$\mathbf{S_1\ S_2\ S_5}$	
Higher small	$\mathbf{S_2^+\ S_3^+\ S_6^+\ S_7^+\ S_{10}^+\ S_{11}^+}$	
Lower large	$\mathbf{L_1^-\ L_4^-\ L_5^-\ L_8^-\ L_9^-\ L_{12}^-}$	
Zero	$\mathbf{Z}$	0
Lower small	$\mathbf{S_1^-\ S_2^-\ S_3^-\ S_4^-\ S_5^-\ S_6^-}$	
Lower median	$\mathbf{M_1^-\ M_3^-\ M_5^-}$	
Lower median	$\mathbf{M_2^-\ M_4^-\ M_6^-}$	
Medium	$\mathbf{M_1\ M_2\ M_3\ M_4\ M_5\ M_6}$	
Extremely small	$\mathbf{S_1^0\ S_3^0\ S_5^0}$	$V_{DC}/12$
Small	$\mathbf{S_3\ S_4\ S_6}$	
Higher small	$\mathbf{S_1^+\ S_4^+\ S_5^+\ S_8^+\ S_9^+\ S_{12}^+}$	
Lower large	$\mathbf{L_2^-\ L_3^-\ L_6^-\ L_7^-\ L_{10}^-\ L_{11}^-}$	
Extremely small	$\mathbf{S_2^0\ S_4^0\ S_6^0}$	$V_{DC}/6$
Small	$\mathbf{S_1\ S_3\ S_5}$	
Higher small	$\mathbf{S_2^+\ S_3^+\ S_6^+\ S_7^+\ S_{10}^+\ S_{11}^+}$	
Large	$\mathbf{L_2\ L_4\ L_6}$	
Zero	$\mathbf{Z}$	$V_{DC}/4$
Lower small	$\mathbf{S_1^-\ B_2^-\ B_3^-\ B_4^-\ B_5^-\ B_6^-}$	
Lower median	$\mathbf{M_2^-\ M_4^-\ M_6^-}$	
Extremely small	$\mathbf{S_1^0\ S_3^0\ S_5^0}$	$V_{DC}/3$
Small	$\mathbf{S_2\ S_4\ S_6}$	
Extremely small	$\mathbf{S_2^0\ S_4^0\ S_6^0}$	$5V_{DC}/12$
Zero	$\mathbf{Z}$	$V_{DC}/2$

(*) [82], [86] show all the states of five-level converters.

[102]. Although this topology was firstly developed for HVDC systems [46], [103], [104], it is also used in AC/AC cycloconverters [105] or medium-voltage and high-power industrial drive applications [40], [42], [106].

The main advantage of this topology is its modularity [42]. Indeed, medium and high output voltage values can be easily achieved by adding more series-connected SMs. Moreover, there is no need to use a common DC bus, since each SM incorporates its own DC bus capacitor, increasing even more



(a) Three-level converter.

(b) Five-level converter.

FIGURE 8. Representation of the multilevel voltage vectors in the $\alpha\beta$-frame.

the converter power density and reducing costs [72]. Likewise, other attractive features are its high efficiency and the high quality of the output voltages [42].

Conversely, MM converters suffer from current circulation within the structure, which increases conduction losses. In addition, this current increases DC-bus capacitor thermal stress since high voltage ripple is produced in such capacitor under low speed operation in EMDS applications [40], [106]. Moreover, as in other multilevel converter, the control complexity of the MM converter increases with the number of voltage levels.

B. COMMON-MODE VOLTAGE IN MULTILEVEL CONVERTERS

Any of the previously presented converters improve the quality of the synthesized waveform as the number of levels is

TABLE 4. Main multilevel inverters and their relationship with the common-mode voltage.

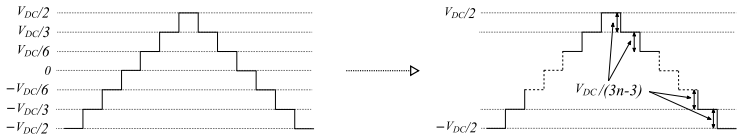
		NPC Fig. 5a		ANPC Fig. 5b		T-type Fig. 5c		FC Fig. 6a		CHB Fig. 6b		MM Fig. 6c	
		3-level	n-level	3-level	5-level	3-level	5-level	3-level	n-level	3-level	n-level	3-level	n-level
Hardware	• Switches(1)	12	6(n-1)	18	24	12	24	12	6(n-1)	12	6(n-1)	SM dependent	
	• Diodes	6	6(n-2)(2)	0	0	0	0	0	0	0	0	SM dependent	
	• DC bus capacitors(3)	2	n-1	2	2	2	4	1	1	3	(3n/2 – 1.5)(4)	0	
	• Extra capacitors	0	0	0	3	0	0	3	(3n-6)(5)	0	0	SM dependent	
	• Inductors	0	0	0	0	0	0	0	0	0	0	6	6
	• Voltage sources	1	1	1	1	1	1	1	1	3	(3n-3)/2	1	1
CMV-related data(6)	• CMV value of each level in the CMV waveform for tree- and n-level converters (see also Table 3)												
	• CMV figures-of-merit Δ_P	1								1			
	Δ_S	1/6								$1/(3n-3)$			
	N_L	7								3n-2			
	N_T	12								6n-6			
Pros and cons	• Advantages	• Single DC-link voltage source • Fewer capacitors than FC • Economical for low levels		• Better loss distribution than NPC • Redundant voltage vectors: fault tolerance • Greater reliability and better *NP* control		• Small switch count • Lower power losses • Redundant voltage vectors: fault tolerance		• Single DC-link voltage source • Redundant switching states: fault tolerance • Low number of active devices		• Modular structure • Easier to provide high voltage • Redundant switching states • High fault tolerance		• Great modularity • Redundancy and reliability • Absence of extra DC-link capacitors • High eficiency	
	• Disadvantages	• Necessary to balance the DC bus capacitors • Unbalanced switching losses • High voltage supported by the clamping diodes • Low frequency ripple in *NP* (for $M_a \uparrow$ and $PF \downarrow$)		• Greater number of active devices • Disadvantages of the NPC and the FC when number of levels is increased		• Necessary to balance the DC bus capacitors • Higher reverse voltage than NPC		• Very bulky as the number of levels is increased • Necessary to precharge capacitors • Reduced modularity • Expensive		• High number of isolated DC sources • Voltage imbalance between different phases		• Higher capacitor voltage ripple • Complex system with multiple variables to control	
References		[10], [107], [108]		[82], [109]–[111]		[61], [64], [71], [88]		[65], [112]–[114]		[76], [77], [97], [115], [116]		[117]–[119]	

Table notes:
(1) Switches (with their free-wheeling diodes).
(2) 6(n-2) is the number of independent diodes (blocking different reverse voltage), but real number of independent diodes (series connection for same reverse voltage distribution) is 3(n-1)(n-2).
(3) Minimum number of DC bus capacitors, withstanding the same voltage.
(4) This expression is only valid for an odd number of levels, since only converters with an odd number of levels are generally shown. As an exception, the 4-level CHB and NPC converters are alternatives shown in the literature.
(5) This expression is the minimum number of capacitors with different voltages (excluding DC-link capacitors). If considered the real number of converter capacitors (series and parallel connection for the same voltage distribution and capacitance) the expression is $(n-1)^2 + 3\sum_{i=1}^{n-2} i^2$.
(6) The depicted CMV waveform and figures-of-merit are obtained assuming all CMV values are available during each switching period (T_{SW}), however, in practice this is not usual, as each modulation technique changes this CMV waveform (see section IV-B).

increased (see Fig. 7). In any case, despite converters are structurally different, all the reviewed multilevel architectures can synthesize the same output voltage profile (see Fig. 7). Table 2 summarizes the output voltage values for three and five levels depending on the switching states,[3] where each converter has its particularities; e.g. the NPC can only synthesize each voltage value with a single switching state. In contrast, the other converters have redundant switching states that can synthesize the same output voltage level.

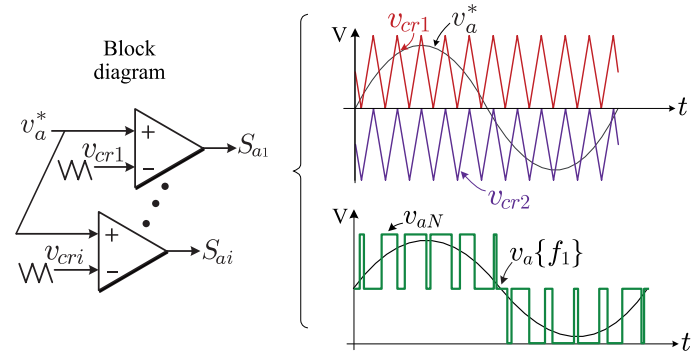
Regarding the vector space, n^3 switching states can be synthesized (total vectors of the SV diagram; see Table III-A5), and they can be simplified as $n^3 - (n-1)^3$ states of the converter with different line-to-line voltage (different verctors of the SV diagram). Due to this vector redundancy, the number of vectors can be reduced to $27 - 8 = 19$ for the three-level converters and $125 - 64 = 61$ for the five-level converters (see Fig. 8).[4] Fig. 8a shows the general space-vector diagram of all three-level converters, which depicts the 27 switching states and 19 voltage vectors. Each switching state can be expressed by an ordinal number array, for example, [−1 0 1] corresponds to the connection of phase A to the negative bus, phase B with zero voltage level (e.g, phase B to *NP* in the NPC converter), and phase C to the positive bus (see Fig. 5 and 6). Likewise, the voltage vectors can be classified according to their amplitude as zero ($\mathbf{Z_i}$), small (upper $\mathbf{S_{iU}}$ and lower $\mathbf{S_{iL}}$), medium ($\mathbf{M_i}$), and large ($\mathbf{L_i}$), where $i = 1, 2 \ldots 6$. Table 2 summarizes this classification.

In accordance with (2), regardless of the way the converter output voltages are synthesized, different CMV values can be obtained. For example, if a three-level converter applies the vector $\mathbf{M_4}$ [−1 0 1], it results in the CMV value of $-V_{DC}/2$ (Table III-A5). The MM converter is an exception, depending on the type of SM chosen [102] the number of switches is different, therefore the switching states and the output voltage cannot be identified directly. Consequently, the CMV will depend both on the resulting converter topology (as a function of the SM chosen) and the modulation used on the converter. However, whatever the SM, the CMV can be generally defined for the MM converter as:

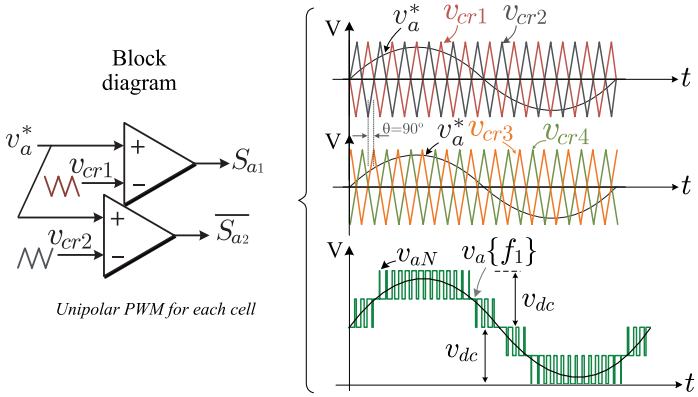
$$v_{CM}(t) = \frac{1}{6}\sum_{i=1}^{3}\left[v_{Li}(t) - v_{Ui}(t)\right], \tag{3}$$

[3]Switching states per phase are represented with numbers from -1 to 1 for the three-level inverter and -2 to 2 for the five-level inverter (see Table 2).

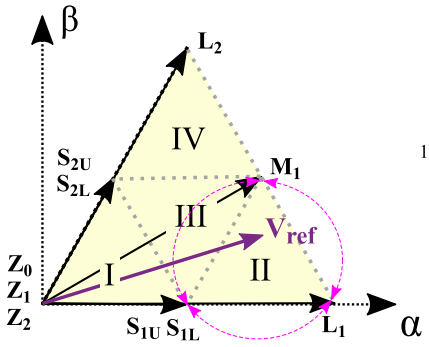
[4]Furthermore, depending on the used devices to generate the line-to-line phase voltage in each converter topology (see Table 2), more than n^3 redundant states can be generated. For example, since the three-level FC converter can synthesize 0 V (see Table 2) with two different switching states, the number of resulting switching states in the vectorial space is 64 for the three-level FC and $2^{3(n-1)}$ generalized for a converter with a higher number of levels [113].



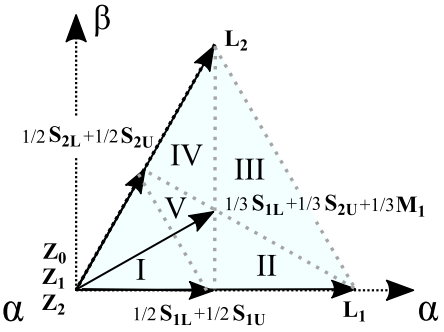
(a) Level-shifted PWM [123].



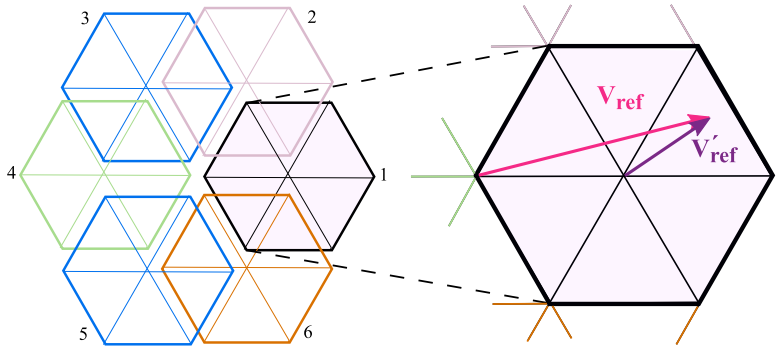
(b) Phase-shifted PWM [43].



(c) 1st sector of NTV-PWM [121].

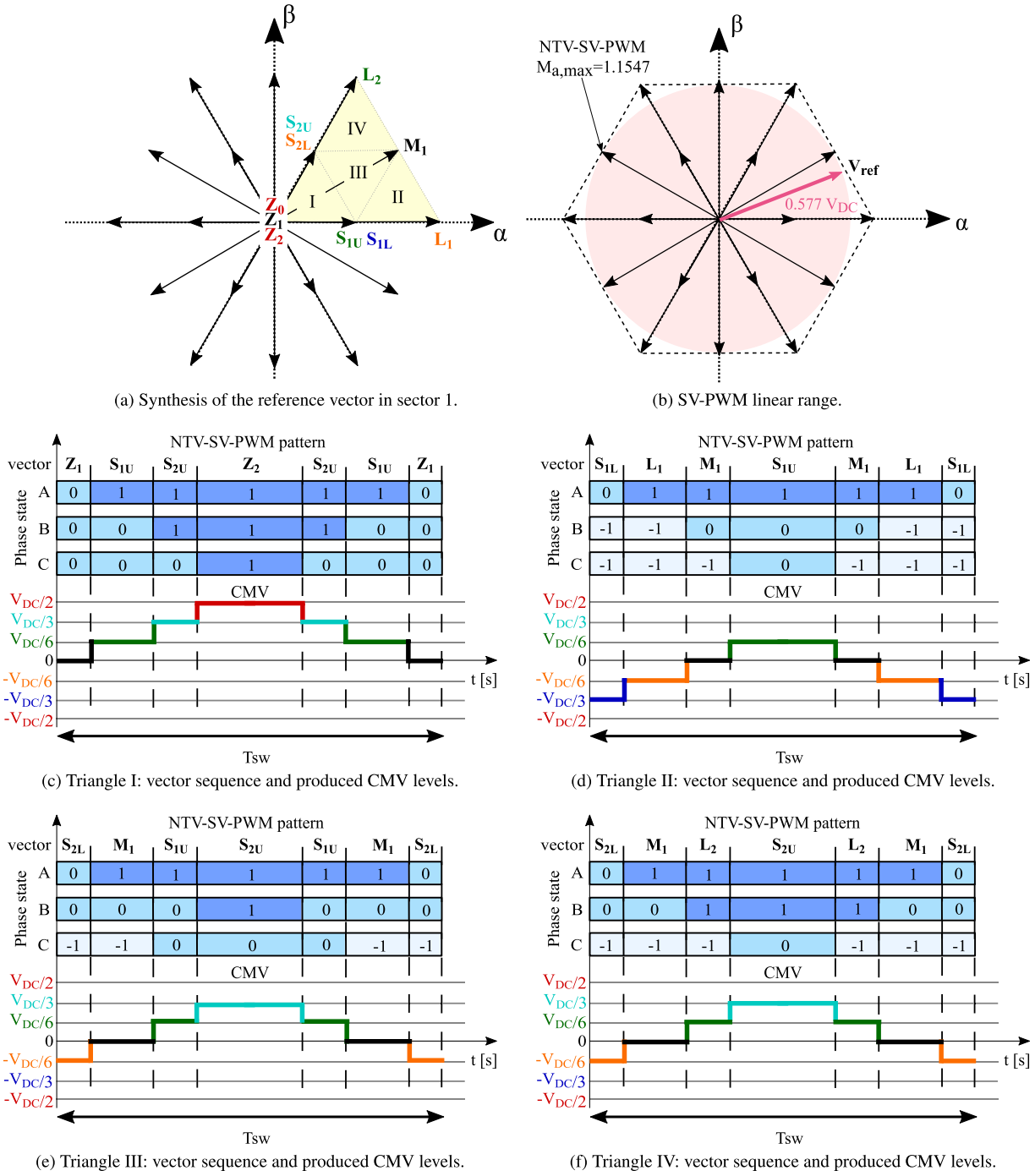


(d) 1st sector of Virtual SV-PWM [128].



(e) Simplified modulation to two-level SV-PWM [129].

FIGURE 9. **Some of the most common modulation techniques traditionally used in multilevel converters.**



(a) Synthesis of the reference vector in sector 1.

(b) SV-PWM linear range.

(c) Triangle I: vector sequence and produced CMV levels.

(d) Triangle II: vector sequence and produced CMV levels.

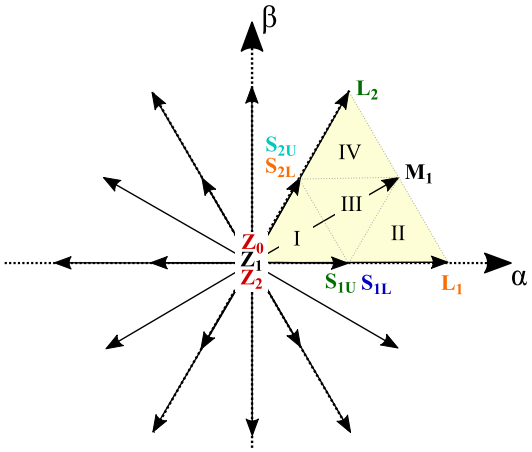
(e) Triangle III: vector sequence and produced CMV levels.

(f) Triangle IV: vector sequence and produced CMV levels.

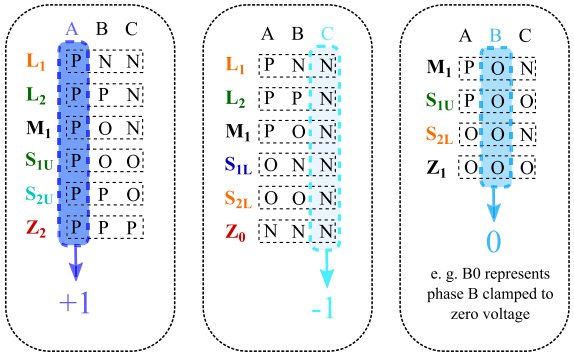
FIGURE 10. Vector representation of the NTV-SV-PWM technique for three-level converters along with the switching states and associated common-mode voltage levels.

where i represents each phase of the converter, and v_{Li} and v_{Ui} the lower-arm and upper-arm voltage of each phase (see Fig. 6c) [117]–[119].

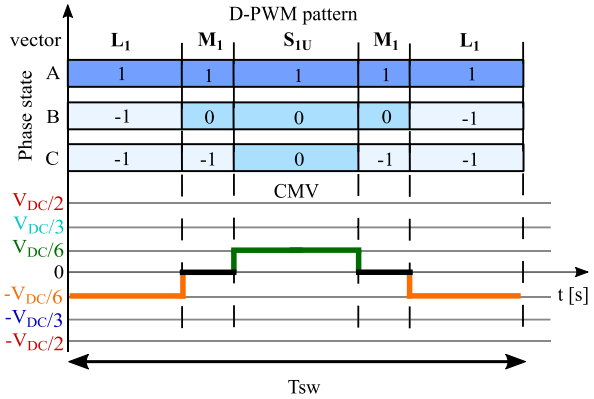
In any case, when traditional pulse-width modulation (PWM) techniques are employed in all these multilevel converters, such as traditional multilevel SV-PWM [120], [121], the CMV values shown in the Table III-A5 are obtained for three- and five-level converters [64], [108], [110]. The number of CMV values increases with the converter output levels (e.g. from 7 to 13 when increased from three to five levels). Consequently, Δ_S is smaller as the number of levels increases. Indeed, Δ_S is reduced from $1/6$ to $1/12$ when the



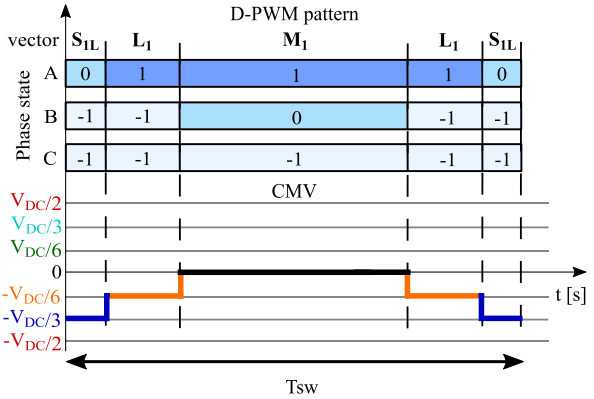
(a) Synthesis of the reference vector in sector 1.



(b) Classification of the vectors in 1st sector by phase voltage level.



(c) Example of a vector sequence with A-phase clamped to $V_{DC}/2$ (state 1) and generated CMV waveform.



(d) Example of a vector sequence with C-phase clamped to $-V_{DC}/2$ (state -1) and generated CMV waveform.

FIGURE 11. Vector representation of the D-PWM technique for three-level converters along with the switching states and associated common-mode voltage levels.

number of converter levels increases from three to five, which can be generalized as $\Delta_S = 1/(3n-3)$. Table 4 shows this last case for the most important multilevel topologies, as well as the main differences of each topology emphasizing their advantages and disadvantages.

Finally, and as it has been previously stated, it is worth noting that the reviewed multilevel architectures do not reduce the CMV by themselves. Thats is, a modification of the PWM algorithm is needed for that purpose. But, those advanced PWM algorithms are specific for multilevel topologies. On this basis, section IV-B reviews some of the most relevant PWM techniques to reduce the CMV in multilevel converters.

IV. ADVANCED MODULATION TECHNIQUES FOR COMMON-MODE VOLTAGE REDUCTION

The modulation schemes for multilevel converters have some differences from those of two levels. However, although each multilevel converter has its differences, the same modulation algorithm can generally be used for all converters as long as they have the same number of levels.[5] In this sense, the most important modulation techniques of multilevel converters, both conventional and for the reduction of CMV, are reviewed below.

A. CONVENTIONAL PWM TECHNIQUES FOR MULTILEVEL CONVERTERS

Multicarrier PWM are the most extended modulation techniques for controlling multilevel converters [122]. Like carrier based algorithms, this technique is based on comparing a high-frequency carrier, normally a triangular signal, with the modulation or reference signal. However, $n-1$ carriers are compared with the reference signal in the multicarrier PWM techniques, where n is the number of the output levels of the converter. The most common multicarrier PWM techniques can be classified as level-shifted (LS) and phase-shifted (PS) PWM respectively.

[5]Note that not all modulation techniques are used equally in all multilevel converters, some are proposed to solve particularities of each converter. For example, various modulation algorithms have been proposed to solve the problem of balancing DC bus capacitors in NPC converters [107], [108], [121].

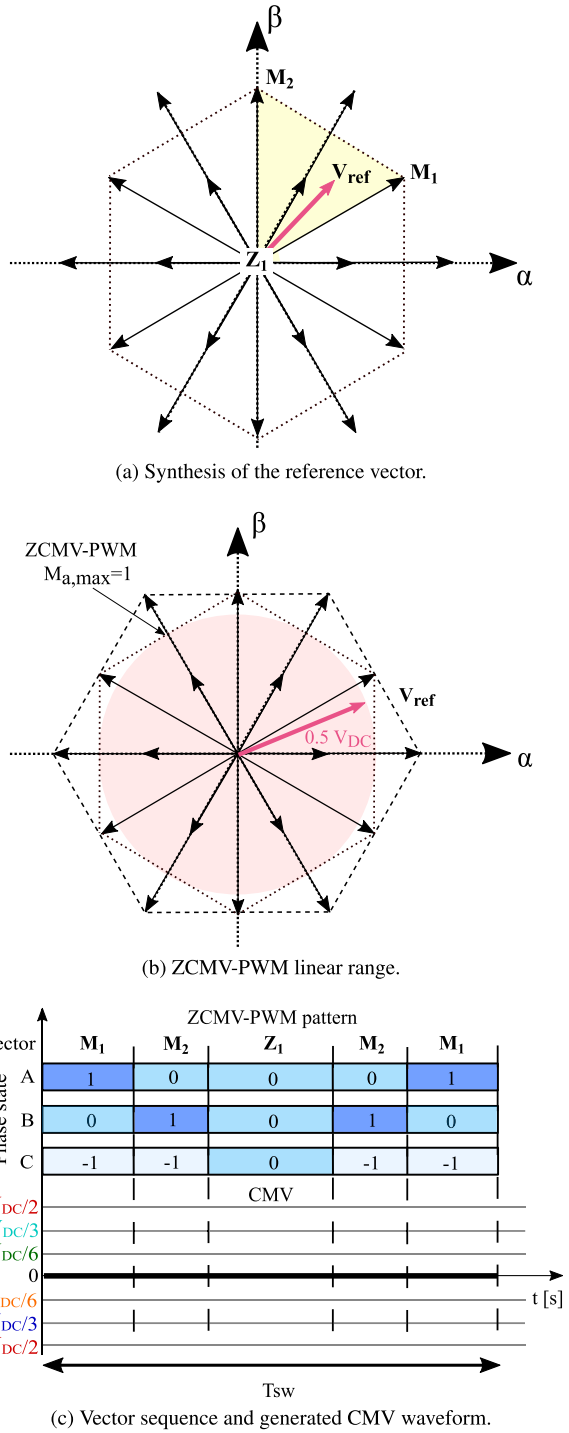


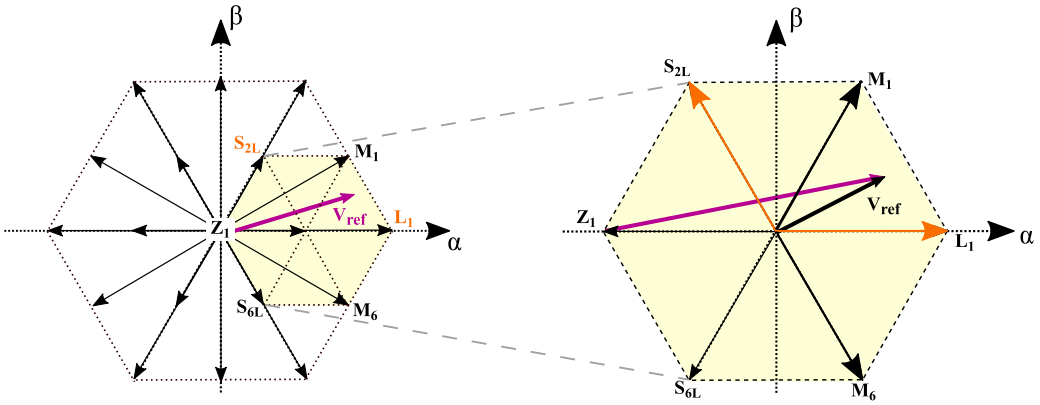
FIGURE 12. Vector representation of the ZCMV-PWM technique for three-level converters along with the switching states and associated common-mode voltage levels.

The LS-PWM techniques consist in distributing N carriers vertically along the modulation amplitude range, where the amplitude of the each carrier corresponds to $V_{DC}/(n-1)$ [123]. Depending on the phase disposition of the carriers, the LS-PWM can be divided into three different techniques [124]. The Phase-disposition PWM (PD-PWM) consists in using all the carriers with the same phase displacement. The alternative phase opposite disposition PWM (APOD-PWM) is based in shifting each carrier 180° from its adjacent carrier. In some converters, this technique can be used for reducing the third order harmonic component from the output voltage [125]. Finally, the Phase opposite disposition (POD-PWM) uses carriers in the negative range of the modulation signal that are 180° shifted from the carriers in the positive range of the modulation signal. Fig. 9a shows an example of PD-PWM which is well situated for NPC and T-Type multilevel converter. However, they are not suitable for other types of converters (CHB, FC, and MMC) [43].

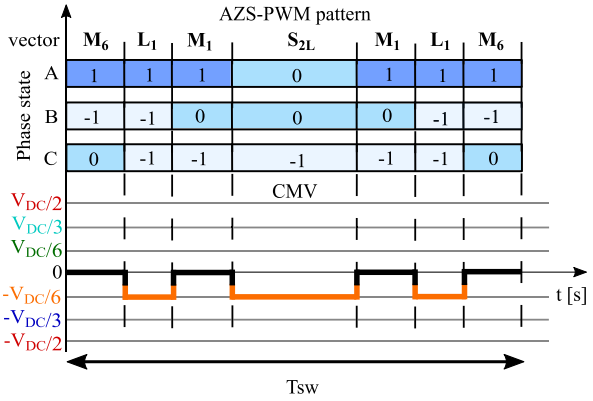
Phase-shifted PWM (PS-PWM) is another highly extended multicarrier modulation technique (Fig. 9b), because it eliminates all low order harmonic components of the output voltage [126] and is easy to implement. In this technique, the peak-to-peak amplitudes of the carriers corresponds to V_{DC}, but they are displaced in phase along the carrier period. That is, the phase displacement between carriers is $\Delta\phi = 2\pi/N$. This technique is suitable for converters such as CHB, FC and MMC. However, it is not suitable for NPC or T-type converter topologies [43].

Regarding SV-PWM, the SV diagram of the three-level multilevel inverters has been introduced according to the switching states of each converter in section III-B. Thus, Fig. 8a shows how this diagram is divided into six sectors as in two-level inverters. In this case, each sector is divided into four triangles labeled from I to IV; see Fig. 9c. This leads to several alternative algorithms to form the reference vector. The most typical is the Nearest three-vector PWM (NTV-PWM), which uses the nearest three states (nodes of the triangle containing the vector) to synthesize the desired voltage vector (see Fig. 9c). As the zero and small vectors can be generated by more than one switching state, different vector sequences can be applied to synthesize $\mathbf{V_{ref}}$ [120], [121], [127]. On the other hand, a more complex SV-based modulation technique and particular to NPC converters, named Virtual SV-PWM (VSV-PWM), allows to control voltage in *NP* over the full linear range on these converters [120], [128]. For it, a set of new virtual vectors is defined as a linear combination of the previous vectors (Fig. 9d). Other alternative for various multilevel converters is to use a conventional two-level three-phase SV-PWM, which is achieved by correcting the reference voltage vector, and dividing the vectorial space into smaller hexagons [129]; see Fig. 9e. Finally, although SVM is usually calculated in the $\alpha\beta$ plane it can also be represented in three-dimensional space (3D-SVM) [130], where apart from the α and β axes, the gamma axis is added in order to compensate harmonics and control the zero sequence in three-phase four-leg converters.

All in all, when comparing the multilevel converter SV with a two-level converter, there are certain similarities. On the one hand, the six large vectors are equivalent to the two-level converter active vectors [121]. Therefore, the same maximum reference vector is synthesized ($0.5773V_{DC}$) and $M_a \in [0, 1.1547]$. On the other hand, only using six



(a) Synthesis of the reference vector.



(b) Vector sequence and generated CMV waveform.

FIGURE 13. Vector representation of the AZS-PWM technique for three-level converters along with the switching states and associated common-mode voltage levels.

large vectors is not the best solution, the nearest vectors to $\mathbf{V_{ref}}$ (zero, small, medium or large) are the most appropriate alternatives in terms of their ability to minimize the switching frequencies of the power devices, improve the quality of the output voltage spectra, and the EMI [121]. In this sense, Fig. 10a shows the nearest vectors that are used to synthesize $\mathbf{V_{ref}}$ in sector 1, Fig. 10b shows the linear range (LR), and Figs. 10c to 10f show the switching state of each phase and the CMV produced by the converter in I to IV triangles.

Note that unlike the modulations for traditional two-level three-phase converter, different sequences of vectors can be applied within the same sector for each T_{SW} (one for each triangle). Therefore, the CMV waveform can also change in each case. Even so, in this case the CMV figures-of-merit are improved to $\Delta_P = 1/2, \Delta_S = 1/6, N_L = 4$ and $N_T = 6$ when comparing with the three-phase two-level inverter.

Despite the CMV is better than in their two-level counterparts, further improvement can be achieved with other modulation techniques. Therefore, the most featured algorithms for CMV reduction are reviewed below.

B. PWM TECHNIQUES FOR THE CMV REDUCTION

1) DISCONTINUOUS PWM TECHNIQUES

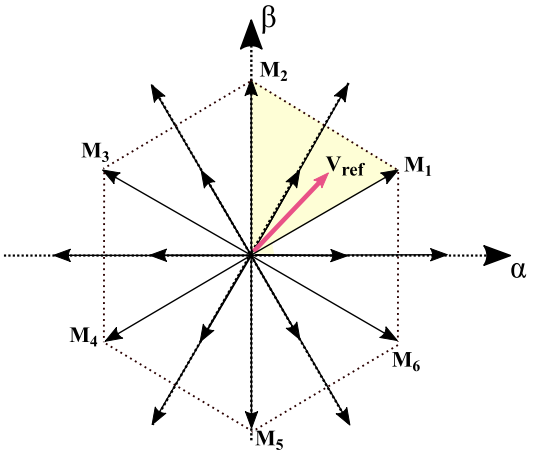
Discontinuous modulation techniques (D-PWM) for multilevel converters are discussed in detail in [131], [132]. As in multiphase converters, discontinuous modulation techniques for multilevel converters aim to reduce the number of commutations per switching period (T_{SW}). Thus, switching losses are reduced and consequently fewer CMV levels and transitions are produced. Fig. 11b shows the classification of the vectors in the first sector so that one of the phases remains clamped to certain voltage level. Likewise, Figs. 11c and 11d show two possible vector sequences in the second triangle. In these examples, the CMV figures-of-merit are $\Delta_P = 1/3$, $\Delta_S = 1/6$, $N_L = 3$ and $N_T = 4$. Furthermore, the LR of both modulation algorithms is the same as SV-PWM since the same vectors are used to synthesize $\mathbf{V_{ref}}$.

It should be pointed out that, despite several D-PWM techniques have been proposed [131], [132], their main objective is not reducing the CMV. So, in the following section RCMV-PWM techniques that have been prepared for this purpose are introduced.

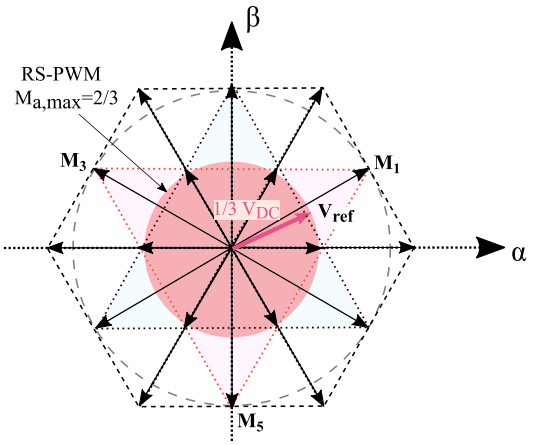
2) REDUCED-CMV PWM (RCMV-PWM) TECHNIQUES

a: ZERO-CMV PWM (ZCMV-PWM)

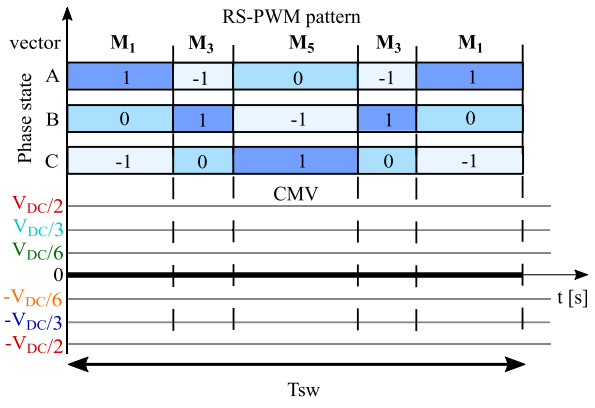
Unlike the other reviewed converters, multilevel converters are able to eliminate completely the CMV. The reason is that some commutation states produce 0 V CMV level. Thanks to this, if only the medium vectors ($\mathbf{M_{1-6}}$) and the $\mathbf{Z_1}$ vector are used to synthesize $\mathbf{V_{ref}}$, the CMV is completely



(a) Synthesis of the reference vector.

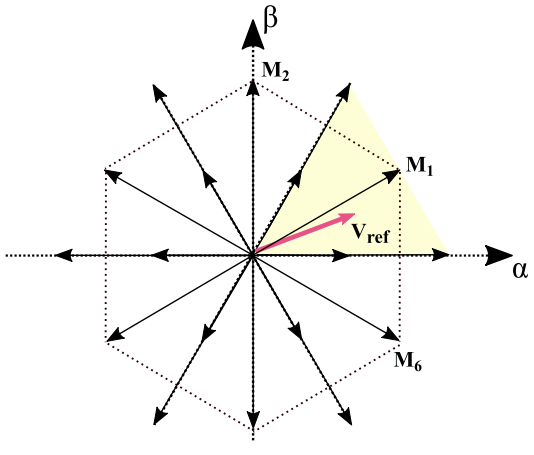


(b) RS-PWM linear range.

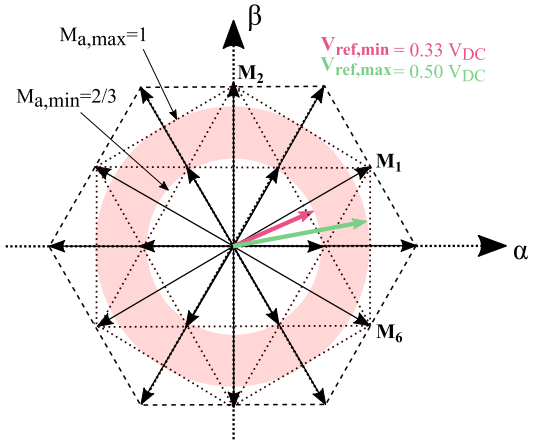


(c) Vector sequence and generated CMV waveform.

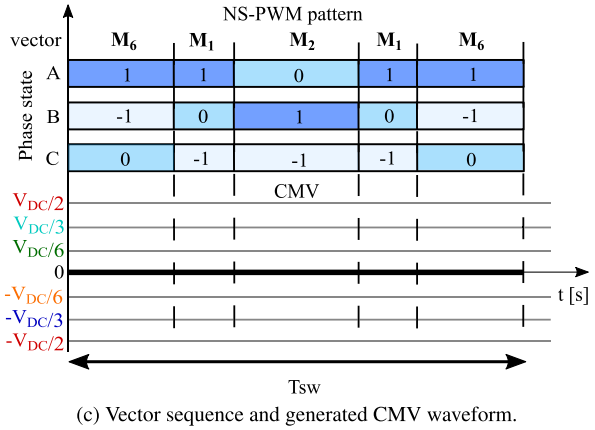
FIGURE 14. Vector representation of the RS-PWM technique for three-level converters along with the switching states and associated CMV levels.



(a) Synthesis of the reference vector.



(b) NS-PWM linear range.



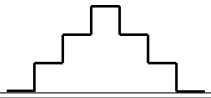
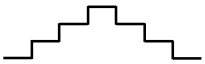
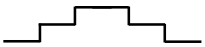
(c) Vector sequence and generated CMV waveform.

FIGURE 15. Vector representation of the NS-PWM technique for three-level converters along with the switching states and associated CMV levels.

eliminated [133], [134]. Fig. 12a shows the synthesis of $\mathbf{V_{ref}}$ for this modulation technique named Zero-CMV PWM (ZCMV-PWM). In this case, the LR is reduced compared to the conventional NTV-PWM and discontinuous modulations (Fig. 12b), where $M_a \in [0, 1]$ and $V_{ref,max} = 0.5V_{DC}$ [135]. However, the best CMV result is obtained from this modulation where $\Delta_P = \Delta_S = N_L = N_T = 0$ (see Fig. 12c).

Given the benefits of ZCMV-PWM in terms of the CMV, some variations of this technique have been investigated. For example, [75]–[77] have presented this modulation technique for five-level converters, where only 19 vectors producing

TABLE 5. Some of the most important modulation techniques to reduce CMV in multilevel converters.

Modulation technique	Figures-of-merit				Increase/decrease (%) over conventional SV-PWM				CMV waveform	Linear range	Refs.
	Δ_P	Δ_S	N_L	N_T	Δ_P	Δ_S	N_L	N_T			
Conventional two-level three-phase voltage source inverter											
Conventional SV-PWM	1	1/3	4	6	-	-	-	-		$0 \leqslant M_a \leqslant 1.15$	[38], [139]
Three-level three-phase inverters											
NTV-PWM	1/2	1/6	4	6	-50	-50	0	0		$0 \leqslant M_a \leqslant 1.15$	[120], [121], [127]
D-PWM	1/3	1/6	3	4	-66.7	-50	-25	-33.3		$0 \leqslant M_a \leqslant 1.15$	[131], [132]
ZCMV-PWM	0	0	0	0	-100	-100	-100	-100		$0 \leqslant M_a \leqslant 1$	[133], [134]
AZS-PWM	1/6	1/6	2	6	-83.3	-50	-50	0		$0 \leqslant M_a \leqslant 1.15$	[108]
RS-PWM	0	0	0	0	-100	-100	-100	-100		$0 \leqslant M_a \leqslant 0.66$	[135]
NS-PWM	0	0	0	0	-100	-100	-100	-100		$0.66 \leqslant M_a \leqslant 1$	[135]

0 V (of the total 125) are used to synthesize $\mathbf{V_{ref}}$. Likewise, in [136] modulation for seven-level converters is featured. On the other hand, [133] also investigates how to implement this technique in the carrier-based approach. Furthermore, in [76], [137] a generalized method based on carrier-based is proposed that serves for both CHB and NPC converters regardless the number of levels.

Considering the above, and given the existence of vectors that generate zero CMV, it is less common to find the classical modulation techniques named RCMV-PWM for multilevel converters. Nonetheless, there are still some works that review these techniques, which are explained below.

b: ACTIVE ZERO-STATE PWM (AZS-PWM)

Following the idea of Fig. 9e, a simplification of the three-level vectorial space to the conventional two-level scheme has been proposed in [108]. This simplification allows the use of the two-level AZS-PWM algorithm to reduce the CMV in multilevel converters. This modulation scheme combines two opposite active vectors to synthesize the zero vector. Fig. 13a shows the synthesis of the reference vector. The LR remains the same as NTV-PWM and discontinuous modulation techniques (all multilevel linear range). Finally, Fig. 13b shows the CMV waveform where its figures-of-merit values are $\Delta_P = \Delta_S = 1/6$, $N_L = 2$ and $N_T = 6$.

c: REMOTE-STATE PWM (RS-PWM)

In [135] two-level RS-PWM scheme is adapted to multilevel converters. This modulation only uses odd/even medium vectors to minimize the produced CMV. Fig 14a shows how $\mathbf{V_{ref}}$ is synthesized in multilevel converters when this algorithm is used. The main drawback of this modulation, as in two-level RS-PWM, is that the LR is dramatically reduced (see Fig 14b). Moreover, as all the medium vectors produce the same CMV, it cannot be improved more than ZCMV-PWM, therefore the CMV waveform is the same (see Fig. 14c), with: $\Delta_P = \Delta_S = N_L = N_T = 0$.

d: NEAR-STATE PWM (NS-PWM)

As in the previous one, the SV implementation resulting from using only medium vectors of NS-PWM is represented in [135]. In this modulation only the adjacent median vectors (see Fig 15a) are used to synthesize $\mathbf{V_{ref}}$ and therefore the LR is reduced as in two-level NS-PWM (see Fig 15b). Likewise, as all the medium vectors generate the same CMV, it cannot be improved more than ZCMV-PWM, therefore the CMV waveform again is identical of ZCMV-PWM (see Fig. 15c), with: $\Delta_P = \Delta_S = N_L = N_T = 0$.

3) OTHER MODULATION TECHNIQUES FOR CMV REDUCTION

In addition to the above techniques, other works have studied more modulation techniques for the CMV reduction which

usually avoid the switching states that generate the highest CMV levels (zero vectors) [107], [109]. However, more ambitious techniques for three-level converters [10], [77], [138] manage to limit the CMV waveform $\pm V_{DC}/6$ range, trying to find a balance between CMV and power losses or DC bus balancing.

As a summary, Table 5 shows the modulation techniques for multilevel converters reviewed in this section, which are compared to the conventional SV-PWM technique of a two-level three-phase VSI. As it can be seen, the multilevel converters together with the appropriate modulation technique, allow to reduce the CMV considerably compared to two-level VSI. In fact, there are techniques that reduce all defined figures-of-merit completely. However, techniques such as RS-PWM or NS-PWM reduce the linear range considerably, thus being the ZCMV-PWM more beneficial than the previous ones, both in CMV reduction and in signal quality.

V. CONCLUSION

Environmental pollution and climate change, among other problems, are driving a complete evolution of the current energy transformation methods towards a more sustainable and efficient 100% renewable energy conversion systems. In order to achieve this goal, power electronics not only play a crucial role as a tool for power conducting in renewable energy sources, but also for controlling motor speed and torque generation in electric machines by varying its input frequency and voltage. Indeed, power inverters are increasingly used to control the rotational speed of these machines and to condition the power provided by a energy source in practically all sectors, but especially in industry and electric transportation.

In such context, the key role of multilevel inverters in electric drives and its relation to common mode voltage has been discussed in this paper. From this review, it can be concluded that despite each multilevel topology has its pros and cons, they allow to synthesize waveforms with higher quality than two-level converters, as well as increase their voltage values and consequently their power ranges. In addition, all multilevel converters (considering the same number of levels) have the possibility of generating the same voltage at each phase output. Therefore, regarding the output voltage, the only difference between multilevel converters is that they can have a different number of redundant states and the switching states are converter topology dependent.

From the CMV point of view, it should be noted that multilevel converters are generally the most promising converters for reducing CMV, since they have redundant switching states (i.e. they synthesize the same output voltages). In this way, those states that generate the same CMV can be selected in order to eliminate CMV transitions. Furthermore, unlike other converters, these power inverters have the advantage that one of the CMV levels that they produced is 0 V, being possible to completely eliminate CMV.

Finally, regarding the modulation techniques oriented to the CMV reduction, the ZCMV-PWM technique for multilevel converters is apparently the most advantageous, both in terms of CMV and in its balance between power losses, signal quality and linear range. This technique achieves 100 % elimination of CMV. However, when modulation techniques are used to reduce CMV, other parameters are usually affected, regardless of whether the technique has been implemented following the carrier-based or space-vector approach. At this point, each technique can bring its own benefits, for example D-PWM techniques use the full linear range of SV and reduce switching losses. Although, these techniques does not improve CMV as much as others (only up to 66.7 % of Δ_P). Likewise, the AZS-PWM technique also uses the entire linear range and further improves the CMV (up to 83.3 % of Δ_P), but has the disadvantage of increasing the harmonic distortion of the converter output current. Therefore, the most suitable modulation technique will depend on the requirements of each application. And it will be up to each user to select the most suitable converter with its corresponding modulation technique that allows a reduced CMV.

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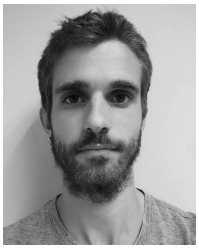

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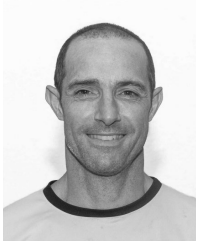

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