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New protection algorithms for HVDC grids

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RESUMEN

Los sistemas HVDC representan una alternativa prometedora para futuras expansiones del sistema eléctrico, interconexiones entre países y conexión de grandes plantas de generación localizadas en áreas remotas, gracias a las ventajas que presentan en comparación con el transporte convencional en corriente alterna. Además, el interés por desarrollar redes HVDC multiterminales ha crecido en los últimos años, sin embargo, su implementación se ha visto ralentizada debido a la complejidad que presenta la protección ante faltas en estos sistemas.

El objetivo principal de esta tesis es proponer un nuevo algoritmo de protección contra faltas, apropiado para redes HVDC multiterminales y capaz de superar las limitaciones presentes en algoritmos existentes. El algoritmo propuesto es un algoritmo de tensión de inductancia basado en el cálculo del ratio entre las medidas de tensión tomadas a ambos lados de la inductancia limitadora y la derivada de dicho ratio. Es capaz de detectar faltas rápidamente y de discriminar de manera selectiva entre faltas dentro y fuera de la zona de protección. También se propone una metodología para la selección del valor umbral necesario para la operación de algoritmos locales. Esta metodología tiene en cuenta tanto los escenarios de falta más perjudiciales, como los transitorios producidos por la apertura de un interruptor. A continuación, se desarrolla un esquema de protección completo que se compone de protecciones de línea primaria y de respaldo, protección de barra y protección ante fallo del interruptor. Esta última protección es, así mismo, un nuevo algoritmo propuesto en la tesis, que presenta una operación más rápida que algoritmos convencionales de detección de fallo en el interruptor.

La operación del esquema de protección propuesto es validada y analizada a través de simulaciones en un modelo de red de cuatro terminales con diferentes escenarios de falta, comparándolo con algoritmos existentes. De esta manera, se verifican las ventajosas características del algoritmo de detección de faltas propuesto y se demuestra que presenta una operación rápida y selectiva, así como una buena sensibilidad a faltas resistivas, lo cual es una limitación presente en los actuales algoritmos locales basados en el cálculo de la derivada.

ABSTRACT

HVDC systems are a promising solution for future expansions of power systems, new interconnections between nations and the connection of large power plants located in remote areas, due to their advantages in comparison with conventional HVAC transmission. Moreover, the interest in developing multi-terminal HVDC grids has increased the recent years, however, their implementation has been limited due to the complexity of achieving proper fault protection of these systems.

The main purpose of this thesis is to propose a novel fault protection algorithm which is suitable for multi-terminal HVDC grids and capable of overcoming the limitations of the existing fault protection algorithms. The proposed fault protection algorithm is an inductor-voltage algorithm based on calculating the ratio between the voltage measurements taken at both sides of the limiting inductor and its derivative. It is capable of achieving fast fault detection and selectively discriminating between faults inside and outside the protection zone. A methodology for the process of selecting adequate threshold values for the operation of local-measurement-based algorithms is also proposed. The threshold selection methodology takes into account the worst fault case scenarios and the transients induced by the opening of a circuit breaker. Then, a complete protection scheme is developed comprising link primary and backup protections, busbar protection and circuit breaker failure protection. The latter protection is also a novel algorithm proposed in this thesis, which presents faster operation than conventional circuit breaker failure algorithms.

The operation of the proposed protection scheme is validated and analysed through simulations in a four-terminal grid model against different fault cases, by comparing it with existing algorithms. This way, the advantageous features of the proposed fault protection algorithm are verified and it is demonstrated that it presents fast and selective operation and high sensitivity to high-resistance faults which is a limitation of existing local derivative-based algorithms.

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LIST OF ABBREVIATIONS

2L-VSC	Two-Level Voltage Source Converter
3L-VSC	Three-Level Voltage Source Converter
AC	Alternating Current
AC-CB	HVAC Circuit Breaker
ANN	Artificial Neural Network
BB	Busbar protection
BiP	Bipole configuration
BU	Backup Protection
CBF	Circuit Breaker Failure protection
Com	Communication-based algorithm
CSC	Current Source Converter
CWT	Continuous Wavelet Transform
DC	Direct Current
DC-CB	HVDC Circuit Breaker
DFT	Discrete Fourier Transform
DiffCurr	Differential Current algorithm
DTFT	Discrete Time Fourier Transform
DWT	Discrete Wavelet Transform
FB-MMC	Full-Bridge Modular Multilevel Converter
FCL	Fault Current Limiter
F_{det}	Fault Detection Method
FFT	Fast Fourier Transform
F_{iso}	Fault Isolation Method

F_{loc}	Fault Location Method
$F_{resistance}$	Fault Resistance
GPar	Grid Partition Method
GTO	Gate Turn-Off thyristor
HB-MMC	Half-Bridge Modular Multilevel Converter
H-CB	Hybrid DC-CB
HIF	High-Impedance Fault
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
I_{DC}	DC current
I_{fault}	Fault current at the fault point
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
I_{relay}	Fault current measured by the relay
LCC	Line commutated converter
LCL-VSC	Inductor-Capacitor-Inductor Voltage Source Converter
LIVRD	Limiting Inductor Voltage-Ratio-Derivative-based algorithm
LIF	Low-Impedance Fault
Loc	Local-Measurement-based algorithm
LV	Inductor-Voltage algorithm
M	Main protection
M-CB	Mechanical DC-CB
MMC	Modular Multilevel Converter
MonoP	Monopole configuration
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTDC	Multi-Terminal HVDC grid
MVDC	Medium Voltage Direct Current
NF	No Failure
NT	No Trip
OC	Overcurrent algorithm
OHL	Overhead Lines
P2P	Point-to-Point

PtG	Pole-to-Ground
PtP	Pole-to-Pole
ROC	Rate-Of-Change
ROCOC	Rate-Of-Change-Of-Current algorithm
ROCOV	Rate-Of-Change-Of-Voltage algorithm
$ROCOV_{bus}$	Bus-Side Voltage-Derivative
$ROCOV_{busMAXCBope}$	Maximum $ROCOV_{bus}$ induced by a DC-CB opening
S-MonoP	Symmetric Monopole configuration
SNR	Signal-to-Noise Ratio
SS-CB	Solid-State DC-CB
T	Trip
t_{BBd}	Detection time of the busbar protection
t_{BBo}	Operation time of the busbar protection
t_{CBFc}	Fault clearing time of the circuit breaker failure protection
t_{CBFd}	Detection time of the circuit breaker failure protection
t_{CBFi}	Initiation time of the circuit breaker failure protection
t_{CBFo}	Operation time of the circuit breaker failure protection
$t_{CBFstandby}$	Standby time of the circuit breaker failure protection
t_{CBFv}	Verification time of the circuit breaker failure protection
$t_{clearing}$	Fault Clearing Time
$t_{detection}$	Fault Detection Time
t_f	Fault inception time
t_{gpar}	Grid Partition Time
THR	Threshold value
$THR_{DiffCurr}$	Differential current threshold value
THR_{LV}	Inductor-voltage threshold value
THR_{OC}	Overcurrent threshold value
THR_{ROCOC}	ROCOC threshold value
THR_{ROCOV}	ROCOV threshold value
THR_{UV}	Undervoltage threshold value
t_{iso}	Fault Isolation Time
t_{loc}	Fault Location Time

t_{Pc}	Fault clearing time of the link primary protection
t_{Pd}	Detection time of the link primary protection
t_{Po}	Operation time of the link primary protection
UV	Undervoltage algorithm
V_{bus}	Bus-Side Voltage
V_{DC}	DC voltage
V_L	Voltage across the inductor
V_{link}	Link-Side Voltage
VR	Voltage-Ratio
VR_{extCV}	VR critical value for an external fault
VR_{intCV}	VR critical value for an internal fault
VR_{max}	Maximum VR value
VR_{min}	Minimum VR value
VRD	Voltage-Ratio-Derivative
VRD_{extCV}	VRD critical value for an external fault
VRD_{intCV}	VRD critical value for an internal fault
VRD_{max}	Maximum VRD value
VRD_{min}	Minimum VRD value
VSC	Voltage Source Converter
WT	Wavelet Transform
Δt_{BB}	Time window of busbar protection
Δt_{BU}	Time window of link backup protection
Δt_{CBF}	Time window of the circuit breaker failure protection
$\Delta t_{CBF\_ROCOVbus}$	Time window of the circuit breaker failure protection to verify DC-CB operation
Δt_P	Time window of link primary protection

Chapter 1.

INTRODUCTION

1.1. Context

Nowadays, the impacts of climate change are starting to be undeniably tangible. As a consequence, governments and organizations are taking actions in order to mitigate the aftermaths of climate change. The main cause for climate change is the emission to the atmosphere of carbon dioxide (CO_2) and other gasses from the burning of fossil fuels. This way, the most relevant steps in the pathway of climate change mitigation is the process of decarbonisation, i.e., the process of reducing CO_2 emissions. The energy sector, and in particular the electricity sector, is one of the major emitters. Thus, decarbonisation of the electrical system requires transforming the current power generation mix into a more efficient and cleaner system. For this aim, renewable energies are considered as the most suitable alternative to conventional fossil-fuel-based power generation.

The encouragement, promotion and support from institutions to install renewable power plants, combined with the reduction of costs that has happened in the last years, has produced an exponential growth in the renewable energy sector. However, this growth must continue the next decades in order to fulfil the objectives of climate change mitigation, such as the European Union's targets of reducing at least 55% the greenhouse gas emissions by 2030, compared to 1990 and of reaching a net-zero emissions balance by 2050 [1]. Moreover, the "Fit for 55" package establish an EU-level target where at least 40% of the overall European energy mix by 2030 must be produced by renewable energy sources [2]. For Spain, these objectives entail a 23% reduction of greenhouse gas emissions, in comparison

to 1990, and a 74% share renewable energy in the electricity generation by 2030 [3]. It is also expected to achieve a 100% of renewable-energy-based electricity generation and to make Spain carbon neutral by 2050 [3].

However, the availability of these resources is variable and dependent on the weather and the geographical location. A significant amount of these renewable power plants will be located in remote areas far away from load centres and/or where the accessibility to the conventional High Voltage Alternating Current (HVAC) transmission grid is limited.

A potential solution is the use of High Voltage Direct Current (HVDC) technology which can facilitate the integration of renewable generation into the electrical system since it presents some advantageous features:

- Lesser number of electrical conductors (two poles vs three phases) [4].
- Lower power losses transmitting the same amount of power [5].
- Lower costs for long transmission distance [6].
- Lower visual impact and footprint [7].
- Capability of interconnecting asynchronous AC systems [8].
- Capability of transmitting power through underground and undersea cables without being limited by the capacitive effect of HVAC transmission [9].

According to this, the critical transmission distances, where a HVDC alternative is more suitable than an equivalent HVAC solution, are 50 km for underground or undersea cables and 200 km for overhead lines [10]. This way, HVDC systems are forecasted as the most economical and promising solution for future expansions of the grid, new interconnections between nations or the connection of large power plants located in remote areas.

HVDC links have been employed since 1954 when the world's first HVDC link was installed in Sweden [10]. Nowadays, there are a large amount of HVDC links installed worldwide such as the two interconnections between Spain and France and the one between mainland Spain and the Balearic Islands:

- 237 km undersea interconnection between Valencia and Majorca is the first HVDC link in Spain and it was put into operation in 2012 [11].
- 64.5 km underground interconnection between Spain and France through the eastern Pyrenees was put into operation in 2015 [12].
- 370 km undersea interconnection between Spain and France through the Bay of Biscay is expected to start its construction in 2023 [13].

HVDC links have been commonly based on the conventional Current Source Converters (CSC) which employ thyristors as switching devices. This is a mature and widely-used conversion technology where the power flow direction is controlled by changing the voltage polarity [14]. However, it needs to be connected to a strong HVAC grid in order to avoid commutation failures in its operation. Thus, these characteristics make its application in weak, islanded or fluctuating renewable-energy-based systems challenging.

As it can be seen in Table 1.1 and Figure 1.1, all current HVDC systems put in operation in Europe have been Point-to-Point (P2P) links and several more P2P projects are planned for the next years. Likewise, a lot of offshore wind power plants are now under construction or are expected to be built in the next years in order to accomplish the targets established by the European Union. However, the connection of these offshore power plants to the onshore stations cannot be achieved by P2P links due to the high amount of links needed which makes this solution technically and economically not viable. Therefore, the interest in developing Multi-Terminal HVDC (MTDC) grids has increased in the recent years in order to improve the integration of renewable-energy-based generation into the power system. Moreover, MTDC grids are a more reliable and robust alternative in the case of a fault condition in the system in comparison to P2P links. The HVDC system is completely shut down during a fault condition in a P2P link while the power flow can continue and be transmitted among the terminals through the healthy links when a fault condition happens in a MTDC grid.

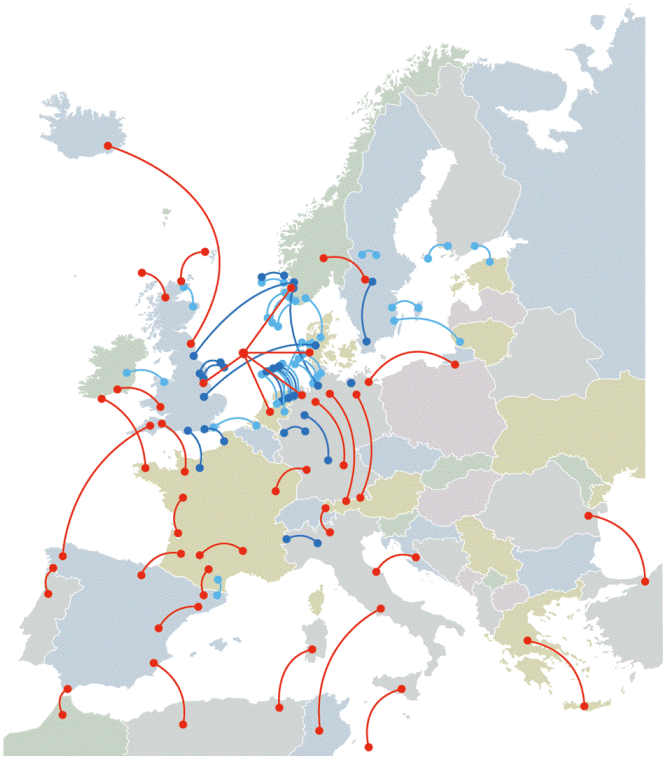

Figure 1.1.- VSC-based HVDC projects in Europe (installed projects in dark blue, under construction projects in light blue and planned projects in red) [17].

Table 1.1.- Installed or planned HVDC projects in Europe [Part 1 of 2].

Project	Countries involved	Length (km)	Voltage (kV)	Power (MW)	Year	Type
Skagerrak 1+2 [18]	Denmark-Norway	230	250	500	1977	CSC
Gotland 2 [19]	Sweden	99.5	150	130	1983	CSC
IFA [20]	France-UK	72	270	2000	1986	CSC
Gotland 3 [19]	Sweden	98	150	130	1987	CSC
Konti-Skan 2 [21]	Denmark-Sweden	147	285	300	1988	CSC
Fenno-Skan [22]	Finland-Sweden	233	400	500	1989	CSC
SACOI 2 [23]	Italy-France	422	200	300	1992	CSC
Skagerrak 3 [18]	Denmark-Noway	230	350	440	1993	CSC
Baltic Cable [24]	Germany-Sweden	262	450	600	1994	CSC
Kontek [25]	Denmark-Germany	170	400	600	1996	CSC
SwePol [26]	Poland-Sweden	245	450	600	2000	CSC
GRITA [27]	Italy-Greece	310	400	500	2001	CSC
Moyle [28]	UK	63.5	250	500	2001	CSC
Estlink [29]	Finland-Estonia	105	150	350	2006	VSC
NorNed [30]	Netherlands-Norway	580	450	700	2008	CSC
StoreBælt [31]	Denmark	56	400	600	2010	CSC
BritNed [32]	UK-Netherlands	245	450	1000	2010	CSC
Romulo [11]	Spain	237	250	400	2011	CSC
Fenno-Skan 2 [22]	Finland-Sweden	303	500	800	2011	CSC
SAPEI [33]	Italy	435	500	1000	2011	CSC
BorWin1 [34]	Germany	200	150	400	2012	VSC
East West Interconnector [35]	Ireland-UK	130	200	500	2012	VSC
Estlink 2 [36]	Finland-Estonia	171	450	650	2014	CSC
HelWin1 [37]	Germany	130	250	576	2015	VSC
HelWin2 [38]	Germany	130	320	690	2015	VSC
NordBalt [39]	Sweden-Lithuania	450	300	700	2015	VSC
Skagerrak 4 [18]	Denmark-Norway	244	500	700	2015	VSC
BorWin2 [40]	Germany	200	300	800	2015	VSC
DolWin1 [41]	Germany	165	320	800	2015	VSC
SylWin1	Germany	205	320	864	2015	VSC
INELFE [12]	Spain-France	64	320	2000	2015	VSC
DolWin2 [42]	Germany	135	320	900	2016	VSC
DolWin3 [43]	Germany	160	320	900	2017	VSC
Caithness - Moray Link [44]	UK	160	320	1200	2018	VSC
Western HVDC Link [45]	UK	422	600	2200	2018	CSC
COBRAcable [46]	Denmark-Netherlands	325	320	700	2019	VSC
BorWin3 [47]	Germany	200	320	900	2019	VSC
Nemo Link [48]	Belgium-UK	140	400	1000	2019	VSC

Table 1.1.- Installed or planned HVDC projects in Europe [Part 2 of 2].

Project	Countries involved	Length (km)	Voltage (kV)	Power (MW)	Year	Type
ALEGrO [49]	Belgium-Germany	100	320	1000	2020	VSC
IFA-2 [50]	France-UK	204	320	1000	2021	VSC
North Sea Link [51]	Norway-UK	730	515	1400	2021	VSC
NORD.LINK [52]	Norway-Germany	623	525	1400	2021	VSC
ElecLink [53]	France-UK	70	320	1000	2022	VSC
NorthConnect [54]	Norway-UK	665	525	1400	2022	VSC
DolWin6 [55]	Germany	90	320	900	2023	VSC
Viking Link [56]	Denmark-UK	765	525	1400	2023	VSC
Shetland HVDC Connection [57]	UK	260	320	600	2024	VSC
DolWin5 [58]	Germany	130	320	900	2024	VSC
Dogger Bank Interconnector [59]	UK	207	320	1200	2024	VSC
FAB Link [60]	France-UK	210	320	1400	2025	VSC
SuedLink DC [61]	Germany	700	525	2000	2027	VSC

Moreover, the development of the modern Voltage Source Converters (VSC) allows an easier implementation of MTDC grids in comparison to CSCs due to its improved power flow controllability and flexibility [4], which allows efficient power transmission from fluctuating and renewable energy sources and improves HVAC system stability during transients [4]. Some VSC-based MTDC systems have been commissioned during the last decade encouraged by the advantages of VSCs over the conventional CSCs:

- A VSC-based MTDC system was commissioned in 2013 in Nan'ao Island, China [15]. It consists of a three-terminal system connecting two converters (100, 50 MVA) located in the island of Nan'ao to a 200 MVA converter located in mainland China [16]. The future integration of a fourth terminal is expected.

- A 200 kV five-terminal VSC-based system was commissioned in Zhoushan archipelago (China) in 2014. It interconnects the most power-consuming islands of the archipelago (Zhoushan, Daishan, Qushan, Yangshan and Sijiao) and integrates wind power.

- The 3000 MW, 500 kV four-terminal Zhangbei MTDC project was put into operation in 2020. It transmits the renewable energy generated in the Hebei province to Beijing [62], [63]. Two of the converter stations are connected to wind power plants, another converter station is a pumped-storage hydropower plant, which suppresses the wind power fluctuations, and the Beijing converter station is the receiving terminal.

Nevertheless, these projects have been conceived us demonstrators, and in their operation, there have been several issues regarding fault protection [64]. Fault conditions have caused a blackout in the system. Accordingly, fault protection remains as one of the biggest challenges in the implementation of MTDC grids. Fault conditions in DC systems induce a sharp collapse of the voltage and a fast rate-of-rise of the fault current due to low system resistance. Moreover, the fast rate-of-rise of the fault current becomes a more constraining feature when VSCs are employed, since they are relatively vulnerable to overcurrents and the DC fault current magnitude can reach damaging levels in less than 10 ms. Another concern presented in fault protection of HVDC systems is that, conversely to HVAC systems, the fault current does not present a "natural" current zero-crossing, which increases the complexity of fault protection. A current zero-crossing must be created in order to interrupt the fault current. Therefore, fault protection of VSC-based systems must overcome the following technical challenges:

- The development of fast and selective protection algorithms.
- The development of fast HVDC circuit breakers capable of creating current zero-crossings, of interrupting high currents and of absorbing high energy.

This thesis focuses on HVDC systems, specifically on the protection of multi-terminal grids employing VSCs. Thus, characteristics of VSCs, system configurations and DC faults are overviewed as well as the different current breaking devices and fault-clearing strategies found in the literature. However, this work is particularly focused on fault detection algorithms, so its main objective is to propose a novel fault protection algorithm able to selectively and sensitively detect DC faults. This way, different types and classifications of fault protection algorithms found in the literature are thoroughly reviewed in order to obtain their characteristics and limitations. According to this, advantageous features are selected and a novel protection algorithm is proposed. The proposed algorithm is comprehensively analysed and evaluated against different fault case scenarios and finally compared with existing algorithms, so as to validate its proper performance.

1.2. Objectives

The purpose of this thesis is to propose a novel fault protection algorithm which is suitable for protecting VSC-based MTDC grids. The proposed fault protection algorithm specifically must overcome the limitations presented in existing algorithms. This way, it has to allow fast, selective and sensitive operation by only employing local measurements. In order to accomplish this goal, the following partial objectives must be achieved:

- Analyse the advantages and limitations of existing fault protection algorithms found in the literature.

- Analyse how to improve or overcome the limitations of existing fault protection algorithms in order to propose a novel fault protection algorithm.
- Develop a complete protection scheme comprising not only link primary protection, but also link backup protection, busbar protection and circuit breaker failure protection.
- Evaluate the influence of parameter variation on the performance of the proposed fault protection algorithm.
- Verify the advantageous features of the proposed fault protection algorithm in comparison with existing fault protection algorithms.

1.3. Structure of the thesis

This thesis is organized and structured in six chapters.

Chapter 1 introduces the aims of this work. Chapter 2 to Chapter 5 are related to fulfilling the objectives of this thesis. This way, Chapter 2 gives a general perspective of VSC-based HVDC systems. Different VSC topologies and submodule types are presented as well as system configurations and DC fault characteristics. Moreover, relevant elements of a protection system are also overviewed. Characteristics of HVDC Circuit Breakers (DC-CB) are presented and analysed according to the employed technology, i.e., mechanical, solid-state and hybrid DC-CBs. Classification of the common fault-clearing strategies used in HVDC systems is also detailed. Then, fault protection algorithms are classified into local-measurement-based and communication-based algorithms according to their characteristics and how they take the measurements needed for their operation. Afterwards, another classification is provided including current-based, voltage-based, traveling-wave-based and artificial-intelligence-based algorithms. In addition, fault protection algorithms found in the literature according to the latter classification are reviewed in order to obtain their advantageous features and limitations.

Chapter 3 provides the theoretical definition of the novel proposed inductor-voltage-based fault protection algorithm. This algorithm is capable of quickly achieving fault detection and also fault discrimination between forward and backward faults by only using locally-available voltage measurements taken at both sides of the limiting inductor. This way, it uses the difference of voltage produced by the damping characteristic of the limiting inductors. Hence, selective fault discrimination is achieved by calculating the ratio between both voltage measurements and fast fault detection is achieved by calculating the derivative of the voltage-ratio. Moreover, a complete protection scheme comprising link primary

and backup protections, busbar protection and circuit breaker failure protection is introduced.

Chapter 4 introduces a methodology for the process of selecting adequate threshold values for local-measurement-based algorithms and, particularly, for the novel fault protection algorithm. Moreover, the performance of the proposed protection scheme is analysed through simulations in a four-terminal grid model using PSCAD software. All segments of the proposed protection scheme, link protection, busbar protection and circuit breaker failure protection, are evaluated against different fault case scenarios while varying the fault parameters (fault type, fault resistance and fault location). In addition, the influence of other system parameters on the operation of the proposed fault protection algorithm is also analysed. These parameters are limiting inductor size, sampling frequency and noise disturbance, as well as fault location. This way, the proposed protection scheme is thoroughly validated through simulations.

Chapter 5 presents a comparison of the proposed fault protection algorithm with other commonly-used fault protection algorithms. The comparison only comprises local-measurement-based algorithms due to their fast operation speed and since the proposed fault protection algorithm fits into that classification. The comparison is divided into two parts. The first part includes the link primary protection and the second part involves the circuit breaker failure protection. The former part compares the proposed fault protection algorithm with the overcurrent algorithm, the undervoltage algorithm, the inductor-voltage algorithm, the rate-of-change-of-current algorithm and the rate-of-change-of-voltage algorithm. The latter part of the comparison studies the proposed circuit breaker failure protection algorithm against a conventional algorithm. This way, the advantages of the proposed fault protection scheme are highlighted while it is demonstrated that it overcomes the limitations found in the common and conventional fault protection algorithms.

Finally, Chapter 6 summarizes the contributions and conclusions extracted from the development of this thesis along with some possible future research lines.

Additionally, two appendices are included in this work. Appendix-A presents in more detail the grid model employed for the evaluation and analysis of the proposed fault protection scheme. Appendix-B presents additional results extracted from the comparison made in Chapter 5.

1.4. Main contributions

The main contributions of this thesis are presented hereunder:

- A methodology for the process of selecting adequate threshold values for local-measurement-based algorithms through simulations. This methodology uses the

worst fault case scenarios and the transients induced by the opening of a DC-CB. This way, selective and sensitive operation is ensured.

- A novel local-derivative-based fault protection scheme which is capable of fast fault detection and selective fault discrimination between forward and backward faults. It is also sensitive to high-resistance faults.

- A complete protection scheme based only on local measurements comprising link primary and backup protections, busbar protection and circuit breaker failure protection.

- A novel circuit breaker failure protection adapted to DC-CBs which is faster than conventional approaches and, thus, it is suitable for its application to VSC-based grids.

1.5. List of publications

The work of this thesis has produced 14 publications: 7 scientific journal publications (one of them is currently under review), 6 contributions to international conferences and 1 book chapter which is pending publication.

Scientific Journal Publications

1. **M. J. Pérez-Molina**, D. M. Larruskain, P. Eguia and V. Valverde, "Local derivative-based fault detection for HVDC grids", IEEE Transactions on Industry Applications, vol. 58, (2), pp. 1521-1530, 2022. DOI: 10.1109/TIA.2021.3138367

2. **M. J. Pérez-Molina**, D. M. Larruskain, P. Eguia and O. Abarrategi, "Circuit Breaker Failure Protection Strategy for HVDC Grids", Energies, vol. 14, (14), 2021. DOI: 10.3390/en14144326

3. **M. J. Perez-Molina**, D. M. Larruskain, P. Eguia Lopez, G. Buigues and V. Valverde, "Review of protection systems for multi-terminal high voltage direct current grids", Renewable and Sustainable Energy Reviews, vol. 144, 2021. DOI: 10.1016/j.rser.2021.111037

4. **M. J. Pérez-Molina**, D. M. Larruskain, P. Eguía López and G. Buigues, "Challenges for Protection of Future HVDC Grids", Frontiers in Energy Research, vol. 8, 2020. DOI: 10.3389/fenrg.2020.00033

5. **M. J. Pérez Molina**, D. M. Larruskain, P. Eguía López and A. Etxegarai, "Analysis of Local Measurement-Based Algorithms for Fault Detection in a

Multi-Terminal HVDC Grid", Energies, vol. 12, (24), 2019. DOI: 10.3390/en12244808

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Chapter 2.

CHARACTERISTICS OF HVDC PROTECTION FOR VSC-BASED GRIDS

Protection of HVDC systems presents higher complexity in comparison with HVAC systems due to the absence of a “natural” current zero-crossing, which is exploited by conventional HVAC protection systems to achieve fault current interruption [65], [66]. Additionally, the fault condition induces a sharp voltage drop and a fast rate-of-rise of the current due to the low impedance of the HVDC grid [67]. The fault-induced traveling waves spread throughout the system in a very short range of time. If VSCs are employed, this situation is even more critical due to the Insulated Gate Bipolar Transistors’ (IGBT) low overcurrent withstand capability [68], up to twice their rated current [69], [70]. If the fault is not quickly cleared, the VSC’s components can be damaged and the entire HVDC grid can be lost with the corresponding large blackout. Consequently, very fast and reliable protection systems are needed in order to avoid this problematic situation [71]. Fault detection, location and clearance must be achieved in a very limited time range, which is assumed to be less than 10 milliseconds [72]. This circumstance is even more restrictive for VSCs without fault-blocking capability since they will depend completely on the protection system for fault clearance. Meanwhile, fault-blocking converters, those who can control the fault current, are not as constrained but they still need a fast protection system in order to quickly remove the effects of the fault and stop its propagation throughout the system. Therefore, appropriate DC-CBs, fault protection algorithms, and fault-clearing strategies have to be developed and

to be adopted so as to minimize the fault condition's effects in both HVDC and HVAC systems.

Fault conditions are dangerous for both system equipment and people. Therefore, faults must be detected, located, isolated and cleared as quickly as possible [5]. HVDC protection systems need to be capable of ensuring safety and minimizing fault impact and component stress. Consequently, their operation must satisfy some performance requirements [73], [74].

A protection system must be sensitive and selective enough to detect all relevant faults while differentiating between internal and external faults to its protection zone. In that sense, it must only operate in case of internal faults so as to ensure an accurate performance. Operation in case of external faults should only be achieved if backup protection is needed. Likewise, system stability must be reached after fault clearance.

However, the most restrictive and critical requirement for the protection of VSC-based systems is the speed requirement due to the fast rate-of-rise of the fault current and the low overcurrent withstand capability of the VSC's components.

This chapter presents in subsection 2.1 the characteristics of VSCs and the different topologies that have been developed over the last decades. Afterwards, the diverse ways that a HVDC system can be configured are explained in subsection 2.2. Fault characteristics in HVDC systems are detailed in subsection 2.3. Then, overviews of breaking devices and fault-clearing strategies are presented in subsections 2.4 and 2.5, respectively, while protection algorithms are the main focus of subsection 2.6.

The work presented in this chapter has been published in:

M. J. Pérez-Molina, D. M. Larruskain, P. Eguía López and G. Buigues, "Challenges for Protection of Future HVDC Grids", Frontiers in Energy Research, vol. 8, 2020.

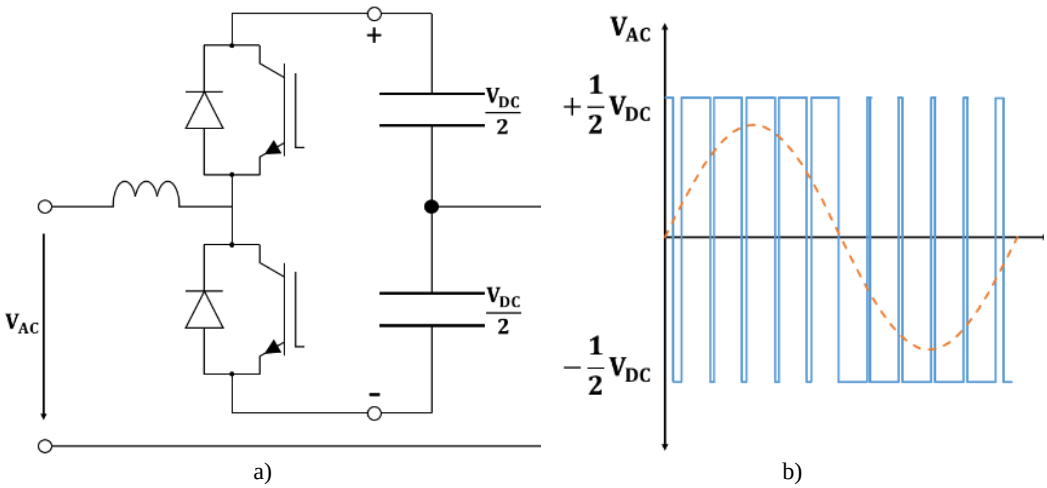
M. J. Perez-Molina, D. M. Larruskain, P. Eguia Lopez, G. Buigues and V. Valverde, "Review of protection systems for multi-terminal high voltage direct current grids", Renewable and Sustainable Energy Reviews, vol. 144, 2021.

2.1. Voltage source converters

Voltage source converters use IGBTs as switching devices instead of the thyristors of conventional CSCs. Therefore, they do not need to be connected to a strong AC system as in the case of CSCs. In addition, these converters employ standard transformers, they can control the magnitude, phase and frequency of the AC voltage allowing independent control of the active and reactive power and they present a smaller footprint and black start capability [75], [76]. These converters keep the voltage output constant [77] and achieve power reversal by changing the current polarity [76]. The improved power controllability and flexibility of VSCs makes easier to implement MTDC grids. A typical three-phase VSC topology is formed by three legs and two arms per leg; the upper and lower arms are connected to the DC positive and negative terminals, respectively. Each leg's midpoint is connected to its respective AC phase. Nowadays, the most common topologies of VSCs are the two-level, three-level and modular multilevel converters [78].

2.1.1. Two-level voltage source converter

The two-level topology, shown in Figure 2.1-a, was the first topology of VSC to be developed. Comparing with CSCs, it presents smaller filtering requirements and approximately half-size footprint. Conversely, it presents weak overcurrent withstand capability, electromagnetic interference generation and high insulation requirements. The two-level topology only produces two output voltage levels (Figure 2.1-b) resulting on high switching losses and harmonic distortion [76]. Hence, harmonic filters are needed due to the square waveform of the generated voltage [79].

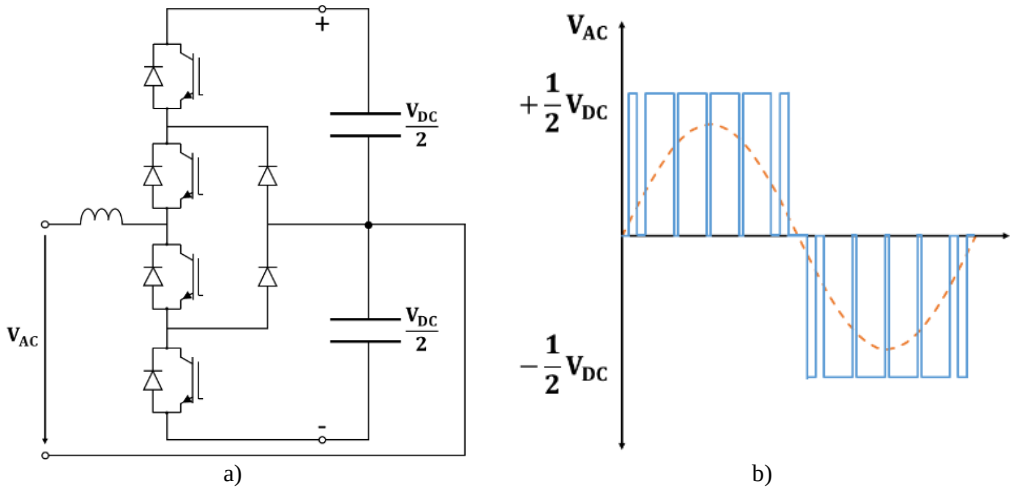


a) b)

Figure 2.1.- Two-level topology a) Scheme (one phase) and b) Voltage output.

2.1.2. Three-level voltage source converter

The three-level diode clamped or neutral point clamped topology presents four IGBT valves, two clamping diode valves and a capacitor, which is split in two series-connected branches. The diode valves are connected to the capacitor midpoint [80], as depicted in Figure 2.2-a. Then, the converter's voltage output varies between $+\frac{1}{2}V_{DC}$, zero and $-\frac{1}{2}V_{DC}$ [76], as it is shown in Figure 2.2-b. This topology presents a reduced switching frequency, and therefore reduced switching losses, voltage stress and insulation requirements. However, the capacitor voltage presents high ripple and needs a complex balancing control, i.e., one of the capacitors cannot be charged until the other capacitor is introduced into the conducting path [76]. In addition, it presents a challenging operation during asymmetrical AC faults due to difficulties on keeping the DC capacitor voltage balanced.



a) b)

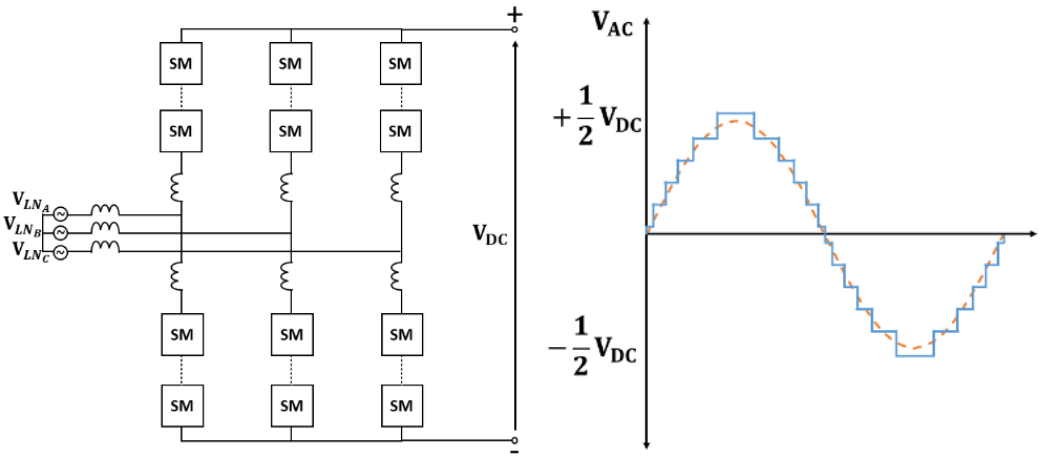
Figure 2.2.- Three-level topology a) Scheme (one phase) and b) Voltage output.

2.1.3. Modular multilevel converter

The Modular Multilevel Converter (MMC) is the most recent topology. Each arm is composed of a large number of identical submodules connected in cascade in series with an inductor [81], as it is shown in Figure 2.3-a. These submodules function as controlled voltage sources [82], [83] and their cascading connection produces high quality high voltage waveforms. Figure 2.3-b depicts the AC voltage generated by sequentially switching the submodules.

The MMC topology presents some advantages over the two-level VSC topology: greater robustness, smaller footprint and higher AC current quality due to the larger number of generated voltage levels, which reduce the voltage stress, the insulation requirements as well as the harmonic content and, consequently, the filtering requirements [78], [79]. In addition, this topology allows easy scalability of the

number of voltage levels and the voltage output [84], smaller converter switching losses due to lower switching frequency requirements of the submodules [85], [86] and reduced manufacturing costs since the submodules present the same structure [87]. They also present better performance than the three-level topology during AC faults. However, the control requirements are higher. There are three different configurations of MMCs regarding the type of submodule employed: half-bridge, full-bridge and hybrid MMCs.



a) b)

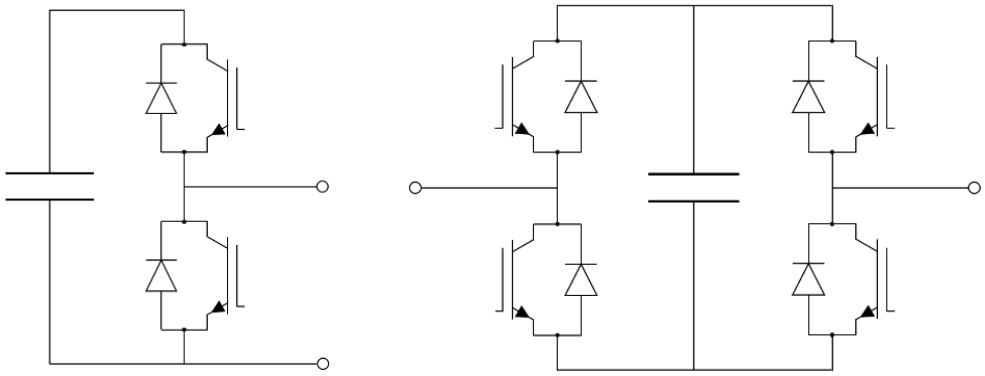
Figure 2.3.- Modular multilevel topology a) Scheme and b) Voltage output.

2.1.3.1 Half-bridge modular multilevel converter

Figure 2.4-a depicts a half-bridge submodule which consists of two IGBTs with two anti-parallel diodes and a capacitor. Half-bridge submodules can only produce a positive voltage and a zero voltage value. This configuration presents the disadvantage of becoming an uncontrolled-rectifier when the submodules are blocked by its internal overcurrent protection, i.e., the AC grid keeps feeding the DC fault current through the anti-parallel diodes.

2.1.3.2 Full-bridge modular multilevel converter

As it is shown in Figure 2.4-b, a full-bridge submodule consists of four IGBTs with four anti-parallel diodes in H bridge arrangement and a capacitor [88]. Hence, it can produce positive, zero and negative voltage values and it allows control and interruption of the DC fault current by reversing the voltage polarity and reactive power support during DC fault conditions. Full-bridge MMCs are also called fault-tolerant or fault-blocking converters since they can control the DC fault current. However, this configuration involves twice the components of a half-bridge submodule and thus it doubles the semiconductor losses.



a) b)

Figure 2.4.- Scheme of the MMC a) half-bridge submodule and b) full-bridge submodule.

2.1.3.3 Hybrid modular multilevel converter

The hybrid MMC combines the advantages of the two previously-mentioned topologies by employing both half-bridge and full-bridge submodules as it is shown in Figure 2.5 [78]. Thus, a certain number of the converter's submodules are configured following the half-bridge topology and the remaining submodules follow the full-bridge topology. Thus, costs and semiconductor losses are reduced in comparison with a full-bridge MMC thanks to the lower number of components employed. Moreover, full-bridge submodules enable the control of DC fault current. Hence, hybrid MMCs are fault-tolerant converters.

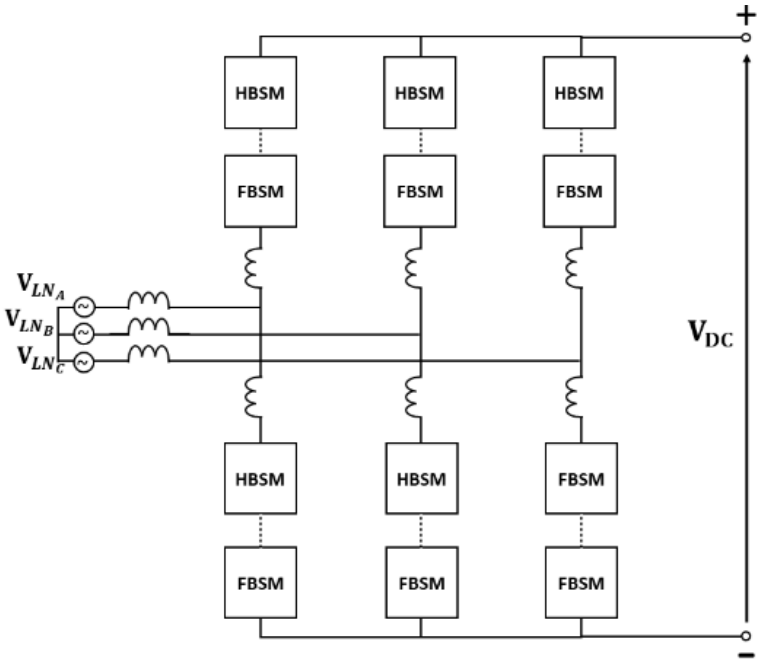


Figure 2.5.- Scheme of the hybrid MMC topology.

2.2. HVDC system configurations

A HVDC system can be configured in back-to-back, asymmetric-monopole, symmetric-monopole or bipole configurations according to the number of converters and poles.

2.2.1. Back-to-back configuration

Figure 2.6 shows the back-to-back configuration which is frequently used to interconnect asynchronous AC systems [89]. It is characterised by having both converters located at the same converter station and, thus, the transmission distance is very short.

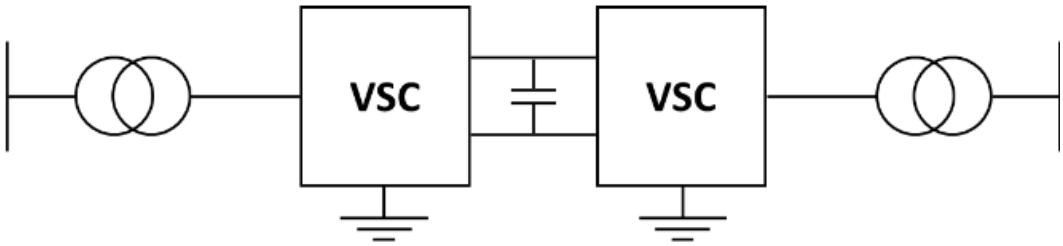


Figure 2.6.- Back-to-back configuration.

2.2.2. Asymmetric-monopole configuration

The asymmetric-monopole configuration presents two converters interconnected by one pole, usually working with negative voltages since the corona effect is lower [90], [91]. The return current flows through the ground or through a dedicated metallic return cable as it is shown in Figure 2.7-a and Figure 2.7-b, respectively. The second option is usually preferred due to environmental restrictions regarding ground currents [92].

2.2.3. Symmetric-monopole configuration

The symmetric-monopole configuration consists of two converters interconnected by two poles, positive and negative, as it is depicted in Figure 2.8. Since it is operated as a monopole, the link cannot continue operating if one of the poles is out of service. This configuration is typically grounded through the midpoint of the DC shunt capacitors and it is the most usual configuration in VSC-based systems [93].

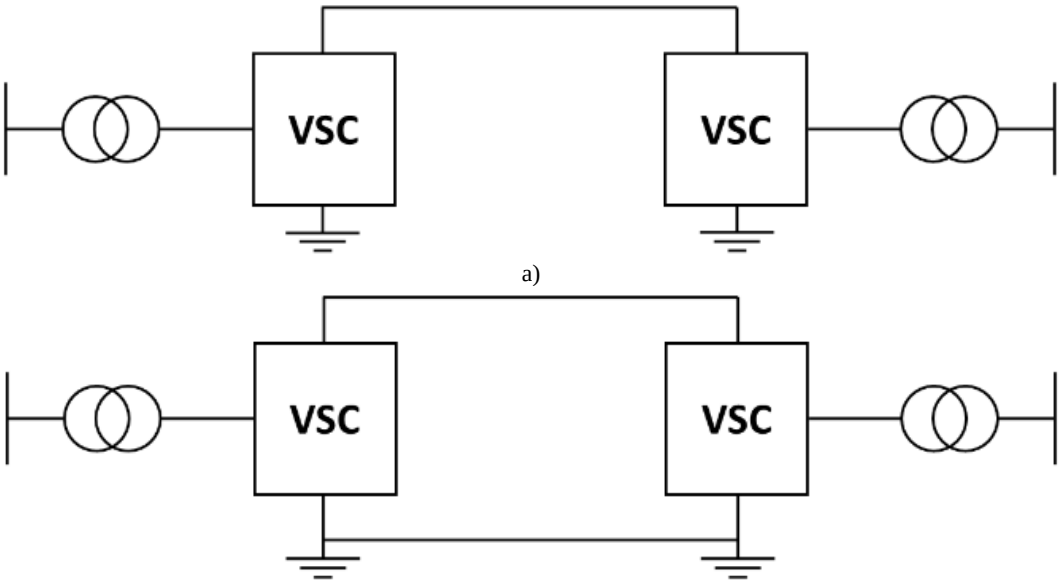


Figure 2.7.- Asymmetric-monopole configuration with a) ground return and b) with dedicated metallic return cable.

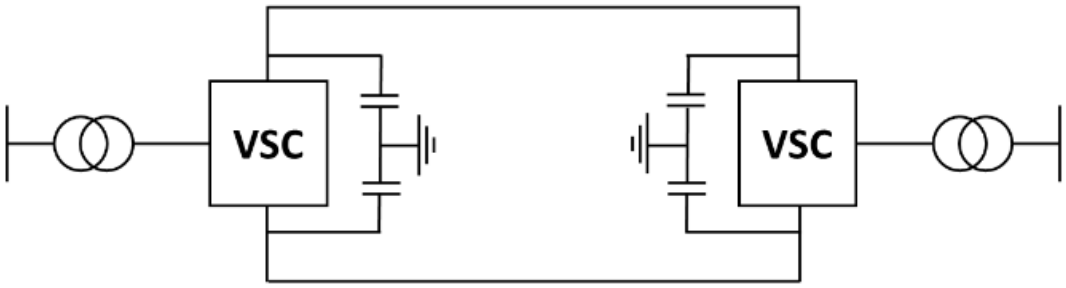


Figure 2.8.- Symmetric-monopole configuration.

2.2.4. Bipole configuration

The bipole configuration, shown in Figure 2.9, similarly to the symmetric-monopole configuration, presents two poles, positive and negative, but they are independently operated. There are four converters in total, two per terminal. One converter is connected to the positive pole and the other converter is connected to the negative pole in each terminal. This configuration usually presents a ground return cable, which is shared by both poles since the ground current is limited due to environmental restrictions. If one pole is out of service, the system can continue operating as an asymmetric-monopole using just the other pole and the ground return cable. This way, the system will transmit half of the total power [94].

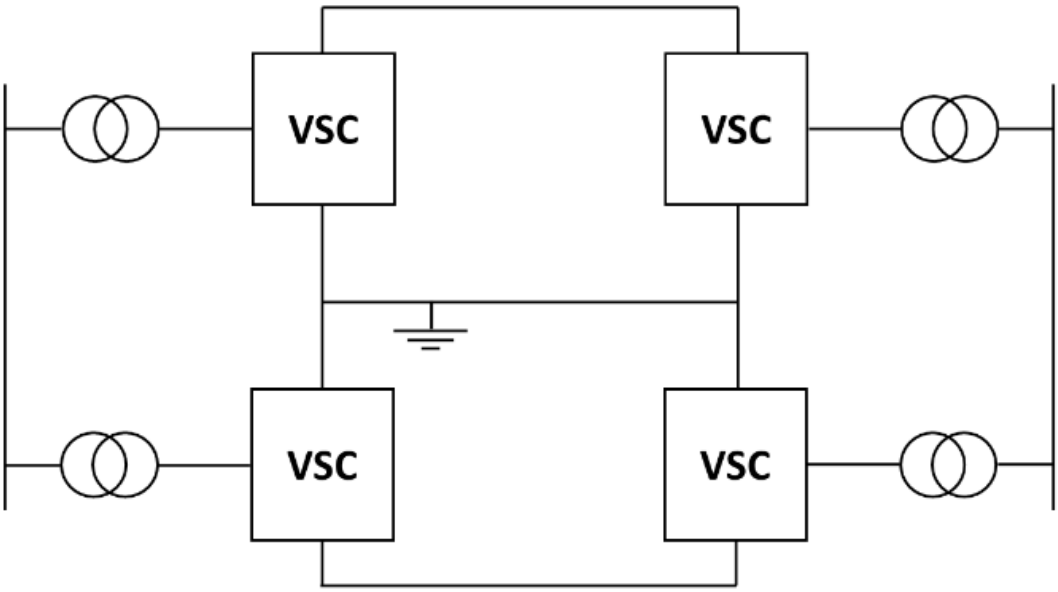


Figure 2.9.- Bipole configuration.

2.3. DC fault characteristics

The most important characteristic of faults in HVDC systems is the absence of a “natural” current zero-crossing, making fault interruption more complex than in HVAC systems. Besides, a fast rate-of-rise and high steady-state value of the fault current and the collapse of the fault voltage make fault protection challenging. The fault characteristics in HVDC systems are analysed in this subsection, specially, in grids employing half-bridge MMCs.

According to the traveling wave theory, a fault induces electromagnetic waves which are spread through the system. When the fault wave arrives to the faulty line’s ends, it is partly reflected to the fault location and partly transmitted to the healthy lines. There are several sources which cause the surge of the fault current:

- The capacitive discharge of the lines is the first contribution to the fault current. As the fault wave travels through the line, its capacitance progressively discharges. The neighbouring lines also contribute to the fault current when the fault wave arrives to the faulty line’s ends. The contribution to the fault current depends on the number of lines interconnected to the terminals related to the faulty line. This stage has a duration of just a few milliseconds.

- The second and main contribution starts when the bus voltage quickly decreases after the fault wave’s arrival, so the capacitors of the converter submodules start discharging and contributing to the fault current. The fault current contribution depends on the converter topology and the number and size of the capacitors.

This stage lasts until the converters' self-protection is triggered or the fault is isolated.

- Lastly, the third and last source contributing to the fault current is the AC system. The converters are blocked by their self-protection scheme to protect the IGBTs against overcurrents, thus, the converter behaves as an uncontrolled-rectifier allowing the AC system to feed the fault current through the submodules' anti-parallel diodes. The fault current contribution depends on the AC system's strength, fault distance and fault resistance. The fault current increases until it is interrupted or it keeps on increasing causing the blocking of all converters and reaching a steady-state value.

The fault type, grounding and configuration of the system determine the prospective steady-state value of the fault voltage and current. A Pole-to-Ground (PtG) fault occurs when one pole and the ground are interconnected through a fault resistance while the interconnection of the negative and positive poles corresponds to a Pole-to-Pole (PtP) fault. Figure 2.10 shows a single-phase diagram of a half-bridge MMC-based system where I_{relay} is the fault current measured by the relay and I_{fault} is the fault current at the fault point. Figure 2.11 compares the fault-induced current and voltages measured by the relays located in both poles during a PtP fault and a positive PtG fault. Fault current and voltage measured by the relay regarding a PtP fault are shown in Figure 2.11-a and –c while those related to a PtG fault are shown in Figure 2.11-b and –d. The fault current at the fault point (I_{fault} in Figure 2.10) is depicted in Figure 2.11-e and –f for a PtP fault and a PtG fault.

A PtP fault causes high currents and low voltages regardless of the grounding type while the effects of a PtG fault depend on the grounding type. A PtG fault induces high fault currents and low fault voltages in low-impedance grounded asymmetric-monopole and bipole configurations while a steady-state fault current of theoretically zero is induced when high-impedance grounded symmetric-monopole (Figure 2.11-b and -f) and bipole configurations are adopted. The faulty pole's voltage drops to zero value and the healthy pole's voltage increases up to twice the rated value since a new ground reference is defined through the PtG fault (Figure 2.11-d). This allows the converters to apply a DC pole-to-pole voltage which prevents a great increase of the fault current. Conversely, the voltage drops to zero in both poles during a PtP fault (Figure 2.11-c). Therefore, the converters cannot apply a DC pole-to-pole voltage during a PtP fault since both poles are affected and the voltage collapses so the fault current significantly increases (Figure 2.11-a and -e). Therefore, a PtP fault produces a greater fault current magnitude than in the case of a PtG fault.

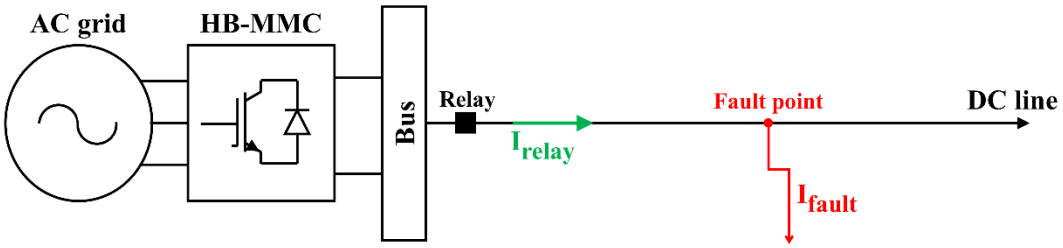


Figure 2.10.- Single-phase diagram of the fault current in a half-bridge MMC-based system.

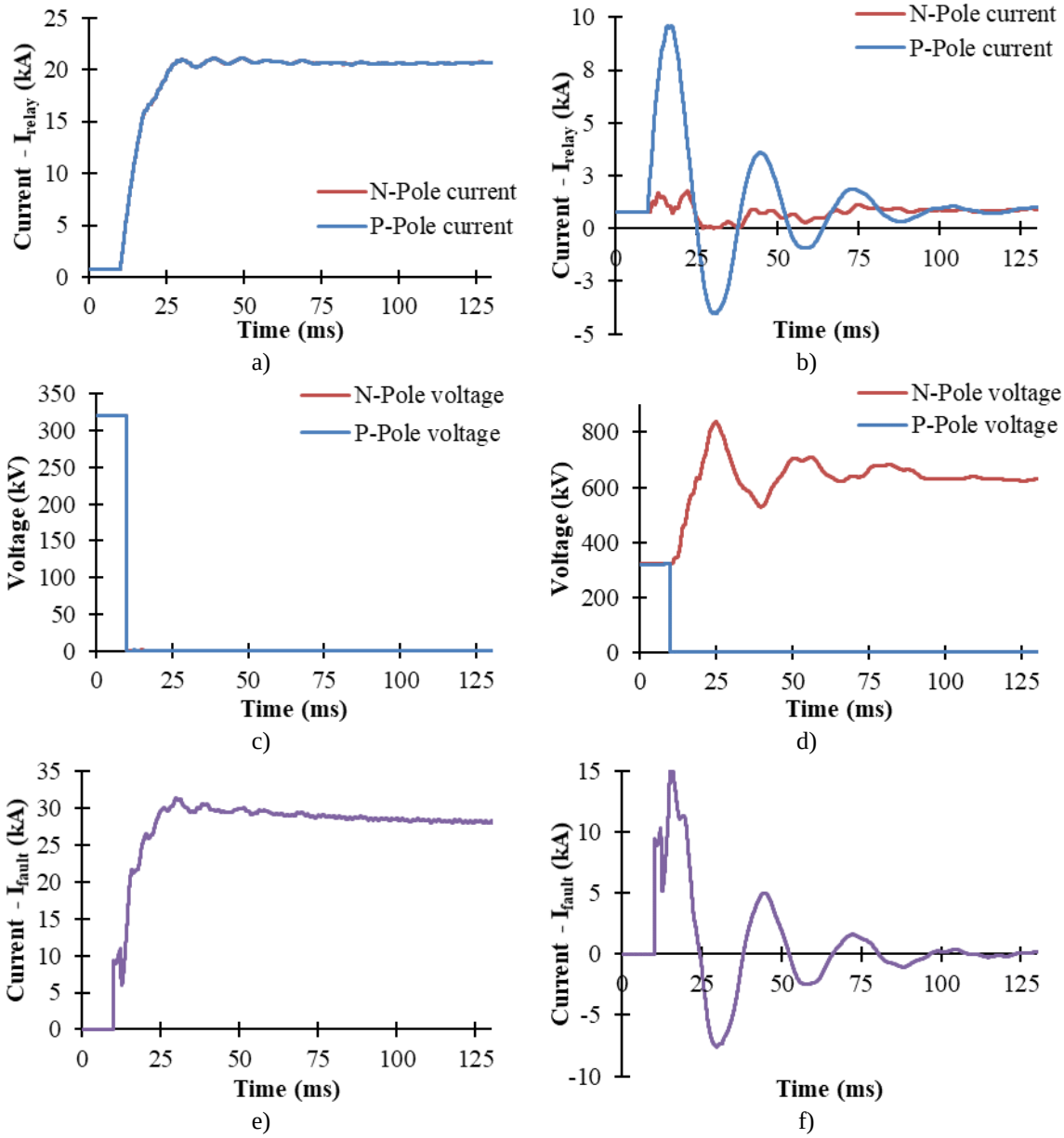


Figure 2.11.- Fault current (I_{relay}) measured by the relay for a) a PtP fault and b) a PtG fault. Fault voltage measured by the relay for c) a PtP fault and d) a PtG fault. Fault current (I_{fault}) at the fault point for for e) a PtP fault and f) a PtG fault. Solid fault simulated in a high-impedance grounded symmetric-monopole system.

2.4. Breaking devices

Protection of conventional CSC-based P2P systems have usually employed AC Circuit Breakers (AC-CBs) located in the HVAC side of the system. The AC-CBs' operation speed takes up to several cycles, i.e., several tens of milliseconds [95], due to mechanical restrictions. In addition, the entire link is de-energized due to the AC-CBs' operation. Therefore, AC-CBs are not appropriate for the protection of large MTDC grids, since the shut down of the entire system is not feasible [96].

Hence, DC-CBs are needed for fast and selective fault protection in MTDC systems. This way, only the affected protection zone is isolated while the remaining healthy protection zones of the grid keep operating [97]. Thus, these breaking devices must be fast enough and capable of creating a current zero-crossing [98] and of interrupting high fault currents [99], so as to allow fault current interruption in less than a few milliseconds [100]. Moreover, DC-CBs must present minimum power losses and costs [101] and energy dissipation capability in order to prevent overvoltages derived from the fault current interruption process [102].

Several topologies of DC-CBs have been developed over the last years. Mechanical DC-CBs are mostly based on commonly-available AC devices and auxiliary components, which produce fault current interruption by reverse current injection or counter voltage generation. Solid-sate DC-CBs consists of semiconductor devices, which allow very fast fault current interruption. Hybrid DC-CBs are a combination of the two previous topologies.

2.4.1. Mechanical circuit breaker

Mechanical DC-CBs (M-CBs) are based on the operation of conventional AC-CBs by using common AC interrupters (vacuum-based, SF6-based, air-blast-based...) and an auxiliary branch, which generates the current zero-crossing in the interrupter, basically, by reverse current injection or counter voltage methods, extinguishing the arc and allowing the complete opening of the M-CB.

The M-CB technology uses conventional and available components which lowers the costs [103], however, since it depends on AC interrupters, its operation is too slow, limited to several tens of milliseconds. On the other hand, M-CBs present low on-state losses.

In addition, the generation of the current zero-crossing adds complexity to the M-CBs in comparison to AC-CBs [67]. In addition, an energy absorber path consisting in surge arrester banks (commonly metal oxide arresters) is needed in order to dissipate the energy stored in the system inductance, since it is technically

more appropriate to absorb the energy in this additional device than in the electric arc generated by the opening of the interrupter [104].

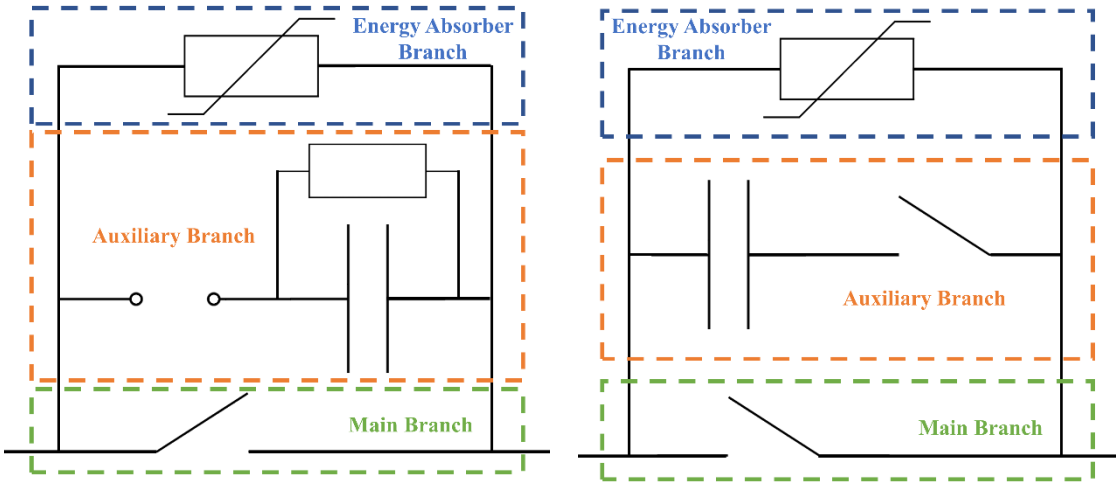
Another important component is the interrupter. Its contacts have to separate a sufficient distance to ensure the adequate dielectric strength. Moreover, its operation speed affects the time needed for arc extinction [105] and the total breaking speed of the M-CB [106].

2.4.1.1 Counter voltage method

The counter voltage method is based on the arc voltage generated by the opening of the switching device, which is opposed in excess to the system voltage, driving the current to zero. Additionally, if an auxiliary branch is employed, the arc voltage will force the fault current to the auxiliary capacitor, charging it and increasing the voltage across the circuit breaker [107]. The voltage across the breaker has to exceed the system voltage, supplying it until the current reaches zero as well as absorbing the magnetic energy stored in the grid inductances [108]. This voltage level must be in the range of 1.2 to 1.5 of the rated voltage [109], [110]. Due to the high capacitance value needed, this method is more appropriate for low voltage systems [107], [111].

The M-CB proposed in [104] (Figure 2.12-a) presents a switch in the normal conduction path of the current and an auxiliary branch consisting of a spark gap in series with a capacitor in parallel to a discharge resistor, and an energy absorber branch. After fault detection, the switch starts to open and an arc voltage is generated, making the gap located in the auxiliary branch to connect the capacitor in parallel to the switch. The capacitor is charged and the current flowing through the arc of the switch is reduced. The arc is deionized and the dielectric strength is re-established, the current is completely commutated to the capacitor which keeps being charged and the voltage across the breaker increases until the surge arrester takes over the fault current and drives it to zero, also absorbing the system energy.

Figure 2.12-b shows a M-CB based on SF6 puffer interrupters which is presented in [112]. Additionally, it presents an energy absorber branch and an auxiliary branch with a capacitor and a switch. When, the interrupter opens after fault detection and the arc voltage is high enough, the current starts commutating to the auxiliary branch (after closing the switch), charging the capacitor. The current commutation generates an oscillating current which creates a current zero-crossing allowing the extinction of the arc [113]. Then, the capacitor voltage keeps rising until the current is commutated to the surge arrester [114].



a) b)

Figure 2.12.- Topology of the counter voltage M-CB proposed a) in [104] and b) in [112].

The topology proposed in [115] is shown in Figure 2.13-a. It presents two SF6 interrupters in series in the main branch with a Gate Turn-Off (GTO) thyristor in parallel with one of them. The auxiliary and energy absorber branches present a capacitor and a surge arrester, respectively, as in previous topologies. When the contacts of the interrupters separate and their arcs are established, the GTO thyristor is turned on, producing a current zero-crossing into the parallel interrupter, extinguishing its arc. Then, the thyristor is turned off and the voltage across the breaker increases rapidly, forcing the current to the capacitor, charging it. A counter voltage is constituted, reducing the current. When this voltage reaches the required level, the current is commutated to the arrester, where it is driven to zero.

2.4.1.2 Reverse current injection method

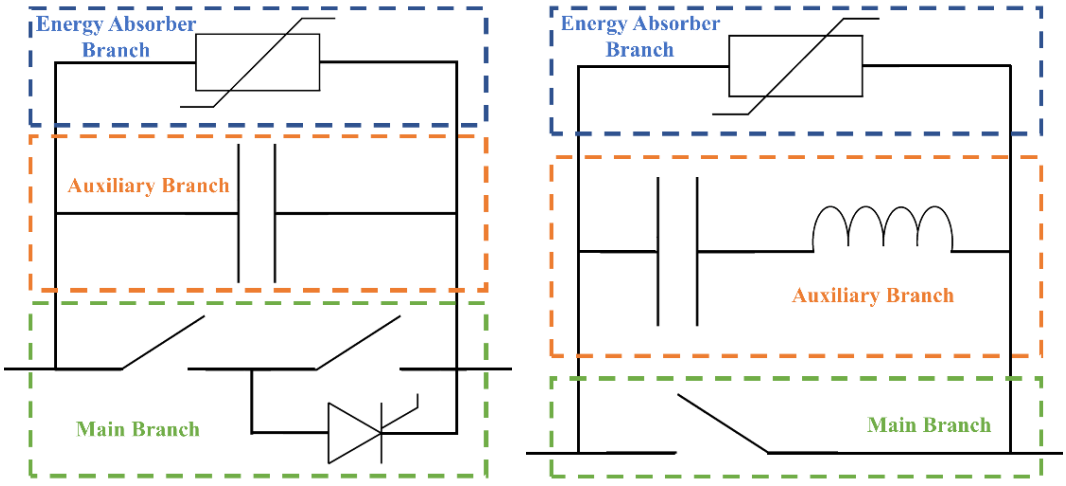
The reverse current injection method consists of producing a current zero-crossing by an auxiliary circuit, commonly a LC resonant circuit where the pre-charged capacitor discharges in opposition to the fault current, in order to extinguish the arc and complete the opening of the switcher. The current injection magnitude needs to exceed the fault current and the initial charge of the commutation capacitor must provide a safety margin to interrupt the largest expected current [116]. The reverse current injection method is a more viable approach for current interruption in high voltage systems since lower capacitances are needed [107], [117].

2.4.1.2.1. Passive resonant method

In this topology, the auxiliary branch consists of a resonant LC circuit which is self-excited or naturally trigged by the arc generated in the opening of the AC interrupter due to its negative resistance and natural fluctuations [118]. When the

resonance is triggered the capacitor discharges an oscillating current which opposes the fault current direction, while the amplitude of the oscillating current increases, a current zero-crossing is produced in the interrupter, allowing the extinction of the arc. Then, the current is commutated to the auxiliary branch where the capacitor is charged. The capacitor voltage rises until the surge arrester takes over the current, dissipating the energy stored in the system inductance and completing the interruption of the fault current [119].

Figure 2.13-b shows a M-CB based on air blast interrupters which is presented in [112]. It also consists of an auxiliary branch with a LC circuit and a surge arrester (zinc oxide) in the energy absorber branch [120]. The passive resonant method is employed so, after opening of the air blast interrupters, the LC circuit is excited due to the negative voltage-current characteristic of the arc and an oscillating current is generated. The amplitude of the oscillating current increases until it reaches the fault current, creating a current zero-crossing in the path of the interrupter [121]. Then, the current is commutated to the auxiliary branch, the voltage across the breaker increases until it reaches the protective level of the surge arrester, when the current is forced to the energy absorber branch and the interruption process is completed [114].



a) b)

Figure 2.13.- Topology of a) the counter voltage M-CB proposed in [115] and b) the passive resonant M-CB proposed in [112].

2.4.1.2.2. Active resonant method

The active resonant method is very similar to the passive resonant method but in this case the capacitor of the LC circuit is pre-charged and it is inserted in the circuit by a switch [119], enabling a faster current interruption [98] since there is no time delay due to the generation of the oscillating current [118]. However, a charging unit is needed, increasing the costs [122]. Another advantage is that the size of the

required capacitor is smaller in this commutation concept than in the passive one [123].

The active resonant method based M-CB presented in [124] employs a SF6 puffer interrupter in parallel with an auxiliary branch consisting of a LC circuit and a closing switch and with an energy absorber branch based on ZnO non-linear resistors, as it is shown in Figure 2.14. After fault detection, the interrupter opens while the closing switch closes, discharging the pre-charged capacitor and superimposing an oscillating current to the fault current. A current zero-crossing is created, and the arc is extinguished, completely commutating the current to the auxiliary branch. The voltage across the breaker rises until the current is forced to the energy absorber branch. Additionally, a restriking voltage suppressing capacitor is connected in parallel to the interrupter and the capacitor of the auxiliary branch is pre-charged through a bypass switch and two charging resistors [125].

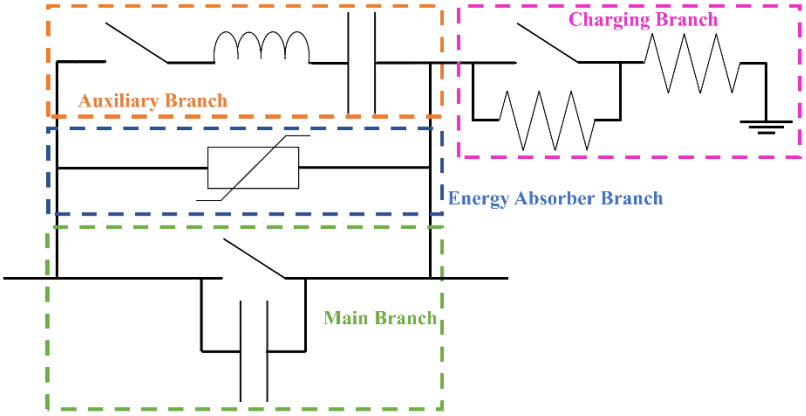
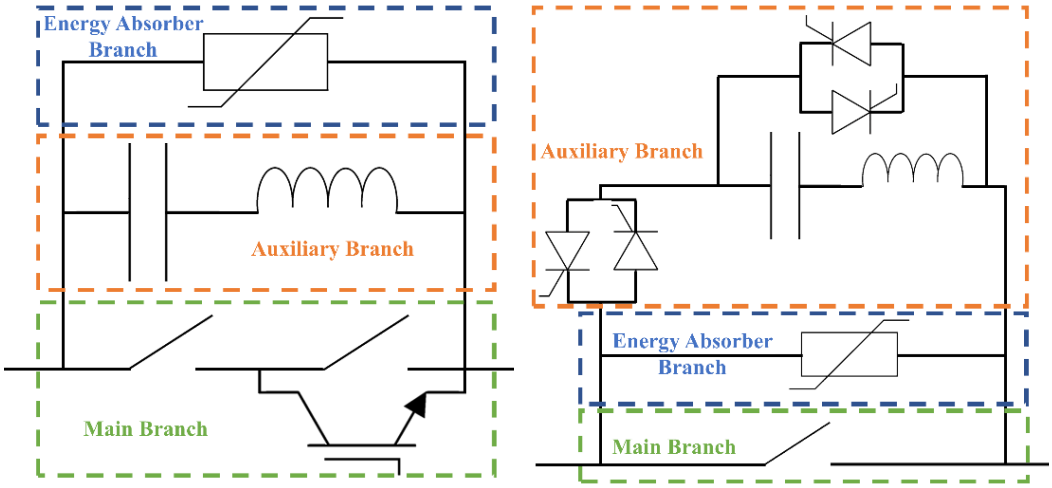


Figure 2.14.- Topology of the active resonant M-CB proposed in [124].

Figure 2.15-a shows another topology presenting a main branch with two SF6 interrupters in series and an IGBT in parallel with one of the interrupter while the auxiliary and energy absorber branches present a LC circuit and a surge arrester, respectively [115]. When the contacts of the interrupters separate and their arcs are established, the IGBT is turned on and it is controlled between high and low impedance at the natural frequency of the LC circuit, exciting the circuit resonance. This way, an oscillating current is superimposed to the fault current, creating a current zero-crossing and, hence, the arcs of the interrupters are extinguished and the current is commutated to the auxiliary branch. The capacitor voltage increases and when it reaches the required level, the current is commutated to the surge arrester, where it is driven to zero.

The M-CB proposed in [126] follows the topology of a basic active resonant circuit breaker but it additionally presents two groups of thyristors, one in the auxiliary branch and another in parallel to the LC circuit, as it is shown in Figure 2.15-b. The pair of thyristors of each group are connected in anti-parallel in order

to provide bidirectional current interruption. After fault detection, the fast mechanical switch of the main branch starts opening and the corresponding thyristor in parallel to the LC circuit turns on, reversing the polarity of the capacitor. After polarity reversal, this thyristor turns off and the one from the other group is turned on, injecting an opposing current and creating a current zero-crossing. The arc is extinguished and the fast mechanical switch completely opens. The current commutates firstly to the auxiliary branch and, then, to the energy absorber branch.

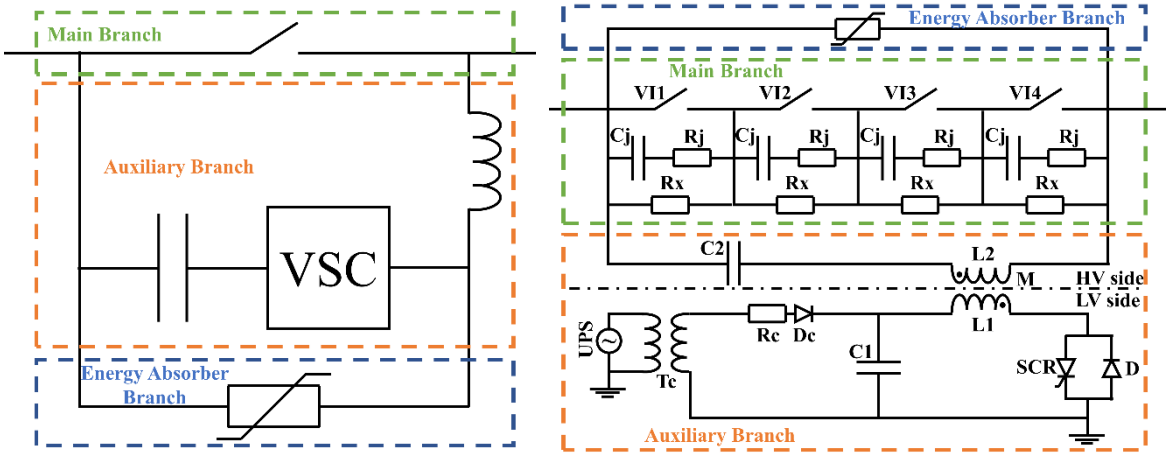


a) b)

Figure 2.15.- Topology of the active resonant M-CB proposed a) in [115] and b) in [126].

The VSC-assisted resonant current (VARC) circuit breaker is a modern model of M-CB. This topology presents a vacuum interrupter actuated by an ultra-fast Thomson-coil mechanism in the main branch. A VSC is introduced in series with the LC resonant circuit in the auxiliary branch to generate an oscillating current. This way, a current zero-crossing is created when the amplitude of the oscillating current reaches the amplitude of the fault current [127]. A prototype with a maximum current interruption capability of 10 kA and a transient interruption voltage of 40 kV was developed within the frame of the PROMOTioN project [128]. This topology is represented in Figure 2.16-a.

A prototype of a 160 kV M-CB was installed in the Nan'ao project [64]. It presents four 40 kV vacuum interrupters (VI) connected in series in the main branch, as it is depicted in Figure 2.16-b. Each interrupter is in parallel with two other branches: a series connection of a resistor (Rj) and a capacitor (Cj) and another resistor (Rx). The auxiliary branch is divided into a high-voltage side and a low-voltage side which are electrically isolated through an air-core transformer (M). The energy absorber branch comprises surge arrester banks. This topology charges the capacitor (C1) in the low-voltage side instead of the high-voltage side through an uninterruptible power system (UPS) boost circuit.



a) b)

Figure 2.16.- Topology of a) the VARC-based M-CB [127], [128] and b) the M-CB installed in the Nan'ao project [64].

2.4.2. Solid-state circuit breaker

Solid-State DC-CBs (SS-CBs) are based on semiconductor components, mostly fully-controlled devices (IGBTs, IGCTs, MOSFETs…) [129]. They present the fastest operating time, in the order of several microseconds [68], [99], due to the almost instantaneous operation of the semiconductors. This technology is fast enough to open before the fault current reaches damaging levels [130], hence it operates with a reduced maximum current due to its operation speed [131]. However, a large number of semiconductors are needed for high voltage applications, which increases the costs of this topology.

In addition, these devices present high on-state voltage drop, hence high on-state losses. A semiconductor with a few kV of voltage rating presents an on-state voltage drop in the order of some volts, generating losses in the range of kW for a current in the order of hundred amperes [108]. These losses can be in the range of 0.1-0.4% of the transmitted power [100] or up to 30% of the power losses of a VSC station [68]. They also present some problems related to asynchronous operation and voltage and current balancing [132].

The basic topology of a SS-CB is shown in Figure 2.17. It consists of two branches: a main conduction branch with the main breaker, which is a series connection of several semiconductor devices, commonly IGBTs, and an energy absorber branch with a surge arrester, usually a metal oxide arrester. During normal operation, the current is conducted through the IGBTs. When a fault is detected, the semiconductor devices are turned off, commutating the current to the energy absorber branch, where it is driven to zero since the arrester voltage is higher than the system voltage, and the energy stored in the system inductance is dissipated.

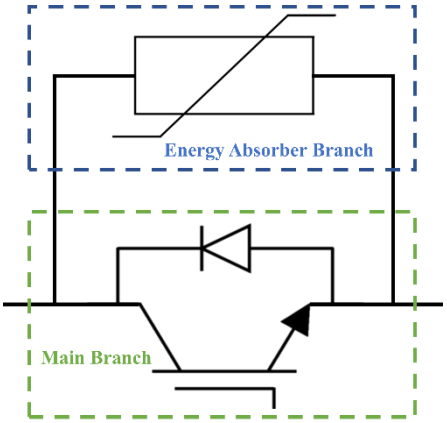


Figure 2.17.- Basic topology of SS-CB.

Figure 2.18 presents a variation of this topology [98], where each IGBT is in parallel with a RCD snubber circuit. In this case, after the IGBTs are turned off due to fault detection, the current is commutated to the snubber circuits, charging the capacitors. The voltage across the circuit breaker increases until it reaches the voltage protection level of the surge arrester, forcing the current to the energy absorber branch where the current interruption process is completed.

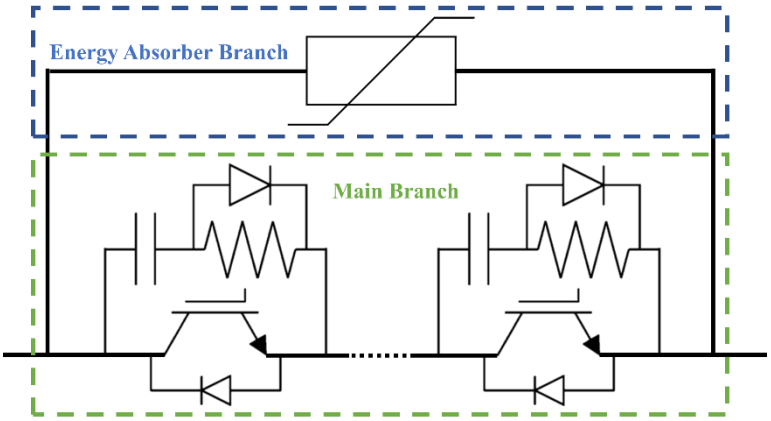


Figure 2.18.- Topology of SS-CB proposed in [98].

The SS-CB proposed in [129] is based on a series connection of IGBTs (or IGCTs) in the main path of the current under normal operation and two thyristor banks, a capacitor, an inductor and two resistors (Figure 2.19). The current pre-charges the capacitor to the nominal voltage level following the path T1-R1-L1-C1. The current interruption process starts by turning off the semiconductors of the main path and triggering the thyristor bank T2; the capacitor discharges through the path L1, R2 and T2. The stored energy is dissipated by R2, cable resistance and fault impedance. Thyristor T2 turns off naturally when the fault current decays below its holding value. This topology presents half the number of semiconductors than the traditional structure. The power losses of this SS-CB are 0.08% of the rated power for IGBTs (0.04% for IGCT).

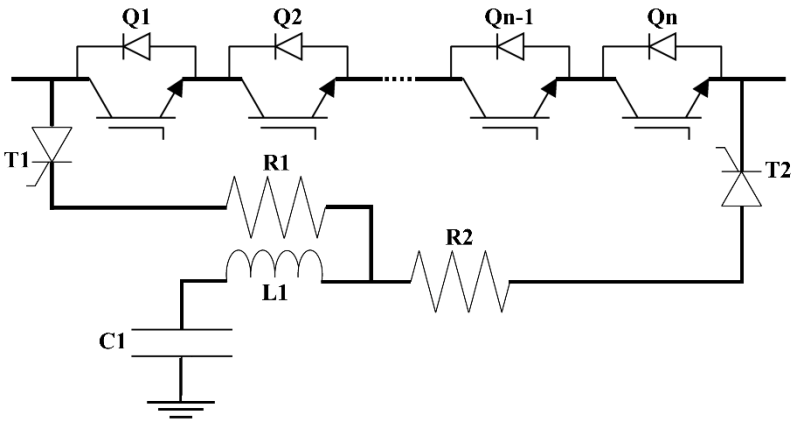


Figure 2.19.- Topology of SS-CB proposed in [129].

Paper [133] presents a SS-CB with fault current limitation (Figure 2.20). The proposed topology is based on IGBT modules located in several different parallel branches. Each IGBT module consists of a metal oxide arrester in parallel with two IGBTs in anti-series connection (bidirectional current interruption). Each branch can limit the fault current thanks to the presence of an inductor. The inductors of each branch are interconnected by thyristors. The branches are classified into current limiting branches and circuit breaking branches, only two branches are of the latter type. Under normal operation, all branches are turned on, in a parallel connection, dividing the current into all branches, reducing the power losses. After fault detection, the current limiting branches are turned off and the thyristors are turned on, connecting the inductors in series, limiting the fault current. Then, the current breaking branches are turned off. The current limitation capacity allows an extra time to confirm the existence of a fault condition. The energy is dissipated in the metal oxide arresters parallel to each IGBT module.

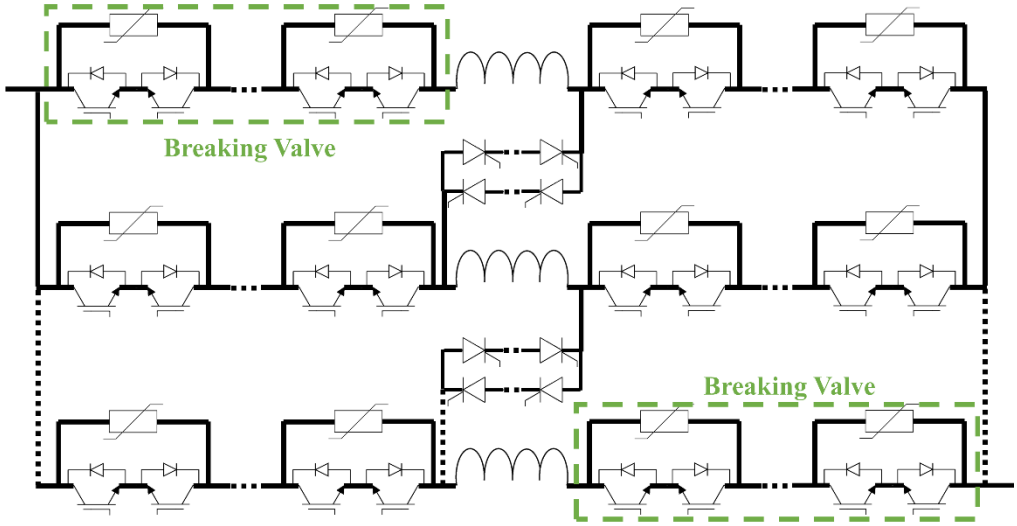


Figure 2.20.- Topology of SS-CB proposed in [133].

2.4.3. Hybrid circuit breaker

The Hybrid DC-CB (H-CB) combines the advantageous characteristics of the M-CBs and the SS-CBs into its topology by mixing mechanical interrupters and semiconductor devices [134]. This way, a fast operation is achieved with lower on-state losses. However, H-CBs still present relatively high costs due to the use of several semiconductor devices and the complexity of its structure [103]. The H-CB topology presents basically three branches. The main branch consists of a fast mechanical switch and a semiconductor-based load commutation switch. The auxiliary branch is formed by a semiconductor-based main breaker and the energy absorber branch by a surge arrester. The main breaker does not contribute to the on-state losses since it only conducts current during the current interruption process, i.e., a brief period of time. Hence, the power losses are mostly caused by the few semiconductor devices that constitute the load commutation switch [70].

After fault detection, the main breaker turns on and the load commutation switch turns off, forcing the current to the auxiliary branch. This way, the fast mechanical switch starts to separate its contacts under a zero current condition with low stress, hence, a fast mechanical disconnector with a lightweight contact system can be employed in this type of DC-CB [103]. In addition, the main limitation of the interruption time of the breaking device is the movement speed of the fast mechanical disconnector [126] since the operating time of the semiconductor devices is almost instantaneous. Then, when the mechanical switch is completely opened, the main breaker is turned off, commutating the current to the energy absorber branch where it is driven to zero while the energy stored in the line inductance is dissipated [135].

Figure 2.21 shows the H-CB topology developed by ABB [136] which employs IGBTs as semiconductor devices and presents a pro-active control, which allows the confirmation of the existence of the fault condition before current interruption [137]. Each cell of the main breaker presents an individual arrester bank [138]. If the line current exceeds a certain value, the current interruption process of the H-CB is initiated and the current is commutated to the main breaker.

Then, a protection algorithm will confirm the existence of the fault condition taking advantages of the time delay imposed by the opening of the contacts of the mechanical disconnector [138]. If a confirmation signal is received or the current value is close to the maximum breaking capability of the H-CB, the main breaker is turned off and the current interruption process is completed, otherwise the current is commutated back to the main branch, stopping the current interruption process [139].

This pro-active control also allows fast backup operation: the line current will be commutated to the auxiliary branch after detecting an overcurrent, allowing fast current interruption if a backup protection signal is received [140].

Additionally, a current limitation control is also available: a certain number of cells of the main breaker are opened during the fault confirmation process in order to control the voltage drop across the H-CB and to limit the current. The current limitation control is limited by the energy dissipation capability of the arrester banks [136]. On the other hand, maintenance on demand can be achieved by commutating the current from the main branch to the auxiliary branch. This way, the power transmission is not interrupted or disturbed [141].

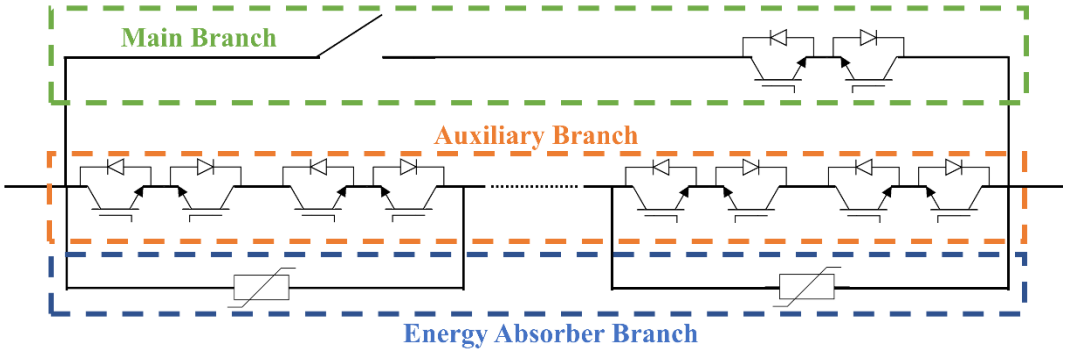


Figure 2.21.- Topology of H-CB developed by ABB [136].

Alstom Grid also developed a H-CB topology [142] presenting the main variation in the thyristor-based auxiliary branch as it is shown in Figure 2.22. This auxiliary branch is formed by two time-delaying branches and an arming branch, consisting of a series stack of thyristors and a capacitor bank. These different branches build the counter voltage needed for fault current interruption in a series of successive stages [143].

After fault detection, the IGBT-based load commutation switch is turned off, the fast mechanical switch starts separating its contacts and the thyristor stack of the first time-delaying branch is turned on. The current commutates to the first time-delaying branch and charges a large capacitor bank in parallel with a low voltage rated surge arrester. This way, the capacitor voltage increases slowly.

When the fast mechanical switch has separated its contacts, the current is commutated to the second time-delaying branch where it charges another capacitor bank in parallel with a surge arrester of higher voltage rate. The current is again commutated to the arming branch charging its capacitor bank and then to the surge arrester, completing the current interruption process [109].

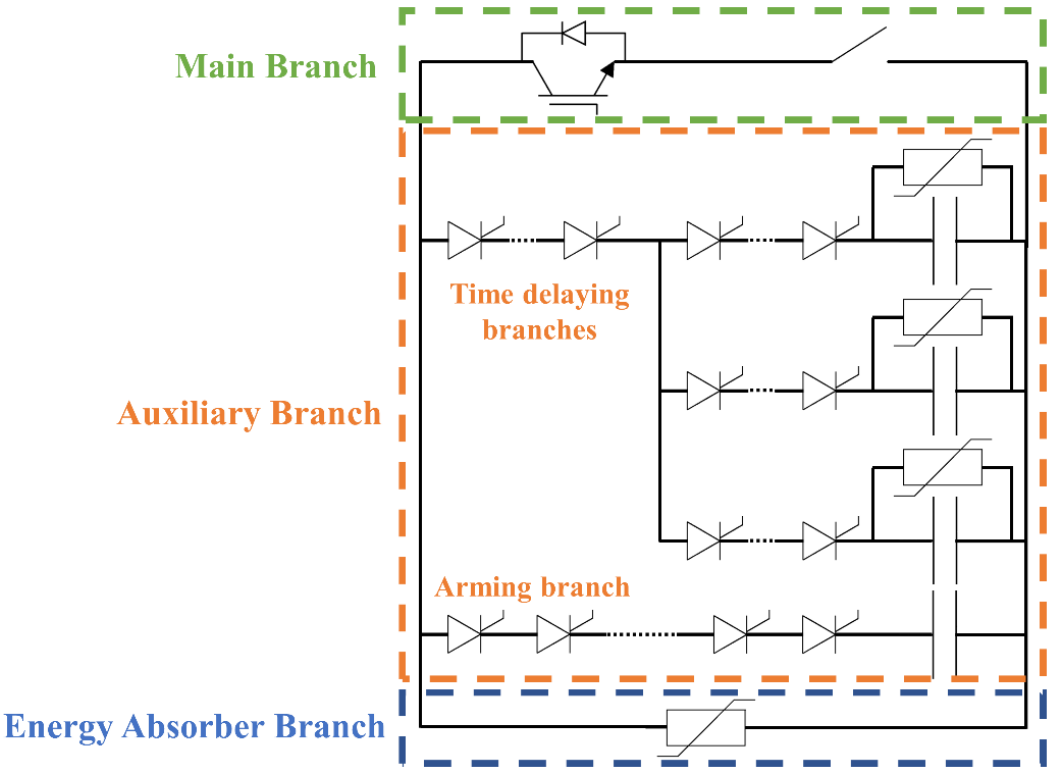


Figure 2.22.- Topology of H-CB developed by Alstom Grid [109].

A H-CB topology based on full-bridge modules (four IGBTs and a capacitor) is proposed in [144]. The main branch consists of a vacuum-based fast mechanical switch and a few modules while the auxiliary branch is formed by a series connection of a large number of modules as it is shown in Figure 2.23.

Likewise, the energy absorber branch is formed by surge arresters. When a fault is detected, the IGBTs of the modules located in the main branch are blocked and the capacitors are charged, generating a counter voltage. The current is commutated to the auxiliary branch and the mechanical switch separates its contacts.

When sufficient opening distance is achieved, the IGBTs of the full-bridge modules of the auxiliary branch are turned off, the capacitors are charged and the voltage across the breaking device increases reaching the protective level of the surge arrester. Then, the current is forced to the energy absorber branch [145]. This H-CB is installed in the Zhoushan MTDC project in China.

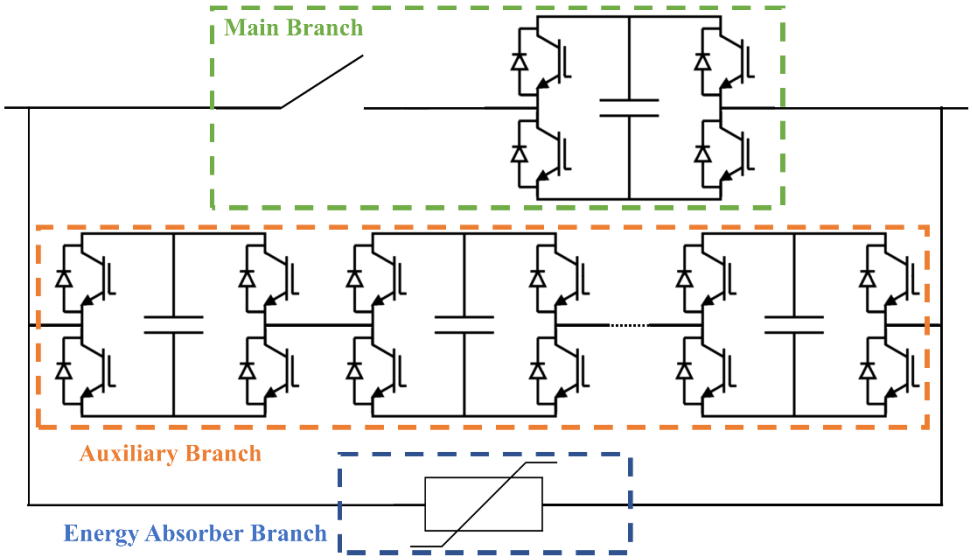


Figure 2.23.- Topology of H-CB with IGBT-based full-bridge modules [145].

The H-CB presented in [146] also employs IGBT-based full-bridge modules in the auxiliary branch, in series with a group of two thyristors in parallel with another group for bidirectional current interruption. As it can be seen in Figure 2.24, the main branch presents a fast mechanical switch and an IGBT-based load commutation switch (IGBTs in anti-series for bidirectional current interruption) [122]. The current interruption process is very similar to the one explain in the previous topology but, in this case, after the blocking of the modules, the current will be commutated to the parallel capacitor of the auxiliary branch since the module capacitors are pre-charged [147].

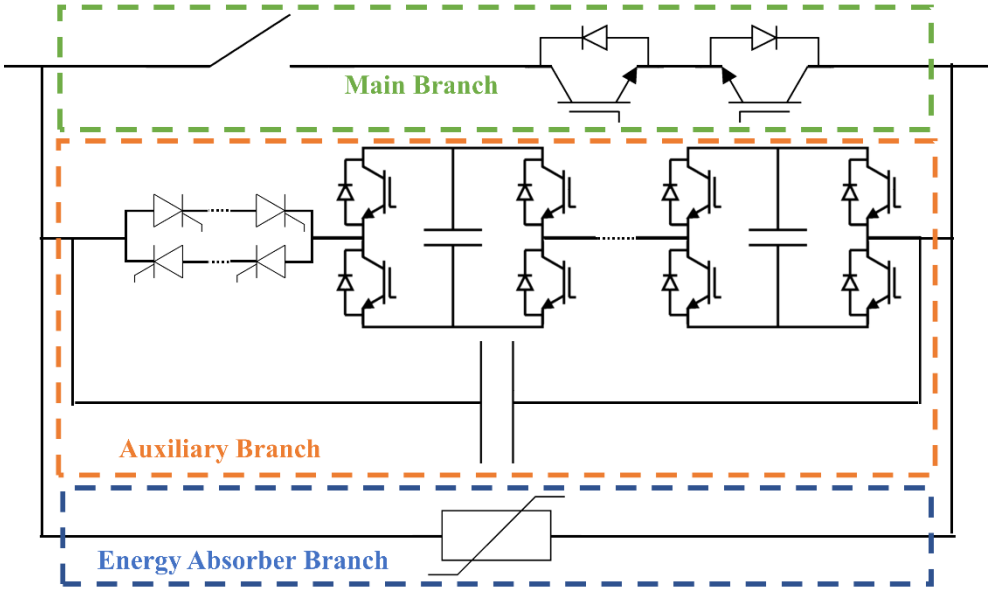


Figure 2.24.- Topology of H-CB presented in [146].

The Zhangbei project implements H-CBs at both ends of each line [63]. This H-CB topology's main branch presents an ultrafast disconnector in series with several IGBT-based H-bridge modules. Meanwhile, the auxiliary branch presents a large amount of cascaded diode-based H-bridge modules as it is shown in Figure 2.25. The diode-based H-bridge module consists of four diodes, two press pack IGBTs and a snubber circuit. This way, the diode-based H-bridge modules allow reducing the number of IGBTs by half.

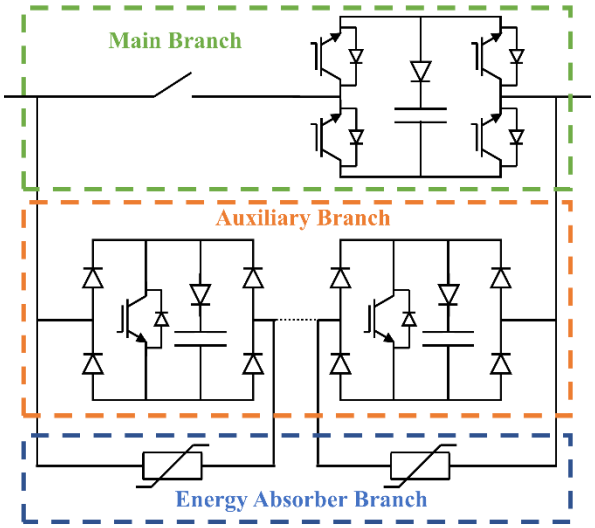


Figure 2.25.- Topology of the H-CB installed in the Zhangbei project [63].

2.4.4. Developed HVDC circuit breakers.

Some DC-CBs have been developed in the recent years by different manufacturers. Moreover, several DC-CBs have been installed (or are planned to be installed) in existing MTDC grids. The most relevant features of these DC-CBs are summarized in Table 2.1.

Table 2.1.- Characteristics of manufactured or installed DC-CBs

Manufacturer/MTDC	Technology	Rated Voltage	Breaking Capability	Operating Time
ABB [140]	Hybrid	320 kV	9 kA	2 ms
Alstom [109]	Hybrid	120 kV	7.5 kA	2 ms
SCiBreak AB [127], [128]	Mechanical	40 kV	10 kA	3 ms
Nan'ao MTDC [64]	Mechanical	160 kV	9.2 kA	3.9 ms
Zhoushan MTDC [145]	Hybrid	200 kV	15 kA	3 ms
Zhangbei MTDC [63]	Hybrid	500 kV	25 kA	3 ms

2.5. Fault-clearing strategies

The fault isolation and clearing processes can affect both the MTDC grid and the HVAC system. Ideally, the fault impact on the healthy zones is minimized by means of isolating only the affected part of the system. This way, stress and possible damages on healthy components are also avoided. Conversely, the adopted fault-clearing strategy varies according to the requirements and fault impact on the interconnected systems [148].

Small MTDC systems and P2P links usually follow a non-selective fault-clearing strategy, i.e., firstly, the entire system is de-energized after fault detection by means of AC-CBs, then, in the case of small MTDC systems, DC switches isolate the faulty part and, finally, the AC-CB are re-closed and the healthy parts of the system are re-energized. This strategy is employed when the shutdown of the entire HVDC system does not have a relevant impact on the stability of the interconnected systems. In addition, the lack of commercially-available DC-CBs has made the non-selective strategy a common solution.

However, a non-selective fault-clearing strategy cannot be applied to a large MTDC grid since shutting it down could severely affect the stability of the interconnected HVAC systems. However, a full-selective strategy, where only the faulty part of the system is isolated, might be more appropriate. This strategy divides the grid into protection zones covering each relevant component, e.g., each line or cable is treated as an independent protection zone. To do this, DC-CBs are placed at the borders of each protection zone. This way, the fault impact is minimized and the healthy zones of the MTDC grid remain unaffected and operative. Consequently, this strategy is very similar to the one adopted in conventional HVAC systems.

Another fault-clearing strategy is the partially-selective strategy which combines the two previously-mentioned strategies. In this case, the MTDC grid is divided into subsystems, which cover several components, and are interconnected through DC links. When a fault is detected inside a certain subsystem, the affected subsystem is de-attached from the remaining ones by a DC-CB or a DC/DC converter which is located in the DC link interconnecting them. Then, the healthy subsystems remain operative while the affected subsystem is de-energized using AC-CBs and the faulty component is isolated employing DC switches. This way, the costs regarding DC-CBs and the impact of a total shutdown of the MTDC grid in the neighbouring HVAC systems can be reduced.

Table 2.2 summarizes and compares the previously-mentioned strategies. The non-selective strategy shows the highest fault-clearing time due to the use of AC-CBs unlike the full-selective strategy which presents the fastest operation since only the affected protection zone is isolated using DC-CBs. The partially-selective

strategy de-attaches the affected subsystems from the remaining healthy ones in a short time and then takes several of tens of milliseconds to isolate the affected component.

Table 2.2.- Comparison of fault-clearing strategies.

Fault-clearing strategy	Philosophy	Breaking device	Fault-clearing time
Non-selective	Shutdown of the entire grid	AC-CBs DC switches	~60 ms
Full-selective	Protection zones	DC-CBs	<10 ms
Partially-selective	Subsystems interconnected by DC links	DC-CBs or DC/DC converters AC-CBs DC switches	System partition: <10 ms Fault isolation: ~60 ms

2.6. Overview of protection algorithms for HVDC systems

The speed requirement is critical in VSC-based HVDC grids due to the fast rate-of-rise of the fault current and the low overcurrent withstand capability of the VSCs' components. Therefore, fast fault detection and location algorithms are needed in order to satisfy this requirement. Protection algorithms must be fast, selective and sensitive enough to detect all relevant fault conditions in their respective protection zone.

Protection algorithms can be classified into local-measurement-based or communication-based algorithms according to how the measurements needed for their operation are taken.

Local-measurement-based algorithms employ only locally-available measurements for their operation [149], [150]. Fault discrimination is achieved by monitoring and measuring the DC current and DC voltage. Local-measurement-based algorithms present high operation speed since only single-ended measurements are taken into account, i.e., there is no information exchange with the other end of the protection zone. However, they present low selectivity due to employing only local measurements [151], [152]. Therefore, limiting inductors are placed at both ends of the protection zone in order to improve the algorithm's selectivity since their damping characteristic makes fault discrimination between

external and internal faults easier to accomplish. Moreover, limiting inductors reduce the rate-of-rise of the fault current, so circuit breakers with lower current interruption capability can be used. However, their size can affect the stability of the system [140] and a higher energy must be dissipated during fault interruption. Likewise, local-measurement-based algorithms need threshold values to allow fault discrimination between external and internal faults. A higher threshold value improves the algorithm's selectivity while reduces its sensitivity, therefore, a trade-off value must be selected. Both the size of the limiting inductors and the threshold values depend on the characteristics of the grid and on the protection algorithm. The threshold value is usually selected through simulations [153]. Undervoltage, overcurrent and derivative-based algorithms are common local-measurement-based methods.

Conversely to local-measurement-based algorithms, communication-based algorithms exchange information between both ends of its corresponding protection zone through a communication channel [149], [150]. Therefore, they are highly selective algorithms that are, however, limited by their operation speed due to the time needed for the information exchange [149], [154], [155], i.e., the communication channel imposes a time delay in the operation of the protection system. This time delay depends on the transmission length and on the medium employed in the communication channel, e.g., the time delay of optical fiber is 0.5 ms per 100 km. Thus, the time delay is a critical parameter in the operation of communication-based algorithms [150], [156]. Moreover, any problem in the communication channel could endanger the protection system's operation, even, in the worst case, reaching a non-operative state [149]. Therefore, communication-based algorithms could present challenges if they are applied to long transmission systems [149], [150], [157], meanwhile, they are suitable as backup protection, operating when the main protection is not able to [150], [158], and against high-resistance faults since the speed requirement is not as restrictive during these conditions [159]. Differential-current and directional-current algorithms are common communication-based methods.

Other protection methods can be found in the literature. Some of these algorithms are based on detecting the fault-induced traveling wave while other algorithms employ artificial intelligence techniques for fault detection and location. Traveling-wave-based algorithms extract the traveling wave's frequency content by means of mathematical transforms, e.g., Wavelet transform and Fourier transform. Artificial-intelligence-based algorithms mostly employ artificial neural networks.

Hereunder, different types of protection algorithms employed in HVDC systems are reviewed. Their characteristics and operation are presented. The following algorithms are classified into current-based, voltage-based, Wavelet-transform-based and artificial-intelligence-based methods.

2.6.1. Current-based protection algorithms

Current-based protection algorithms employ DC current's features, e.g., magnitude and rate-of-rise. The most common current-based protection algorithms are reviewed in the following subsections.

2.6.1.1 Overcurrent algorithm

The overcurrent (OC) algorithm is a basic current-based method which locally monitors the DC current magnitude and compares it with a certain threshold value [149]. A fault is detected when the DC current overcomes the pre-defined threshold value as in (2.1) where I_{DC} is the current magnitude and THR_{OC} is the discriminating threshold value [154].

$$\text{Fault detection} \implies I_{DC} > THR_{OC} \tag{2.1}$$

It presents high operation speed, due to the fast rate-of-rise of the fault current, and low selectivity [151], [152] since only local data is employed. Moreover, its application to high-resistance faults can be challenging due to the lower maximum magnitude and slower rate-of-rise of the fault current during these conditions; the threshold value might not be overcome and the fault will not be detected. This method can be widely found in the literature.

An OC protection for a radial MTDC system is proposed in [160]. The current magnitude is compared with an OC threshold value of 2.1 p.u. for fault detection. OC protection method is also employed in the protection of a four-terminal symmetric-monopole MTDC system in [161] and of a three-terminal MTDC system in [162]. Likewise, paper [152] proposes an inverse time OC method which protects a three-terminal bipole MTDC system; the higher the current is, the faster the operation will be.

Authors of [163] propose a coordination method for OC relays based on communication between the relays. A reduced number of H-CBs are used to reduce costs, so they are placed on the active elements' connection points. The H-CBs operate after fault detection by instantaneous OC relays. Afterwards, the OC relays exchange operation information to locate the fault allowing switches to isolate the faulty part and, then, the H-CBs are reclosed.

In [164], DC-CBs divide a five-terminal VSC-based grid into two protection zones, i.e., a partially-selective strategy is implemented. These devices are located in the DC link that interconnects both zones. Thus, when a fault is detected by an OC algorithm, the DC-CBs operate and disconnect the protection zones, allowing the healthy zone to remain operative. Finally, the AC-CBs of the faulty zone are triggered. A similar protection strategy is presented in [165]. Apart from the

protection zone division by DC-CBs, an alternative using DC/DC converters is proposed. Fault detection is achieved when the arm current of the DC/DC converters exceeds its internal overcurrent threshold value, and the converters are blocked disconnecting the zones. Same authors of [165] use the DC/DC converter alternative as protection strategy for a six-terminal MTDC grid in [166].

An analysis of the OC method is presented in [167] for a four-terminal symmetric-monopole MMC-based system. H-CBs and 150 mH limiting inductors are employed, adopting a full-selective strategy. The OC performance is tested against different fault conditions. This way, the OC algorithm presents an operation time in the range of 1 to 7 ms, depending on the fault distance. In addition, it presents better performance against PtP fault conditions than against PtG fault conditions, in the case of high-resistance faults.

Reference [168] proposes a combination of the OC algorithm with a multiple decision criteria in a four-terminal bipole MMC-based grid. SS-CBs are employed for current interruption while no limiting inductors are placed in the system. The multiple decision criteria is based on an undervoltage algorithm, on detecting first a negative current and a subsequently positive current within a determined time range, and on a current-derivative algorithm. This way, the selectivity and sensitivity of the protection scheme are improved. Fault conditions with impedances of 0.5 Ω and 20 Ω are cleared in 8.74 ms and 11.26 ms, respectively.

2.6.1.2 Rate-of-change-of-current algorithm

The Rate-Of-Change-Of-Current (ROCOC) algorithm is a derivative-based method. Therefore, the DC current is measured and its derivative is calculated. The current-derivative is ideally zero during normal operation while a significant change in its value happens during fault conditions. This value variation makes the current-derivate a distinct fault marker that can be used in fault discrimination. Nevertheless, fluctuation and disturbances produce a non-zero current-derivative value during normal operation. Then, the current-derivative is compared with a pre-defined threshold value, improving the protection system's selectivity [150], [154], [169]. Fault detection is achieved when the calculated current-derivative overcomes the threshold value as it is shown in (2.2), where I_{DC1} and I_{DC2} are the DC current's magnitude at times t_1 and t_2, being time t_2 higher than time t_1.

$$\text{Fault detection} \implies \text{ROCOC}=\frac{dI_{DC}}{dt}=\frac{\Delta I_{DC}}{\Delta t}=\frac{I_{DC_2}-I_{DC_1}}{t_2-t_1}>THR_{ROCOC} \tag{2.2}$$

The current-derivative algorithm presents faster fault detection than the overcurrent algorithm due to the fast increase of the fault current which generates a sharp current-derivative value [170]. However, the current-derivative produced by a remote high-resistance internal fault can be lower than the current-derivative

induced by a solid external fault due to the slower rate-of-rise of the current during high-resistance fault conditions [149]. Thus, high-resistance faults might be difficult to detect using the ROCOC algorithm.

Paper [171] presents a ROCOC-based protection system. It is concluded, through simulations and experimental studies, that this method presents reliable and fast operation. An analysis of the applicability of a communication-based algorithm to a five-terminal MTDC system is presented in [157]. This algorithm compares the ROCOC sign at both ends of a link. A fault is detected when both ROCOCs present the same sign. The authors assert that the applicability of a communication-based algorithm in this system is challenging, since the critical fault-clearing times cannot be satisfied because of the imposed communication time delay.

A protection system consisting of a ROCOC algorithm protects a three-terminal bipole MTDC grid in [172]. The DC current is measured locally, its derivative is calculated and then its first peak is analysed. A forward fault is detected if this peak shows a positive polarity. If the peak is negative, the fault is located in the backward direction. 10 mH Fault Current Limiters (FCLs) are placed in series with DC-CBs at both ends of each link so as to enhance the selectivity. The protection operation time is lower than 3 ms.

Reference [173] presents a protection scheme for a three-terminal bipole MTDC system against faults with different impedances. Inductive FCLs are employed to ensure selectivity while limiting the increase of the current. The calculated ROCOC value is compared with a threshold value of 1.5 kA/ms. The current polarity is monitored to add directional selectivity. Furthermore, an OC-based supervision criterion has to be fulfilled in order to trip the DC-CBs.

Similarly, a ROCOC algorithm is applied to the MTDC system presented in [167]. A discriminating threshold value of 3 kA/ms and limiting inductors with a size of 100 mH are employed in this case. This method presents a detection time around 1 ms, depending on the fault distance. However, its application to detect high-resistance faults is challenging.

Reference [174] presents a fault location algorithm consisting of the Rate-Of-Change (ROC) of the discharging current of the converter filter capacitor. It can be employed to detect both high- and low-impedance faults, since the initial ROC is very similar for both cases and it is mostly dependent on the fault location. However, this method is still challenging because the ROC decays exponentially over time, so a delay in the measurements might mean a non-accurate location of the fault, mistaking it with an external fault.

Reference [175] proposes a fault detection algorithm based on calculating the correlation-coefficient between the ROC of the DC line current and the ROC of the discharging current of the DC link capacitor. This way, the correlation-coefficient

is calculated when the ROC of the line current surpasses a certain threshold value. Fault detection is achieved when this coefficient is close to the unity. This method shows a detection time lower than 1 ms, which is not influenced by the fault location.

A faulty conductor identification algorithm based on the ROCOC is presented in [170] for a three-terminal bipole VSC-based system. This algorithm allows discrimination between PtG faults, PtP faults and faults involving the dedicated metallic return conductor. The fault marker is the ratio between the maximum ROCOC of two conductors. The fault type is identified by comparing the value of this ratio, for different pairs of conductors, with their respective threshold values.

2.6.1.3 Differential-current algorithm

Differential-current algorithm is a communication-based method based on summing the input and output currents of a link or busbar [150], [154]. The differential-current presents a value near zero during normal condition since the currents measured at both ends of the corresponding protection zone are approximately equal but with opposite polarities. Meanwhile, the differential-current presents a non-zero value during fault conditions indicating that the currents measured present the same polarity but different magnitudes. Therefore, this feature can be used as a fault marker. The differential-current in a busbar is calculated in (2.3) where I_{DCi} is the current flowing through each link connected to the busbar and "n" is the number of links connected to the busbar while the differential-current in a link L_{ij} is calculated in (2.4) where I_{DCij} is the current measured at one end of the link and I_{DCji} is the current measured at the other end of the link.

$$\text{Fault detection} \implies \text{DiffCurr}_{bus} = \sum_{i=1}^{n} I_{DC_i} > \text{THR}_{\text{DiffCurr}} \tag{2.3}$$

$$\text{Fault detection} \implies \text{DiffCurr}_{line} = I_{DC_{ij}} + I_{DC_{ji}} > \text{THR}_{\text{DiffCurr}} \tag{2.4}$$

Comparison with a threshold value is implemented in order to avoid nuisance operation due to oscillations and fluctuations. Thus, fault detection is achieved when the differential-current exceeds the threshold value. Nevertheless, the differential-current algorithm's operation speed is limited by the communication time delay, which is dependent on the communication channel medium and on the transmission distance. Then, it might not be fast enough if the transmission distance is very long. However, it presents great performance against high-resistance faults.

A differential-current algorithm is proposed in [72] as the main protection of a five-terminal bipole VSC-based grid. An optical fiber channel is employed in the communication channel. This algorithm requires that three consecutive samples fulfil the detection condition in order to produce the trip signal. This way, the

probability of misdetection is considerably reduced. The protection system operates properly in cases of high-resistance faults, up to 200 Ω. The same protection system and grid are used in [176], but resistive superconducting FCLs are employed, limiting the increase of the DC current and helping the DC-CBs to interrupt lower values of current. Likewise, [177] uses the same protection system and MTDC grid presented in [72], [176].

The differential-current-based protection system proposed in [178] covers main, busbar and backup protections of a five-terminal bipole MTDC system. Optical fiber is used as communication channel medium. As in [72], [176], the main protection needs three consecutive samples to generate the trip signal. In the case of the busbar protection, all the currents flowing in and out the busbar through the branches are summed to detect faults located between the converter station and the relays located at the beginning of every link. The backup protection aims to operate in cases of failure of the main protection by tripping all the DC-CBs located in the closest busbar; its operation starts after a certain time delay.

The same protection system proposed in [178] is used again in [179] but, in this case, a four-terminal symmetric-monopole MTDC system is protected and fault-tolerant inductor-capacitor-inductor converters (LCL-VSC) are employed. This type of converters allows limiting the DC current during fault conditions up to the rated current value [180]. The fault-clearing time is around 30-60 ms.

Reference [181] proposes a differential-current algorithm for fault detection and identification in a four-terminal MTDC system. Reference [182] presents a four-terminal full-bridge MMC-based system. This type of converter can actively control DC currents and, this way, the requirement of operation speed is not that critical. Due to this, a differential-current algorithm is chosen as the main protection.

Reference [183] presents a protection strategy with a series of current measuring sensors distributed every 30 km along the links of a five-terminal MTDC system employing half-bridge MMCs. This way, the measurements taken by two consecutive optical sensors are used to calculate a series of differential-currents, and, then, they are compared with a threshold value. The communication time delay is limited by the distance between adjacent sensors. The differential-current calculation is part of the first of the three stages of the protection strategy. The second stage ensures the fault detection by observing the ROCOC and the last one ensures there is no sensor failure. This strategy enables high speed operation, better stability and reliability.

2.6.1.4 Directional-current algorithm

The directional-current algorithm consists of monitoring the current polarity and, thus, it detects faults located in the forward direction. It is a communication-based

algorithm since the trip signals are issued when the current polarity is positive (flowing from bus to line) in both ends of the protection zone, i.e., the fault is detected as a forward fault at both ends of the protection zone [150]. As a communication-based algorithm, it presents high selectivity but a limited operation speed due to the communication time delay [149].

A directional-current fault detection method is presented in [184] for a four-terminal symmetric-monopole VSC-based system. During fault conditions, both currents are flowing from the buses to the link. A supervision criterion is added to avoid misdetection: current at both link ends must exceed a certain threshold value.

Authors of [185] propose two alternatives for fault detection: one combining overcurrent and undervoltage algorithms, and a ROCOC-based one. In addition, a directional element is included by monitoring the fault current polarity.

Protection of a four-terminal MTDC grid is achieved in [186] by a directional OC algorithm. Therefore, when an overcurrent is detected, the current polarity at the limits of the protection zone is monitored. If the current polarity is the same at both ends, the fault is located inside the protection zone.

2.6.2. Voltage-based protection algorithms

Voltage-based protection algorithms are those that employ features of the DC voltage such as magnitude, rate-of-rise, etc. Common voltage-based protection algorithms are reviewed hereunder.

2.6.2.1 Undervoltage algorithm

The undervoltage (UV) algorithm consists of measuring the DC voltage's magnitude. A fault induces a collapse of the DC voltage, so a fault can be detected by comparing the DC voltage's magnitude with a pre-defined threshold value. Fault detection is achieved when the DC voltage falls to a value lower than the threshold value as it is shown in (2.5) where V_{DC} is the voltage magnitude and THR_{UV} is the discriminating threshold value.

$$\text{Fault detection} \implies V_{DC} < THR_{UV} \tag{2.5}$$

The undervoltage algorithm presents high operation speed since it only employs local measurements. However, its application to high-resistance faults is challenging since the fault-induced voltage drop is reduced under these conditions, so the voltage might not drop to a value lower than the pre-defined threshold value and the fault will not be detected.

An UV algorithm is proposed in [187] to protect a four-terminal symmetric-monopole MTDC grid. A fault is detected when the voltage drops under a certain threshold value. DC-CBs and 100 mH limiting inductors are placed at both ends of each link.

Similarly, authors of [167] apply the UV algorithm to the same system presented in [187]. However, in this case, three successive samples of the voltage have to drop under a discriminating threshold value of 0.1 p.u. A sampling frequency of 10 kHz and 150 mH limiting inductors are used. Hence, the UV method achieves fault detection in approximately 1 ms however it presents low sensitivity to high-resistance faults.

On the other hand, a combination of the UV and the OC algorithm is presented in [188] and applied to the same system presented in [187]. Three consecutive samples of the voltage magnitude lower than a threshold value are needed to achieve fault discrimination, as in reference [167]. Moreover, the UV and OC algorithms work independently. This way, the protection system detects a fault when one of the two conditions (OC or UV) is fulfilled.

Likewise, another UV-OC combination is presented in reference [156]. Both OC and UV conditions have to be satisfied in this case in order to achieve fault detection. Once again, the UV condition consists of three consecutive samples. In addition, a communication system is implemented for better performance with long transmission distances.

2.6.2.2 Rate-of-change-of-voltage algorithm

The Rate-Of-Change-Of-Voltage (ROCOV) algorithm is a local-measurement-based method which is based on calculating the voltage-derivative. It presents very high operation speed due to the fault-induced sharp collapse of the DC voltage. Due to the fault-induced voltage collapse, the calculated voltage-derivative values are negative values so fault detection is achieved when the ROCOV value drops below a certain negative threshold value as it is shown in (2.6) where V_{DC1} and V_{DC2} are the DC voltage magnitudes at time t_1 and t_2; being time t_2 higher than time t_1.

$$\text{Fault detection} \implies \text{ROCOV}=\frac{dV_{DC}}{dt}=\frac{\Delta V_{DC}}{\Delta t}=\frac{V_{DC_2}-V_{DC_1}}{t_2-t_1}<THR_{ROCOV} \quad (2.6)$$

Moreover, the fault resistance does not affect the performance of the voltage-derivative algorithm as much as it affects the undervoltage algorithm's operation, i.e., even if the DC voltage drop is not as pronounced, it is still very abrupt, therefore, the calculated voltage-derivative value is considerably high (in absolute value) in comparison to normal conditions. Thus, it can be a local-measurement-

based solution to detect high-resistance faults as long as a suitable threshold value is selected.

Reference [189] proposes a ROCOV-based protection for a nine-terminal bipole MTDC system. The rate-of-change of the DC link voltage is calculated and then it is compared with a certain threshold value. This protection system adopts a full-selective fault-clearing strategy, placing H-CBs in series with 100 mH limiting inductors at both ends of each link. This way, only the faulty link will be isolated.

Similarly, a ROCOV algorithm protects a four-terminal symmetric-monopole MMC-based grid in [167]. The ROCOV is calculated locally and compared with a discriminating threshold value of -200 kV/ms. As in the previous reference, H-CBs and limiting inductors with a size of 100 mH are selected, following a full-selective strategy. The ROCOV method presents a detection time lower than 1 ms and it is capable of detecting high-impedance faults up to 750 Ω PtP faults and 400 Ω PtG faults.

Authors of [190] present a ROCOV method for fault detection in a four-terminal bipole MMC-based system. The operation of this algorithm is challenging against fault conditions with impedances higher than 100 Ω. Thus, authors propose an adaptive threshold value to improve its selectivity against high-impedance faults: a curve fitting method is employed to estimate a fault impedance interval and, then, the adaptive threshold value is obtained, taking into account the maximum ROCOV value for an external fault condition with the estimated impedance.

Reference [191] presents a ROCOV-based protection system for a three-terminal bipole VSC-based system with one Overhead Line (OHL) and two underground cables. 100 mH inductors delimit the protection zones. The ROCOV is employed as the main link protection and busbar protection. The main protection calculates the ROCOV locally at both ends of the line.

Authors of [192] propose a method to identify the fault direction for improved reliability, sensitivity and speed of the protection method presented in [191]. Thus, the ROCOV at both sides of the line terminal inductors are compared: if the line-side ROCOV is the highest, the fault is located in the protected line; otherwise, it is an external or busbar fault. In addition, an undervoltage condition is used as a supervision criterion. In order to improve the performance against high-impedance faults, a communication channel is added since the speed requirement is not a constraint.

2.6.2.3 Inductor-voltage algorithm

Limiting inductors are implemented in VSC-based grids as a way to reduce the rate-of-rise of the fault current, so DC-CBs with lower current interruption

capability can be employed. They also delimit the borders of a protection zone thanks to their damping characteristic so external fault waves are attenuated and can be discriminated from internal fault waves. Therefore, protection systems can profit from this feature and employ the voltage generated across the inductor after fault inception as a fault marker. For selectivity purposes, the voltage, V_L, across the limiting inductor is compared with a threshold value. Fault detection is achieved when the threshold value is overcome by V_L, as it is shown in (2.7); where L is the inductance, di/dt is the current-derivative, V_{bus} is the voltage measurement taken at the bus-side of the inductor, V_{link} is the voltage measurement taken at the link-side and THR_{LV} is the threshold value needed to achieve fault detection.

$$\text{Fault detection} \implies V_L = L \cdot \frac{di}{dt} = V_{bus} - V_{link} > THR_{LV} \tag{2.7}$$

The voltage across the limiting inductors is used as a fault marker in [193]. If this voltage exceeds a determined threshold value, a trip signal is issued. Similarly, authors of [194] employ the voltage across the limiting inductor as a fault marker. Fault type discrimination is achieved by comparing the difference between the inductor voltages of both poles: a PtP fault is identified if this difference is lower than a pre-defined threshold value; otherwise, a PtG fault is identified and the faulty pole is the one with the highest absolute inductor voltage. In addition, a communication-based backup protection for high-resistance faults is presented; a fault is detected when the absolute inductor voltage is higher than a threshold value, which is lower than the main protection threshold value. Then, the amplitude and directional information of the inductor voltages at both ends of the protection zone are used for faulty line and faulty pole identification, respectively. This method was tested through simulations in a four-terminal VSC-based grid. It operates within 1 μs for low-resistance faults and within 2 ms for high-resistance faults.

Authors of [195] also propose a fault detection algorithm based on the voltage variation across the 200 mH inductors of a meshed three-terminal symmetric-monopole MMC-based system. The time interval required by the DC voltage across the inductor to exceed two threshold values is used as fault marker. This way, a fault is detected when this time interval is less than a certain threshold value, since the voltage across the inductor increases faster for internal faults.

On the other hand, reference [196] presents a main and backup protection scheme based on the ratio of the transient voltages at both sides of the limiting inductors. During fault conditions, the transient voltage in the line-side of the limiting inductor will be higher than the transient voltage in the converter side, increasing the value of the ratio. Hence, a fault is detected when the ratio overcomes a pre-defined threshold value. The main protection only uses local measurements while the backup protection employs a communication system in order to improve the performance of the protection scheme against high-resistance faults. It is

analysed in a five-terminal symmetric-monopole VSC-based grid with 10 mH limiting inductors.

Similarly, the authors of [197] also employ measurements at both sides of the limiting inductors. In this case, this alternative is based on comparing the ratio between the ROCOV at both sides of the limiting inductors with a threshold value; forward fault detection is achieved when the ratio overcomes the threshold value. This implies higher operation speed. Fault detection and discrimination are achieved in less than 200 microseconds.

2.6.3. Traveling-wave-based protection algorithms

A fault condition induces a variation in the current and voltage waveforms that is quickly propagated throughout the HVDC system [149], [154]. Traveling-wave-based algorithms consist of detecting this variation when it arrives to the relay point by extracting some useful information from the waveforms [149], [150]. Mathematical transforms, like the Fourier and Wavelet transforms, extract these interesting features from the current and voltage waveforms.

Traveling-wave-based algorithms present fast and accurate performance [71], [198]. However, the main limitations are the complexity of the mathematical modelling of the traveling wave, the detection of the wave-head, the incapability of detecting close-up faults, the different traveling wave speed in underground cables and OHLs, and the need of a high sampling rate [199].

2.6.3.1 Fourier transform

Fourier Transform is a very relevant signal processing tool which is used to extract a signal's frequency content, i.e., its frequency-amplitude representation. However, no time information is available in a Fourier-transformed signal. In other words, the Fourier Transform indicates the existence of a frequency component regardless of the inception instant of this component [200].

Discrete Time Fourier Transform (DTFT) is used in [201] to analyse the frequency spectral pattern of the DC current. Fault detection is achieved by observing the distortion of the frequency due to the high frequency content.

Fault detection is achieved in [202] using the ratio between the standard deviation and the mean value of a certain range of the frequency spectrum obtained by the Fast Fourier Transform (FFT). Regarding fault location, the relationship between the gap between consecutive frequency peaks and the fault distance is used: the closer the fault is to the relay point, the larger the frequency gap is. PtP and PtG faults are discriminated comparing the frequency spectrum of both poles.

2.6.3.2 Wavelet transform

The Wavelet Transform (WT) extracts the frequency information from the traveling wave by employing a multiresolution analysis; the signal is analysed at different frequencies and resolutions [6]. Thus, the low frequency content is obtained with high frequency resolution but low time resolution while the high frequency content is obtained with high time resolution but low frequency resolution [200]. Moreover, there are some variations of the Wavelet transform. The most common ones are the Continuous Wavelet transform and the Discrete Wavelet transform.

WT is used to extract the energy content of the positive line DC current in [203]. A decision tree is formed using the energy-coefficients to recognize the fault location and type. The current-wavelet-coefficients are used as input data for a fuzzy voter in reference [204] in order to figure out the affected line and the fault type. A fault location algorithm is added to this method in reference [205]. It consists of the time difference between the arrivals of the first traveling wave and the first reflected wave.

Internal faults are detected in [206] when the wavelet-coefficient modulus maxima extracted from the DC current presents the same polarity (negative for negative pole and positive for positive pole). The faulty pole is detected comparing the values of the wavelet modulus maxima in both poles.

Since similar amplitudes of the forward and backward current traveling waves indicate an internal fault condition, authors of [207] propose using the ratio of the wavelet modulus maxima of these two waves as a fault marker. Internal fault detection is achieved when the ratio is within 0 and 1, and both modulus maxima are higher than a pre-defined threshold value. Finally, the fault type is determined comparing the polarities and values of the wavelet modulus maxima at both ends of the link.

A backup protection consisting of wavelet packet energy entropy is presented in [208] against high-resistance PtG faults. Wavelet packet process the current signal and extracts its energy entropy content. Then, the wavelet energy entropy is compared with a threshold value, discriminating between internal and external faults. Finally, the fault can be classified using the ratio between the wavelet energy entropies of both poles.

The protection system of [209] employs a stationary, translation-invariant, WT: the fast dyadic WT in which the calculations are simplified due to sampling the scale parameter along a dyadic sequence. Only local measurements are employed and it is based on three independent criteria: voltage-wavelet-coefficients, current-wavelet-coefficients, along with voltage-derivative and magnitude. Fault detection is achieved when two out of the three criteria are fulfilled. This redundancy

improves the selectivity and reliability. In addition, faulty cable discrimination is achieved by comparing the voltage-wavelet-coefficient amplitudes.

2.6.3.2.1. Continuous Wavelet transform

The Continuous Wavelet Transform (CWT) overcomes the time resolution problem associated with the application of the Fourier Transform. It is calculated for each frequency component of the signal by changing the window's width. It is dependent on the scale and translation parameters. The former parameter indicates the window's width while the latter parameter indicates the time information and window's location in the signal. This transform does not present the time resolution problem that is related to the Fourier transform, however, it requires a considerable amount of time regarding computation [200].

Reference [198] uses the CWT to detect and locate fault conditions. Fault detection is achieved when the CWT-coefficient is higher than a certain threshold value. These coefficients also indicate the traveling wave arrival times to the terminals. The time difference between both arrivals is used in fault location estimation. Likewise, authors of [210] employ the CWT to detect the arrival time of the traveling waves at both ends of the link in order to locate the fault condition.

2.6.3.2.2. Discrete Wavelet transform

The Discrete Wavelet Transform (DWT) presents lower complexity and computation time than the CWT. The DWT filters the frequency content of the signal, employing both high-pass and low-pass filters, and processes it at different scales. Hence, the signal is decomposed into frequency bands with different resolutions by using consecutive low-pass and high-pass filtering. The high-pass filter's outcomes are the coefficients of a decomposition level while the low-pass filter's outcomes continue the filtering and decomposition process. Therefore, the higher-level-coefficients, those corresponding with low frequency content, present higher frequency resolution and lower time resolution than the lower-level-coefficients, those corresponding with high frequency content [200].

DWT extracts the high frequency content from the DC current in [171], [211]-[213]. The DWT-coefficients are used as fault markers so they are compared with a threshold value to detect fault conditions. Conversely, [214] uses DWT to process the voltage traveling wave while DWT extracts the current transient high frequency energy in [215].

Reference [216] employs the DWT to obtain the high frequency and energy-coefficients from the DC current. If the energy-coefficients exceed a certain threshold value and DC currents flows in a positive direction, a fault is detected.

DWT extracts the energy and high frequency contents of the DC current wave in [217]. The amplitude of the high frequency transients is used for fast fault detection. The energy-coefficients at both ends of the same pole are similar during normal operation; otherwise, a fault condition is taking place. Then, the energy difference can be used as a fault marker, which is named operating signal. However, a restraining signal is calculated for better selectivity. This signal is the sum of the energy-coefficients at both ends of the same pole. Hence, fault discrimination is achieved by calculating the ratio between the operating and restraining signals; a trip signal is issued when the operating signal is dominant. Finally, the fault distance is calculated using the arrival time of the traveling waves which are detected when a high frequency peak takes place.

Reference [218] employs the DWT to extract the frequency content of the forward and backward voltage traveling waves. Then, a ratio between the amplitudes of the forward and backward traveling waves is calculated. A forward fault is detected if the ratio is lower than a pre-defined threshold value. Otherwise, a backward fault is detected.

2.6.4. Artificial Intelligence methods

Artificial Intelligence consists of computing concepts, which can recognize patterns and identify highly nonlinear class boundaries in the input data [7]. Artificial intelligence techniques try to resemble the behaviour of human beings by trying to automate rational decisions made by a person. These techniques can include missing data, adapt to evolving situations and improve their performance progressively thanks to accumulated experience [199].

The operation of Artificial Neural Networks (ANN) is inspired by the biological neural networks' behaviour [7]. ANNs present distributed representation and strong learning capability and are capable of recognising patters and of interpolating within the parameter space [219]. They can distinguish non-linear relationships between input and output data without knowing their internal processes after being properly trained. Then, they can employ the fault signal's features to diagnose the system [220]. Although ANNs present fast, robust and accurate operation [221], the required training process is time-consuming since it is specific to each system [5].

Reference [199] proposes an ANN-based protection scheme. It detects, locates and classifies faults in a three-terminal MTDC grid. Three different ANNs achieve these three fault identification operations, independently. Moreover, it shows fast speed (less than 5 ms), reliability and accuracy in fault detection and location, and an improved robustness to high-impedance and close-up faults. The input data for the three ANNs is the high frequency content from the fault current signal, which is extracted using the Discrete Fourier Transform (DFT), and only the magnitude of the frequencies is used.

Authors of [222] present a comparison between three different ANN-based algorithms for fault detection and location in a four-terminal VSC-based system. These three algorithms are based on local current measurements. The first algorithm directly uses DC current samples as input data. Meanwhile, in the second one, the DFT processes the DC current to extract its frequency spectrum, which would be the input data of the ANNs. In the case of the third algorithm, the input data is composed by the wavelet-coefficients extracted from the DC current using the DWT. Each line of the grid has two ANNs, for fault detection and location, respectively. From the comparison of the three algorithms, it is concluded that the third one presents better performance and accuracy, since the responses of the other two ones present difficulties during far-end fault conditions.

2.6.5. Comparison

A comparison of the different protection systems found in the literature for MTDC systems is summarised in Table 2.3, in alphabetical order, according to the protection system used. Firstly, the protection systems are classified considering the grid's characteristics:

- VSC technology: two-level VSC (2L-VSC), three-level VSC (3L-VSC), LCL-VSC, half-bridge MMC (HB-MMC) or full-bridge MMC (FB-MMC).
- System configuration: monopole (MonoP), symmetric-monopole (S-MonoP) or bipole (BiP).
- Line type and length: regarding the use of OHL or cables in the MTDC and their respective lengths.

Then, the different protection systems are classified regarding their characteristics:

- Local-measurement-based algorithm (Loc) or communication-based algorithm (Com).
- Adopted fault-clearing strategy: full-selective, partially-selective or non-selective.
- Breaking device: AC-CB, DC switch, DC-CB, H-CB, SS-CB, M-CB or DC/DC converter.
- Size of the limiting inductors located in series with the DC-CBs.
- Performance against high-impedance fault ($F_{resistance}$).

- Fault detection time ($t_{detection}$): related to the time needed by the algorithm to detect a fault.

- Fault clearing time ($t_{clearing}$): includes the algorithm's fault detection time and the breaking device's operating time.

The remaining abbreviations used in Table 2.3 are: fault detection method (F_{det}), fault location method (F_{loc}), fault location time (t_{loc}), fault isolation method (F_{iso}), fault isolation time (t_{iso}), grid partition method (GPar), grid partition time (t_{gpar}), main protection (M), busbar protection (BB), backup protection (BU), differential-current (DiffCurr), high-impedance fault condition (HIF), low-impedance fault condition (LIF).

From this comparison, it can be concluded that local-measurement-based algorithms are the most usual ones, instead of communication-based algorithms, due to their faster operation. It must be highlighted that a considerably high number of protection systems employ a combination of several methods. By using each method for different conditions, their advantageous characteristics are combined and the performance of the protection system is improved in terms of selectivity, sensitivity and robustness.

Similarly, the most common converter technology is the half-bridge MMC, whilst the most used system configurations are bipole and symmetric-monopole. Likewise, full-selective strategies are predominant, as well as H-CBs, which are chosen rather than SS-CBs and M-CBs. Meanwhile, AC-CBs are selected when non-selective and partially-selective strategies are adopted. In the case of partially-selective strategies, DC-CBs are preferred for the grid partition stage, while AC-CBs and DC switches are preferred for the fault isolation stage. Furthermore, the size of the limiting inductors varies mainly in the range of 50 and 150 mH, being the most common value 100 mH.

To sum things up, it can be concluded that the tendency is to use a combination of protection algorithms for improved reliability, preferably local-measurement-based algorithms due to speed and operation constraints in transmission distances of hundreds of kilometres. In addition, full-selective fault-clearing strategies, along with H-CBs, may have great relevance in future projects, as, e.g., in the Zhangbei MTDC project in China [64].

Table 2.3.- Comparison of the reviewed protection algorithms. [Part 1 of 5]

Ref.	Year	Algorithm	Loc/Com	Converter Topology	System Config.	OHL or Cable	Link length (km)	Fault-clearing strategy	Breaking device	Inductor size (mH)	$F_{resistance}$ (Ω)	$t_{detection}$ (ms)	$t_{clearing}$ (ms)
[199]	2017	ANN	Loc	2L-VSC	S-MonoP	OHL	200	Full	DC-CB	-	100	4.5 26 (t_{loc})	-
[222]	2018			VSC	MonoP		650, 530, 370					<5	
[198]	2012	CWT	Com	VSC	-	OHL	24, 44, 97	Full	DC-CB	-	-	-	-
[210]	2014					Cable	5, 20, 30, 40, 50, 70				100		
[72]	2012	DiffCurr	Com	VSC	BiP	Cable	25, 50, 75, 100, 200	Full	DC-CB	40	200	0.3-1	-
[177]	2014			VSC		OHL	25, 50, 75, 100, 200		DC-CB	-	10	-	-
[176]	2013			2L-VSC		Cable	25, 50, 75, 100, 200		DC-CB	-	500	-	-
[178]	2013			2L-VSC		Cable	25, 50, 75, 100, 200		H-CB	30	200	-	1-3
[182]	2018			FB-MMC		Both	200, 300, 400, 500		M-CB	5	400	-	20
[181]	2014	DiffCurr	Com	VSC	S-MonoP	Cable	-	Full	-	-	-	-	-
[223]	2015			VSC			100, 150, 200		H-CB	-	-	-	-
[179]	2015			LCL-VSC			600		DC-CB	-	-	-	30-60
[183]	2017			HB-MMC			90, 120, 150, 180, 300		H-CB	150	300	-	3-4
[184]	2015	Directional-current	Com	VSC	S-MonoP	Cable	-	Full	SS/H/M-CB	50-100	7	-	1/2-5/60
[186]	2015	Directional-current	Com	HB-MMC	S-MonoP	Cable	35.5, 100, 107, 110, 200	Non	AC-CB and DC switch	-	7	-	60
[185]	2013	Directional-current	Loc	2L-VSC	-	Cable	300, 500	Full	DC-CB	-	-	-	15

Table 2.3.- Comparison of the reviewed protection algorithms. [Part 2 of 5]

Ref.	Year	Algorithm	Loc/Com	Converter Topology	System Config.	OHL or Cable	Link length (km)	Fault-clearing strategy	Breaking device	Inductor size (mH)	$F_{resistance}$ (Ω)	$t_{detection}$ (ms)	$t_{clearing}$ (ms)
[201]	2016	DTFT	Loc	MMC	S-MonoP	Both	200	Full	DC-CB	-	-	-	-
[217]	2016	DWT	Com	2L/3L-VSC/ HB-MMC	BiP	Both	60, 200, 300	Full	DC-CB	-	300	-	-
[224]	2017	DWT	Loc	VSC	BiP	Both	30, 60, 200, 300	Full	SS/H CB	-	150	-	2.2/3.2
[171]	2018			VSC	-	-	-		DC-CB	-	-	-	-
[215]	2019			VSC	-	OHL	100, 200, 300		DC-CB	100	300	1	-
[213]	2016			2L-VSC	-	Cable	-		H-CB	10	-	-	-
[212]	2017			MMC	MonoP	-	100, 200		DC-CB	-	500	1	-
[216]	2016			HB-MMC	BiP	Cable	200, 300, 400		DC-CB	-	-	1	-
[218]	2020			MMC	-	OHL	542, 908		-	50, 150, 500	-	-	-
[214]	2018	M: DWT BB: DiffCurr	Loc	MMC	S-MonoP	OHL	100, 120, 150, 180, 200, 300, 600	Full	H-CB	150	500	1	-
[202]	2018	FFT	F_{Det}: Loc F_{Loc}: Com	VSC	-	Cable	170, 200, 360, 460	Full	DC-CB	-	Solid	1 10 (t_{loc})	-
[193]	2014	Inductor Voltage	Loc	2L-VSC	BiP	Cable	25, 50, 75, 100, 200	Full	DC-CB	10, 15, 20, 25, 30, 35, 40, 45	50	-	1-2
[195]	2017			MMC	S-MonoP	Both	100, 150			200	1000	1-4	-
[194]	2018			HB-MMC	S-MonoP/ BiP	Cable	100, 200			150	380	LIF: 0.001 HIF: 2	-
[196]	2017	Inductor Voltage	M: Loc BU: Com	VSC	S-MonoP	Both	70, 100, 200	Full	DC-CB	10	200	0.2-0.9	-

Table 2.3.- Comparison of the reviewed protection algorithms. [Part 3 of 5]

Ref.	Year	Algorithm	Loc/Com	Converter Topology	System Config.	OHL or Cable	Link length (km)	Fault-clearing strategy	Breaking device	Inductor size (mH)	$F_{resistance}$ (Ω)	$t_{detection}$ (ms)	$t_{clearing}$ (ms)
[163]	2014	OC	Com	VSC	-	-	-	Partially	H-CB and DC switch	-	100	-	H-CB: 5 DC switch: 70 (t_{iso})
[160]	2010	OC	Loc	VSC	-	Cable	-	Full	DC-CB	-	-	-	-
[152]	2015			HB-MMC	BiP		200, 300		-	10, 100, 500	-	-	2-3
[162]	2017			HB-MMC	-		-		H-CB	8	-	-	5
[167]	2019			HB-MMC	S-MonoP		100, 150, 200		H-CB	150	PtP: 200 PtG: 20	1-5	3-7
[164]	2015	OC	Loc	HB-MMC	-	Cable	50, 80, 100	Partially	GPar: DC-CB F_{Iso}: AC-CB	100	-	-	12-13 (t_{gpar}) 63-65 (t_{iso})
[165]	2016						50, 80, 100		GPar: DC-CB or DC/DC conv. F_{Iso}: AC-CB and DC switch			-	DC-CB: 7-9 (t_{gpar}) DC/DC conv.: 3-6 (t_{gpar}) 83-87 (t_{iso})
[166]	2016						50, 75, 80, 100, 120		GPar: DC/DC converter F_{Iso}: AC-CB and DC switch or M-CB			-	4-8 (t_{gpar}) AC-CB: 104-108 (t_{iso}) M-CB: 24-28 (t_{iso})
[161]	2016	M: OC BB: DiffCurr	M: Loc BB: Loc/Com	HB-MMC	S-MonoP	Cable	100, 150, 200	Full	DC-CB	100	Solid	-	-
[168]	2018	OC-UV-ROCOC combination	Loc	HB-MMC	BiP	OHL	50, 320, 330, 450	Full	SS-CB	Not employed	20	-	8.74-11.26

Table 2.3.- Comparison of the reviewed protection algorithms. [Part 4 of 5]

Ref.	Year	Algorithm	Loc/Com	Converter Topology	System Config.	OHL or Cable	Link length (km)	Fault-clearing strategy	Breaking device	Inductor size (mH)	$F_{resistance}$ (Ω)	$t_{detection}$ (ms)	$t_{clearing}$ (ms)
[130]	2018	OC-ROCOC-WT combination	Loc	2L-VSC	S-MonoP	Cable	200	Full	DC-CB	-	10	1.4	-
[157]	2014	ROCOC	Com	2L-VSC	-	Cable	170, 200, 360, 400	Full	DC-CB	-	Solid	-	2-9
[174]	2012	ROCOC	Loc	VSC	-	Cable	-	Full	DC-CB	-	-	-	-
[171]	2018			VSC	-	-	-		DC-CB	-	-	-	-
[172]	2015			MMC	BiP	Cable	150, 400		DC-CB	10	Solid	-	3
[170]	2019			HB-MMC	BiP	Both	100,500, 1500		DC-CB	40	50	1	-
[167]	2019			HB-MMC	S-MonoP	Cable	100, 150, 250		H-CB	100	PtP: 5 PtG: 2	0.095-1.25	2.095–3.25
[173]	2016	M: ROCOC BU: DiffCurr	M: Loc BU: Com	MMC	BiP	Cable	150, 400	Full	DC-CB	25	M: 75 BU: 400	-	M: 2-3 BU: 13
[175]	2018	ROCOC correlation-coefficient	Loc	VSC	S-MonoP	Cable	200	Full	DC-CB	100	10	-	1
[191]	2016	ROCOV	Loc	MMC	BiP	Both	100, 500, 1500	Full	H-CB	100	-	-	3
[197]	2018			MMC	BiP	Both	100, 500, 1100, 1500			40	200	0.2	-
[167]	2019			HB-MMC	S-MonoP	Cable	100, 150, 200			100	PtP: 750 PtG: 400	0.005-1.1	2.005–3.1
[190]	2020			MMC	BiP	OHL	500			200	300	1	-
[189]	2015	M: ROCOV HIF: OC	Loc	MMC	BiP	Both	100, 200, 300, 400, 500	Full	H-CB	100	10	-	3
[192]	2017	M: ROCOV HIF: ROCOV-UV	M: Loc HIF: Com	MMC	BiP	Both	100, 500, 1500	Full	H-CB	50, 100, 125	200	-	3

Table 2.3.- Comparison of the reviewed protection algorithms. [Part 5 of 5]

Ref.	Year	Algorithm	Loc/Com	Converter Topology	System Config.	OHL or Cable	Link length (km)	Fault-clearing strategy	Breaking device	Inductor size (mH)	$F_{resistance}$ (Ω)	$t_{detection}$ (ms)	$t_{clearing}$ (ms)
[187]	2015	UV	Loc	HB-MMC	S-MonoP	Cable	100, 150, 200	Full	H-CB	100	-	3-4	5-6
[167]	2019									150	PtP: 15 PtG: 5	0.205-1.375	2.205–3.375
[156]	2019	UV-OC combination	Com	HB-MMC	S-MonoP	Cable	100, 150, 200	Full	H-CB	100	Solid	4-5	6-7
[188]			Loc									0.35-3.35	2.35-5.35
[206]	2018	WT	Com	2L-VSC	BiP	OHL	100, 120, 150	Full	DC-CB	-	400	-	3
[207]	2018			2L-VSC	BiP	Cable	80, 100, 150, 200			-	400	-	-
[208]	2019			MMC	S-MonoP	OHL	50, 100, 150, 200			100	1000	-	-
[209]	2011	WT	Loc	VSC	BiP	Cable	400	Full	DC-CB	-	Solid	1	-

2.7. Conclusion

This chapter has presented the main characteristics of HVDC systems and modern VSCs. The advantageous characteristics of the VSC technology which facilitate the development of MTDC systems have been presented and thus the different topologies (2L-VSC, 3L-VSC and MMC) have also been introduced. Likewise, the different submodule structures employed in the MMC topology and their characteristics have been detailed. In addition, the different ways of configuring a HVDC system have been outlined.

Fault conditions in HVDC systems are more complex to be dealt with than in HVAC systems due to the fault-induced DC voltage's collapse and the DC current's fast rate-of-rise. Moreover, the VSCs commonly employed in MTDC grids present a low overcurrent withstand capability that only allows a very limited range of time for fault clearance before being damaged.

Hence, fast protection systems and DC-CBs capable of operating in this short range of time while interrupting high currents are needed. SS-CBs can satisfy these requirements, however, they present very high costs due to the large number of semiconductor devices needed in their operation. Conversely, M-CBs present low costs in comparison but their operation speed is limited by the AC interrupter employed in their main branch. Therefore, H-CBs are seen as the most appropriate alternative for future MTDC systems since they present faster operation than M-CBs and lower costs than SS-CBs. Additionally, features like the pro-active control make them stand out.

Likewise, the fault-clearing strategy applied to the HVDC system makes a great difference in how a fault condition affects the grid. Non-selective fault-clearing strategies are not appropriate for its application to large MTDC systems since a complete shut down of the system is not feasible. On the other hand, partially-selective fault-clearing strategies can be adopted in a MTDC system if its size is relatively small or if the shut down of a large part of the HVDC grid does not imply an important negative effect on the interconnected HVAC systems. However, the full-selective fault-clearing strategy is the most appropriate and efficient one to be applied in MTDC systems since the fault-induced effects are minimized and only the affected part of the grid is de-energized while the remaining parts continue their operation without significant disturbances. Nevertheless, the full-selective fault-clearing strategy requires DC-CBs at both borders of each protection zone, which can considerably increase the costs. Moreover, DC-CBs are still not commercially available.

Different types of protection algorithms applied to HVDC systems have been reviewed. Communication-based algorithms present the highest selectivity however their limited operation speed due to the communication time delay makes

their application to VSC-based grids complex and relegated to backup protection or specific conditions like high-resistance fault detection. Conversely, local-measurement-based algorithms present the fastest operation and even if their selectivity is not the best, it can be compensated by using limiting inductors and appropriate threshold values. Moreover, the operation and characteristics of common current-based, voltage-based, traveling-wave-based and artificial-intelligence-based HVDC algorithms found in the literature have been reviewed in this section.

It can be concluded that the current tendency of protection systems for MTDC grids employs predominantly local-measurement-based algorithms, as well as H-CBs, full-selective strategy and half-bridge MMCs. Moreover, the preferred system configuration varies between bipole and symmetric-monopole. Similarly, the most selected size of the limiting inductors is 100 mH. In addition, a combination of different protection methods can benefit the performance of the protection system.

Chapter 3.

LIMITING INDUCTOR VOLTAGE-RATIO-DERIVATIVE-BASED PROTECTION SCHEME

Limiting inductors are a key element for the proper operation of local-measurement-based protection systems in HVDC grids since they provide a clear delimitation of the protection zones by damping external traveling waves. This damping characteristic is very useful for fault detection purposes as the voltage across the limiting inductor can be used as a fault marker.

Figure 3.1 shows how the voltage measurements are taken at both sides of the limiting inductor. The voltage measured at the bus-side of the inductor is V_{bus} while V_{link} is the voltage measured at the link-side.

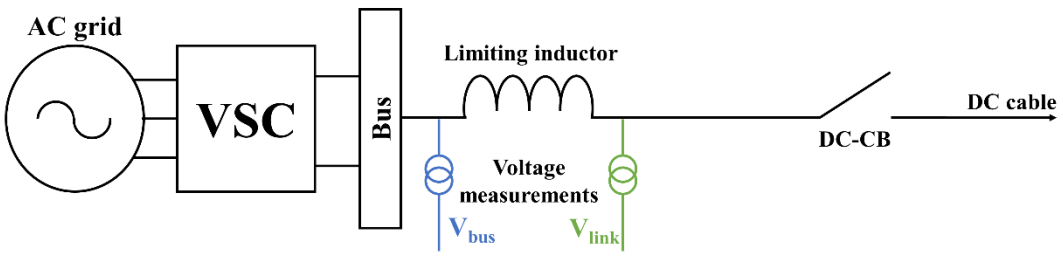


Figure 3.1.- Diagram of the voltage measurements at both sides of the limiting inductor.

The voltage across the inductor is zero during normal operation (constant DC current) since an inductor under direct current ideally behaves as a short-circuit. Thus, the voltages measured at both sides of the inductor are equal. Conversely, a fault condition produces a difference of voltage between V_{link} and V_{bus}.

The difference between the voltages at both sides of the limiting inductor causes the voltage across it (V_L) to increase, as it can be seen in (3.1) where L is the inductance, di/dt is the current-derivative, V_{bus} is the voltage measurement taken at the bus-side of the inductor and V_{link} is the voltage measurement taken at the link-side. Thus, this feature is an indicative of the presence of a fault condition in the system and can be employed as a fault marker.

$$V_L = L \cdot \frac{di}{dt} = V_{bus} - V_{link} \tag{3.1}$$

A novel local-measurement-based protection scheme based on the Limiting Inductor Voltage-Ratio-Derivative (LIVRD) is presented in this thesis. Therefore, the characteristic difference of voltage between the limiting inductor's sides during a fault condition can be easily observed by calculating the ratio between the voltage measurements taken at both sides of the limiting inductor.

Moreover, the ratio provides fault direction discrimination and acts as a directional element. Likewise, the derivative of this ratio is also calculated in order to obtain high speed fault detection. These two elements operate in parallel so as to enable a reliable operation of the protection system.

Therefore, the main characteristic of the proposed LIVRD protection scheme are:

- Local-measurement-based operation; the protection scheme can operate reliably without a communication system.
- Fast operation since local measurements and a derivative element are employed.
- Forward and backward fault discrimination thanks to the directional element.
- No need of supervision criteria such as an overcurrent element.

The proposed LIVRD protection scheme is presented in the next subsections. Fault discrimination is based on the calculation of the ratio between the local voltage measurements taken at both sides of the limiting inductor presented in subsection 3.1 and the derivative-based algorithm that allows fast fault detection is characterized in subsection 3.2. Finally, the complete protection system and the combined parallel operation of the two previously-mentioned elements are presented in subsection 3.3.

The work presented in this chapter has been published in:

M. J. Pérez-Molina, D. M. Larruskain, P. Eguia and O. Abarrategi, "Circuit Breaker Failure Protection Strategy for HVDC Grids", Energies, vol. 14, (14), 2021.

M. J. Perez-Molina, P. Eguia, D. M. Larruskain, E. Torres and J. C. Sarmiento-Vintimilla, "Single-ended limiting inductor voltage-ratio-derivative protection scheme for VSC-HVDC grids", International Journal of Electrical Power & Energy Systems (under review).

3.1. Voltage-ratio-based fault discrimination

The damping characteristic of the limiting inductors can be employed to discriminate between forward and backward faults. This way, fault discrimination can be implemented by only using local voltage measurements taken at both sides of the limiting inductor. Forward faults are assumed to be those located in the link where the relay and circuit breakers are placed while backward faults are those located at the bus-side of the limiting inductor, i.e., at the busbar or in a neighbouring link connected to the busbar.

The two voltage measurements, i.e., link-side voltage (V_{link}) and bus-side voltage (V_{bus}), are equal during normal operation, since the DC current is constant as it is shown in (3.2).

$$\text{Normal operation: } i_{DC} = \text{constant} \implies \frac{di}{dt} = \frac{(V_{bus} - V_{link})}{L} = 0 \iff V_{bus} = V_{link} \quad (3.2)$$

Meanwhile, a fault condition causes a difference of voltage and a change in the DC current, i.e., a positive rate-of-rise of the DC current during a forward fault and a reversal of the current polarity (the current flows out of the protection zone) and, thus, a negative rate-of-rise in the case of a backward fault.

Moreover, the difference of voltage is positive during a forward fault since V_{link} sharply collapses while the collapse of V_{bus} is attenuated, then, V_{link} presents a lower value than V_{bus} (3.3).

$$\text{Forward fault: } i_{DC} > 0 \implies \frac{di}{dt} = \frac{(V_{bus} - V_{link})}{L} > 0 \iff V_{bus} > V_{link} \quad (3.3)$$

On the contrary, a backward fault produces a negative difference of voltage since, this time, the collapse of V_{link} is attenuated while V_{bus} sharply collapses, so V_{link} presents a greater value than V_{bus} (3.4).

$$\text{Backward fault: } i_{DC} < 0 \implies \frac{di}{dt} = \frac{(V_{bus} - V_{link})}{L} < 0 \iff V_{bus} < V_{link} \tag{3.4}$$

Therefore, the difference of voltage between V_{link} and V_{bus} is a very good indicative of the existence of a fault condition in the system and its location, so the ratio between these two measurements can be employed in order to quickly discriminate between forward and backward faults. Calculation of the Voltage-Ratio (VR) is shown in (3.5).

$$\text{Voltage-ratio: } VR = \frac{V_{link}}{V_{bus}} \tag{3.5}$$

As it was previously demonstrated, V_{link} and V_{bus} are equal during normal operation, so the calculated VR will be equal to one (3.6).

$$\text{Normal operation: } V_{bus} = V_{link} \implies VR = 1 \tag{3.6}$$

However, a forward fault causes the VR to present a value lower than one since V_{link} is lower than V_{bus} (3.7) while the VR presents a value higher than one during backward faults (3.8), as it is depicted in Figure 3.2 (fault inception t = 1 ms).

$$\text{Forward fault: } V_{bus} > V_{link} \implies VR < 1 \tag{3.7}$$

$$\text{Backward fault: } V_{bus} < V_{link} \implies VR > 1 \tag{3.8}$$

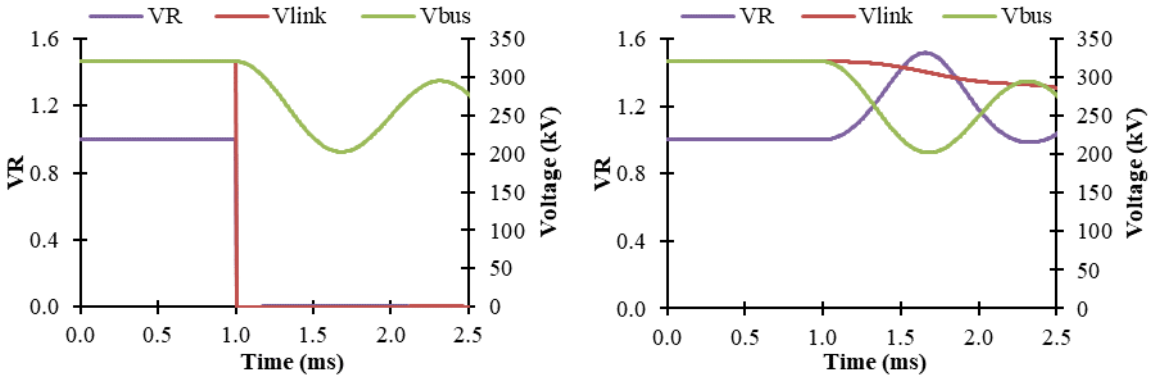


Figure 3.2.- VR, V_{link}, V_{bus} signals during a) a forward fault and b) a backward fault.

Therefore, the VR provides directionality to the protection scheme. A comparison of the calculated VR and threshold values can improve the selectivity of the protection scheme. This way, forward and backward faults can be detected by comparing the VR with threshold values THR_1 and THR_2, respectively. THR_1 should be a positive value and lower but close to one while THR_2 should be higher than one. These values will depend on the characteristics of the protected grid. Hence, a forward fault is detected when the VR drops under the value of THR_1 (3.9)

and a backward fault is detected when the VR overcomes THR_2 (3.10). The process of fault discrimination using the VR algorithm is depicted in Figure 3.3.

Forward fault location: $VR<THR_1$ (3.9)

Backward fault location: $VR>THR_2$ (3.10)

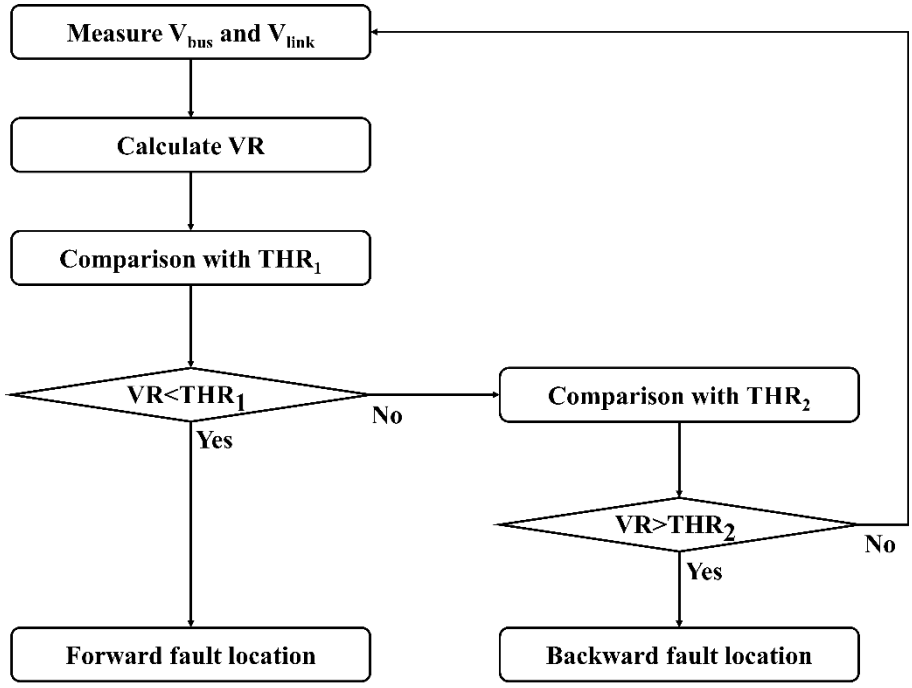


Figure 3.3.- Flow chart of the fault discrimination process using the VR algorithm.

3.2. Voltage-ratio-derivative-based fault detection

Local-measurement-based algorithms employing derivative calculations present the fastest fault detection capability. Hence, the derivative of the VR presented in subsection 3.1 is calculated in order to improve the operation speed of the protection system. The Voltage-Ratio-Derivative (VRD) is calculated following equation (3.11), where VR_{t_1} and VR_{t_2} are the VR values calculated at times t_1 and t_2; being t_2 higher than t_1.

$$VRD = \frac{dVR}{dt} = \frac{VR_{t_2} - VR_{t_1}}{t_2 - t_1} \tag{3.11}$$

The VR presents a constant value equal to one during normal operation as it is shown in (3.6), hence, the VRD presents a zero value (3.12).

Normal operation: $VR = 1 \implies VRD = 0$ (3.12)

When a forward fault occurs, the VR takes a value lower than one according to (3.7), thus, the calculated VRD is a negative value (3.13).

Forward fault: $VR < 1 \implies VRD < 0$ (3.13)

Conversely, the VR presents a value higher than one during a backward fault as stated in (3.8), forcing the VRD to take a positive value (3.14), as it is depicted in Figure 3.4 (fault inception t = 1 ms).

Backward fault: $VR > 1 \implies VRD > 0$ (3.14)

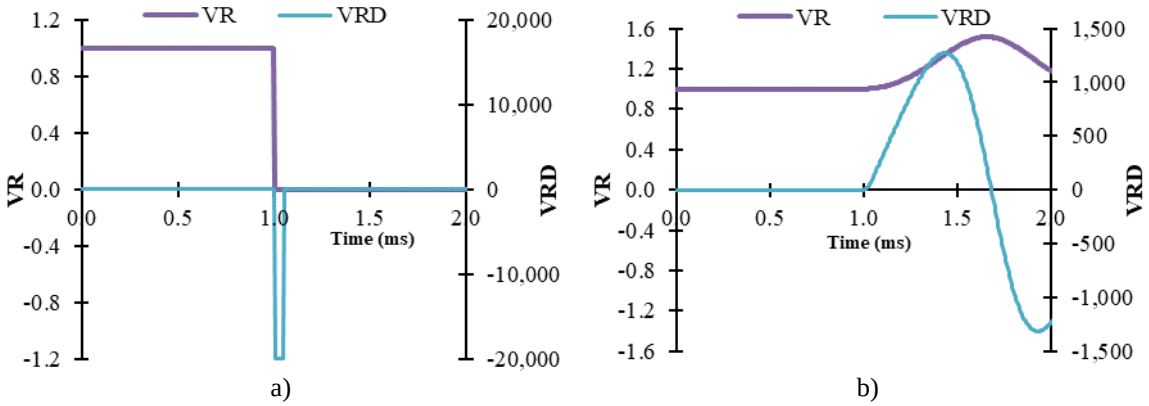


Figure 3.4.- VR and VRD signals during a) a forward fault and b) a backward fault.

As in the case of the VR-based fault discrimination process, improved performance is obtained if the VRD is compared with threshold values. This way, nuisance operation against temporary variations of the voltage signal is avoided. Fault conditions are detected by comparing VRD with two threshold values, i.e., THR_3 and THR_4, respectively. THR_3 is a negative value while THR_4 is a positive value, both values depend on the characteristics of the protected system. Then, if VRD drops under the value of THR_3 a forward fault is detected (3.15). Conversely, if VRD takes a value higher than THR_4 a backward fault detected (3.16). The process of fault detection with the VRD algorithm is depicted in Figure 3.5.

Forward fault detection: $VRD < THR_3$ (3.15)

Backward fault detection: $VRD > THR_4$ (3.16)

Moreover, the sampling frequency is an important parameter for the performance of this algorithm since it directly affects the VRD calculation (3.17). Higher sampling frequencies can benefit the fault detection and discrimination processes, since they enable the detection of the abrupt changes in the measured signal in a shorter time.

$$VRD = \frac{dVR}{dt} = \frac{\Delta VR}{\Delta t} = \left(VR_{t_2} - VR_{t_1}\right) \cdot f \tag{3.17}$$

This way, a higher sampling frequency produces a higher absolute value of the VRD during a fault condition due to the abrupt collapse of the DC voltage. Meanwhile, the VRD values during normal operation conditions are not significantly affected by the selected sampling frequency since the measured signals are constant. However, high sampling frequencies might cause a nuisance operation due to detecting disturbances in the measurements which are not related to a fault condition but to normal operation transients. Thus, it must be carefully selected. The effects of this parameter on the proposed algorithm are analysed in subsection 4.4.2.

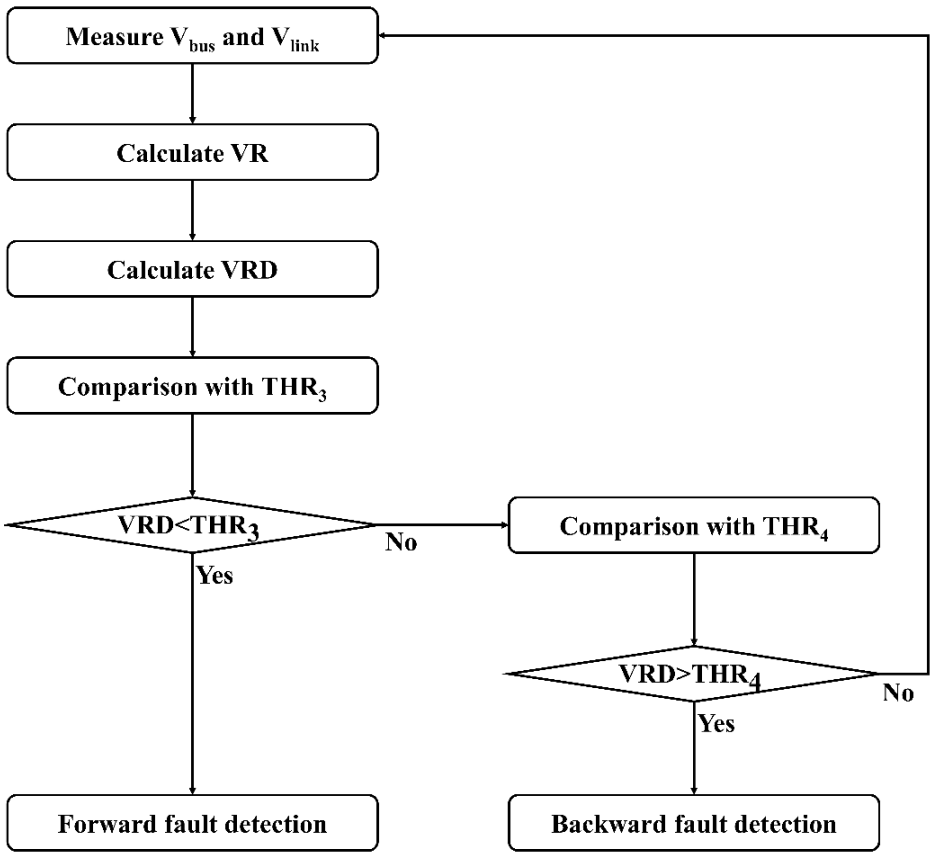


Figure 3.5.- Flow chart of the fault detection process using the VRD algorithm.

3.3. Proposed LIVRD protection scheme

The VR and VRD algorithms defined in the previous sections are included and combined in the LIVRD protection algorithm proposed in this thesis. Their parallel and simultaneous operation allows to combine their advantageous characteristics, i.e., directionality and high-speed operation, while improving the reliability and selectivity of the combined protection algorithm. The novel LIVRD algorithm is employed in the development of a complete protection scheme.

Likewise, the protected grid is divided into protection zones in order to ensure the selectivity of the LIVRD protection scheme. In consequence, each link and busbar are considered an independent protection zone. This way, link and busbar protections are based on the combined operation of VR and VRD algorithms, enabling internal and external fault discrimination in the corresponding protection zone. Fault detection and discrimination processes concurrently operate. The VRD algorithm presents very fast detection of faults in the system. Nevertheless, nuisance operation might occur due to fluctuations in the measured signals induced by normal operation conditions. Fluctuations could produce a peak in the VRD value, which might satisfy the criterion stated in (3.15), i.e., falsely detecting a forward fault. In order to avoid this misoperation, no trip signal will be sent to the corresponding circuit breaker unless the criterion stated in (3.9) is also fulfilled. Both criteria (3.9) and (3.15) must be simultaneously fulfilled to properly detect a forward fault. Likewise, criteria (3.10) and (3.16) must be simultaneously satisfied in the case of backward fault detection. Figure 3.6 shows the combined and concurrent process of fault detection and discrimination.

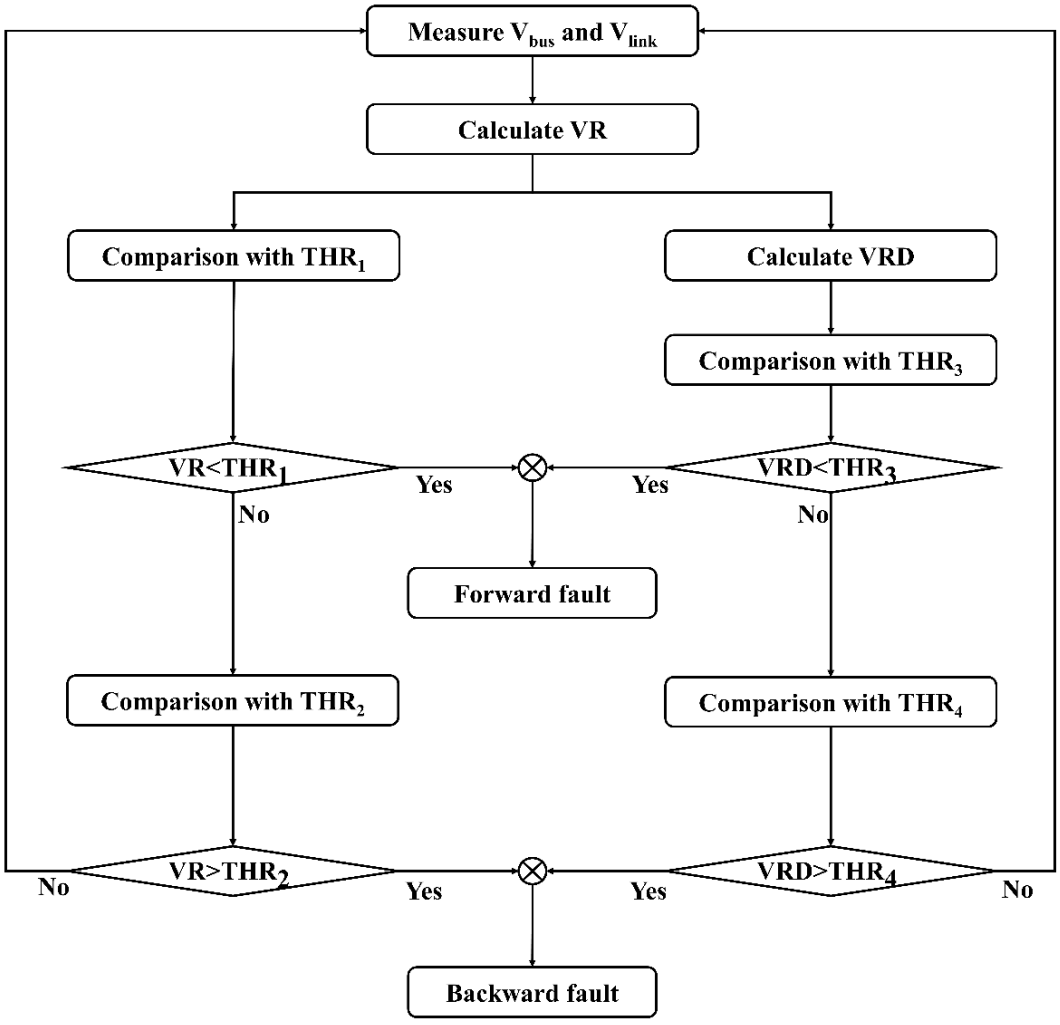


Figure 3.6.- Flow chart of the combined fault discrimination and detection process.

Moreover, this thesis also proposes a novel algorithm able to detect an improper operation of a DC-CB, i.e., a fault is detected and the trip signal is issued but the circuit breaker does not operate, causing a failure in the fault clearing process. The proposed circuit breaker failure protection is capable of detecting a failure of the corresponding circuit breaker and clearing the fault condition faster than conventional protections. Subsections 3.3.1, 3.3.2 and 3.3.3 define the link, busbar and circuit breaker failure protections, respectively.

3.3.1. Link protection

Link protection covers the protection of each link of the system as an independent element. Hence, limiting inductors are required at the ends of each link in order to properly delimit the protection zones since the link protection is based on a local-measurement-based inductor-voltage algorithm. This way, only the protected link is isolated when a fault occurs within it. Link protection detects faults located in the links which interconnect the different VSCs. It can be divided into link primary protection and link backup protection.

3.3.1.1 Link primary protection

Link primary protection is related to the detection of all faults occurring inside the corresponding protection zone, i.e., the link. Link primary fault detection is achieved by the relays located in the affected link.

Then, link primary protection covers the forward fault detection and discrimination segments presented in subsections 3.1 and 3.2. According to this, the link primary protection detects an internal fault when criteria (3.9) and (3.15) are satisfied. Both criteria must be fulfilled in a time interval Δt_P, i.e., when one of the criteria is satisfied, the remaining one must be fulfilled before the time interval Δt_P passes. Then, trip signals are issued to the corresponding circuit breakers and fault isolation and clearance is quickly achieved, only limited by the time needed by the circuit breakers to operate, which is commonly 2 ms for H-CBs. The link primary protection is summarized in Figure 3.7.

3.3.1.2 Link backup protection

Sometimes, the link primary protection fails to detect a fault condition due to a problem in its operation. Thus, the fault is not cleared by the circuit breakers since they have not received the required trip signal for its operation. Therefore, a link backup protection is needed in order to allow fault detection in case of failure in the primary relay.

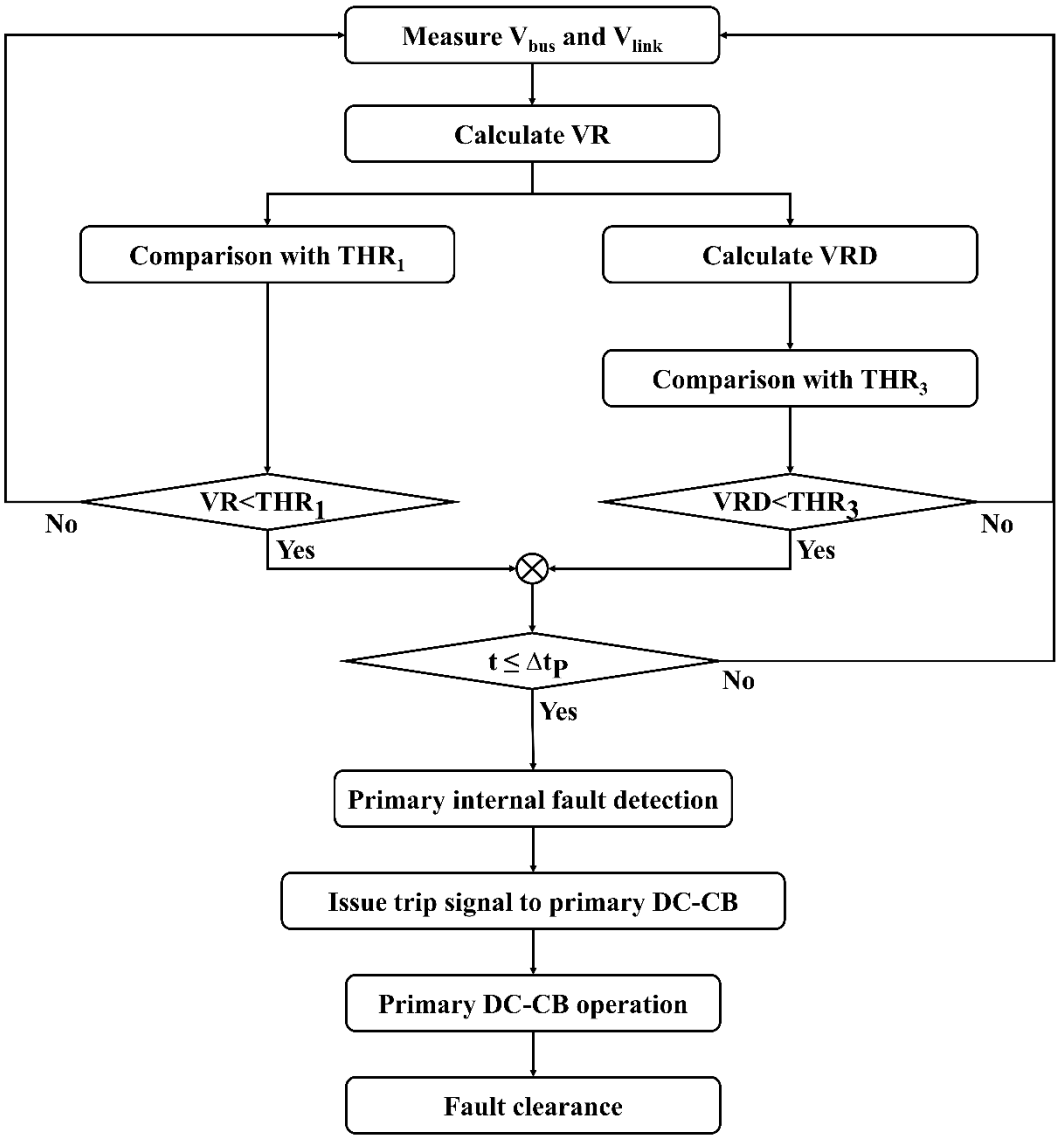


Figure 3.7.- Flow chart of the link primary protection.

The proposed link backup protection presents a similar operation to the link primary protection since it is also based on the VR and VRD algorithms. As these algorithms are able to detect backward faults, the link backup protection is based on the reverse reach of the neighbouring relays. Moreover, the proposed link backup protection is implemented at busbar level and it is based on the comparison of the VR and VRD measurements taken by all relays interconnected at the same busbar. Therefore, a busbar connected to "n" links requires "n-1" pairs of measurements for the operation of the link backup protection, i.e., equations (3.5) and (3.11) for each relay. The communication delay between relays can be considered negligible due to the proximity between all relays. Hence, failure of relay $R_{i,a}$ located in link "i,a", which is interconnected to Bus_i, is detected when all neighbouring relays simultaneously detect a backward fault by fulfilling criteria (3.10) and (3.16), as it is shown in (3.18), where $R_{i,j}$ is the relay located in link "i,j", being (j=1,..,n) and ($a \in j$).

$$\text{For } Bus_i,\ R_{i,a} \text{ failure detection} \Longrightarrow \forall R_{i,j} \wedge (j \neq a): \begin{cases} VR_{R_{i,j}} > THR_2 \\ \& \\ VRD_{R_{i,j}} > THR_4 \end{cases} \quad (3.18)$$

Then, a trip signal is issued to the circuit breaker located in the affected link and the fault clearing process is completed. Both criteria must be fulfilled in a time interval Δt_{BU}, i.e., when one of the criteria is satisfied, the remaining one must be fulfilled before the time interval Δt_{BU} passes. The link backup protection presents very fast fault detection since it is only slightly slower than the link primary protection as it is demonstrated in Chapter 4. The operation of the link backup protection is represented in Figure 3.8.

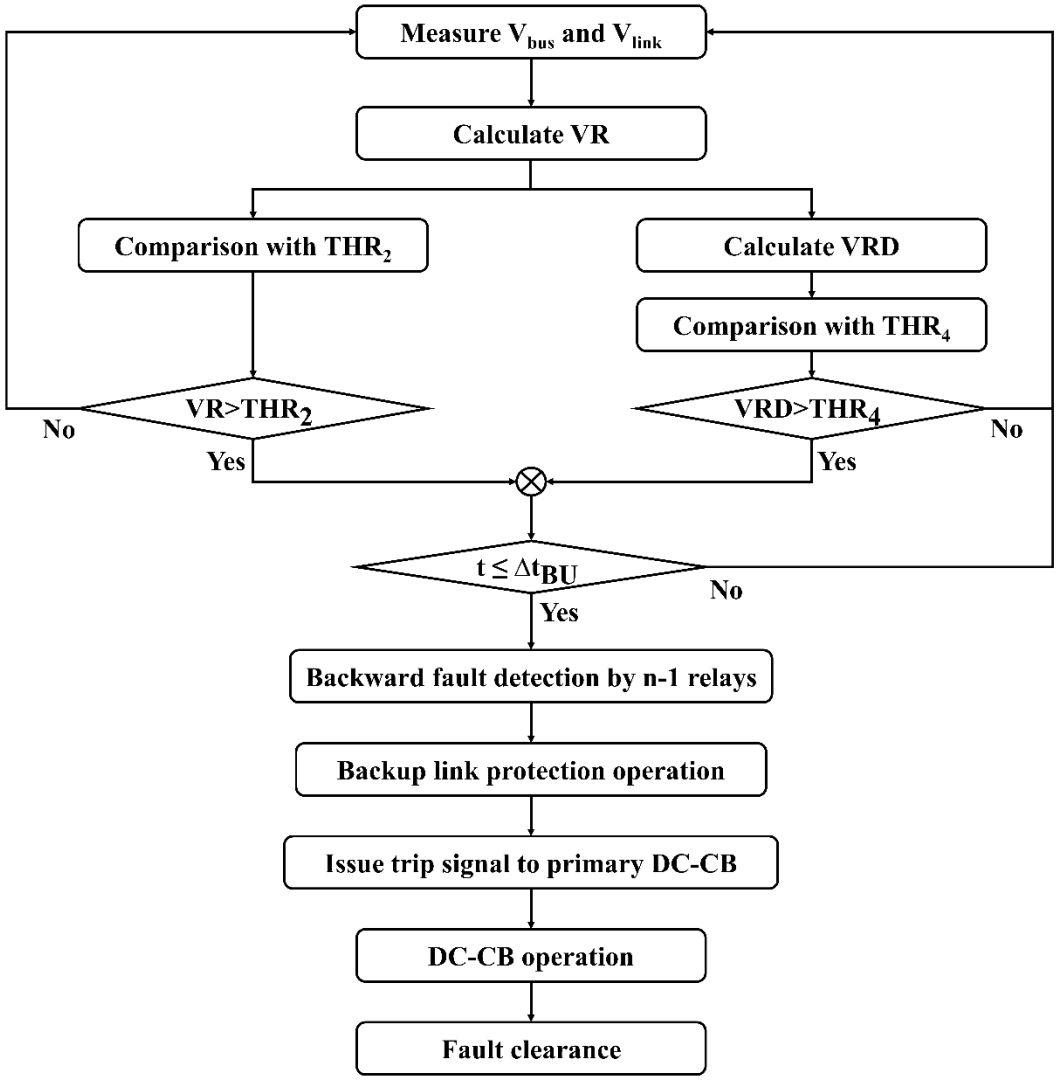


Figure 3.8.- Flow chart of the link backup protection.

3.3.2. Busbar protection

A busbar interconnects several transmission links with a converter. Busbars must be protected against internal faults. When an internal busbar fault occurs, all circuit breakers connected with the busbar must operate in order to isolate the fault.

In case of fault at a busbar, all relays connected to it detect a backward fault. Therefore, busbar fault detection is achieved when all relays connected to the busbar simultaneously detect a backward fault (criteria (3.10) and (3.16)) and trip signals are sent to all corresponding circuit breakers. Both criteria must be fulfilled in a time interval Δt_{BB}, i.e., when one of the criteria is satisfied, the remaining one must be fulfilled before the time interval Δt_{BB} passes.

The criterion of busbar fault detection is shown in (3.19) for Bus_i. There are "n" links connected to Bus_i. Therefore, when all the relays interconnected to Bus_i satisfy criteria (3.10) and (3.16), an internal fault is detected by the busbar protection. $VR_{R_{ij}}$ and $VRD_{R_{ij}}$ are the values of the VR and VRD calculated by relay $R_{i,j}$ located in link "i,j", being (j=1,..,n). Fast busbar fault detection is obtained since the actual distance between the busbar fault and the relays can be considered negligible.

$$\text{Busbar fault detection: For } Bus_i \implies \forall R_{i,j}: \begin{cases} VR_{R_{i,j}} > THR_2 \\ \& \\ VRD_{R_{i,j}} > THR_4 \end{cases} \tag{3.19}$$

3.3.3. Circuit breaker failure protection

Malfunction of a circuit breaker happens when it does not properly operate and it is not able to clear the fault after receiving the corresponding trip signal. A failure of the corresponding circuit breaker causes an improper clearing of the fault condition, which is still fed through one end of the affected link. The reliability of the MTDC grid must be ensured, thus, a Circuit Breaker Failure (CBF) protection must be applied in order to detect the improper operation of the circuit breaker located in the affected link.

Conventional circuit breaker failure protections detect the failure of the link primary protection after the link primary protection's estimated fault clearing time has passed. However, the restrictive speed requirement related to VSC-based grids entails the implementation of a fast circuit breaker failure protection, which is capable of detecting and interrupting the fault current before it overcomes the current constraints of the circuit breakers and the VSCs [225].

Thus, the objective of the circuit breaker failure protection is to detect the failure in the operation of a DC-CB of an adjacent link. The circuit breaker failure protection operates when a fault occurs in an adjacent link but the corresponding link primary protection does not operate correctly due to a failure of its DC-CB. Therefore, all neighbouring relays (interconnected to the same bus of the malfunctioning DC-CB) must be able to detect a fault condition occurring in their backward direction and the malfunction of the circuit breaker located in the affected link, so their corresponding circuit breakers operate in order to properly complete the fault clearance process.

In this regard, this thesis presents a circuit breaker failure protection based on local voltage measurements which is capable of quickly detecting the DC-CB's failure before the estimated fault clearing time has passed. This way, the system has to interrupt a lower fault current than when a conventional circuit breaker failure protection waits until the estimated fault clearing time passes. This method has been implemented due to the restrictive speed requirement related to VSC-based systems, i.e., the fast rate-of-rise of the fault current and the low overcurrent withstand capability of the VSC's components.

The LIVRD circuit breaker failure protection, similarly to the link backup protection previously explained in subsection 3.3.1.2, is implemented at busbar level and it is based on the comparison of the VR and VRD measurements taken by all relays interconnected to the same busbar, i.e., equations (3.5) and (3.11) for each relay. Then, the LIVRD circuit breaker failure protection initiates its process when all neighbouring relays satisfy criteria (3.10) and (3.16).

Additionally, the circuit breaker operation is verified by checking the bus-side voltage-derivative ($ROCOV_{bus}$) value. Calculation of the voltage-derivative using measurements taken at the bus-side of the limiting inductor, i.e., V_{bus}, are shown in (3.20), where V_{bus_1} and V_{bus_2} are the DC voltage magnitudes measured at the bus-side of the limiting inductor at time t_1 and t_2; being time t_2 higher than time t_1.

$$ROCOV_{bus} = \frac{dV_{bus}}{dt} = \frac{\Delta V_{bus}}{\Delta t} = \frac{V_{bus_2} - V_{bus_1}}{t_2 - t_1} \tag{3.20}$$

The $ROCOV_{bus}$ value can indicate if the primary circuit breaker has operated and the fault clearance process has started since the correct operation of the link primary protection will induce the recovery of the voltage of the faulty link, i.e., an abrupt voltage increase and, thus, a high positive voltage-derivative value.

Figure 3.9 shows time steps of the LIVRD link primary protection and the circuit breaker failure protection. After fault inception (t_f), fault detection by the link primary protection is achieved at time t_{Pd} and a trip signal is sent to the corresponding circuit breaker, operating at time t_{Po} and completing fault clearance at time t_{Pc}.

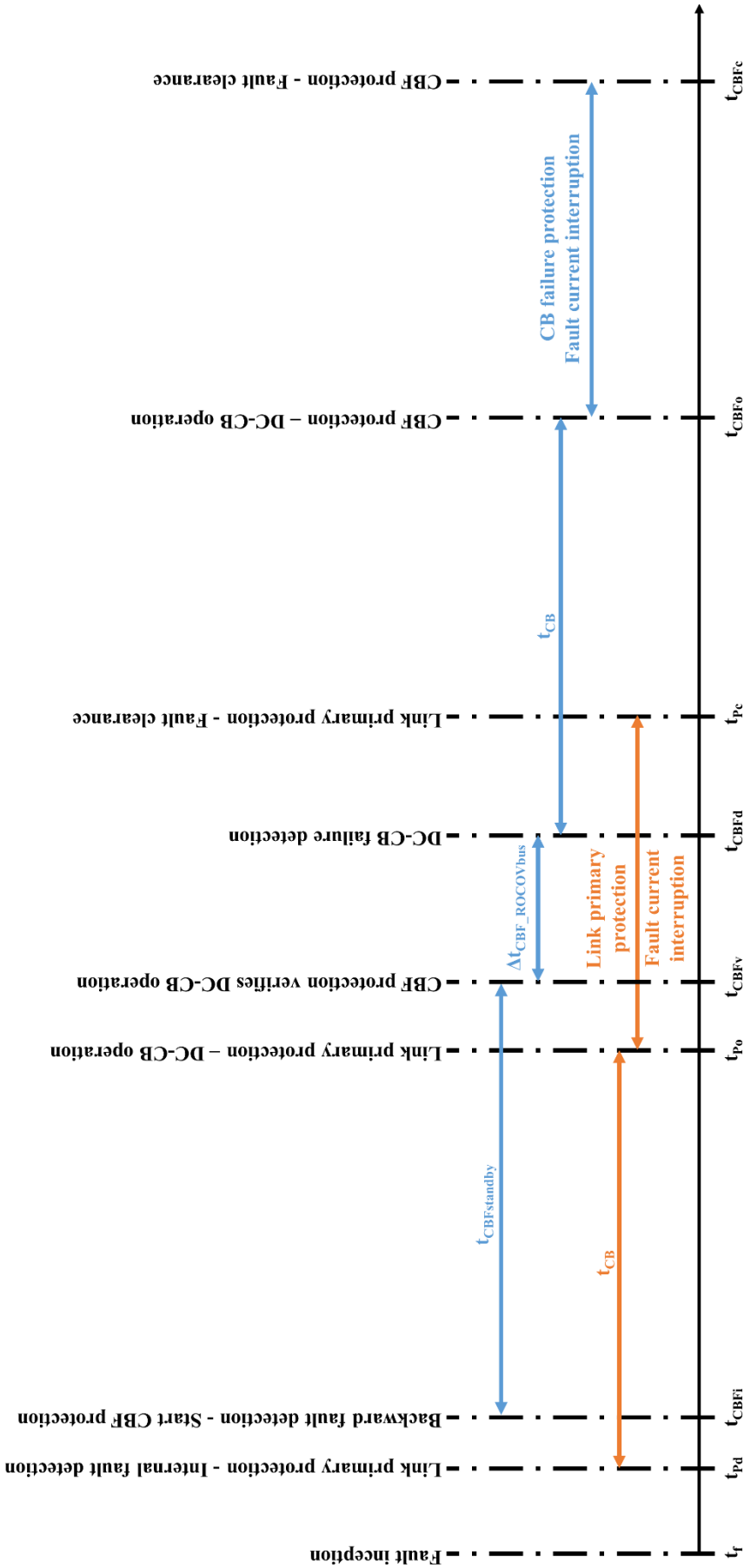


Figure 3.9.- Time steps of the proposed protection scheme, including link primary protection and circuit breaker failure protection.

Likewise, the circuit breaker failure protection is initiated at time t_{CBFi} when all neighbouring relays simultaneously satisfy criteria (3.10) and (3.16) in a time interval Δt_{CBF}, i.e., when one of the criteria is satisfied, the remaining one must be fulfilled before the time interval Δt_{CBF} passes.

Afterwards, the circuit breaker operation is verified at t_{CBFv} by checking the $ROCOV_{bus}$ value calculated by all neighbouring relays after a standby time, $t_{CBFstandby}$, slightly greater than the operating time, t_{CB}, of a circuit breaker, e.g., the operating time of a H-CB is in the range of 2 ms. Therefore, if the $ROCOV_{bus}$ value overcomes a positive threshold value (THR_5) in a time interval, $\Delta t_{CBF\_ROCOV_{bus}}$, after the standby time, $t_{CBFstandby}$, the DC-CB has properly operated (3.21), otherwise, a failure of the DC-CB is detected (3.22) at t_{CBFd}. Trip signals are issued to the neighbouring circuit breakers which operate at t_{CBFo} and complete the fault clearance process at t_{CBFc}. Figure 3.10 summarizes the operation of the proposed circuit breaker failure protection.

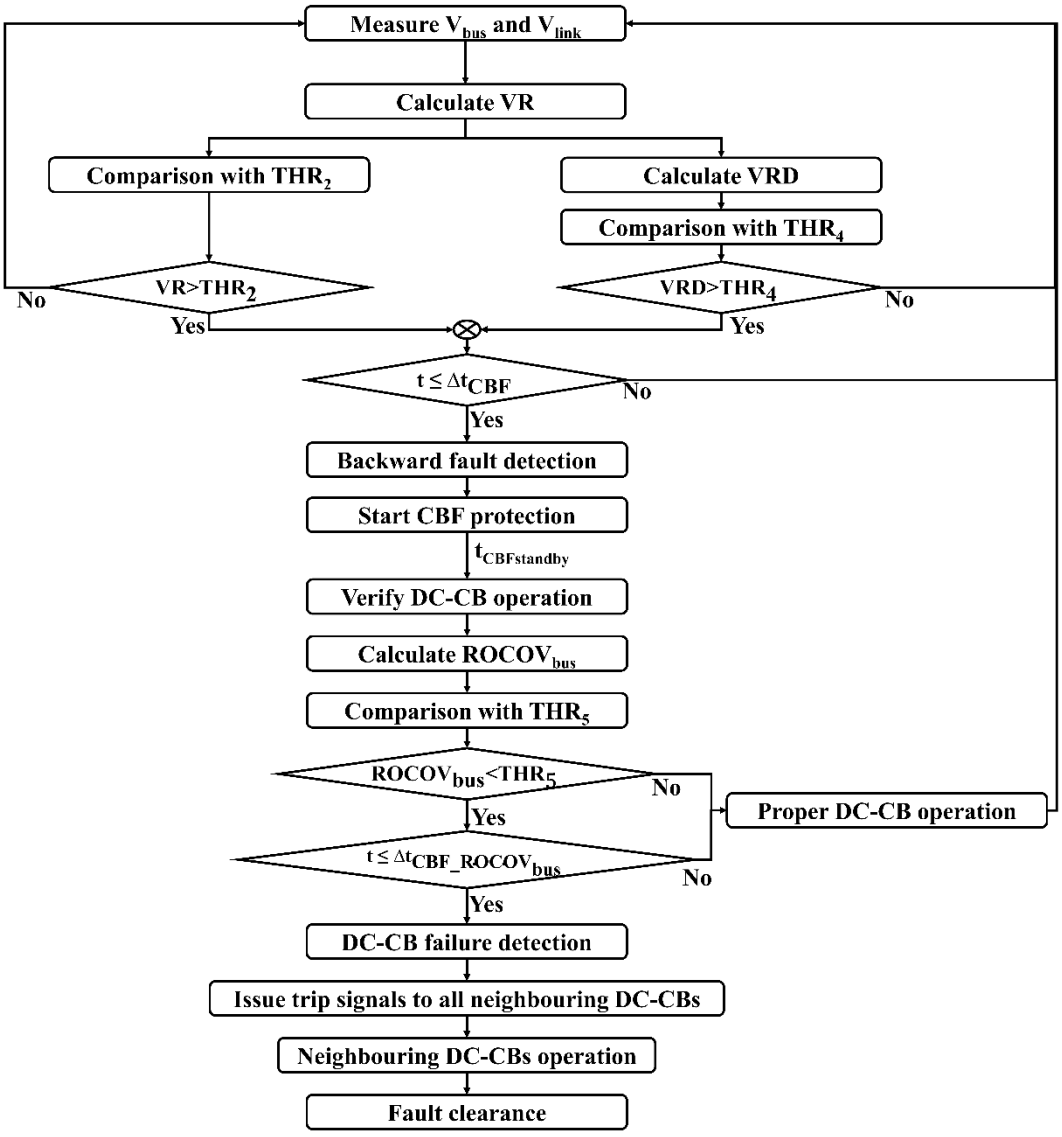


Figure 3.10.- Flow chart of the proposed circuit breaker failure protection.

Detection of correct primary operation: $ROCOV_{bus}>THR_5$ (3.21)

Detection of primary operation failure: $ROCOV_{bus}<THR_5$ (3.22)

Obviously, the operation of the circuit breaker failure protection will produce a bigger effect on the system since all neighbouring circuit breakers must operate in order to properly isolate and clear the fault due to the improper operation of the corresponding circuit breaker.

3.4. Conclusion

Local-measurement-based protection systems have been widely studied in recent years for their application in HVDC grids due to their advantageous operation speed. According to this tendency, this thesis proposes a novel LIVRD fault protection algorithm consisting in calculating the voltage-ratio between the voltage measurements taken at both sides of the limiting inductor and its derivative.

The LIVRD protection algorithm presents a directionality capability provided by the voltage-ratio and a fast operation speed due to the calculation of the voltage-ratio-derivative. This way, the voltage-ratio-derivate is in charge of fault detection while the voltage-ratio discriminates between forward and backward faults, thus, confirming internal or external fault detection in the corresponding protection zone. Taking into account these features, a complete protection scheme is developed in this thesis. This protection scheme covers link primary and backup protections, busbar protection and circuit breaker failure protection.

Link primary protection employs only local derivative-based measurements and it is based on detecting forward faults. It operates against all faults located in the link and presents high operation speed and selectivity. Meanwhile, link backup protection operates when the link primary protection is incapable of detecting the fault and of issuing the corresponding trip signals due to a failure of the relay. The link backup protection uses the reverse reach of the neighbouring relays to detect a backward fault and issues the trip signal to the circuit breaker placed in the affected link, so the fault is properly cleared. It presents high operation speed since it is just slightly slower than the link primary protection. Therefore, both the link primary and link backup protections are based on local voltage measurements and in the calculation of VR and VRD. This local-measurement-based inductor-voltage method has been implemented for both primary and link backup protections due to the restrictive speed requirement related to VSC-based systems, i.e., the fast rate-of-rise of the fault current and the low overcurrent withstand capability of the VSC's components. This way, fast and selective link primary and link backup protections are achieved.

On the other hand, a busbar protection, which is also based on the VR and VRD algorithms, is presented. In this case, an internal busbar fault is detected when all the relays interconnected to the same busbar detect a backward fault. Fast and selective busbar fault detection is achieved due to the use of VR and VRD measurements.

Additionally, a novel circuit breaker failure protection, which detects the improper operation of a circuit breaker, is also implemented. Similarly, the circuit breaker failure protection is based on the VR and VRD algorithms while also employing the $ROCOV_{bus}$ calculation so as to verify the operation of the corresponding circuit breaker. After circuit breaker failure detection, all neighbouring circuit breakers connected to the same bus of the malfunctioning circuit breaker operate. The proposed LIVRD circuit breaker failure protection operates faster than similar conventional protections since it is capable of quickly detecting the circuit breaker failure before the estimated fault clearing time has passed. This allows the operation of the circuit breaker failure protection to fit in the restrictive speed constrains associated to VSC-based grids.

In conclusion, this thesis proposes a local-measurement-based protection scheme that covers link, busbar and circuit breaker failure protections. The LIVRD protection scheme presents high detection speed since only local measurements are employed and no communication channel is needed. Moreover, limiting inductors and threshold values allow a high selective and sensitive operation.

Chapter 4.

ANALYSIS OF THE NOVEL LIVRD PROTECTION SCHEME

The objective of this chapter is to analyse and evaluate the novel LIVRD fault protection algorithms developed in Chapter 3. The LIVRD algorithms are thoroughly examined through Electromagnetic Transient (EMT) simulations. The EMT simulation software employed is PSCAD software.

The performance of the novel LIVRD protection scheme is validated by simulating different fault cases varying their parameters: fault location, fault type and fault resistance. Effects of other relevant parameters on its performance such as inductor size, sampling frequency and noise disturbance are also analysed. This way, a thorough analysis of the proposed protection algorithms is performed and the fast and reliable operation of the protection scheme is demonstrated.

The LIVRD protection scheme developed in this thesis is validated in the multi-terminal grid model presented in subsection 4.1 and thoroughly described in Appendix-A. Hence, the proposed link, busbar and circuit breaker failure protections are implemented and evaluated in this chapter. The threshold values required for the proper operation of the different protection segments are firstly selected in subsection 4.2 where a selection methodology is proposed and explained. Then, subsection 4.3 analyses the operation of the LIVRD protection scheme against different fault cases. Finally, the influence of relevant parameters (inductor size, sampling frequency, fault location and noise disturbance) on the proposed protection scheme are analysed in subsection 4.4.

The work presented in this chapter has been published in:

M. J. Pérez-Molina, P. Eguia, D. M. Larruskain, G. Buigues and E. Torres, "Non-unit ROCOV scheme for protection of multi-terminal HVDC systems", in 22nd European Conference on Power Electronics and Applications (EPE ECCE Europe 2020), Lyon, France, 7-11 September 2020.

M. J. Pérez-Molina, D. M. Larruskain, P. Eguia and O. Abarrategi, "Circuit Breaker Failure Protection Strategy for HVDC Grids", Energies, vol. 14, (14), 2021.

M. J. Pérez-Molina, D. M. Larruskain, P. Eguia and V. Valverde, "Local derivative-based fault detection for HVDC grids", IEEE Transactions on Industry Applications, vol. 58, (2), pp. 1521-1530, 2022.

M. J. Perez-Molina, P. Eguia, D. M. Larruskain, E. Torres and J. C. Sarmiento-Vintimilla, "Single-ended limiting inductor voltage-ratio-derivative protection scheme for VSC-HVDC grids", International Journal of Electrical Power & Energy Systems (under review).

4.1. Four-terminal MMC-based grid model

The LIVRD protection scheme is validated through simulation in PSCAD in a four-terminal MMC-based meshed grid (Appendix-A) presented in [187] and available in [226]. Four HB-MMCs interconnect two offshore wind power plants to two onshore AC systems through five undersea cables. Links are 100, 150 and 200 km long, as it is shown in Figure 4.1. Cables are modelled using frequency dependent models.

HB-MMCs are not capable of controlling the DC fault current, i.e., they are not fault-blocking converters. When a DC fault occurs, the converter's submodules are blocked due to the operation of its internal overcurrent protection. Then, they behave as uncontrolled-rectifiers which allow the AC system to feed the fault through the submodules' anti-parallel diodes.

Thus, a protection system is needed to rapidly detect and clear DC faults. The proposed protection scheme is implemented so as to fulfil the restrictive requirement of speed related to VSC-based systems. The proposed protection scheme is based on local-measurement-based algorithms, thus, 100 mH limiting inductors are placed in both ends of each link of the system. This way, the system is divided in independent protection zones. These protection zones cover the most relevant elements of the system, i.e., cables and busbars. Figure 4.2 shows how each cable is addressed as an independent protection zone with a 100 mH limiting inductor in series with a DC-CB in each end.

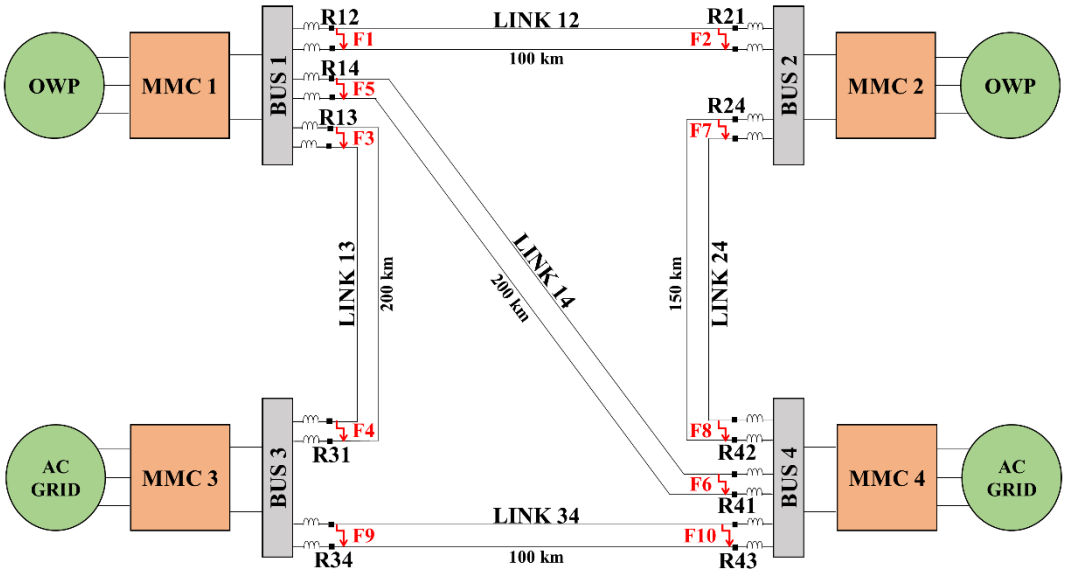


Figure 4.1.- Scheme of the four-terminal grid modelled in PSCAD with fault locations.

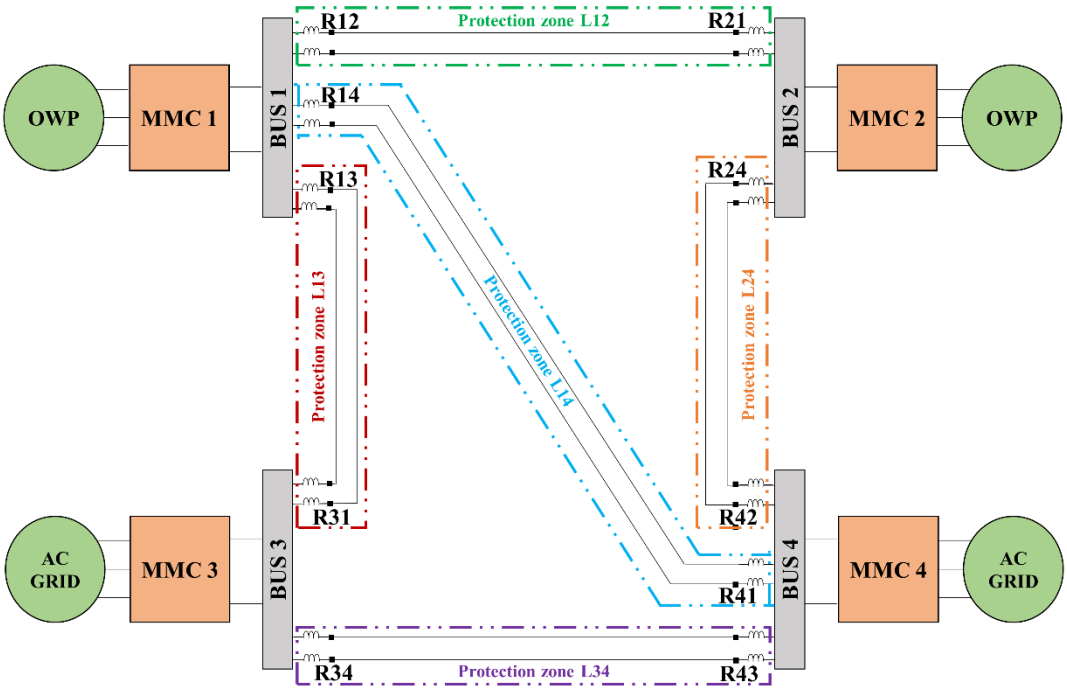


Figure 4.2.- Protection zones for link protection.

Similarly, Figure 4.3 depicts each busbar as an independent protection zone, protected by all relays and DC-CBs located in the cables connected to the busbar. Therefore, a full-selective fault-clearing strategy has been adopted, so only the faulty protection zone is isolated, while the remaining zones of the system continue operating and the effects of the fault are minimized. Moreover, an operating time of 2 ms is assumed for the DC-CBs simulating the operation of a H-CB.

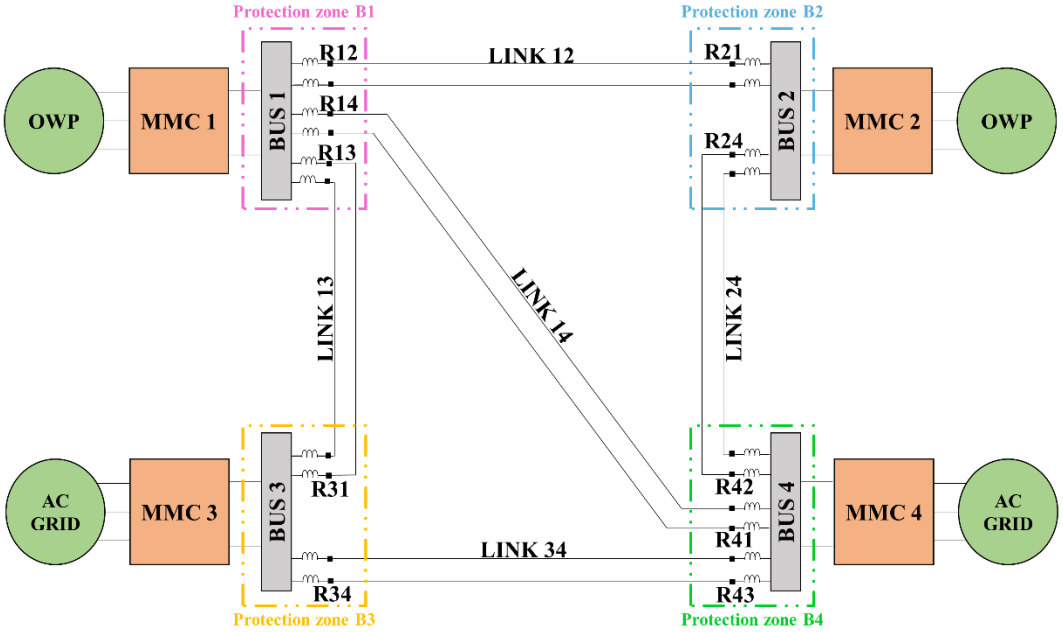


Figure 4.3.- Protection zones for busbar protection.

The novel LIVRD algorithms developed in this thesis are validated in this multi-terminal grid model. Figure 4.1 shows the locations of the fault cases which are simulated in the analysis and evaluation of the performance of the proposed protection scheme. The performance of the link, busbar and circuit breaker failure protections are implemented and evaluated in the following subsections.

4.2. Threshold selection methodology

The threshold value is very relevant for the performance of local-measurement-based protection since it directly affects the selectivity and sensitivity of the protection algorithm. A higher threshold value improves the selectivity and ensures the detection of internal faults but worsens the sensitivity, making some high-resistive faults difficult to detect. Conversely, a lower threshold value improves the sensitivity, improving the capability of detecting fault conditions with higher resistance but it lowers the selectivity, increasing the probability of improperly detecting external faults located near to the local end as internal faults, and causing a nuisance operation of the protection system.

Thus, the selection of threshold values is an essential process for the proper operation of a local-measurement-based algorithm and it is usually carried out through simulations. Therefore, this chapter proposes and validates a methodology to determine the threshold values. The proposed threshold selection methodology takes into account the worst case scenarios for each protection as well as transients induced by the opening of a DC-CB.

Moreover, high-resistance faults must be taken into account in the threshold selection process since a threshold value which has been selected considering only solid faults might not be able to detect high-resistance faults.

Firstly, threshold values THR_1 and THR_3, regarding the link primary protection, are selected in subsection 4.2.1. Then, selection of threshold values THR_2 and THR_4 is achieved in subsection 4.2.2. These threshold values are employed in the operation of the link backup protection, the busbar protection and the initiation of the circuit breaker failure protection. Afterwards, threshold value THR_5 related to the verification process of the circuit breaker failure protection is determined in subsection 4.2.3.

4.2.1. Selection of threshold values THR_1 and THR_3

In the case of the link primary protection, the worst fault cases are internal faults located at the remote end of the protection zone and external faults located near the local end. Internal faults located at the remote end of the protection zone are difficult to detect due to the attenuation of the traveling wave signals. External faults located near the local end can produce a sufficiently high traveling wave to cause the false detection of an internal fault and the consequent nuisance operation.

Threshold values THR_1 and THR_3, regarding the link primary protection, have been selected by simulating the fault conditions depicted in Figure 4.1, which represent the worst fault cases for each relay, e.g., F2 is the worst internal fault case scenario for relay R12 and the worst external fault case scenario for relay R24.

Likewise, these worst fault cases have been analysed for both solid and 200 Ω faults and both PtP and PtG faults, even though PtP faults in cables are not common. This way, the selected threshold values ensure the accurate detection of fault conditions up to 200 Ω, guarantying a suitable performance of the proposed LIVRD protection scheme, since fault conditions with resistances higher than 200 Ω are rare [72], [176]. Moreover, 100 mH limiting inductors and a sampling frequency of 20 kHz are used in this threshold selection process.

During a fault condition, both VR and VRD values have to be lower than the link primary protection's threshold values to allow fault detection. As it was mentioned in subsections 3.1 and 3.2, THR_1 must be a value lower than one (3.9) and THR_3, a negative value (3.15). Additionally, the following conditions must be fulfilled:

- A critical value for the worst internal fault case ($VR_{int_{CV}}$ and $VRD_{int_{CV}}$) is the maximum of the calculated signal.

- The threshold value should be greater than the critical internal fault value to ensure internal fault detection.
- A critical value for the worst external fault case ($VR_{ext_{CV}}$ and $VRD_{ext_{CV}}$) is the minimum of the calculated signal.
- The threshold value should be lower than the critical external fault value to avoid nuisance operation.

Thus, the appropriate operation of the link primary protection is ensured if the selected threshold value is a value between the mentioned critical values, as it is shown in as it is depicted in Figure 4.4 and (4.1) for THR_1 and Figure 4.5 and (4.2) for THR_3.

$$VR_{int_{CV}} < THR_1 < VR_{ext_{CV}} \quad (4.1)$$

$$VRD_{int_{CV}} < THR_3 < VRD_{ext_{CV}} \quad (4.2)$$

The selection process of these threshold values regarding link primary protection is summarized in the flow chart depicted in Figure 4.6.

However, these critical values do not consider the transients derived from the DC-CB opening and also from busbar faults, which should not be detected by the link primary protection. Therefore, link primary protection's threshold values of 0.95 and -1000 for THR_1 and THR_3, which were initially selected, are employed in the next series of simulations taking into account the transients induced by the opening of a DC-CB and by busbar faults.

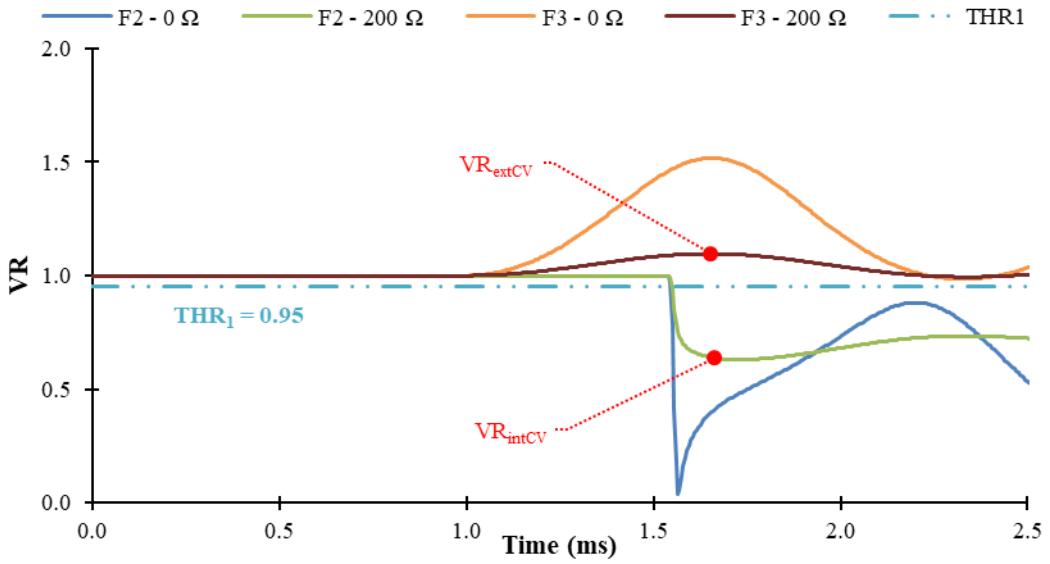


Figure 4.4.- Selection of threshold value THR_1 according to the worst fault case scenarios for relay R12.

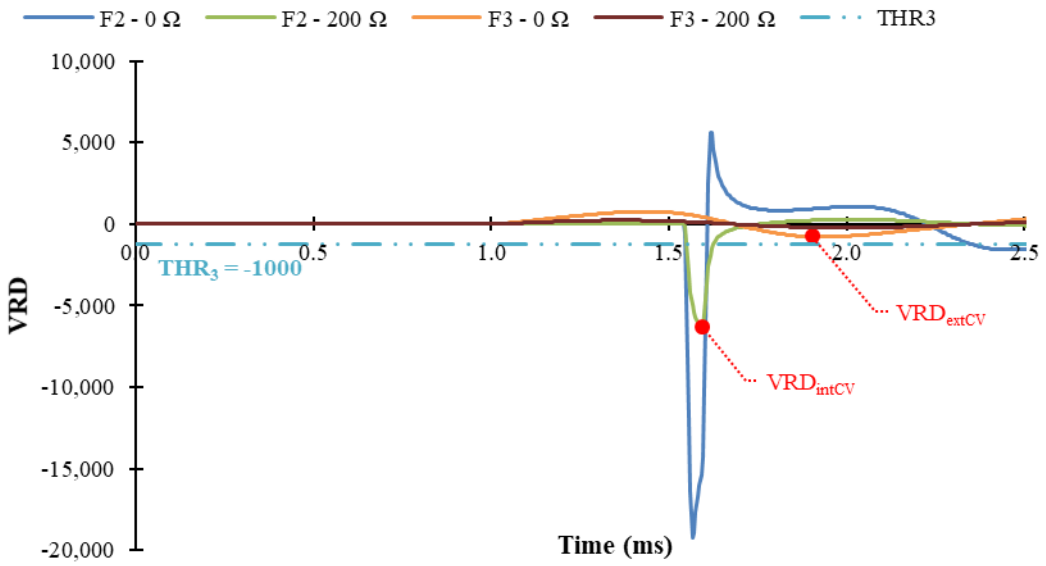


Figure 4.5.- Selection of threshold value THR_3 according to the worst fault case scenarios for relay R12.

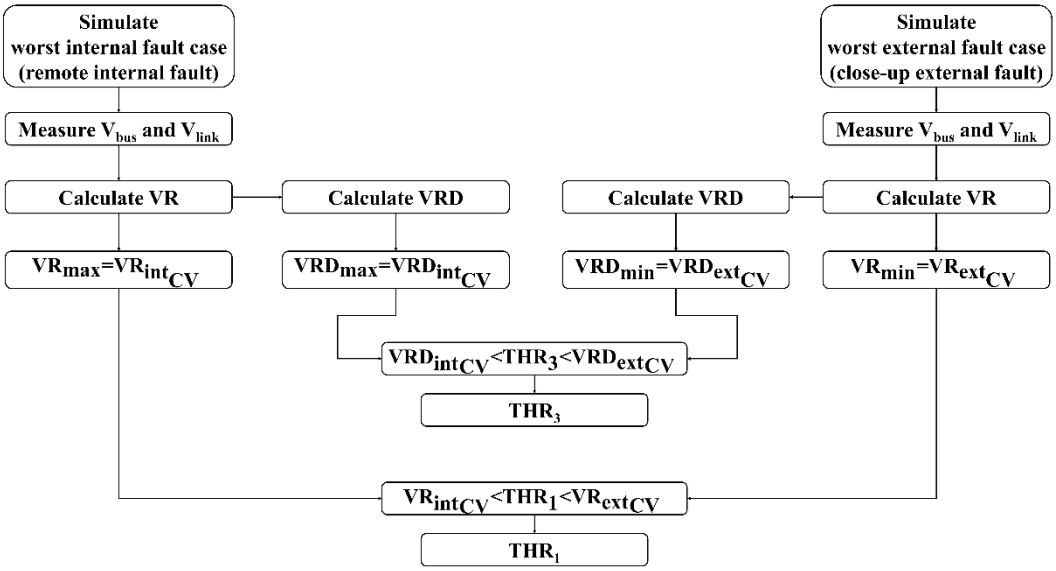


Figure 4.6.- Flow chart of the selection of threshold values THR_1 and THR_3.

This second series of simulations also follow the flow chart depicted in Figure 4.6 but also taking into account busbar-fault-induced transients. According to the results of this second series of simulations, some initial threshold values needed to be updated since they did not ensure the proper performance of the protection system for all relays due the transients induced by the opening of a DC-CB as it can be seen in Figure 4.7. Transients induced by busbar faults did not affect the selected threshold values since they present very high positive values (Figure 4.8). This way, the updated threshold values THR_1 and THR_3 for each relay that ensure a selective and accurate operation are summarized in Table 4.1.

Moreover, the LIVRD algorithm achieves fault detection when the VR- and VRD-based criteria are simultaneously satisfied. Thus, a time interval Δt_P needs to be selected in order to verify this criterion. A 100 µs time interval Δt_P is selected. This way, fault detection is achieved when both criteria are fulfilled in a time interval of two consecutive samples for a 20 kHz sampling frequency.

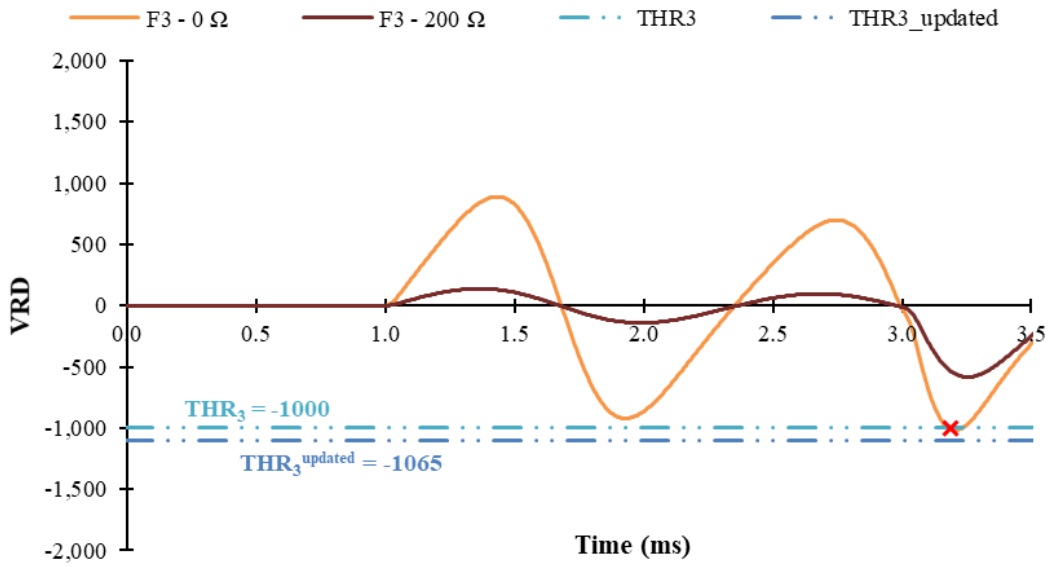


Figure 4.7.- Selection of the updated threshold value THR_3 for relay R12.

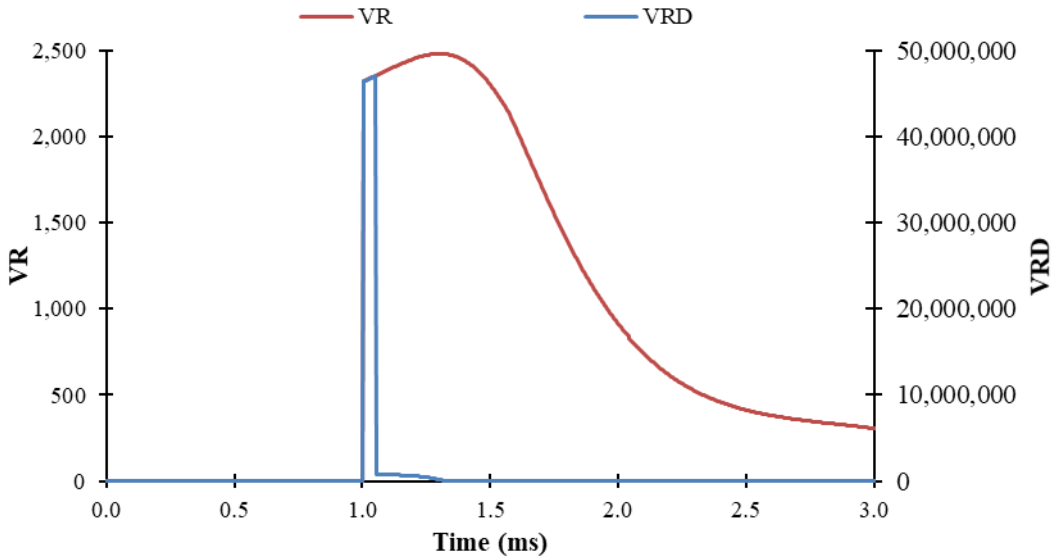


Figure 4.8.- Influence of the busbar-fault-induced transients in the threshold value selection.

4.2.2. Selection of threshold values THR_2 and THR_4

The previously-explained threshold value selection process is also similarly carried out in order to select the threshold values THR_2 and THR_4 related to link backup protection, busbar protection and circuit breaker failure protection algorithms of the proposed protection scheme. However, the critical values for THR_2 and THR_4 are different from the case of the link primary protection.

Since the link backup protection aims to detect backward faults in the neighbouring links, the worst fault cases are a backward fault located in the remote end of the protected neighbouring link and a close-up forward fault located in the link where the relay is placed, which could produce a high enough transient triggering false backup detection.

This critical remote backward fault is an external fault for the relay's primary protection zone, so it is the worst external fault case while the close-up forward fault is an internal fault to its primary protection zone, so it is the worst internal fault case. In Figure 4.2, the link backup protection of link 12 is handled by relays R13 and R14 in one terminal and relay R24 in the other one.

Thus, fault F2 is the worst external fault case for relays R13 and R14 while faults F3 and F5 are their corresponding worst internal fault cases. Fault F2 must be detected by the link backup protection of relays R13 and R14 while faults F3 and F5 must not be detected by this protection. Similarly, fault F1 is the worst external fault case for relay R24 while fault F7 is its worst internal fault case. Fault F1 must be detected by the link backup protection of relay R24 while fault F7 must not be detected.

This way, both the VR and VRD values need to be greater than the threshold value to allow backup fault detection. As it was mentioned in subsections 3.1 and 3.2, THR_2 must be a value greater than 1 (3.10) and THR_4, a positive value (3.16). According to this:

- A critical value for a remote external fault case ($VR_{ext_{CV}}$ and $VRD_{ext_{CV}}$) is the minimum of the calculated signal.
- The threshold value should be lower than the critical external fault value to ensure backup fault detection.
- A critical value for a close-up internal fault case ($VR_{int_{CV}}$ and $VRD_{int_{CV}}$) is the maximum of the calculated signal.
- The threshold value should be greater than the critical internal fault value to avoid a nuisance initiation of the backup process.

Thus, the appropriate operation of the link backup protection is ensured if the selected threshold value is a value between the mentioned critical values, as it is shown in Figure 4.9 and (4.3) for THR_2 and in Figure 4.10 and (4.4) for THR_4.

$$VR_{int_{CV}} < THR_2 < VR_{ext_{CV}} \tag{4.3}$$

$$VRD_{int_{CV}} < THR_4 < VRD_{ext_{CV}} \tag{4.4}$$

The threshold values THR_2 and THR_4 selected for the link backup protection are also appropriate for the busbar protection since busbar faults are close-up backward faults. Similarly, these threshold values are also appropriate for the circuit breaker failure protection since this algorithm is initiated when a backward link fault is detected.

Moreover, the VR- and VRD-based fault detection criteria must be fulfilled simultaneously in order to achieve fault detection by the LIVRD algorithm. Thus, a time interval is selected in order to accomplish it. The time intervals Δt_{BU}, Δt_{BB} and Δt_{CBF} employed by the link backup protection, the busbar protection and the initiation of the circuit breaker failure protection are 100 μs, i.e., two samples for a 20 kHz sampling frequency. This way, fault detection is achieved when both criteria are fulfilled in a time interval of two consecutive samples.

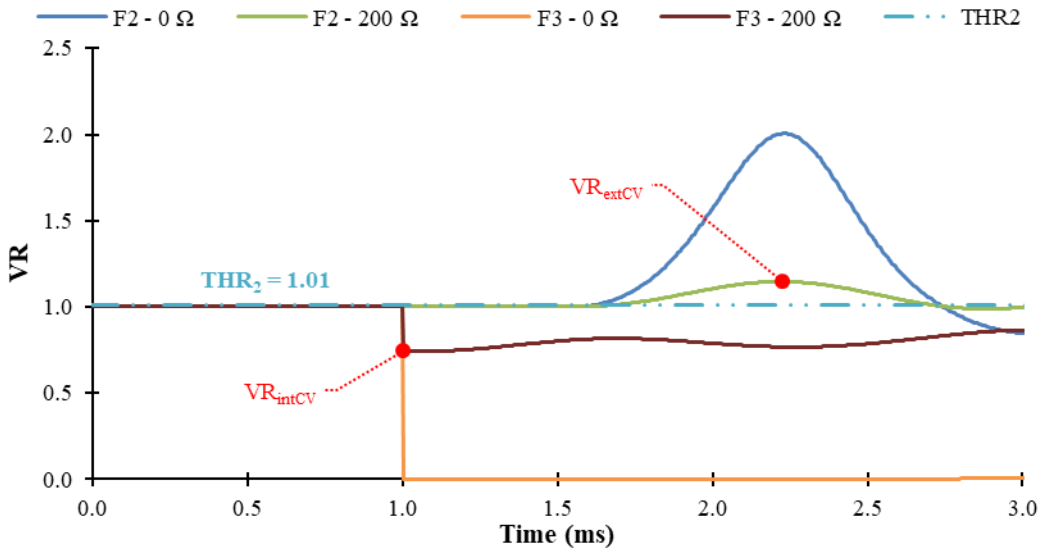


Figure 4.9.- Selection of threshold value THR_2 according to the worst fault case scenarios for relay R13.

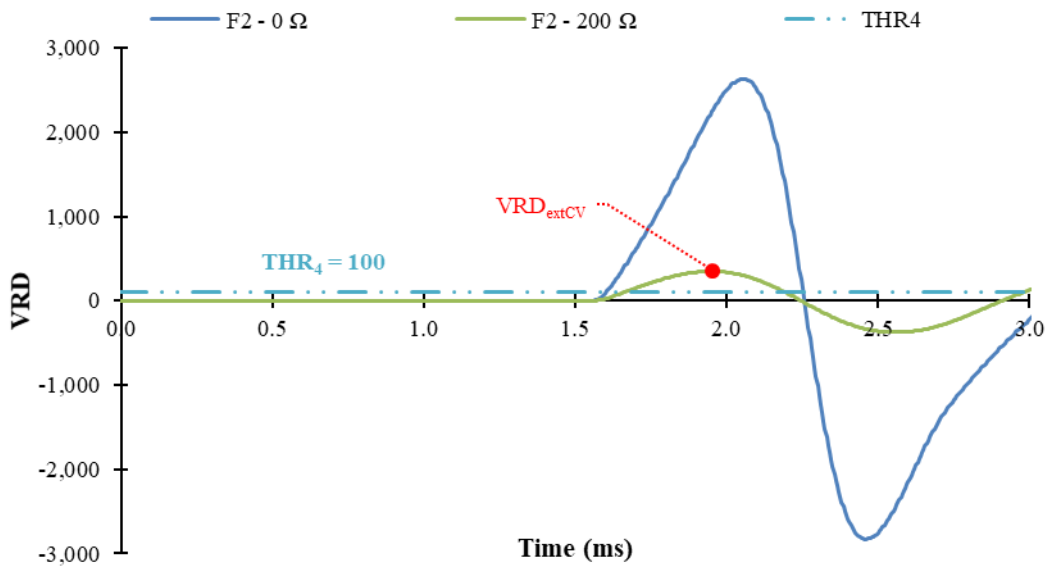


Figure 4.10.- Selection of threshold value THR_4 according to the worst fault case scenarios for relay R13.

4.2.3. Selection of threshold value THR_5

On the other hand, threshold value THR_5 related to the bus-side voltage-derivative ($ROCOV_{bus}$) employed in the circuit breaker failure protection algorithm is also similarly selected. Threshold value THR_5 is required for the verification process of proper DC-CB operation.

The proper operation of the DC-CB induces an increase in the V_{bus} and a consequent positive $ROCOV_{bus}$ value. Thus, THR_5 is a positive value; if it is overcome by the calculated $ROCOV_{bus}$, proper circuit breaker operation is detected (3.21), otherwise, a DC-CB failure is detected (3.22) and the circuit breaker failure protection operates. Thus, THR_5 must be lower than the maximum $ROCOV_{bus}$ induced by the proper operation of a neighbouring circuit breaker (4.5), as it can be seen in Figure 4.11.

$$THR_5 < ROCOV_{bus_{MAX_{CB_{ope}}}} \tag{4.5}$$

The selection process of threshold values THR_2, THR_4 and THR_5 regarding link backup protection, busbar protection and circuit breaker failure protection is summarized in the flow chart depicted in Figure 4.12.

Additionally, the verification process starts at t_{CBFv} after the standby time, $t_{CBFstandby}$, and the calculated $ROCOV_{bus}$ value must overcome THR_5 in a time less than time interval, $\Delta t_{CBF\_ROCOV_{bus}}$. If THR_5 is not overcome in $\Delta t_{CBF\_ROCOV_{bus}}$, a failure of the DC-CB is detected.

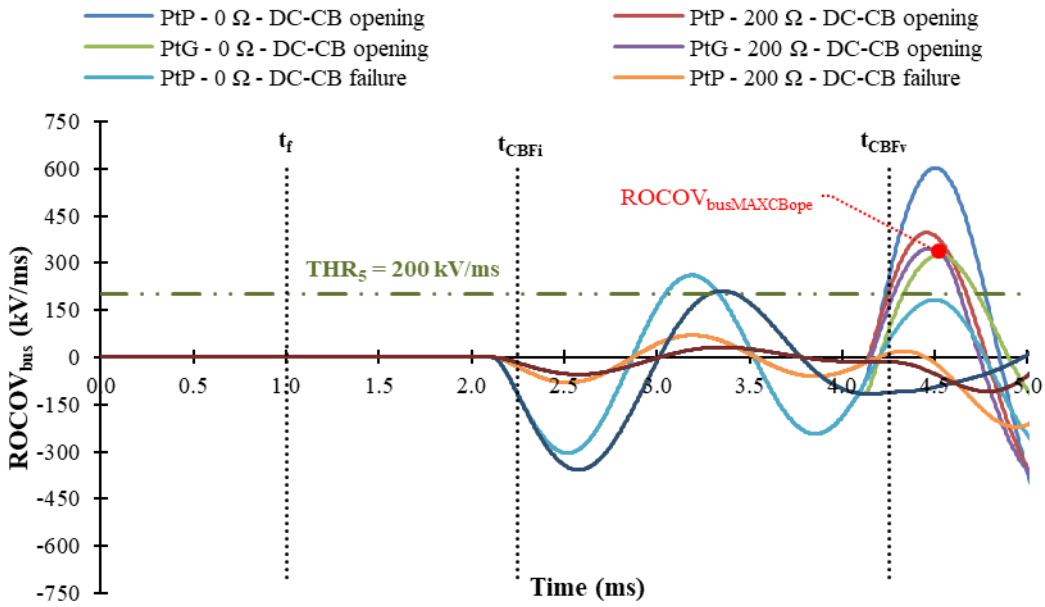


Figure 4.11.- Selection of threshold value THR_5 according to the worst fault case scenario (fault F4 and failure of DC-CB13) for relay R12.

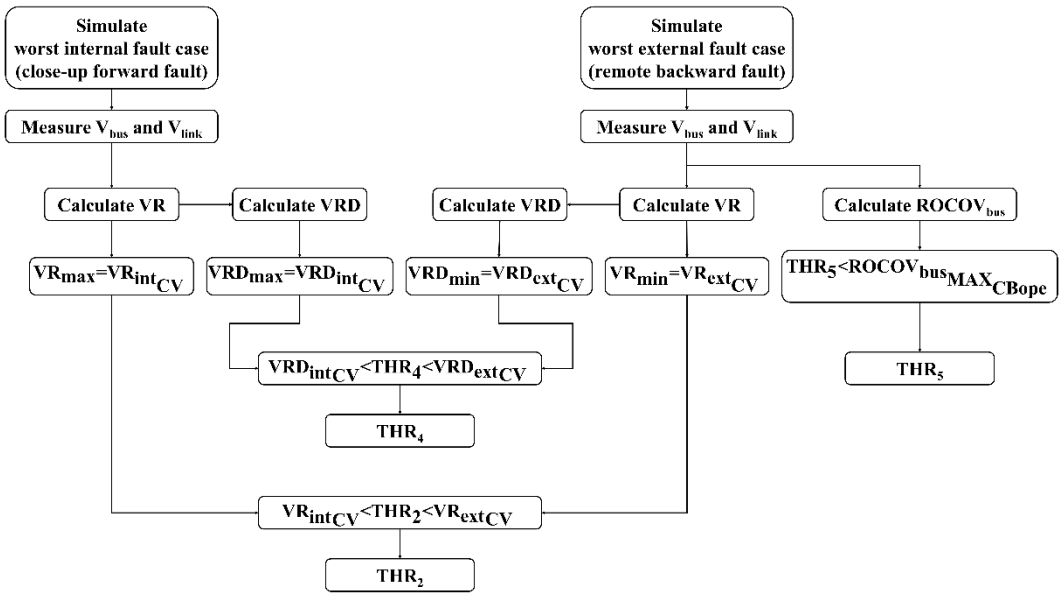


Figure 4.12.- Flow chart of the selection of threshold values THR_2, THR_4 and THR_5.

This time interval is in the order of 150 to 250 μs, i.e., three to five samples taking into account a sampling frequency of 20 kHz, in order to be able to detect the transients induced by the operation of a DC-CB. The specific time intervals for each relay are selected so as to ensure the detection of the proper DC-CB operation.

The time interval and the selected thresholds values for the link primary and backup protections, busbar protection and circuit breaker failure protection are summarized in Table 4.1. These threshold values are employed in the analyses presented in the following subsections.

Table 4.1.- Selection of threshold values and time intervals for each relay according to the protection algorithms.

Relay	Link protection						Busbar protection			Circuit breaker failure protection				
	Primary			Backup										
	THR_1	THR_3	Δt_P (µs)	THR_2	THR_4	Δt_{BU} (µs)	THR_2	THR_4	Δt_{BB} (µs)	THR_2	THR_4	Δt_{CBF} (µs)	THR_5 (kV/ms)	$\Delta t_{CBF\_ROCOV_{bus}}$ (µs)
R12	0.95	-1065	100	1.01	100	100	1.01	100	100	1.01	100	100	200	150
R13	0.95	-1000	100	1.01	100	100	1.01	100	100	1.01	100	100	200	150
R14	0.95	-1065	100	1.01	100	100	1.01	100	100	1.01	100	100	200	150
R21	0.95	-1000	100	1.01	100	100	1.01	100	100	1.01	100	100	200	250
R24	0.95	-1000	100	1.01	100	100	1.01	100	100	1.01	100	100	100	250
R31	0.95	-1000	100	1.01	120	100	1.01	120	100	1.01	120	100	100	200
R34	0.95	-1000	100	1.01	120	100	1.01	120	100	1.01	120	100	100	200
R41	0.95	-1000	100	1.01	115	100	1.01	115	100	1.01	115	100	350	200
R42	0.95	-1000	100	1.01	100	100	1.01	100	100	1.01	100	100	350	200
R43	0.95	-1000	100	1.01	100	100	1.01	100	100	1.01	100	100	350	200

4.3. Performance analysis of the LIVRD protection scheme

The proposed LIVRD protection scheme is validated in this subsection by testing it against different fault conditions. Each case is considered as a solid fault condition as well as a 200 Ω fault condition. Fault cases with a resistance higher than 200 Ω are rare [72], [176]. Both PtG and PtP faults have been analysed. The protection performance is tested through simulations in the four-terminal grid presented in Appendix-A. Fault locations are depicted in Figure 4.1. A relatively low sampling frequency of 20 kHz and common 100 mH limiting inductors are employed.

4.3.1. Link protection

The novel LIVRD link protection proposed in this thesis covers each cable of the meshed grid as an independent protection zone. This way, the link protection only operates against faults located in the cables. Limiting inductors are employed to delimit the borders of each protection zone. Therefore, only the affected cable is isolated while the remaining zones of the grid continue their operation. Both link primary and link backup LIVRD protection algorithms proposed in Chapter 3 are evaluated.

4.3.1.1 Link primary protection

The LIVRD link primary protection is in charge of detecting all faults located within the borders of its protection zone. It is based on detecting forward faults by using the VR and VRD algorithms as it was previously explained in subsection 3.3.1.

The results of the performance analysis are summarized in Table 4.2 where the detection time (t_{Pd}) and the possible nuisance operation of the external relays (trip – T, no trip – NT) are indicated for each simulated case. The selected threshold values THR_1 and THR_3 are those summarized in Table 4.1 for each relay. As it can be seen, each simulated fault condition is properly detected and no nuisance operation by external relays occur. DC-CBs operate 2 ms after fault detection is achieved, since it is assumed the implementation of a H-CB.

Close-up fault conditions are detected in a few microseconds while remote faults located at 200 km (longest cable in the system) are detected in around 1 ms. Moreover, close-up faults are quickly detected regardless of the fault type or fault resistance as well as solid remote faults. Meanwhile, detection of 200 Ω remote faults is delayed (50 μs) compared to solid fault cases. However, the slowest

detection time obtained from these series of simulations is 1.150 ms (200 Ω and 200 km fault case) which is still a very fast fault detection; circuit breakers operate at 3.150 ms.

The fast operation speed of the proposed link primary protection is successfully validated and satisfies the speed requirement related to VSC-based systems. Therefore, this analysis demonstrates the fast, selective and reliable operation of the proposed link primary protection algorithm.

Figure 4.13 depicts the current, VR and VRD signals during the simulated PtP F1 fault case with fault inception at 1 ms. Both solid and 200 Ω faults are represented. Detection and circuit breaker operation times for each case are also presented in the figures.

Table 4.2.- Performance of the link primary protection against 0 Ω and 200 Ω PtG and PtP fault conditions.

Fault	**Relay**	**Pole-to-Ground Fault**			**Pole-to-Pole Fault**		
		t_{Pd} (ms)		External relays	t_{Pd} (ms)		External relays
		0 Ω	200 Ω		0 Ω	200 Ω	
F1	R12	0.050	0.050	NT	0.050	0.050	NT
	R21	0.600	0.600		0.600	0.600	
F2	R12	0.600	0.600	NT	0.550	0.550	NT
	R21	0.050	0.050		0.050	0.050	
F3	R13	0.050	0.050	NT	0.050	0.050	NT
	R31	1.100	1.150		1.100	1.150	
F4	R13	1.100	1.150	NT	1.100	1.150	NT
	R31	0.050	0.050		0.050	0.050	
F5	R14	0.050	0.050	NT	0.050	0.050	NT
	R41	1.100	1.150		1.100	1.150	
F6	R14	1.100	1.150	NT	1.100	1.150	NT
	R41	0.050	0.050		0.050	0.050	
F7	R24	0.050	0.050	NT	0.050	0.050	NT
	R42	0.850	0.850		0.850	0.850	
F8	R24	0.850	0.850	NT	0.850	0.850	NT
	R42	0.050	0.050		0.050	0.050	
F9	R34	0.050	0.050	NT	0.050	0.050	NT
	R43	0.550	0.600		0.600	0.600	
F10	R34	0.600	0.600	NT	0.600	0.600	NT
	R43	0.050	0.050		0.050	0.050	

The rate-of-rise of the fault current is attenuated during high-resistance faults and it is not as sharp as the one in the case of solid faults. However, this effect can be considered negligible in terms of fault detection, since both the VR and VRD signals cross their respective threshold values almost instantaneously when the fault-induced traveling wave arrives to the relay point. Moreover, it can be seen that the VR and VRD signals cross their corresponding threshold values with enough margin. The proposed algorithm is selective and sensitive enough to detect both solid and high-resistance fault conditions.

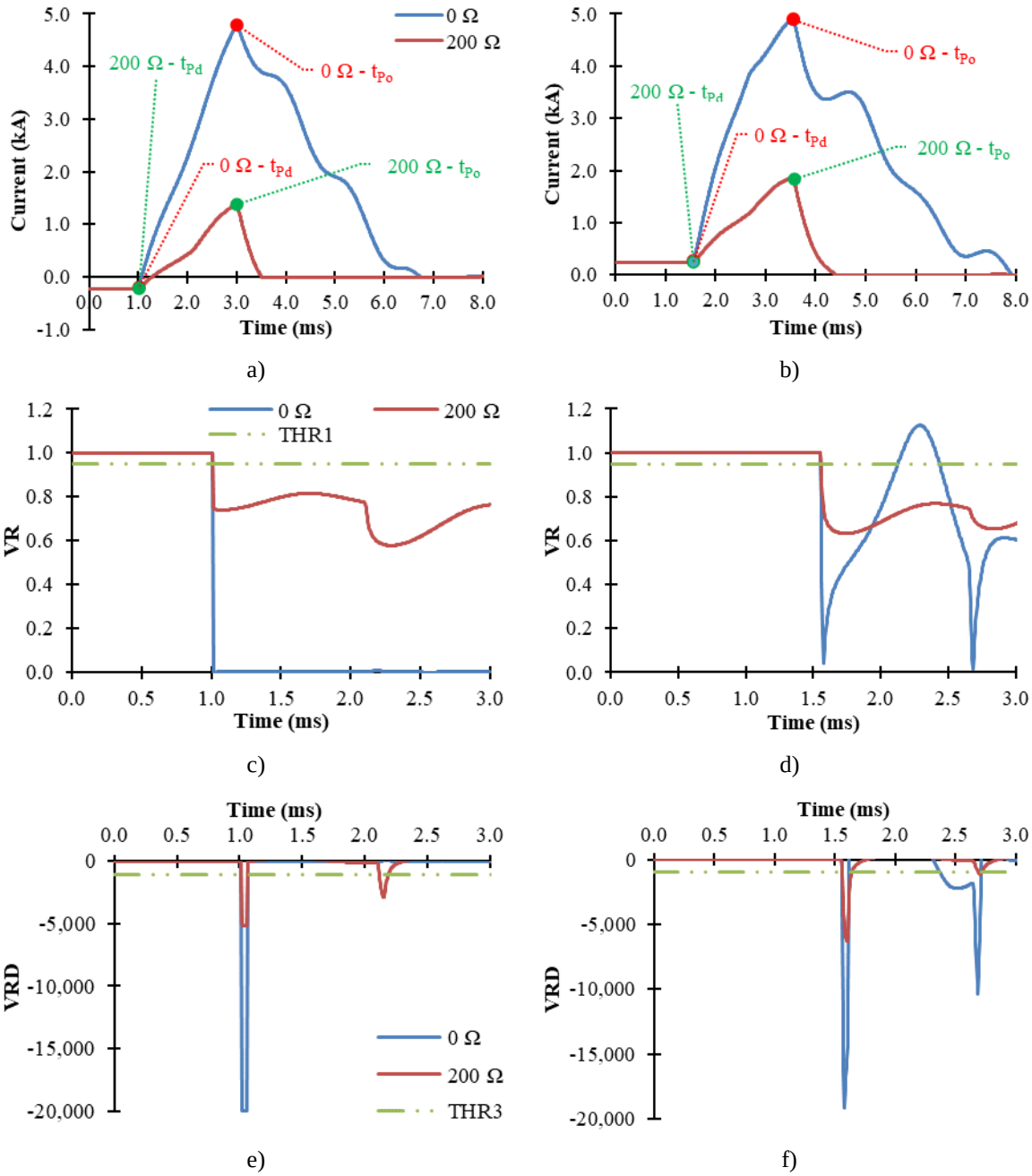


Figure 4.13.- Current, VR and VRD signals during a PtP fault (F1); a), c) and e) are measured by relay R12 and b), d) and f) are measured by relay R21.

4.3.1.2 Link backup protection

The link primary protection might not be able to detect link faults due to a malfunction of its relay. Thus, a link backup protection must be implemented in order to detect link faults when the link primary protection is not capable. This way, system reliability and security are ensured. The proposed LIVRD link backup protection consists of employing the reverse reach of the neighbouring relays, i.e., detection of backward faults by the local-measurement-based VR and VRD algorithms as explained in subsection 3.3.1.2. Threshold values THR_2 and THR_4, which are needed for the correct operation of the LIVRD link backup protection, are those indicated in Table 4.1.

The performance of the link backup protection is evaluated by simulating the same fault case scenarios as in the previous subsection, so as to compare the operation of link primary and link backup protections. Therefore, solid and 200 Ω PtP and PtG fault cases are simulated varying their location in the system. The results of the evaluation are summarized in Table 4.3 where detection time of the link backup protection (t_{BUd}) is indicated in milliseconds. The relay presenting a failure in its operation for each simulated case is indicated in the "Malfunctioning relay" column. Each fault case has been simulated twice varying which relay presents a malfunctioning link primary protection. "Backup relays" column indicates which neighbouring relays are in charge of link backup protection in each simulated case according to the malfunctioning relay.

Comparing with performance of the link primary protection (see Table 4.2), Table 4.3 shows how the link backup protection detects close-up solid faults slightly more slowly than the link primary protection. Remote solid faults are detected with a time delay between 50 and 150 μs according to the fault location. Meanwhile, the link backup protection presents a time delay up to 250 μs in comparison with the link primary protection in the case of high-resistance fault conditions. However, the time delay regarding the operation of the link backup protection is not significant, it satisfies the speed requirement and allows fast backup operation against link faults.

Other conclusions can be extracted from Table 4.3. The link backup protection is capable of quickly detecting solid faults, regardless of the fault type, while it presents a slight delay, in the range of 50-100 μs, when detecting 200 Ω PtG faults in comparison with 200 Ω PtP faults. Moreover, there is a delay up to 200 μs during detection of 200 Ω PtG faults in comparison with solid PtG faults, while this delay is only in the range of 100 μs when detection of 200 Ω and solid PtP faults are compared. Once again, these time delays are not of great importance. Therefore, the fast and reliable operation of the LIVRD link backup protection algorithm has been successfully demonstrated through this evaluation.

Table 4.3.- Performance of the link backup protection against 0 Ω and 200 Ω PtG and PtP fault conditions.

Fault	Malfunctioning Relay	Backup relays	Backup fault detection time t_{BUd} (ms)			
			Pole-to-Ground Fault		Pole-to-Pole Fault	
			0 Ω	200 Ω	0 Ω	200 Ω
F1	R12	R13, R14	0.100	0.250	0.100	0.150
	R21	R24	0.650	0.750	0.650	0.700
F2	R12	R13, R14	0.650	0.750	0.650	0.700
	R21	R24	0.100	0.250	0.100	0.150
F3	R13	R12, R14	0.100	0.250	0.100	0.150
	R31	R34	1.250	1.400	1.250	1.300
F4	R13	R12, R14	1.200	1.350	1.200	1.300
	R31	R34	0.100	0.300	0.100	0.200
F5	R14	R12, R13	0.100	0.250	0.100	0.150
	R41	R42, R43	1.250	1.350	1.250	1.300
F6	R14	R12, R13	1.200	1.350	1.200	1.300
	R41	R42, R43	0.100	0.250	0.100	0.200
F7	R24	R21	0.100	0.250	0.100	0.150
	R42	R41, R43	0.950	1.100	0.950	1.000
F8	R24	R21	0.950	1.050	0.950	1.000
	R42	R41, R43	0.100	0.300	0.100	0.150
F9	R34	R31	0.100	0.300	0.100	0.150
	R43	R41, R42	0.650	0.750	0.650	0.750
F10	R34	R31	0.650	0.800	0.650	0.700
	R43	R41, R42	0.100	0.300	0.100	0.200

Fault current during the simulated PtP F1 fault case with failure of relay R12 is depicted in Figure 4.14 (fault inception at 1 ms). Operation of link primary (dot-dashed line) and link backup (solid line) protections are compared. As it can be seen, the link backup protection is only slightly slower than the link primary protection. Moreover, Figure 4.15 shows how the calculated VR and VRD signals cross their respective threshold values and properly detect fault F1 during both solid and high-resistance fault case scenarios.

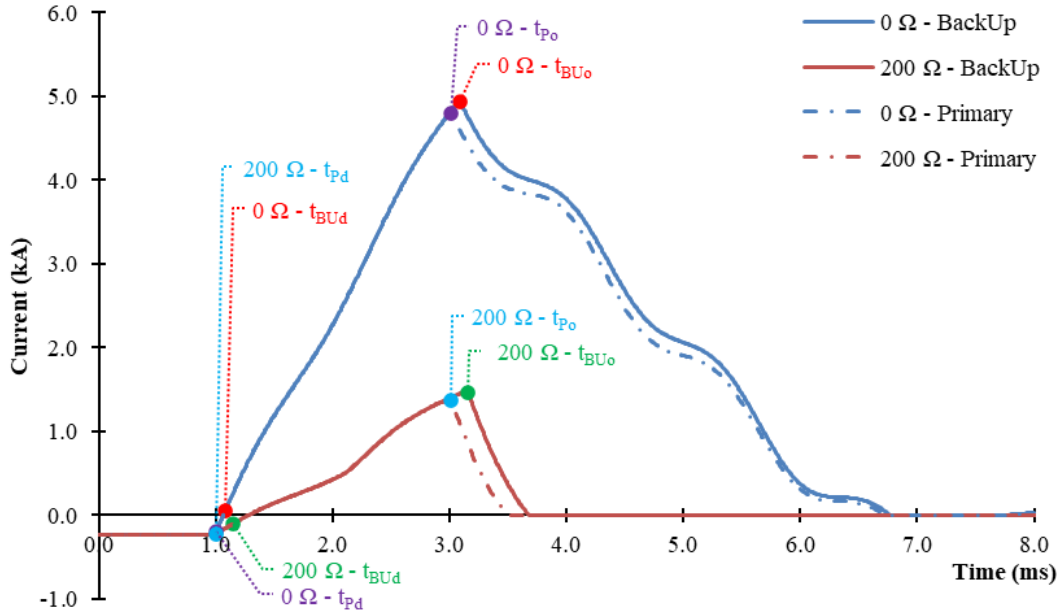
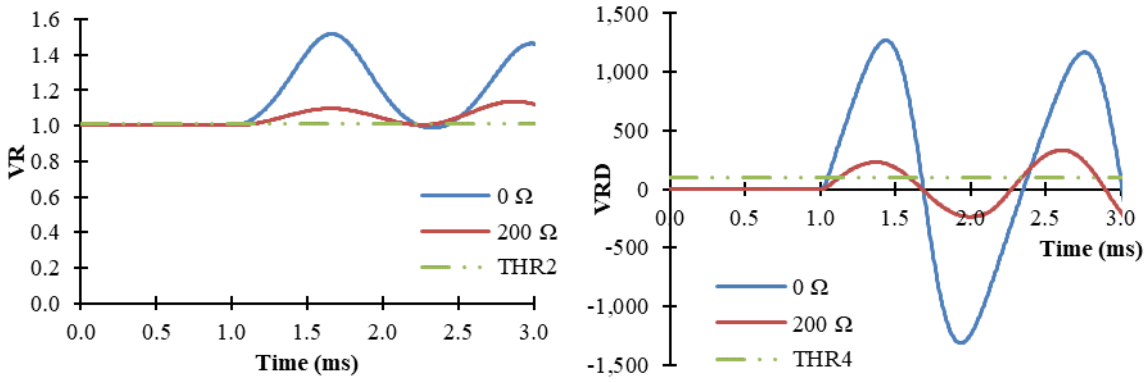


Figure 4.14.- Comparison of fault current signals during a PtP fault (F1) for link primary (dot-dashed line) and link backup (solid line) protections (failure of relay R12).



a) b)

Figure 4.15.- a) VR and b) VRD signals measured by relay R13 for link backup protection (failure of relay R12) during a PtP fault (F1).

Similarly, Figure 4.16 shows the fault current during the same fault case (fault inception at 1 ms) but with failure of relay R21. Figure 4.17 depicts the VR and VRD signals measured by relay R24 which is able to detect fault F1 by using the

link backup protection. Therefore, it is demonstrated the proper and fast operation of the link backup protection algorithm, which, once more, is only slightly slower than the link primary protection algorithm. Thus, it is suitable for VSC-based grids.

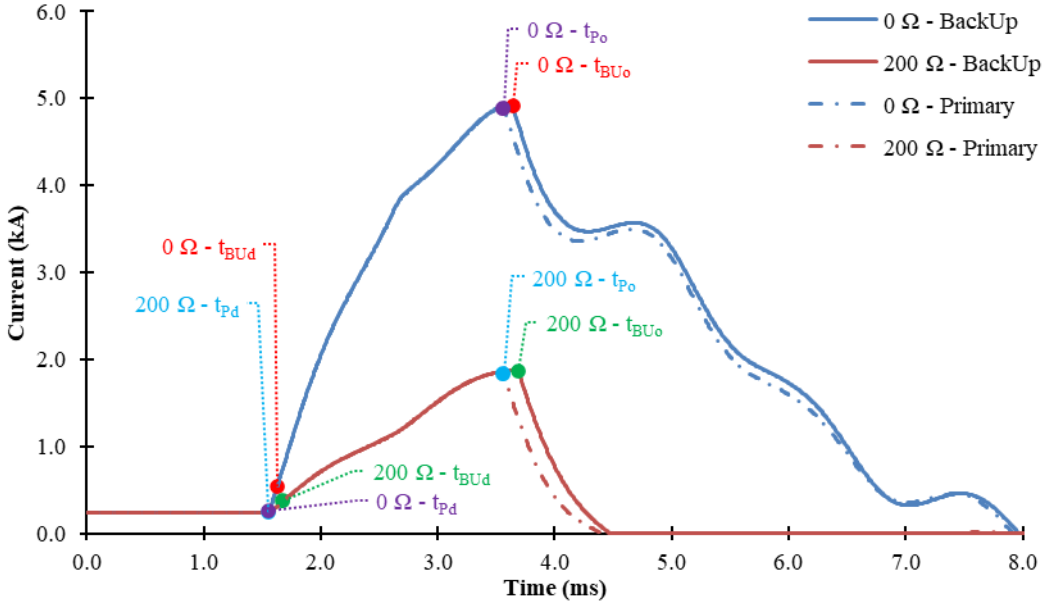
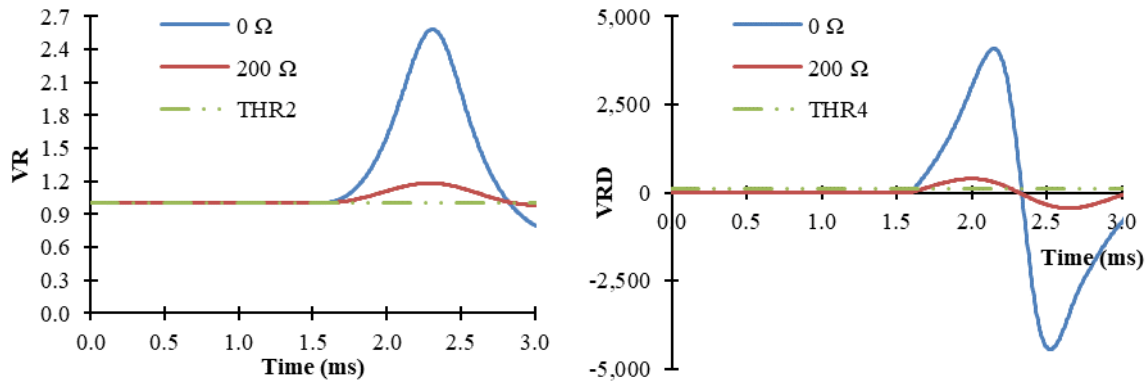


Figure 4.16.- Comparison of fault current signals during a PtP fault (F1) for link primary (dot-dashed line) and link backup (solid line) protections (failure of relay R21).



a) b)

Figure 4.17.- a) VR and b) VRD signals measured by relay R24 for link backup protection (failure of relay R21) during a PtP fault (F1).

4.3.2. Busbar protection

The busbar protection, similarly to the link backup protection, is based on the reverse reach of the relays placed in the links interconnected to the protected busbar, as it is explained in subsection 3.3.2. In this case, all relays connected to the protected busbar must simultaneously detect a backward fault.

In order to validate the performance of the busbar protection, operation against 0 Ω and 200 Ω busbar faults is analysed. Faults cases at the four busbars of the multi-terminal grid presented in Appendix-A are simulated. Simulations results are summarised in Table 4.4.

Busbar faults can be considered close-up backward faults, thus, they are quickly detected by the busbar protection, as it can be seen in Table 4.4. All simulated cases are properly detected in 50 μs regardless of the fault resistance.

Moreover, the event of a busbar fault does not produce the nuisance operation of any external relays. Thus, the link protection of the external relays placed in the system does not detect this kind of fault. Therefore, it can be said that the threshold values that are employed in the operation of the link protection have been correctly selected and they are selective enough to only detect link faults. This way, the proper operation of the busbar protection is demonstrated through this analysis as well as the selective operation of the link protection.

Table 4.4.- Performance of the busbar protection against 0 Ω and 200 Ω fault conditions.

Faulted busbar	**Relay**	**Detection time (ms)**		**External relays**
		0 Ω	**200 Ω**	
Bus 1	R12	0.050	0.050	NT
	R13			
	R14			
Bus 2	R21	0.050	0.050	NT
	R24			
Bus 3	R31	0.050	0.050	NT
	R34			
Bus 4	R41	0.050	0.050	NT
	R42			
	R43			

During a solid busbar fault, the bus-side voltage V_{bus} collapses sharply to zero value (Figure 4.18-a) producing very high positive values in the VR and VRD calculations according to (3.5) and (3.11) (Figure 4.18-c and –d, respectively). Thus, the busbar fault is almost instantaneously detected by the busbar protection

(t_{BBd}) and, then, the circuit breakers operate (t_{BBo}) to complete fault clearance, as it can be seen in Figure 4.18-b which depicts the fault currents measured by relays R12, R13 and R14 during a fault inside Bus 1 (fault inception at 1 ms). Link-side voltages V_{link} measured by all relays are superimposed in the figure as well as bus-side voltages V_{bus}. VR and VRD waves are also superimposed. Fault current presents a negative value since it is flowing from the link to the busbar.

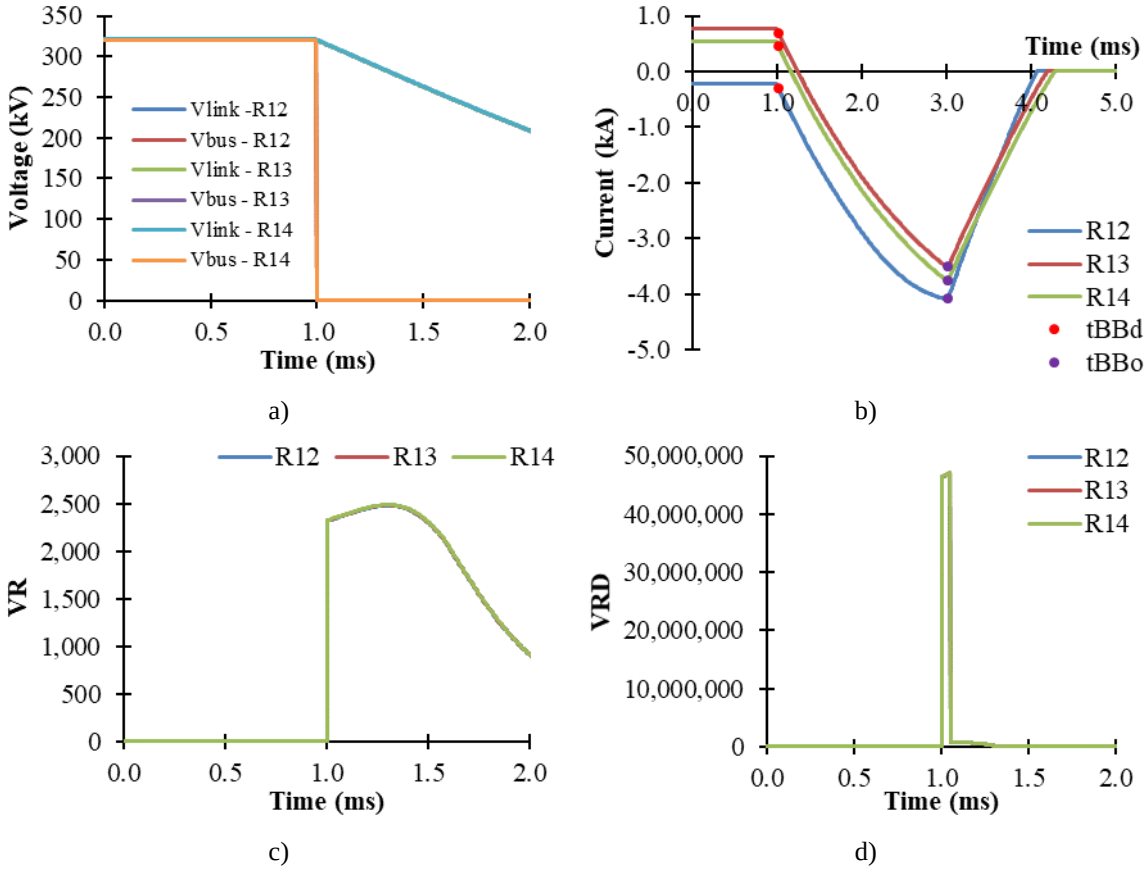


Figure 4.18.- Measurements taken by relays R12, R13 and R14 during a solid fault at Bus 1: a) V_{link} and V_{bus}, b) fault currents, c) VR and d) VRD.

Similarly, the bus-side voltage V_{bus} sharply drops to a certain value during a 200 Ω busbar fault. Even if the voltage collapse is attenuated, the difference between V_{link} and V_{bus} produces high enough values of VR and VRD to cross their corresponding threshold values, as it can be seen in Figure 4.19. Additionally, Figure 4.19-b shows how the rate-of-rise of the fault current during a high-resistance fault is also attenuated.

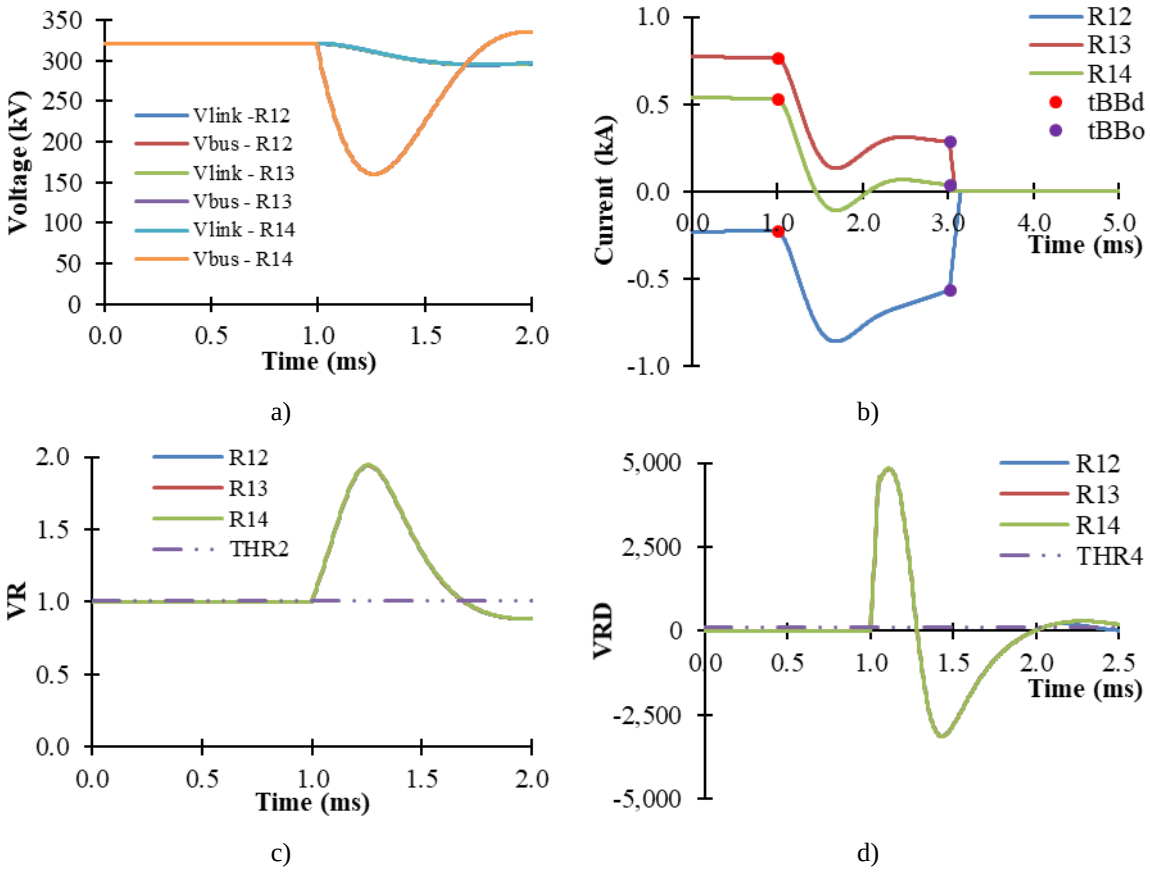


Figure 4.19.- Measurements taken by relays R12, R13 and R14 during a 200 Ω fault at Bus 1: a) V_{link} and V_{bus}, b) fault currents, c) VR and d) VRD.

4.3.3. Circuit breaker failure protection

The VR and VRD algorithms initiate the circuit breaker failure protection while the $ROCOV_{bus}$ algorithm is employed in the verification process of DC-CB operation, as it is explained in subsection 3.3.3. The performance of the LIVRD circuit breaker failure protection algorithm is evaluated in this subsection against the same fault cases analysed in previous subsections (Figure 4.1).

Figure 4.20 depicts the fault current caused by a PtP fault for both solid and 200 Ω fault cases (fault inception at 1 ms). Operation of link primary protection and circuit breaker failure protection are compared. The simulated fault case is F1 which is located in link 12, at the beginning of the cable from Bus 1. Thus, relay R12 operates as link primary protection while relay R13 (along with relay R14) operates as circuit breaker failure protection when circuit breaker DC-CB12 presents a failure in its operation. Additionally, Figure 4.21 and Figure 4.22 show the VR and VRD signals measured by relays R12 and R13, respectively. Figure 4.23 depicts the calculation of $ROCOV_{bus}$ by relay R13.

Link primary protection's fault detection time (t_{Pd}) for solid and 200 Ω faults is similar and almost instantaneous, after the fault-induced traveling wave arrival at the relay point. Meanwhile, the circuit breaker failure protection initiates its process at time t_{CBFi} when it detects a backward fault, slightly after fault detection by the link primary protection. Initiation time of the circuit breaker failure during a 200 Ω fault is slower than during a solid fault, due to the attenuation produced in the signals. Link primary protection's fault detection time and circuit breaker failure protection's initiation time are also depicted in Figure 4.21 and Figure 4.22, corresponding with the moment the VR and VRD signals cross their respective threshold values.

For a solid PtP F1 fault, the relay R12 (link primary protection) detects the fault at, t_{Pd}, 1.050 ms (0.050 ms after fault inception as it is indicated in Table 4.7) and sends the trip signal to circuit breaker DC-CB12 which operates after 2 ms. The H-CB operates at time, t_{Po}, 3.050 ms and interrupts a maximum fault current of 4.8 kA. Fault clearance is completed at time, t_{Pc}, 6.750 ms (5.750 ms from fault inception).

Similarly, relay R13 detects a backward fault and initiates the circuit breaker failure protection at time, t_{CBFi}, 1.100 ms (0.100 ms after fault inception as it is indicated in Table 4.7). Then, the circuit breaker failure protection keeps on standby during time $t_{CBFstandby}$, equal to the operating time of the circuit breaker, and then it starts the process of verifying the proper operation of the corresponding circuit breaker at time 3.100 ms. Relay R13 verifies the proper operation of circuit breaker DC-CB12 by checking the bus-side voltage-derivative, $ROCOV_{bus}$, within a time window $\Delta t_{CBF\_ROCOV_{bus}}$ of 150 μs (see Table 4.1).

If the calculated $ROCOV_{bus}$ overcomes the corresponding threshold value THR_5 (200 kV/ms, see Table 4.1) during the time window $\Delta t_{CBF\_ROCOV_{bus}}$, circuit breaker DC-CB12 has properly operated and the fault clearance process has started. Otherwise, a failure in the operation of circuit breaker DC-CB12 is detected and a trip signal is sent to circuit breaker DC-CB13 (relay R14 similarly operates and sends a trip signal to circuit breaker DC-CB14).

For a solid PtP F1 fault, relay R13 detects the failure of circuit breaker DC-CB12 at time, t_{CBFd}, 3.250 ms ($t_{CBFd} = t_{CBFi} + t_{CBFstandby} + \Delta t_{CBF\_ROCOV_{bus}}$), i.e., 2.250 ms from fault inception, as it can be seen in Figure 4.23 and Table 4.5.

Circuit breaker DC-CB13 (and DC-CB14) operates after 2 ms at time, t_{CBFo}, 5.250 ms, interrupting a maximum fault current of 9.622 kA. Fault clearance is completed at time t_{CBFc}, around 10.550 ms (9.550 ms from fault inception).

Table 4.5.- Comparison of link primary protection and circuit breaker failure protection for failure of DC-CB12 during a solid PtP F1 fault. Time steps (ms) and maximum fault current interrupted (kA).

Fault	Link primary protection					Circuit breaker failure protection					
	Relay	t_{Pd}	t_{Po}	t_{Pc}	I_{max}	Relay	t_{CBFi}	t_{CBFd}	t_{CBFo}	t_{CBFc}	I_{max}
F1 PtP solid	R12	1.050	3.050	6.750	4.800	R13	1.100	3.250	5.250	10.550	9.622

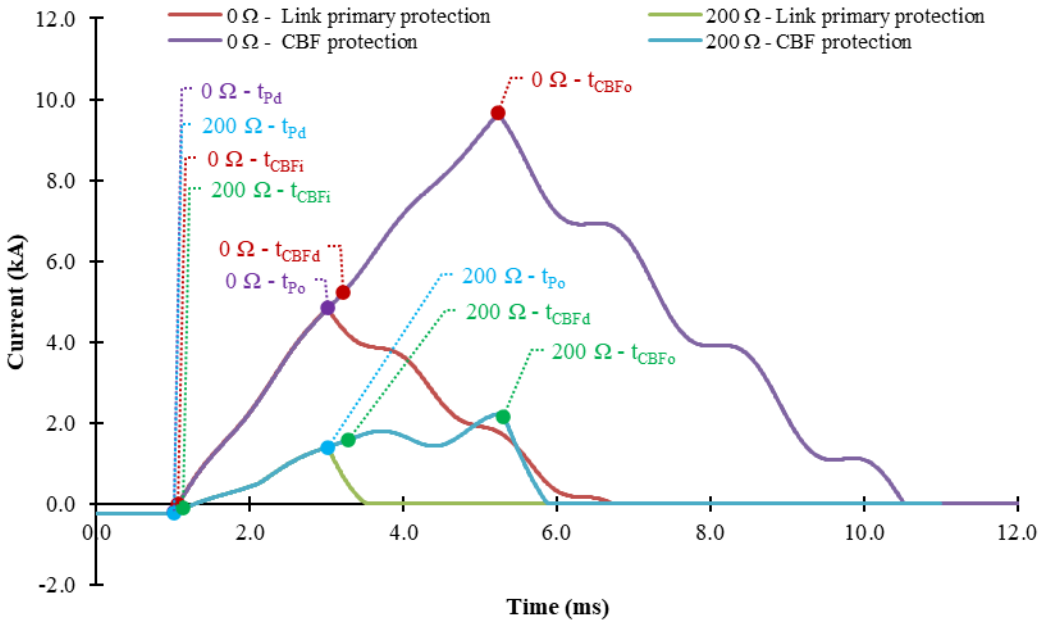
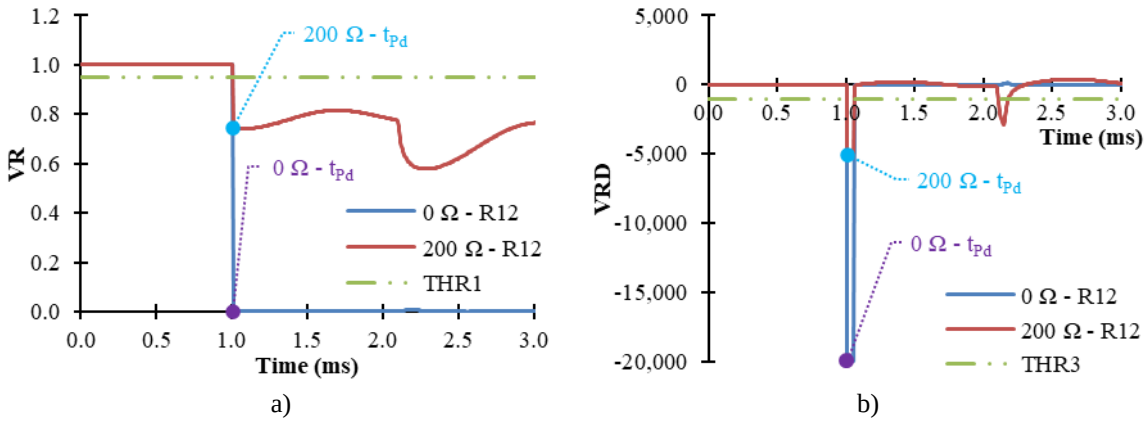


Figure 4.20.- Fault current induced by solid and 200 Ω PtP F1 faults during operation of link primary protection and circuit breaker failure protection with failure of DC-CB12.



a) b)

Figure 4.21.- Measurements of a) VR and b) VRD signals by relay R12 (link primary protection) during solid and 200 Ω PtP F1 faults and failure of DC-CB12.

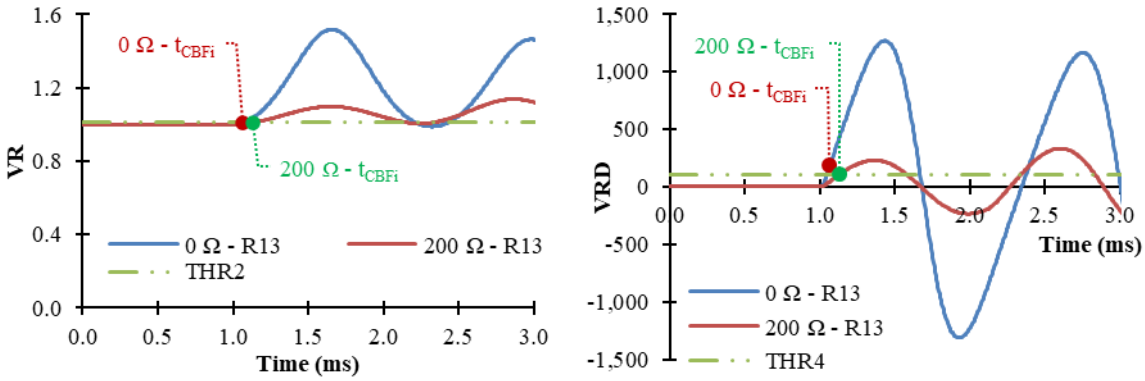


Figure 4.22.- Measurements of a) VR and b) VRD signals by relay R13 (circuit breaker failure protection) during solid and 200 Ω PtP F1 faults and failure of DC-CB12.

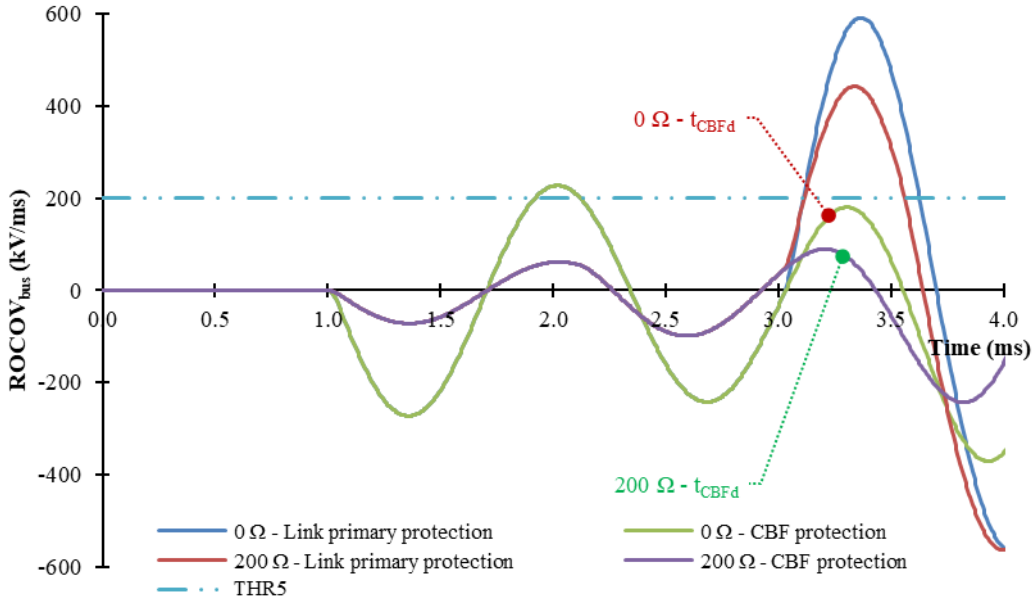


Figure 4.23.- $ROCOV_{bus}$ calculation by relay R13 for verification of DC-CB12 operation during solid and 200 Ω PtP F1 faults for proper operation and failure.

Similarly to the previously-explained fault case scenario, Figure 4.24, Figure 4.25 and Figure 4.26 show the fault current, VR, VRD and $ROCOV_{bus}$ signals regarding a PtP F1 fault but measured by the relays located at the other end of link L12, i.e., relay R21 (link primary protection) and relay R24 (circuit breaker failure protection). Contrary to the previous case, circuit breaker DC-CB12 properly operates while circuit breaker DC-CB21 presents a failure.

Relay R21 detects a forward fault at time, t_{Pd}, 1.600 ms (0.600 ms after fault inception, as it is indicated in Table 4.7). A trip signal is sent to circuit breaker DC-CB21 which operates at time, t_{Po}, 3.600 ms (2.600 ms from fault inception). The circuit breaker DC-CB21 interrupts a maximum fault current of 4.885 kA. The fault clearing process ends at time, t_{Pc}, 7.950 ms, i.e., 6.950 ms after fault inception.

Likewise, relay R13 detects a backward fault and initiates the circuit breaker failure protection at time, t_{CBFi}, 1.650 ms, i.e., 0.650 ms after fault inception. The proposed circuit breaker failure protection keeps on standby until time $t_{CBFstandby}$ passes, when it verifies the proper operation of circuit breaker DC-CB21. The $ROCOV_{bus}$ signal is checked during a time window $\Delta t_{CBF\_ROCOV_{bus}}$ of 250 μs (see Table 4.1).

The $ROCOV_{bus}$ does not cross threshold value THR_5 (100 kV/ms, see Table 4.1), so failure of circuit breaker DC-CB21 is detected at time, t_{CBFd}, 3.900 ms ($t_{CBFd} = t_{CBFi} + t_{CBFstandby} + \Delta t_{CBF\_ROCOV_{bus}}$), i.e., 2.900 ms from fault inception, as it can be seen in Figure 4.27 and Table 4.6. Thus, a trip signal is sent to circuit breaker DC-CB24 which operates at time, t_{CBFo}, 5.880 ms, interrupting a fault current of 7.826 kA. Fault clearance is completed at time, t_{CBFc}, 11.200 ms, i.e., 10.185 ms after fault inception.

Table 4.6.- Comparison of link primary protection and circuit breaker failure protection for a solid PtP F1 fault with failure of DC-CB21. Time steps (ms) and maximum fault current interrupted (kA).

Fault	Link primary protection					Circuit breaker failure protection					
	Relay	t_{Pd}	t_{Po}	t_{Pc}	I_{max}	Relay	t_{CBFi}	t_{CBFd}	t_{CBFo}	t_{CBFc}	I_{max}
F1 PtP solid	R21	1.600	3.600	7.950	4.885	R24	1.650	3.900	5.900	11.200	7.826

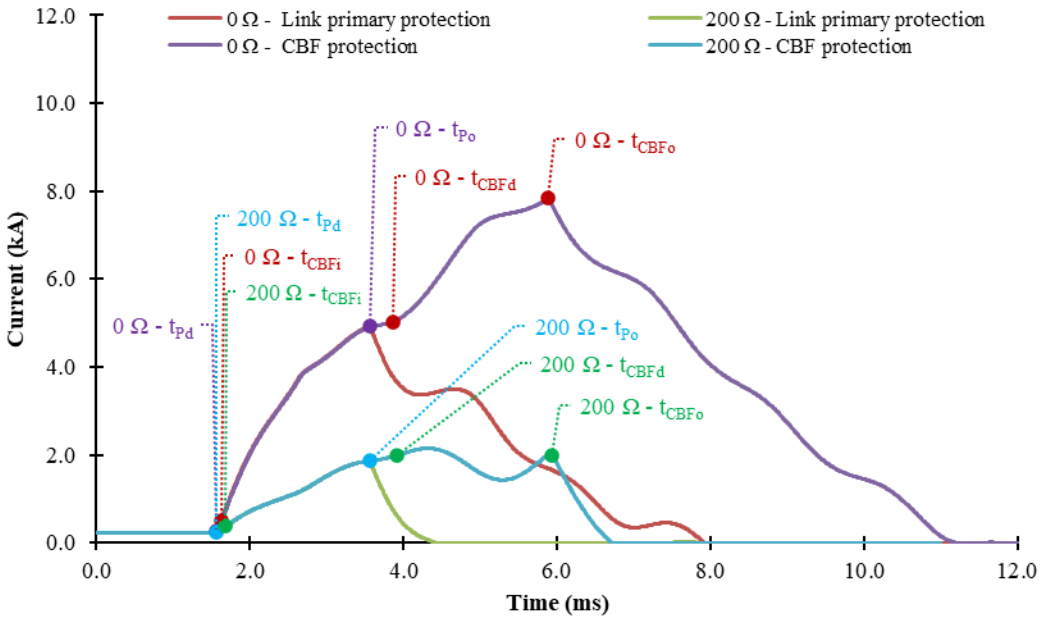
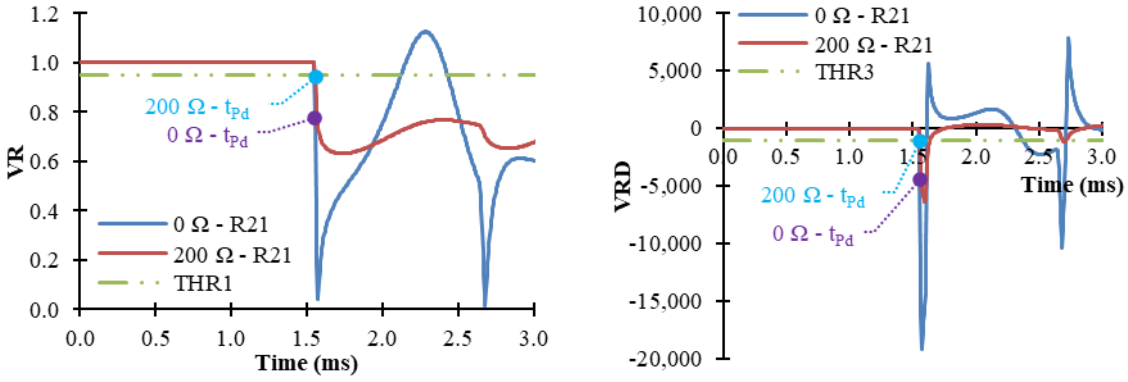
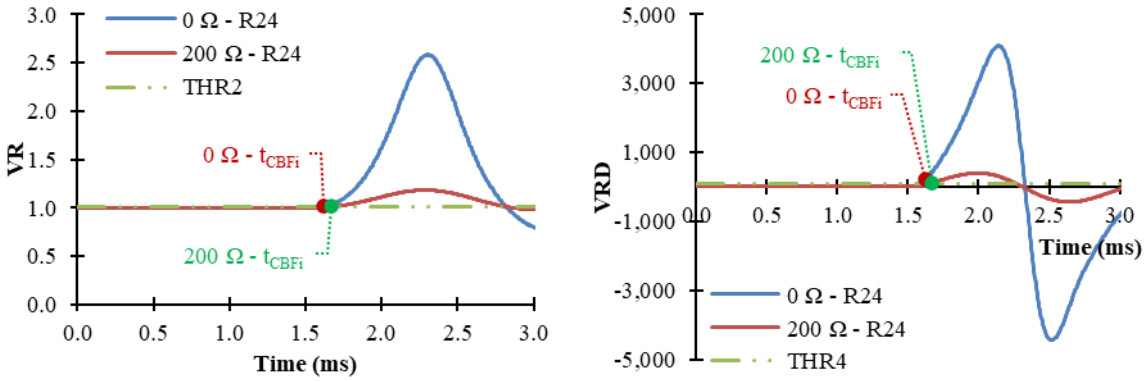


Figure 4.24.- Fault current induced by solid and 200 Ω PtP F1 faults during operation of link primary protection and circuit breaker failure protection with failure of DC-CB21.



a) b)

Figure 4.25.- Measurements of a) VR and b) VRD signals by relay R21 (link primary protection) during solid and 200 Ω PtP F1 faults and failure of DC-CB21.



a) b)

Figure 4.26.- Measurements of a) VR and b) VRD signals by relay R24 (circuit breaker failure protection) during solid and 200 Ω PtP F1 faults and failure of DC-CB21.

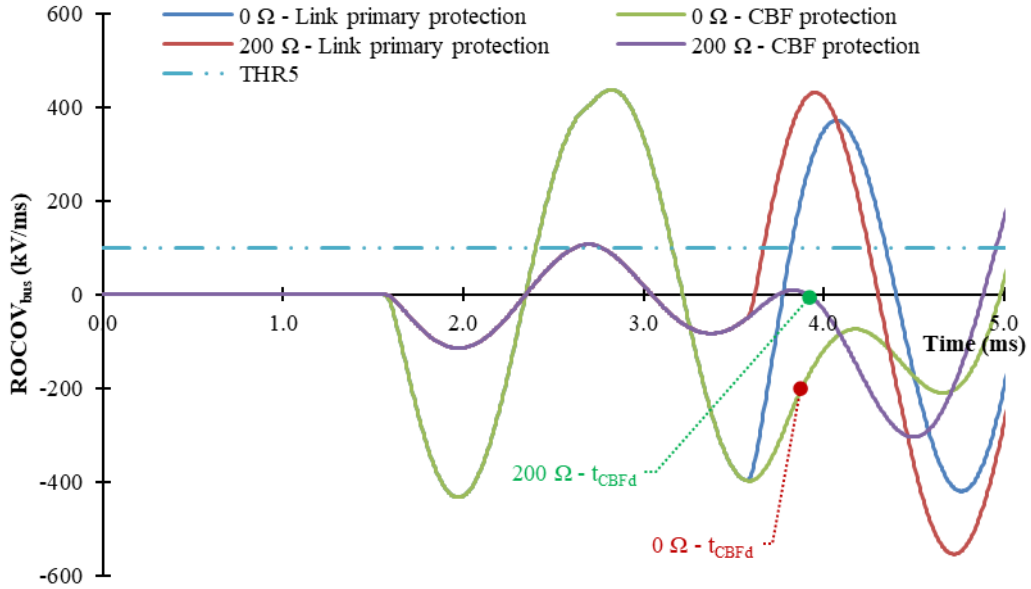


Figure 4.27.- $ROCOV_{bus}$ calculation by relay R24 for verification of DC-CB21 operation during solid and 200 Ω PtP F1 faults for proper operation and failure.

The results of the performance analysis of the LIVRD circuit breaker failure protection are summarized in Table 4.7, where detection times of link primary (t_{Pd}) and circuit breaker failure protections are indicated in order to compare them. Two different times are indicated for the circuit breaker failure protection: the time where the process is started (t_{CBFi}), because the neighbouring relays have detected a backward fault, and the time where a circuit breaker failure is detected (t_{CBFd}) by the $ROCOV_{bus}$ algorithm. If proper operation of the circuit breaker is detected "NF" (No Failure) is indicated in the t_{CBFd} column. Malfunctioning circuit breakers are represented by highlighting in bold and cursive their corresponding relay in the "Relay" column.

The circuit breaker failure protection starts up to 100 μs after the detection time of the link primary protection during solid faults and up to 200 μs when a 200 Ω fault occurs, being slightly slower during 200 Ω PtG faults than during 200 Ω PtP faults. On the other hand, the circuit breaker failure protection is up to 150 μs slower detecting 200 Ω PtG faults than solid PtG faults, while this delay is only in the order of tens of microseconds in the case of PtP faults. Moreover, there is no difference between initiation time and detection time during solid faults regardless of the fault type, while it needs a few more tens of microseconds to detect a 200 Ω PtG fault compared to a 200 Ω PtP fault.

Additionally, taking into account a 2 ms operating time of H-CB, if the proposed circuit breaker failure protection is employed, the neighbouring circuit breakers operate in the range of 4 to 6 ms after fault inception, depending on the fault type, resistance and location. This demonstrates that the proposed circuit breaker failure protection presents fast operation and can satisfy the restrictive speed requirement related to VSC-based systems. It must also be highlighted that all simulated cases are correctly detected by both the primary and circuit breaker failure protections, respectively, and no nuisance operation of external relays is produced. Therefore, the performance of the circuit breaker failure protection is validated.

Table 4.7.- Performance of the circuit breaker failure protection against 0 Ω and 200 Ω fault conditions. [Part 1 of 3]

Fault	Relay	Pole-to-Ground Fault						Pole-to-Pole Fault						Neighbouring relays
		0 Ω			200 Ω			0 Ω			200 Ω			
		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		
			t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)	
F1	***R12***	0.050	0.100	2.250	0.050	0.250	2.400	0.050	0.100	2.250	0.050	0.150	2.300	R13, R14
	R21	0.600	0.650	NF	0.600	0.750	NF	0.600	0.650	NF	0.600	0.700	NF	R24
F1	R12	0.050	0.100	NF	0.050	0.250	NF	0.050	0.100	NF	0.050	0.150	NF	R13, R14
	R21	0.600	0.650	2.900	0.600	0.750	3.000	0.600	0.650	2.900	0.600	0.700	2.950	R24
F2	***R12***	0.550	0.650	2.800	0.600	0.750	2.900	0.550	0.650	2.800	0.550	0.700	2.850	R13, R14
	R21	0.050	0.100	NF	0.050	0.250	NF	0.050	0.100	NF	0.050	0.150	NF	R24
F2	R12	0.550	0.650	NF	0.600	0.750	NF	0.550	0.650	NF	0.550	0.700	NF	R13, R14
	R21	0.050	0.100	2.350	0.050	0.250	2.500	0.050	0.100	2.350	0.050	0.150	2.400	R24
F3	***R13***	0.050	0.100	2.250	0.050	0.250	2.400	0.050	0.100	2.250	0.050	0.150	2.350	R12, R14
	R31	1.100	1.250	NF	1.150	1.400	NF	1.100	1.250	NF	1.150	1.300	NF	R34
F3	R13	0.050	0.100	NF	0.050	0.250	NF	0.050	0.100	NF	0.050	0.150	NF	R12, R14
	R31	1.100	1.250	3.450	1.150	1.400	3.600	1.100	1.250	3.450	1.150	1.300	3.500	R34
F4	***R13***	1.100	1.200	3.400	1.150	1.350	3.550	1.100	1.200	3.400	1.150	1.300	3.450	R12, R14
	R31	0.050	0.100	NF	0.050	0.300	NF	0.050	0.100	NF	0.050	0.200	NF	R34
F4	R13	1.100	1.200	NF	1.150	1.350	NF	1.100	1.200	NF	1.150	1.300	NF	R12, R14
	R31	0.050	0.100	2.300	0.050	0.300	2.500	0.050	0.100	2.300	0.050	0.200	2.400	R34

Table 4.7.- Performance of the circuit breaker failure protection against 0 Ω and 200 Ω fault conditions. [Part 2 of 3]

Fault	Relay	Pole-to-Ground Fault						Pole-to-Pole Fault						Neighbouring relays
		0 Ω			200 Ω			0 Ω			200 Ω			
		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		
			t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)	
F5	***R14***	0.050	0.100	2.250	0.050	1.150	2.400	0.050	0.100	2.250	0.050	0.150	2.350	R12, R13
	R41	1.100	1.250	NF	0.250	1.350	NF	1.100	1.250	NF	1.150	1.300	NF	R42, R43
F5	R14	0.050	0.100	NF	0.050	0.250	NF	0.050	0.100	NF	0.050	0.150	NF	R12, R13
	R41	1.100	1.250	3.450	1.150	1.350	3.600	1.100	1.250	3.450	1.150	1.300	3.500	R42, R43
F6	***R14***	1.100	1.200	3.400	1.150	1.350	3.500	1.100	1.200	3.400	1.150	1.300	3.450	R12, R13
	R41	0.050	0.100	NF	0.050	0.250	NF	0.050	0.100	NF	0.050	0.200	NF	R42, R43
F6	R14	1.100	1.200	NF	1.150	1.350	NF	1.100	1.200	NF	1.150	1.300	NF	R12, R13
	R41	0.050	0.100	2.300	0.050	0.250	2.450	0.050	0.100	2.300	0.050	0.200	2.400	R42, R43
F7	***R24***	0.050	0.100	2.350	0.050	0.250	2.500	0.050	0.100	2.350	0.050	0.150	2.400	R21
	R42	0.850	0.950	NF	0.850	1.100	NF	0.850	0.950	NF	0.850	1.000	NF	R41, R43
F7	R24	0.050	0.100	NF	0.050	0.250	NF	0.050	0.100	NF	0.050	0.150	NF	R21
	R42	0.850	0.950	3.150	0.850	1.100	3.300	0.850	0.950	3.150	0.850	1.000	3.200	R41, R43
F8	***R24***	0.850	0.950	3.200	0.850	1.050	3.300	0.850	0.950	3.200	0.850	1.000	3.250	R21
	R42	0.050	0.050	NF	0.050	0.300	NF	0.050	0.100	NF	0.050	0.150	NF	R41, R43
F8	R24	0.850	0.950	NF	0.850	1.050	NF	0.850	0.950	NF	0.850	1.000	NF	R21
	R42	0.050	0.100	2.300	0.050	0.300	2.500	0.010	0.100	2.300	0.050	0.150	2.400	R41, R43

Table 4.7.- Performance of the circuit breaker failure protection against 0 Ω and 200 Ω fault conditions. [Part 3 of 3]

Fault	Relay	Pole-to-Ground Fault						Pole-to-Pole Fault						Neighbouring relays
		0 Ω			200 Ω			0 Ω			200 Ω			
		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		Primary t_{Pd} (ms)	CB failure		
			t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)		t_{CBFi} (ms)	t_{CBFd} (ms)	
F9	***R34***	0.050	0.100	2.300	0.050	0.300	2.500	0.010	0.100	2.300	0.050	0.150	2.400	R31
	R43	0.550	0.650	NF	0.600	0.750	NF	0.550	0.650	NF	0.550	0.550	NF	R41, R42
F9	R34	0.050	0.100	NF	0.050	0.300	NF	0.010	0.100	NF	0.050	0.150	NF	R31
	R43	0.550	0.650	2.850	0.600	0.750	3.000	0.550	0.650	2.850	0.550	0.750	2.950	R41, R42
F10	***R34***	0.600	0.650	2.850	0.600	0.750	3.000	0.600	0.650	2.850	0.600	0.700	2.950	R31
	R43	0.050	0.100	NF	0.050	0.300	NF	0.050	0.100	NF	0.050	0.200	NF	R41, R42
F10	R34	0.600	0.650	NF	0.600	0.750	NF	0.600	0.650	NF	0.600	0.700	NF	R31
	R43	0.050	0.100	2.300	0.050	0.300	2.500	0.050	0.100	2.300	0.050	0.200	2.400	R41, R42

4.4. Influence of parameters in the LIVRD protection scheme

This subsection analyses the influence of relevant parameters in the performance of the LIVRD fault protection algorithms. The analysed parameters are:

- Size of the limiting inductor
- Sampling frequency employed in the derivative calculation
- Fault location
- Noise disturbance

This way, the LIVRD protection scheme is evaluated by analysing how the variation of the mentioned parameters affects its performance.

4.4.1. Influence of the limiting inductor size

To study the influence of the inductor size, fault F1 is applied at 1 ms while the inductance size varies between 100 and 150 mH. According to Figure 4.1, fault F1 is located at the beginning of link 12 from Bus 1, thus, it is within the limits of the protection zone covered by relays R12 and R21. Fault F1 is detected as a close-up fault by relay R12 while it is detected as a remote fault by relay R21. The fault case is also simulated varying the fault type and fault resistance.

Figure 4.28 presents the VR and VRD curves related to a PtP fault for both a solid (Figure 4.28-a) and a 200 Ω fault (Figure 4.28-b) while varying the size of the limiting inductor. Measurements taken by relay R12 are represented by solid lines and measurements taken by relay R21 are represented by dot-dashed lines. Threshold values are depicted by dotted lines.

The VR-related threshold value THR_1 is 0.95 for both relays while the VRD-related threshold value THR_3 is -1065 for R12 and -1000 for R21. Threshold values THR_3 are superimposed in the figures due to the figure scale. Similarly, Figure 4.29 presents the VR and VRD curves related to a PtG fault for both a solid (Figure 4.29-a) and a 200 Ω fault (Figure 4.29-b) while varying the size of the limiting inductor. Table 4.8 summarizes the fault detection time of the link primary and backup protections for each simulated case.

As it is shown in Figure 4.28 and Figure 4.29, all curves are superimposed regardless of the fault type and fault resistance. Moreover, fault detection time of the link primary protection does not vary regardless of the inductor size or the fault

features as it is indicated in Table 4.8. Then, the influence of the variation of the size of the limiting inductor on the link primary protection can be considered negligible.

Table 4.8.- Fault detection time by link primary and backup protections regarding variation of the inductor size.

Inductor size	**Fault F1**		**R12** t_{Pd} **(ms)**	**R21** t_{Pd} **(ms)**	**R13** t_{BUd} **(ms)**
	Fault Type	**Fault Resistance**			
100 mH	PtG	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.250
	PtP	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.150
110 mH	PtG	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.250
	PtP	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.150
120 mH	PtG	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.300
	PtP	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.150
130 mH	PtG	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.300
	PtP	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.200
140 mH	PtG	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.300
	PtP	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.200
150 mH	PtG	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.350
	PtP	0 Ω	0.050	0.600	0.100
		200 Ω	0.050	0.600	0.200

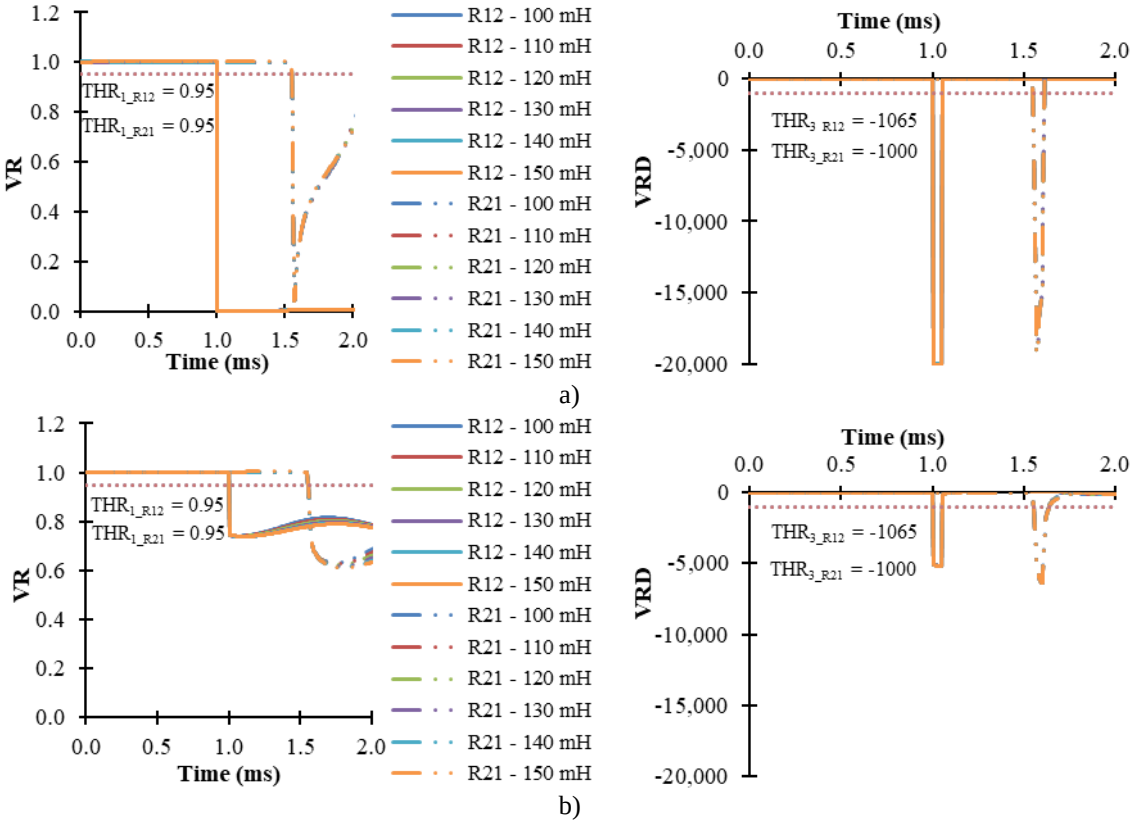


Figure 4.28.- VR and VRD signals measured by relays R12 and R21 for a) solid and b) 200 Ω PtP fault (F1) with inductance variation (100 to 150 mH).

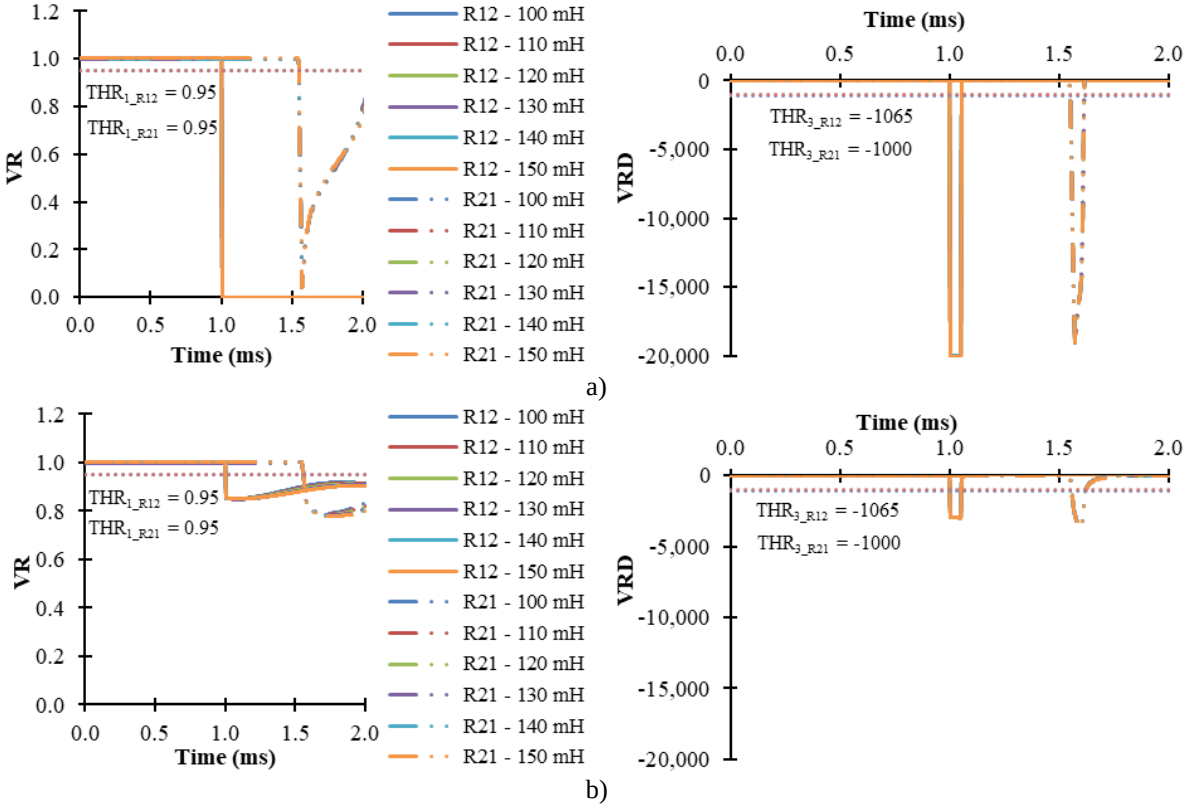


Figure 4.29.- VR and VRD signals measured by relays R12 and R21 for a) solid and b) 200 Ω PtG fault (F1) with inductance variation (100 to 150 mH).

On the other hand, Figure 4.30 and Figure 4.31 show VR and VRD signals measured by relay R13 which, together with relay R14, covers the link backup protection and circuit breaker failure protection in case of malfunction of R12 or DC-CB12.

Figure 4.30 presents the VR and VRD curves related to a PtP fault for both a solid (Figure 4.30-a) and a 200 Ω fault (Figure 4.30-b) while varying the size of the limiting inductor.

Similarly, Figure 4.31 presents the VR and VRD curves related to a PtG fault for both a solid (Figure 4.31-a) and a 200 Ω fault (Figure 4.31-b) while varying the size of the limiting inductor.

As it is shown in Figure 4.30 and Figure 4.31, the size of the limiting inductor affects the performance of the protection algorithms based on the reverse reach. A higher inductor size produces a greater attenuation in the measurements, which slows down fault detection speed, especially during high-resistance faults, as it can be seen in Table 4.8.

Therefore, since the link protection does not require a large inductor size, the LIVRD protection scheme can properly operate with a 100 mH inductor, which is a common inductor size for VSC-based grids according to the literature (subsection 2.6.5) and the review made in Chapter 2.

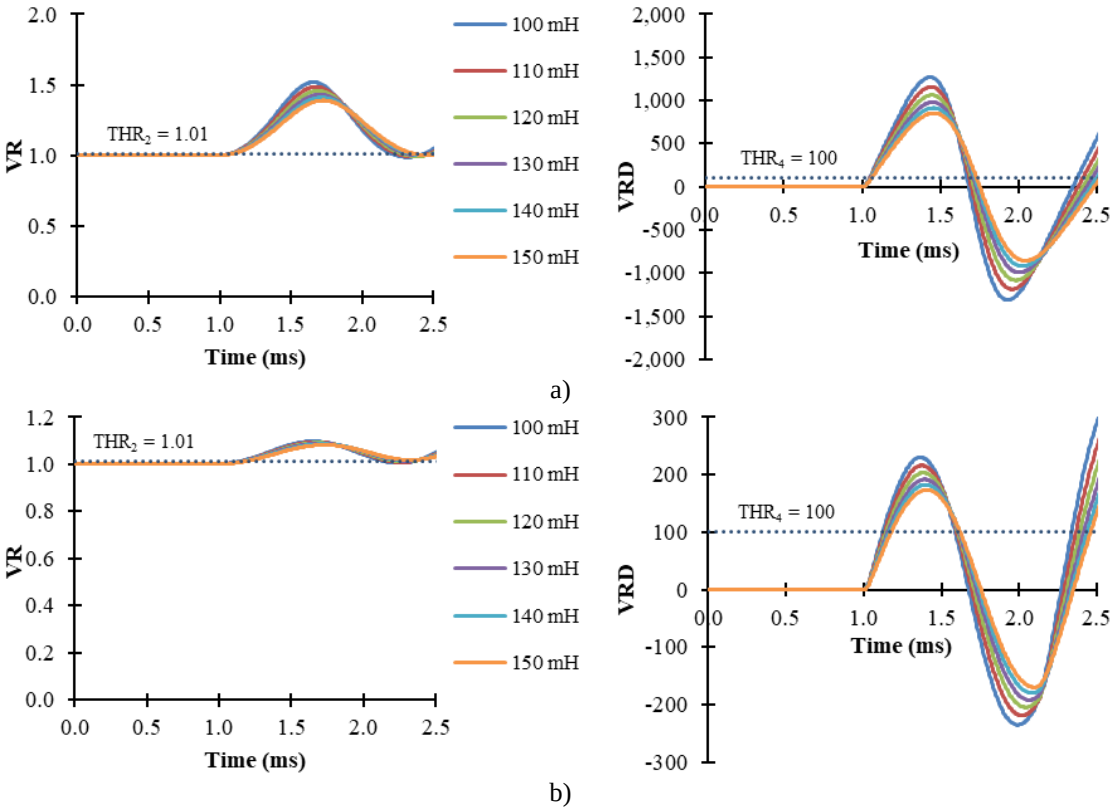


Figure 4.30.- VR and VRD signals measured by relay R13 for a) solid and b) 200 Ω PtP fault (F1) with inductance variation (100 to 150 mH).

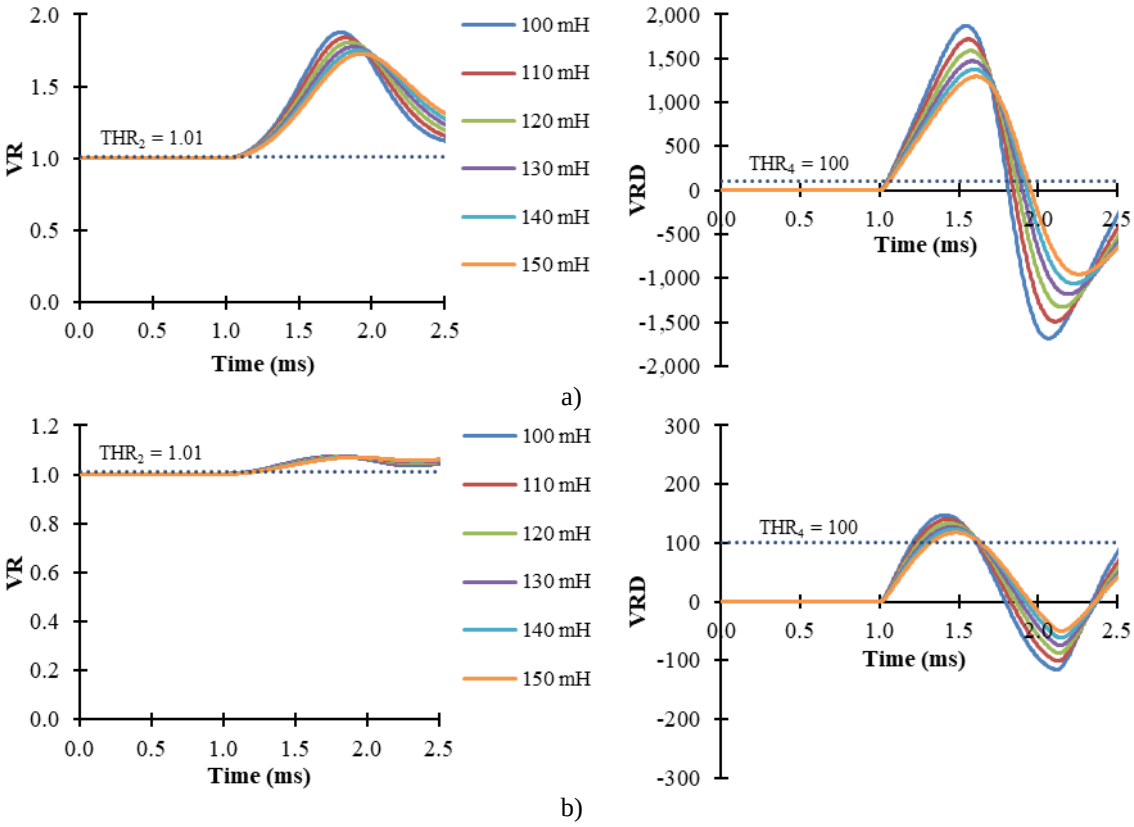


Figure 4.31.- VR and VRD signals measured by relay R13 for a) solid and b) 200 Ω PtG fault (F1) with inductance variation (100 to 150 mH).

4.4.2. Influence of the sampling frequency

Sampling frequency has a considerable effect on the VRD calculation, since the selected sampling frequency is a parameter directly employed in the calculation of the VRD (see equation (3.17)).

A higher sampling frequency produces a higher VRD value (in absolute terms) for the same VR variation, as it is shown in Figure 4.32 and Figure 4.33 for 10, 15, 20, 25 and 30 kHz sampling frequency values. Figure 4.32 is related to relay R12 for a close-up forward fault (F1) located within its protection zone while Figure 4.33 is related to relay R13 where F1 is detected as a backward fault. Fault is applied at 1 ms varying the fault type and the fault resistance.

This influence can benefit the link primary protection in terms of fault discrimination since it accentuates the difference of values between normal conditions (VRD is approximately zero), or external faults to the protection zone (VRD is positive), and the internal fault conditions (VRD presents a higher absolute value for a higher sampling frequency).

A higher fault resistance produces an attenuation in the fault-induced drop of the V_{link} and V_{bus}, which causes an important attenuation in both the VR and VRD

signals. This reduction in the VR variation can be compensated by increasing the sampling frequency, producing a higher VRD value for the reduced high-resistance fault-induced VR value, as it is shown in Figure 4.32. Therefore, a higher sampling frequency can make high-resistance faults, especially PtG-fault-induced signals which are more attenuated, easier to detect. However, a higher sampling frequency might produce a nuisance operation of the protection scheme due to misdetecting variations in the measured signal related to normal operation conditions as a fault condition.

The LIVRD algorithm achieves fault detection in the first sample after fault inception regardless of the sampling frequency, even though, a higher sampling frequency will cause faster fault detection due to the shorter time interval between samples.

On the other hand, a variation of the sampling frequency does not produce a significant effect on the link backup protection since the measurements taken by relay R13 are mostly superimposed as shown in Figure 4.33. Thus, the effect on the reverse reach of the relays can be considered negligible. Therefore, a relatively low sampling frequency of 20 kHz is appropriate for the LIVRD protection scheme.

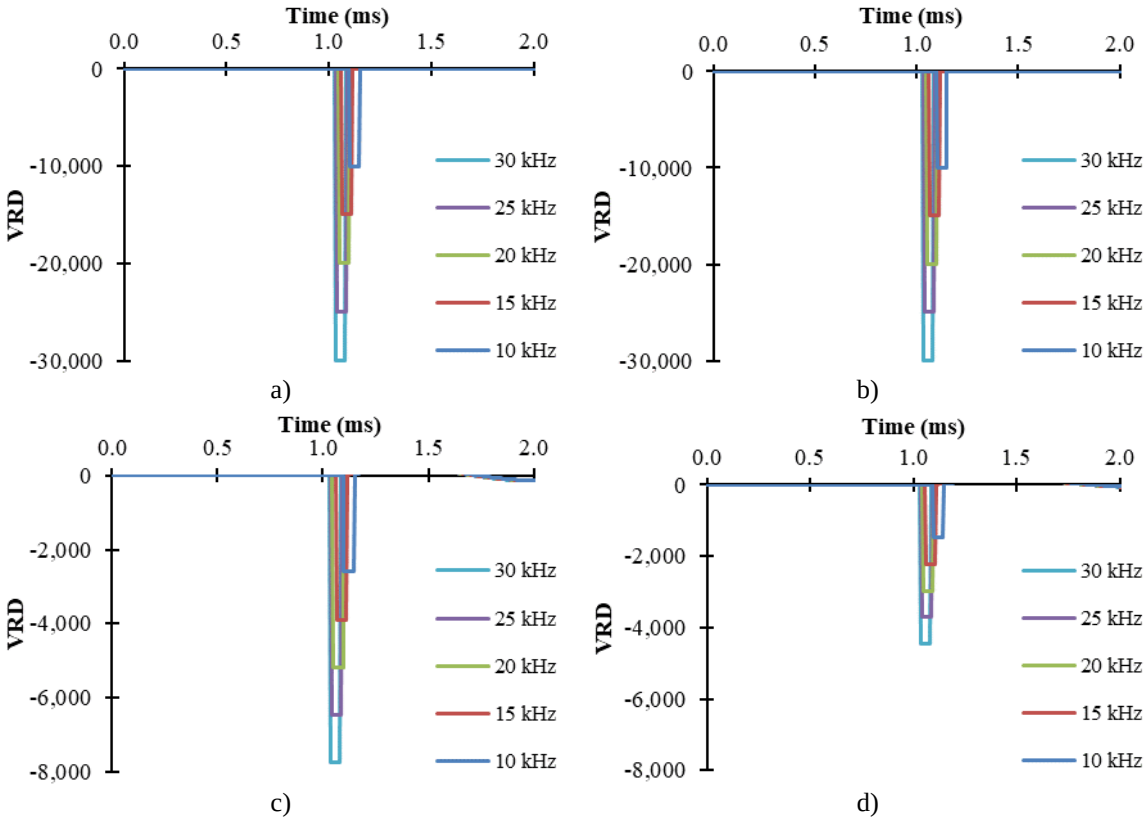


Figure 4.32.- VRD signals measured by relay R12 for a) solid PtP fault, b) solid PtG fault, c) 200 Ω PtP fault and d) 200 Ω PtG fault (F1) with sampling frequency variation (10 to 30 kHz).

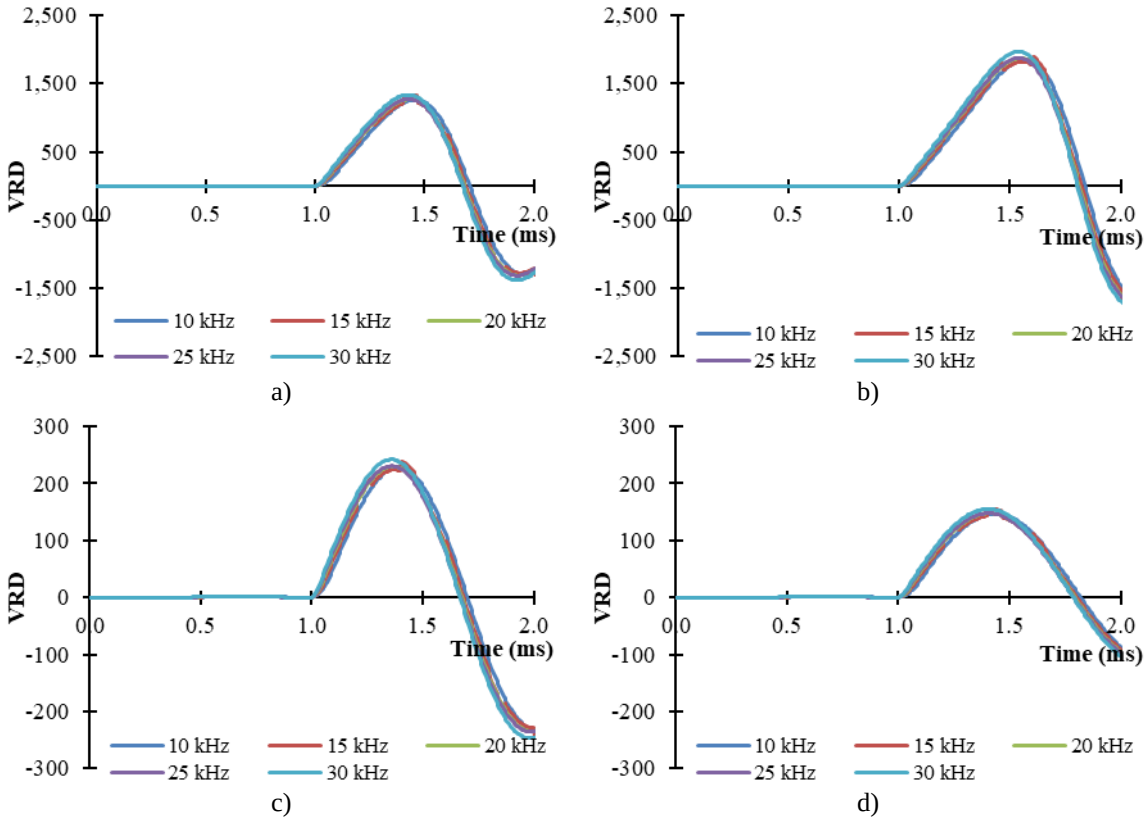


Figure 4.33.- VRD signals measured by relay R13 for a) solid PtP fault, b) solid PtG fault, c) 200 Ω PtP fault and d) 200 Ω PtG fault (F1) with sampling frequency variation (10 to 30 kHz).

4.4.3. Influence of the fault location

Another important aspect to analyse is the effect of the fault location in the performance of the protection scheme. The analysis is performed for fault case F2 and the analysed measurements are those related to relays R12 and R13, as in previous subsections.

Fault F2 is a remote fault and it is applied at t=1 ms while varying the cable length and, hence, the fault location between 50 to 500 km from the end where relay R12 is placed. The fault scenario is also simulated varying the fault type and the fault resistance. VR and VRD measurements from relay R12 are shown in Figure 4.34 and Figure 4.35 while VR and VRD measurements from relay R13 are presented in Figure 4.36 and Figure 4.37. Figure 4.34 and Figure 4.36 depict the measurements of relays R12 and R13 during a solid fault while Figure 4.35 and Figure 4.37 show the measurements taken during a 200 Ω fault.

It must be highlighted that only the first peak value of each VR and VRD wave is represented in the figures with a solid line while the rest of the curve is represented with a dotted line in order to allow a clearer display of the different curves.

A longer distance to fault affects the detection time of the protection scheme, due to the traveling wave delay. It also attenuates the voltage signals and, hence, the VR signal. The attenuation of the VR signals implies that its rate-of-change is less abrupt, then, the VRD is greatly affected by the distance to the fault. Therefore, fault conditions located at a longer distance might be challenging to detect, especially in case of high-resistance faults which are even more attenuated.

The LIVRD protection scheme can detect all the simulated solid faults (up to 500 km away from the relay point) regardless of the fault type while using the threshold values set in the selection process presented in subsection 4.2. However, these threshold values are not sensitive enough to detect high-resistance faults located at a distance higher than 300 km (Figure 4.35 and Figure 4.37), since the threshold selection process only took into account the longest cable length presented in the VSC-based system depicted in Figure 4.1, i.e., 200 km.

Therefore, if the proposed protection scheme needs to be implemented in a system with longer cable lengths, the threshold selection process should be obviously redone taking into account the new system characteristics. However, it could be the case that for very long distances the traveling wave induced by a remote internal fault might be more attenuated than the one induced by a close-up external fault. Thus, less sensitive threshold values would have to be selected in order to keep a selective operation and to avoid misoperation during close-up external faults. However, the fault protection algorithm would not be able to cover the complete cable length due to its reduced sensitivity.

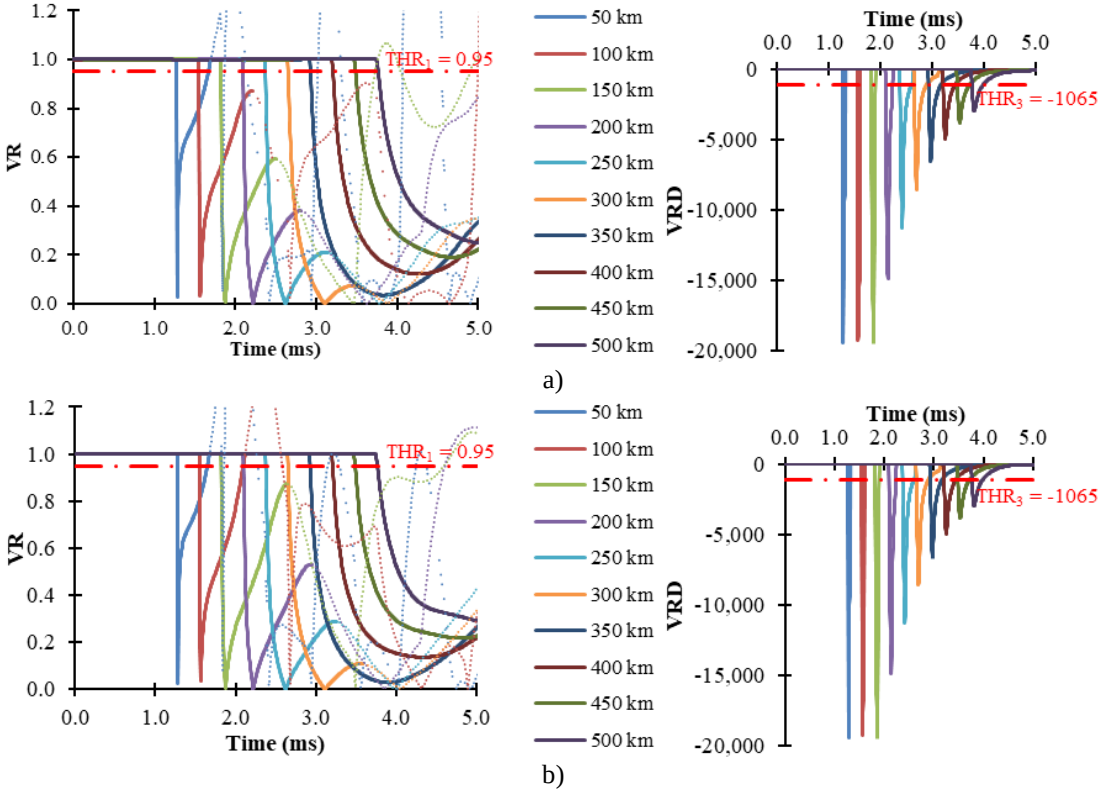


Figure 4.34.- VR and VRD signals measured by relay R12 for solid a) PtP fault and b) PtG fault (F2) with fault location variation (50 to 500 km).

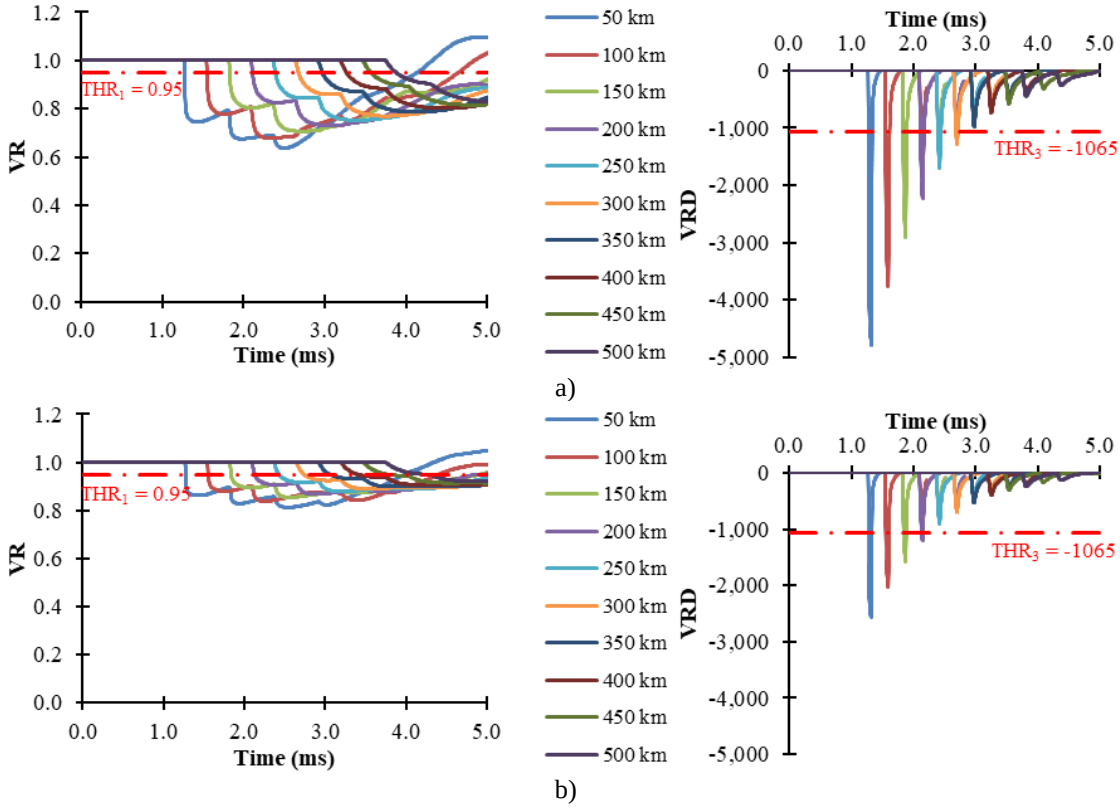


Figure 4.35.- VR and VRD signals measured by relay R12 for 200 Ω a) PtP fault and b) PtG fault (F2) with fault location variation (50 to 500 km).

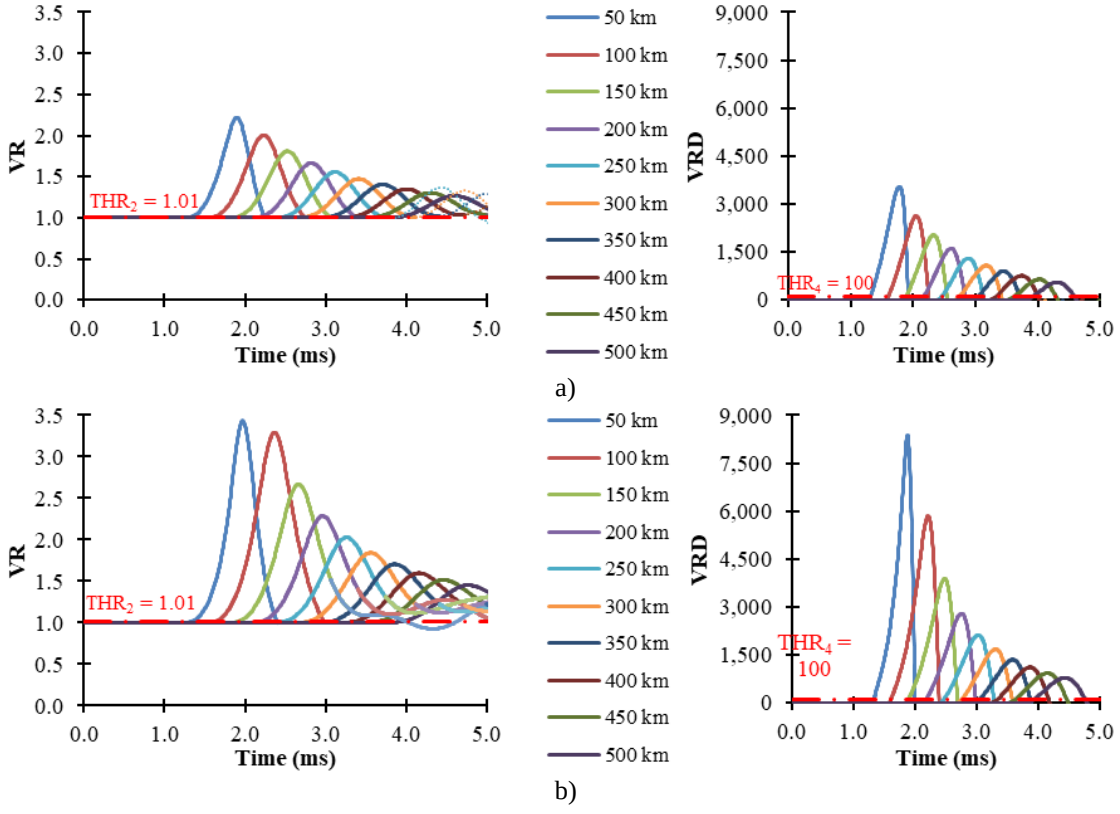


Figure 4.36.- VR and VRD signals measured by relay R13 for solid a) PtP fault and b) PtG fault (F2) with fault location variation (50 to 500 km).

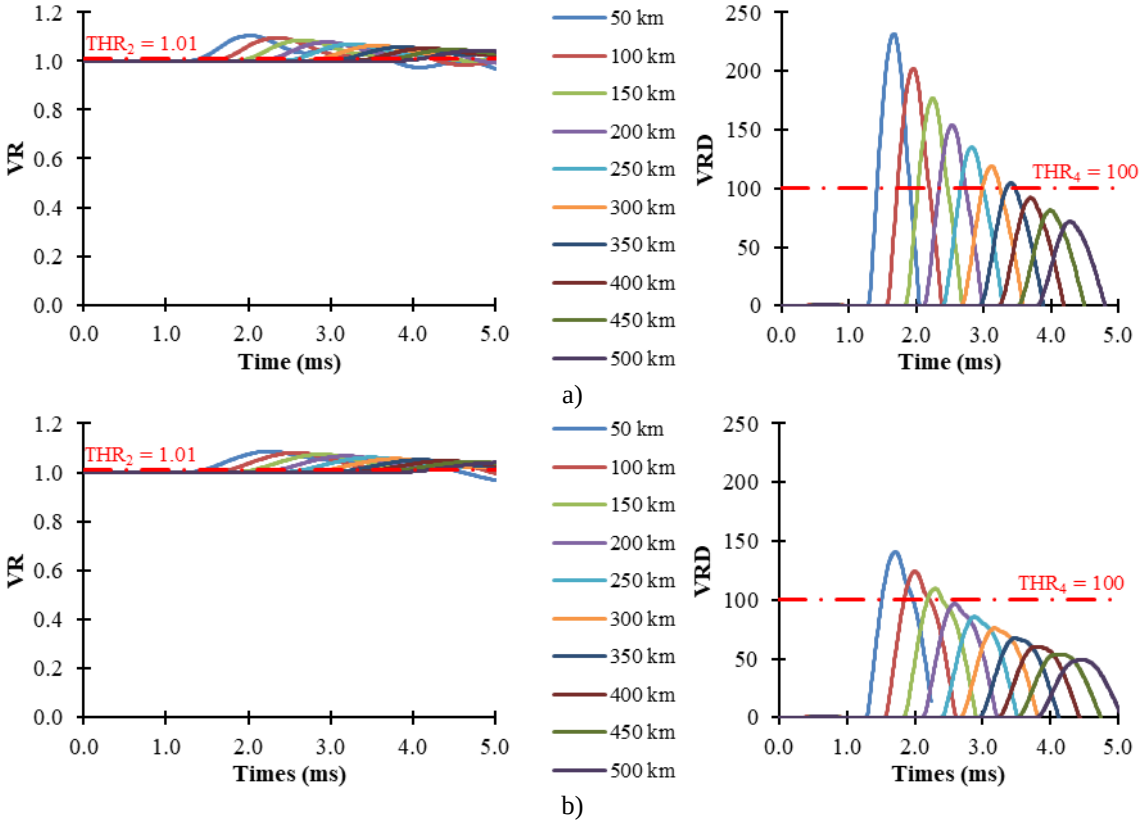


Figure 4.37.- VR and VRD signals measured by relay R13 for 200 Ω a) PtP fault and b) PtG fault (F2) with fault location variation (50 to 500 km).

4.4.4. Influence of the noise disturbance

All the analyses performed so far have supposed ideal measurements. However, in a real implementation the values measured have a noise component due to the non-ideal nature of the measurement devices. This way, the performance of the LIVRD protection scheme under noise disturbance conditions is analysed in this subsection.

Fault F1 located in link 12, right in front of relay R12 is simulated for a range of signal-to-noise ratios (SNR) of 30, 40, 50, 60, 70 and 80 dB. The SNR is a parameter that compares the desired signal power to the background noise power. Thus, a low SNR means a higher level of noise in relation to the signal.

The range of SNRs employed in this subsection has been selected according to other similar analyses found in the literature [71], [207], [227], [228].

Fault inception is at t=1 ms. This fault is selected as a worst case scenario since it is located at the end of the protection zone for relay R21 and it can produce a nuisance operation of the neighbouring external relays located at Bus 1. Both solid as well as 200 Ω PtP and PtG faults are simulated.

The following figures show VR and VRD curves with SNR from 30 to 80 dB. Figure 4.38 and Figure 4.39 correspond to relay R12. Figure 4.40 and Figure 4.41 correspond to relay R21. Figure 4.42 and Figure 4.43 correspond to relay R13. These figures also show additional graphics with zoom in the pre-fault regime of the simulations in order to present a better visualization of the influence of the noise disturbance.

As it can be seen, the VRD measurement is more impacted by the noise disturbance than the VR one since derivative calculations are more affected by the alterations in the ideal signal; these abrupt changes are easily detected by derivative calculations so it might produce a nuisance protection operation. Relays R12 and R21 are able to properly detect the fault under all the simulated fault cases with a SNR above 40 dB. During normal conditions, VR and VRD values do not satisfy the fault detection conditions while the fault is quickly detected after fault inception. However, a SNR of 30 dB causes the fulfilment of the fault detection criteria during normal operation conditions, thus, a nuisance operation might take place.

Moreover, the noise disturbance does not significantly affect the fault detection time of the link primary protection as it can be seen in Table 4.9. The fault detection time does not vary since the sharp fault-induced voltage drop is not significantly affected by the noise disturbance as it is depicted in the figures.

Table 4.9.- Analysis of the fault detection time (in milliseconds) of the link primary protection during noise disturbances.

Relay	**SNR (dB)**	**Pole-to-Ground Fault**		**Pole-to-Ground Fault**	
		0 Ω	**200 Ω**	**0 Ω**	**200 Ω**
R12	**without noise**	0.050	0.050	0.050	0.050
	40	0.050	0.050	0.050	0.050
	50	0.050	0.050	0.050	0.050
	60	0.050	0.050	0.050	0.050
	70	0.050	0.050	0.050	0.050
	80	0.050	0.050	0.050	0.050
R21	**without noise**	0.600	0.600	0.600	0.600
	40	0.600	0.600	0.600	0.600
	50	0.600	0.600	0.600	0.600
	60	0.600	0.600	0.600	0.600
	70	0.600	0.600	0.600	0.600
	80	0.600	0.600	0.600	0.600

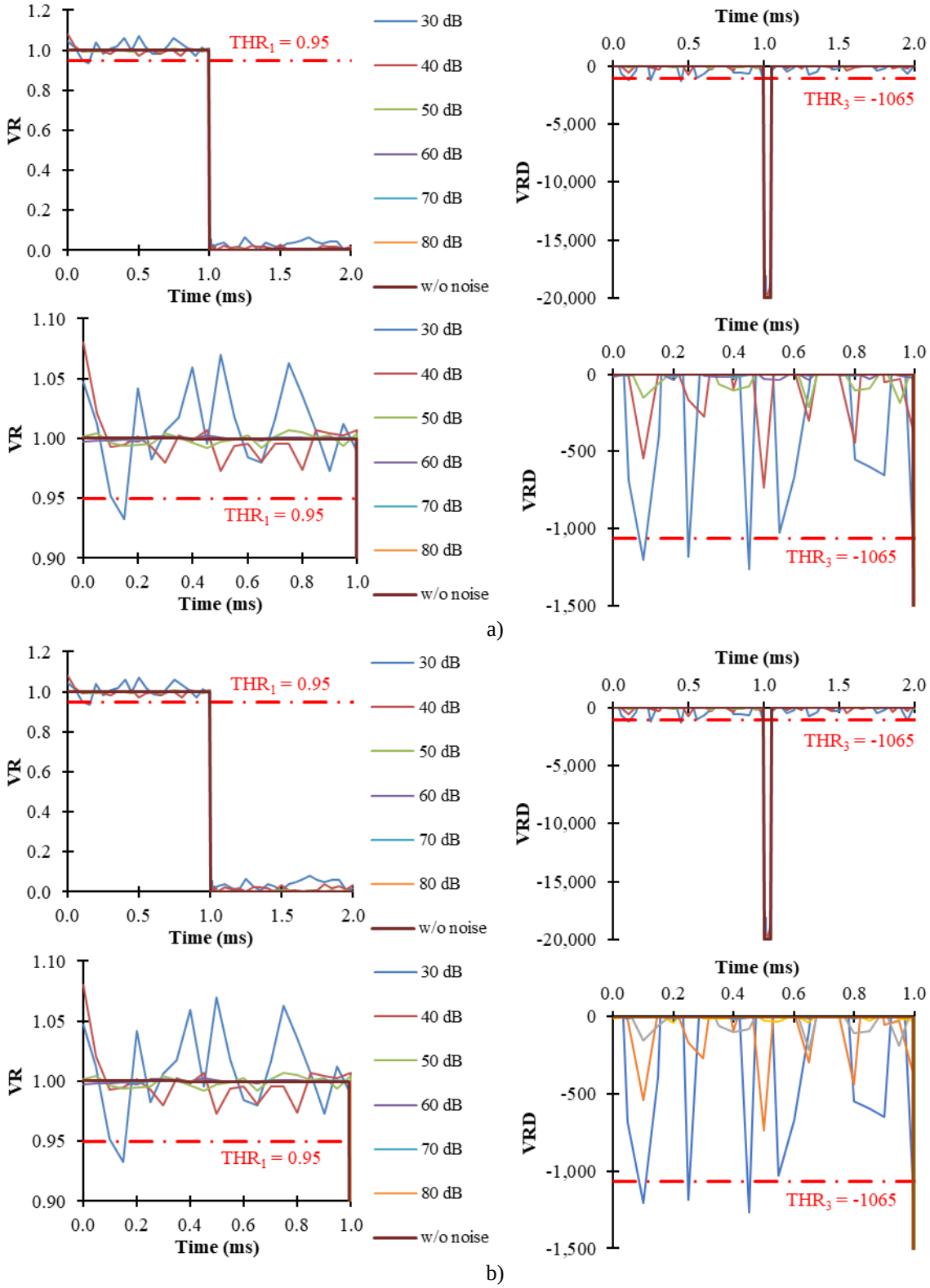


Figure 4.38.- VR and VRD signals measured by relay R12 for solid a) PtP fault and b) PtG fault (F1) with noise disturbance variation (30 to 80 dB).

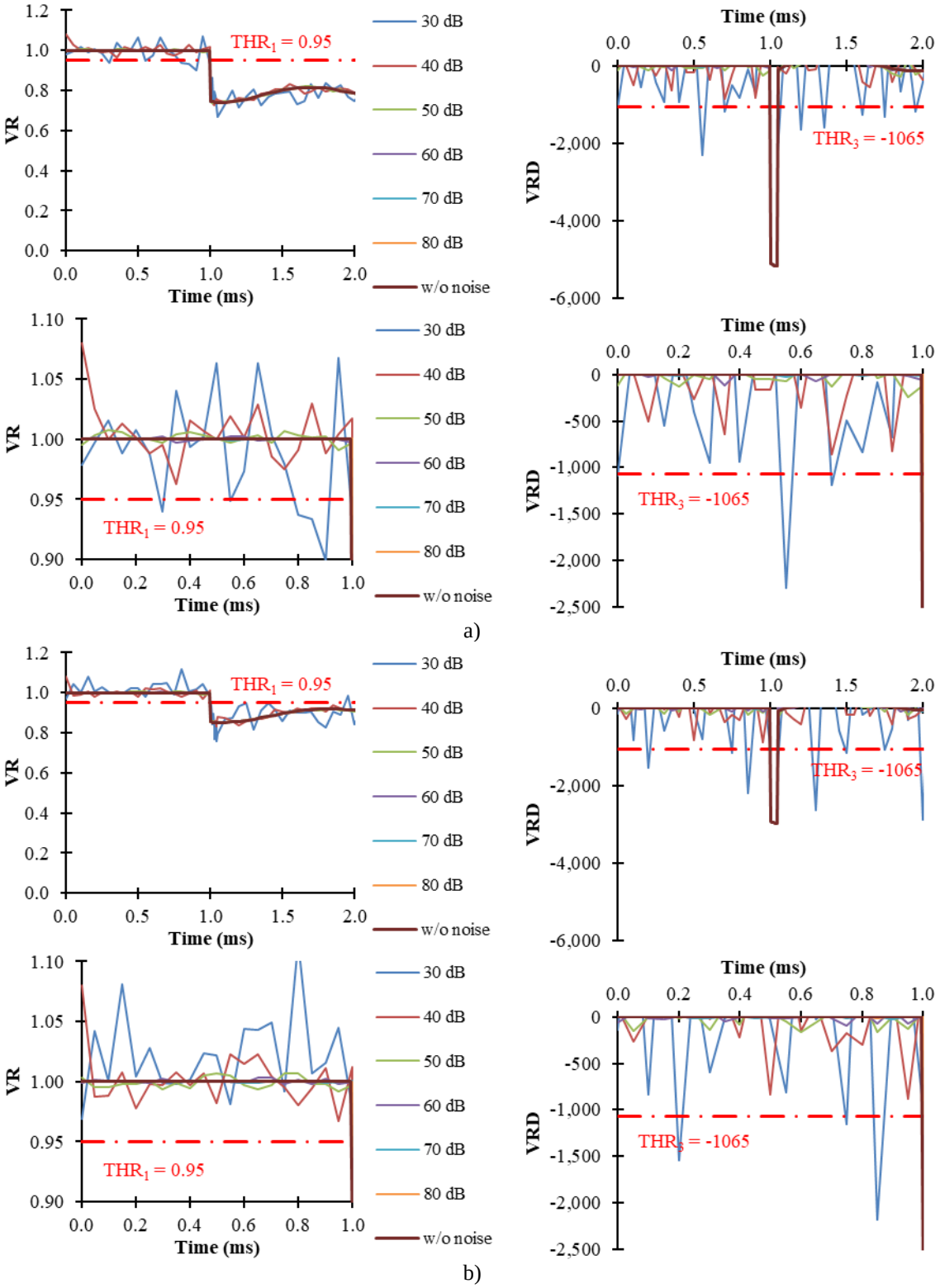


Figure 4.39.- VR and VRD signals measured by relay R12 for 200 Ω a) PtP fault and b) PtG fault (F1) with noise disturbance variation (30 to 80 dB).

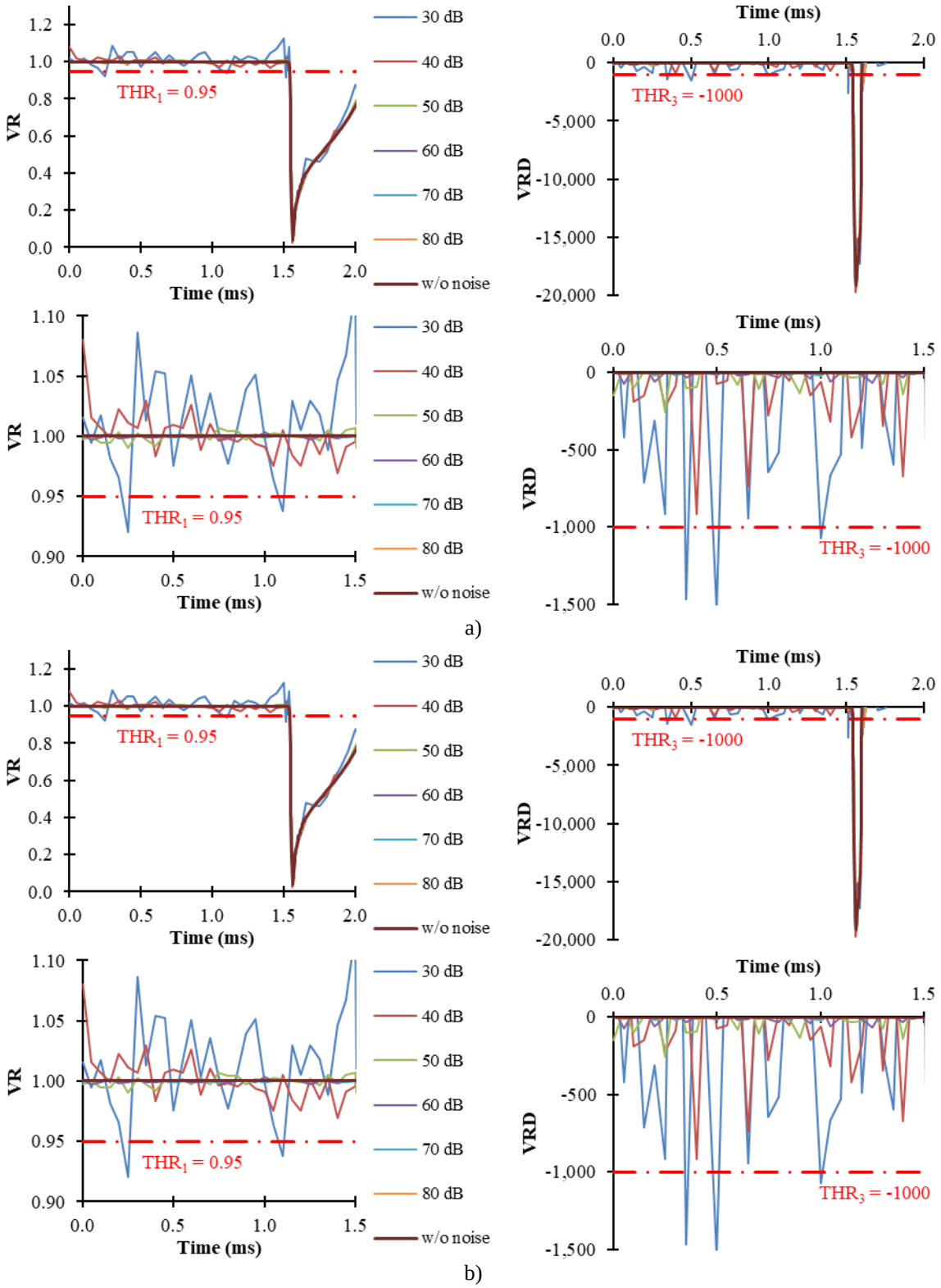


Figure 4.40.- VR and VRD signals measured by relay R21 for solid a) PtP fault and b) PtG fault (F1) with noise disturbance variation (30 to 80 dB).

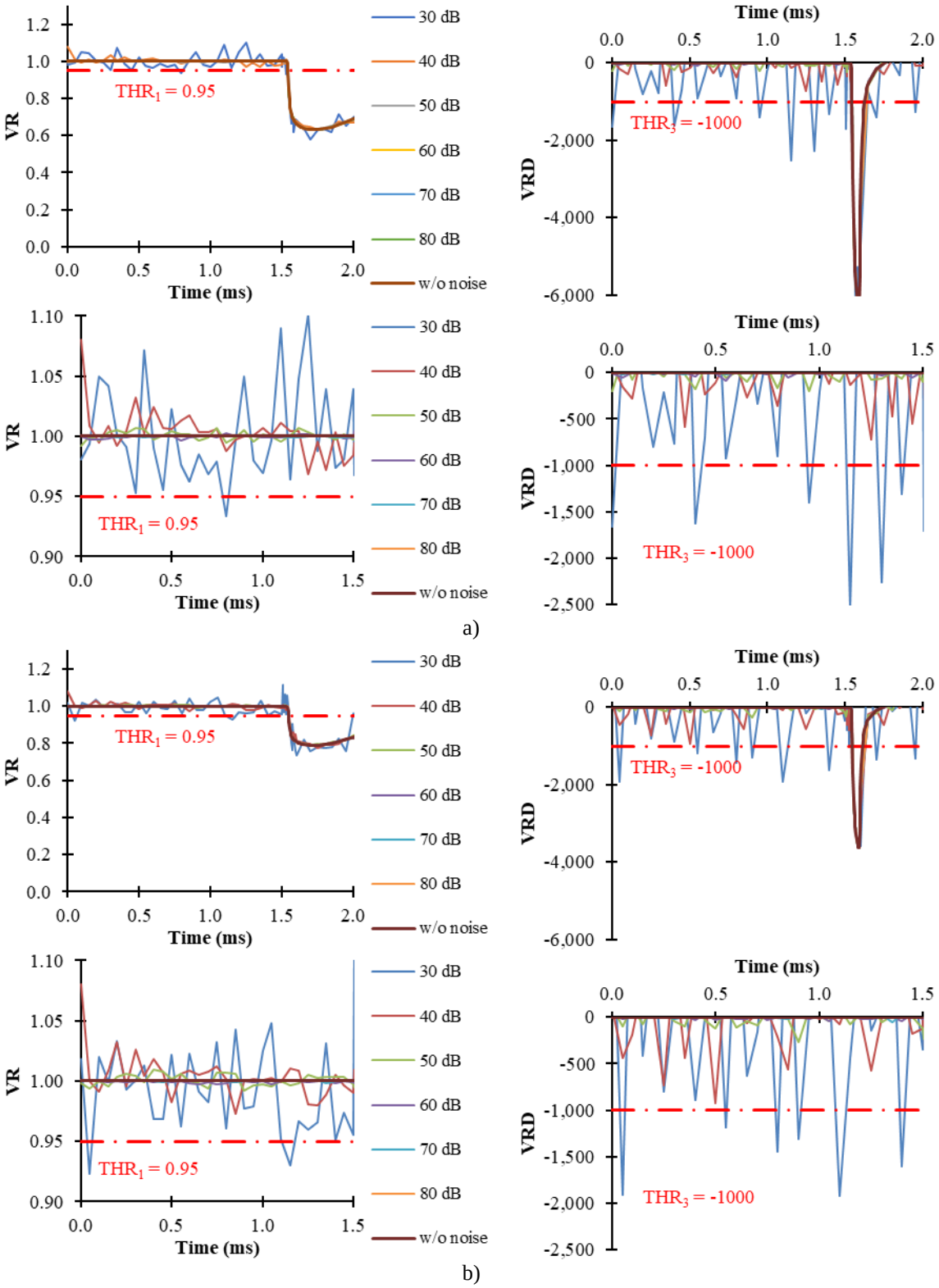


Figure 4.41.- VR and VRD signals measured by relay R21 for 200 Ω a) PtP fault and b) PtG fault (F1) with noise disturbance variation (30 to 80 dB).

On the other hand, no nuisance operation of the neighbouring relay R13 at Bus 1 as link primary protection occurs for SNRs above 40 dB, as it is represented in Figure 4.42 and Figure 4.43. The link primary protection of relay R13, which covers link faults in link 13, is selective enough to not improperly detect fault F1 as a forward fault in link 13 for SNRs above 40 dB. However, nuisance operation might happen for a SNR of 30 dB.

Conversely, the VRD calculation of the link backup protection of relay R13 is significantly affected by the noise disturbance for a SNR of 30 and 40 dB and a nuisance operation might occur. However, the link backup protection properly operates for SNRs of 50 dB or higher. This way, relay R13 acting as link backup protection, which covers link faults in link 12 during failure of relay R12, is able to detect fault F1.

According to this, the proposed link primary protection presents proper operation under noise disturbances over a SNR of 40 dB while the algorithms based on the reverse reach, i.e., link backup, busbar and circuit breaker failure protection, do it under SNRs of 50 dB or higher. The LIVRD protection scheme presents some problems in its operation when the SNR is lower than these values. The proposed protection scheme could be adapted to lower SNR values by selecting higher threshold values which will enhance its selectivity or by employing filters. However, proper performance for the mentioned SNRs is in line with other results found in the literature [71], [207], [227], [228].

4.5. Conclusion

In this chapter, the performance of the LIVRD protection scheme proposed in this thesis has been analysed and validated through simulations in PSCAD against different fault case scenarios. Additionally, a methodology for the selection of the threshold values, taking into account the worst fault case scenarios, has been elaborated. The selected threshold values ensure the proper operation of the proposed LIVRD protection scheme against fault conditions with resistances up to 200 Ω.

The results of the evaluation show how the novel LIVRD protection algorithms allow to create a protection scheme for MTDC grids that is fast, selective and reliable.

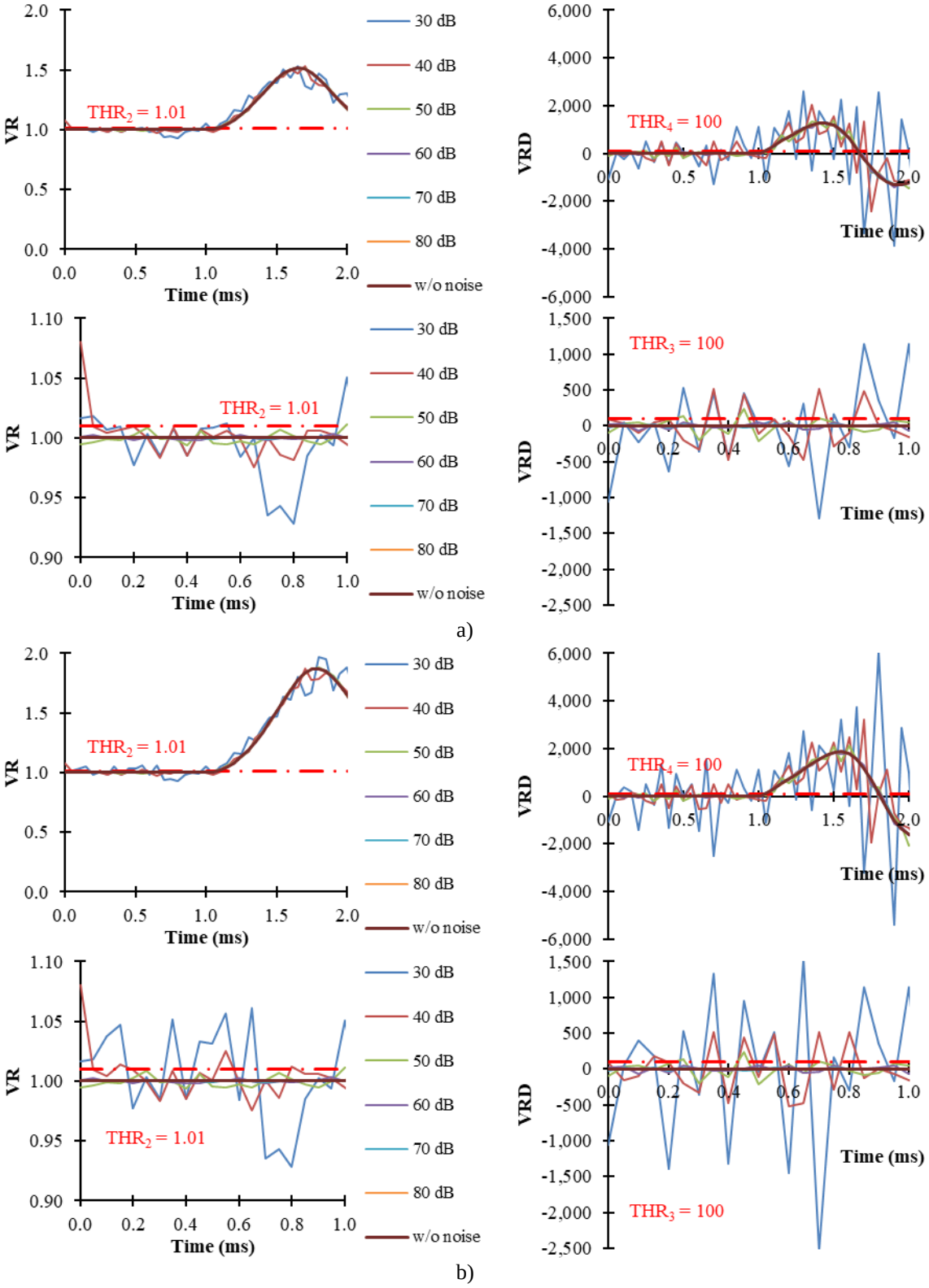


Figure 4.42.- VR and VRD signals measured by relay R13 for solid a) PtP fault and b) PtG fault (F1) with noise disturbance variation (30 to 80 dB).

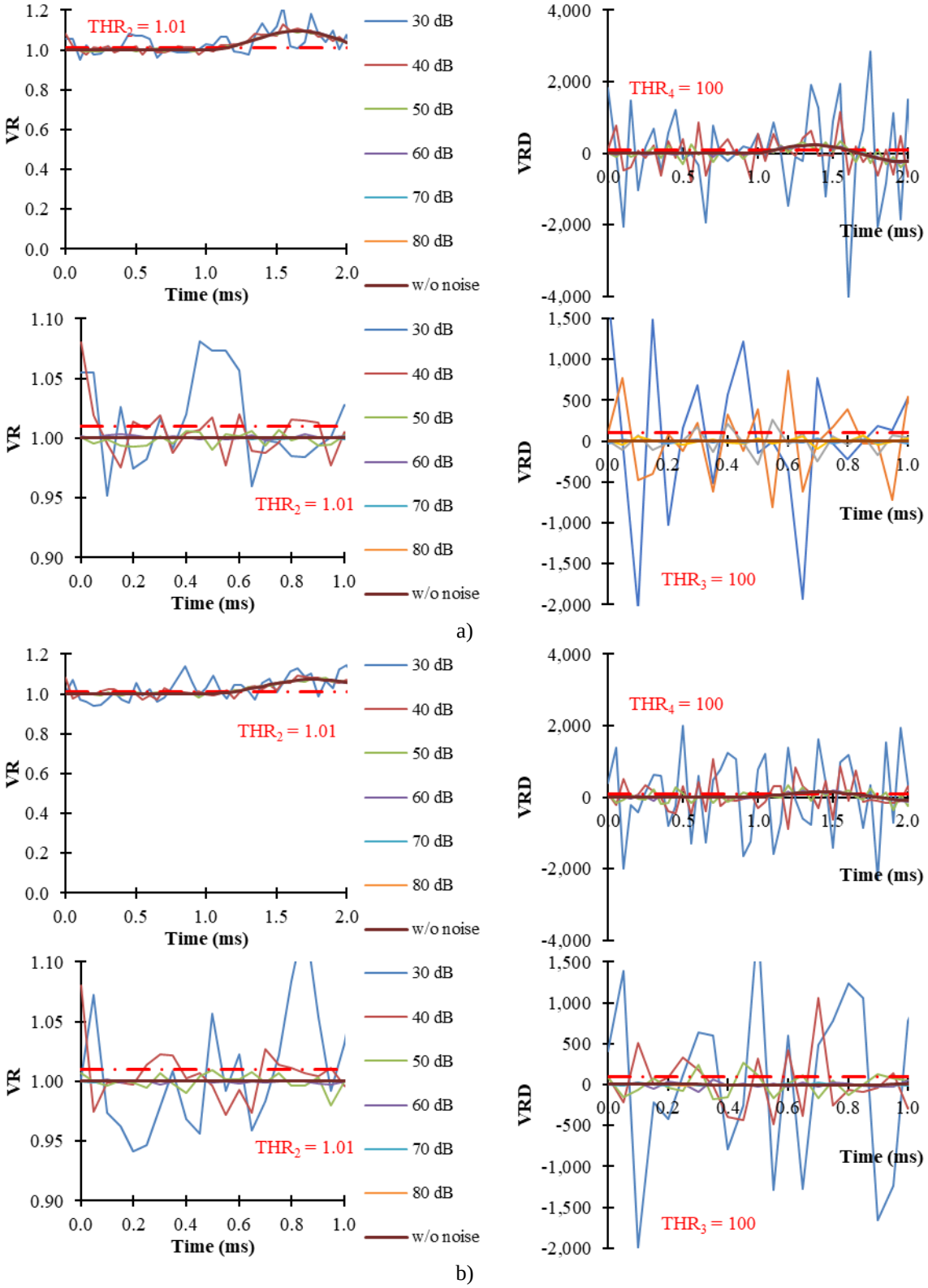


Figure 4.43.- VR and VRD signals measured by relay R13 for 200 Ω a) PtP fault and b) PtG fault (F1) with noise disturbance variation (30 to 80 dB).

The influence of important parameters such as the inductor size, the sampling frequency, the fault location and the noise disturbance has been evaluated. The effect of the inductor size is negligible while the effects of the fault resistance and sampling frequency are significant. The fault location also affects the operation but increasing the sampling frequency can adapt the proposed protection scheme to longer distances to fault. The performance of the proposed protection scheme has also been validated for SNRs over 40 dB for the link primary protection and over 50 dB for the reverse-reach-based protections, i.e., link backup, busbar and circuit breaker failure protections.

Moreover, the LIVRD protection scheme presents a fast fault detection capability in the range of a few microseconds for close-up fault conditions thanks to the VRD algorithm. Besides, the proposed protection scheme employs the VR algorithm to provide directionality and to enable fault discrimination. This way, faults can be detected in the backward and forward direction and, thus, link backup protection using the reverse reach of the relays can be achieved. Fault discrimination is also quickly achieved since only local voltage measurements are used. In addition, the proposed protection scheme properly operates against faults with a resistance up to 200 Ω and can be adapted to detection of higher fault resistances by recalculating the threshold values.

In summary, the advantageous characteristics of the LIVRD protection scheme are fast fault detection and discrimination, sensitive operation against high-resistance faults in addition to the adaptability to even higher fault resistances as well as longer distances to fault. Moreover, the proper operation is demonstrated by using only local voltage measurements, a relatively low sampling frequency and a common limiting inductor size, i.e., 20 kHz and 100 mH, respectively.

Chapter 5.

COMPARISON OF THE LIVRD ALGORITHM WITH EXISTING PROTECTION ALGORITHMS

The characteristics of the novel LIVRD protection algorithms proposed in this thesis are examined in this chapter by comparing it with existing algorithms commonly found in the literature. Since the LIVRD algorithm is a local-measurement-based algorithm, other existing local-measurement-based algorithms are employed in the analysis, i.e., overcurrent, undervoltage, rate-of-change-of-current, rate-of-change-of-voltage and inductor-voltage algorithms. Additionally, the novel LIVRD circuit breaker failure protection is compared with a conventional circuit breaker failure protection. Operation speed and high-resistance fault detection capability are compared and evaluated. This way, suitability to VSC-based grids is demonstrated. This comparison employs results extracted from PSCAD simulations. Therefore, this section highlights the advantageous characteristics of the novel LIVRD protection scheme.

The work presented in this chapter has been published in:

M. J. Pérez-Molina, D. M. Larruskain, P. Eguia Lopez, O. Abarrategi and M. Santos-Mugica, "A comparison of non-unit and unit protection algorithms for HVDC grids", in AEIT HVDC International Conference 2019, Florence, Italy, 9-10 May 2019.

M. J. Pérez-Molina, P. Eguia-Lopez, D. M. Larruskain-Eskobal, M. Santos-Mugica and R. Rodriguez-Sanchez, "Evaluation of an overcurrent and undervoltage protection algorithm for HVDC systems", in 17th International Conference on Renewable Energies and Power Quality (ICREPQ'19), La Laguna, Tenerife, Spain, 10-12 April 2019.

M. J. Pérez Molina, D. M. Larruskain, P. Eguía López and A. Etxegarai, "Analysis of Local Measurement-Based Algorithms for Fault Detection in a Multi-Terminal HVDC Grid", Energies, vol. 12, (24), 2019.

M. J. Pérez-Molina, P. Eguía-Lopez, D. M. Larruskain, M. Santos Mugica and R. Rodriguez-Sanchez, "Evaluation of a Local Fault Detection Algorithm for HVDC Systems", Renewable Energy and Power Quality Journal, vol. 17, pp. 262-267, 2019.

M. J. Pérez Molina, P. Eguia Lopez, D. M. Larruskain, A. Etxegarai and S. Apiñaniz-Apiñaniz, "Fault detection based on ROCOV in a multi-terminal HVDC grid", in 18th International Conference on Renewable Energies and Power Quality (ICREPQ'20), Granada, Spain, 2-4 September 2020.

M. J. Pérez Molina, D. M. Larruskain Escobal, P. Eguia Lopez and V. Valverde Santiago, "Fault detection based on ROCOV and ROCOC for multi-terminal HVDC systems", in 20th IEEE Mediterranean Electrotechnical Conference (MELECON 2020), Palermo, Italy, 16-18 June 2020, pp. 506-511.

M. J. Pérez-Molina, P. Eguia, D. M. Larruskain, G. Buigues and E. Torres, "Non-unit ROCOV scheme for protection of multi-terminal HVDC systems", in 22nd European Conference on Power Electronics and Applications (EPE ECCE Europe 2020), Lyon, France, 7-11 September 2020.

M. J. Pérez-Molina, D. M. Larruskain, P. Eguia and O. Abarrategi, "Circuit Breaker Failure Protection Strategy for HVDC Grids", Energies, vol. 14, (14), 2021.

M. J. Pérez-Molina, D. M. Larruskain, P. Eguia and V. Valverde, "Local derivative-based fault detection for HVDC grids", IEEE Transactions on Industry Applications, vol. 58, (2), pp. 1521-1530, 2022.

M. J. Pérez-Molina, P. Eguia Lopez, D. M. Larruskain, A. Etxegarai and S. Apiñaniz-Apiñaniz, "Non-unit fault detection in Multiterminal HVDC grids", in Trends in Renewable Energies and Power Quality, M. Perez-Donsion and G. Vitale, Eds. Newcastle, UK: Cambridge Scholars Publishing. (to be published)

M. J. Pérez-Molina, P. Eguia, D. M. Larruskain, G. Buigues and E. Torres, "Performance of a protection system for DC grids", in 20th International

Conference on Renewable Energies and Power Quality (ICREPQ'22), Vigo, Spain, 27-29 July 2022. (accepted)

M. J. Perez-Molina, P. Eguia, D. M. Larruskain, E. Torres and J. C. Sarmiento-Vintimilla, "Single-ended limiting inductor voltage-ratio-derivative protection scheme for VSC-HVDC grids", International Journal of Electrical Power & Energy Systems (under review).

5.1. Link primary protection

In this section, the performance of the proposed LIVRD link primary protection algorithm, defined in section 3.3.1.1, is evaluated by comparing it with other existing algorithms. The comparison is focused in operation speed and high-resistance fault detection capability. Different algorithms are compared through PSCAD simulations.

The LIVRD algorithm proposed in this thesis is a local-measurement-based algorithm, in order to satisfy the speed requirement associated to VSC-based grids. Therefore, this section compares the proposed protection algorithm with other existing local-measurement-based algorithms, since they present the fastest fault detection speed. These algorithms are overcurrent, undervoltage, inductor-voltage, ROCOC and ROCOV.

The comparison is performed by simulating different fault cases in link 14 of the four-terminal grid depicted in Figure 4.1. Fault location varies between 0 and 200 km with increments of 25 km. These fault distances are measured from the end of link 14 next to Bus 1, e.g., a 25 km fault location means the fault is located at 25 km from relay R14 and at 175 km from relay R41. Moreover, the fault resistance is also varied between 0 Ω and 200 Ω with increments of 50 Ω. Additionally, both PtG and PtP faults are considered.

5.1.1. Overcurrent algorithm

The proposed LIVRD scheme is compared with the widely-used overcurrent algorithm, explained in subsection 2.6.1.1. The proposed LIVRD protection scheme employs in this comparison the threshold values which are presented in Table 4.1 while the OC algorithm uses a threshold value of 1.5 kA for all relays. The OC threshold value has been selected in order to ensure selectivity and sensitivity during its implementation in the four-terminal grid model. This way, relay R14 only operates against faults located inside its corresponding protection zone, i.e., faults F5 and F6 located in link 14, as it can be seen in Figure 5.1.

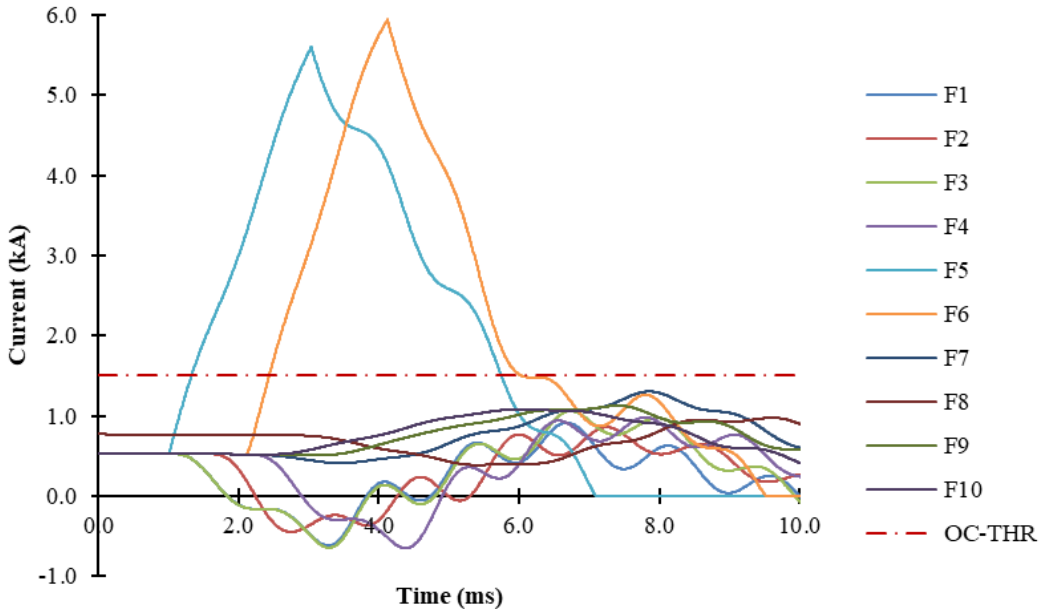


Figure 5.1.- Selection of threshold value for the OC algorithm (measured by relay R14).

Results of the simulations for both algorithms are summarized in Table B.1 of Appendix-B and depicted in Figure 5.2 and Figure 5.3 for relay R14 and Figure 5.4 and Figure 5.5 for relay R41.

Figure 5.2 and Figure 5.4 compare the fault detection time and maximum interrupted fault current of both algorithms for all simulated fault cases. The LIVRD algorithm is represented by a circle and the OC algorithm is represented by a triangle. Figure 5.3 and Figure 5.5 show the fault-induced current signals measured by relays R14 and R41, respectively, for all the simulated fault cases, together with the OC threshold value for better visualization of the performance of the OC algorithm.

As it can be seen in Table B.1, the LIVRD algorithm is able to detect all the simulated fault cases up to 250 Ω, regardless of the fault type, location and resistance. Its fault detection time barely changes regardless of the fault case parameters.

Meanwhile, the OC algorithm properly detects PtG faults up to 50 Ω and PtP faults up to 150 Ω while it fails detecting PtG faults for resistances above 100 Ω and PtP faults for resistances above 200 Ω which are located at higher distances. The fault current rate-of-rise is attenuated with the fault resistance, so it takes more time for the fault current to overcome the OC threshold value, decreasing the operation speed of the OC algorithm. This attenuation also makes the fault current not to overcome the OC threshold value in some fault cases with high fault resistance and farther fault locations, thus, making fault detection impossible for the OC algorithm.

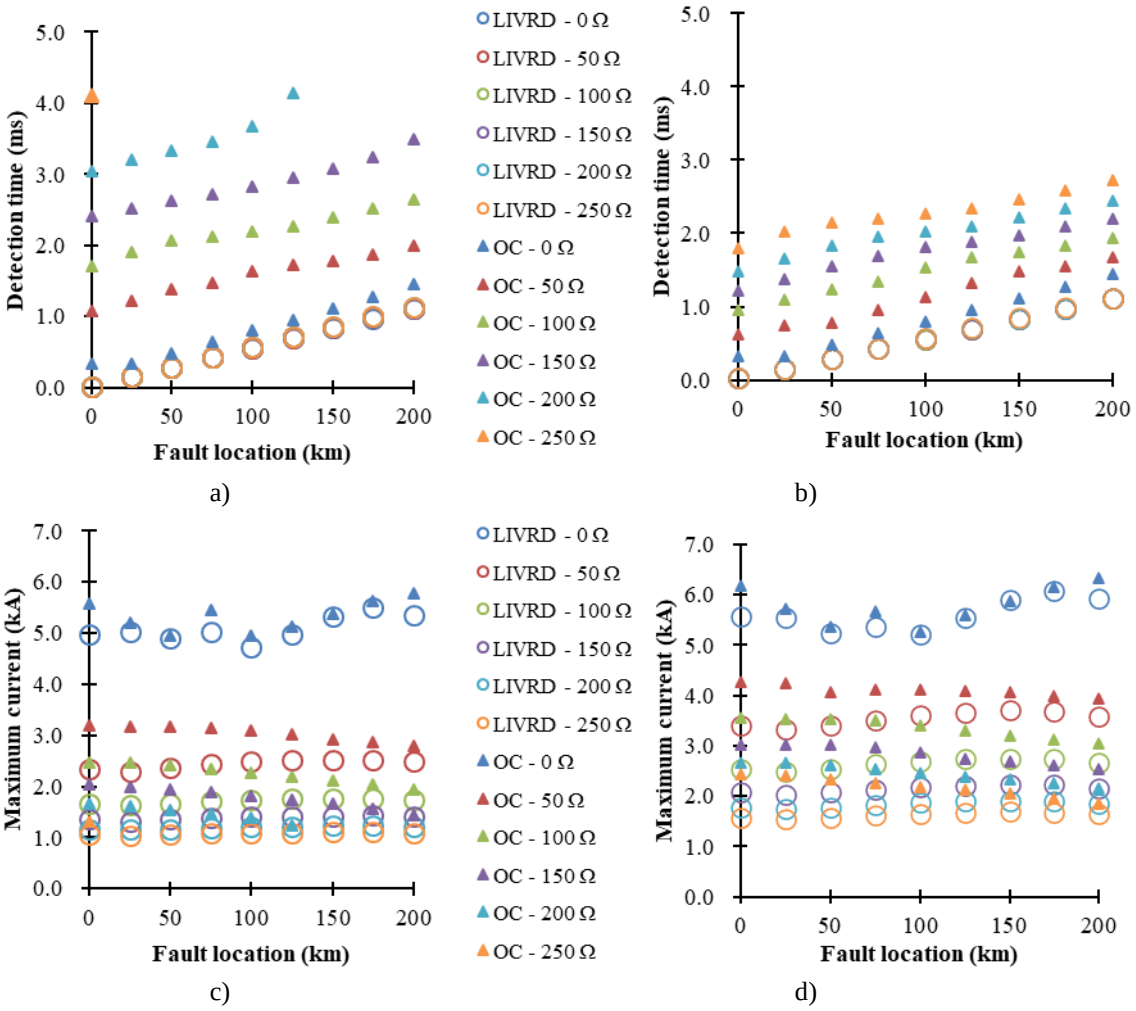


Figure 5.2.- Comparison of the OC and LIVRD algorithms (relay R14) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

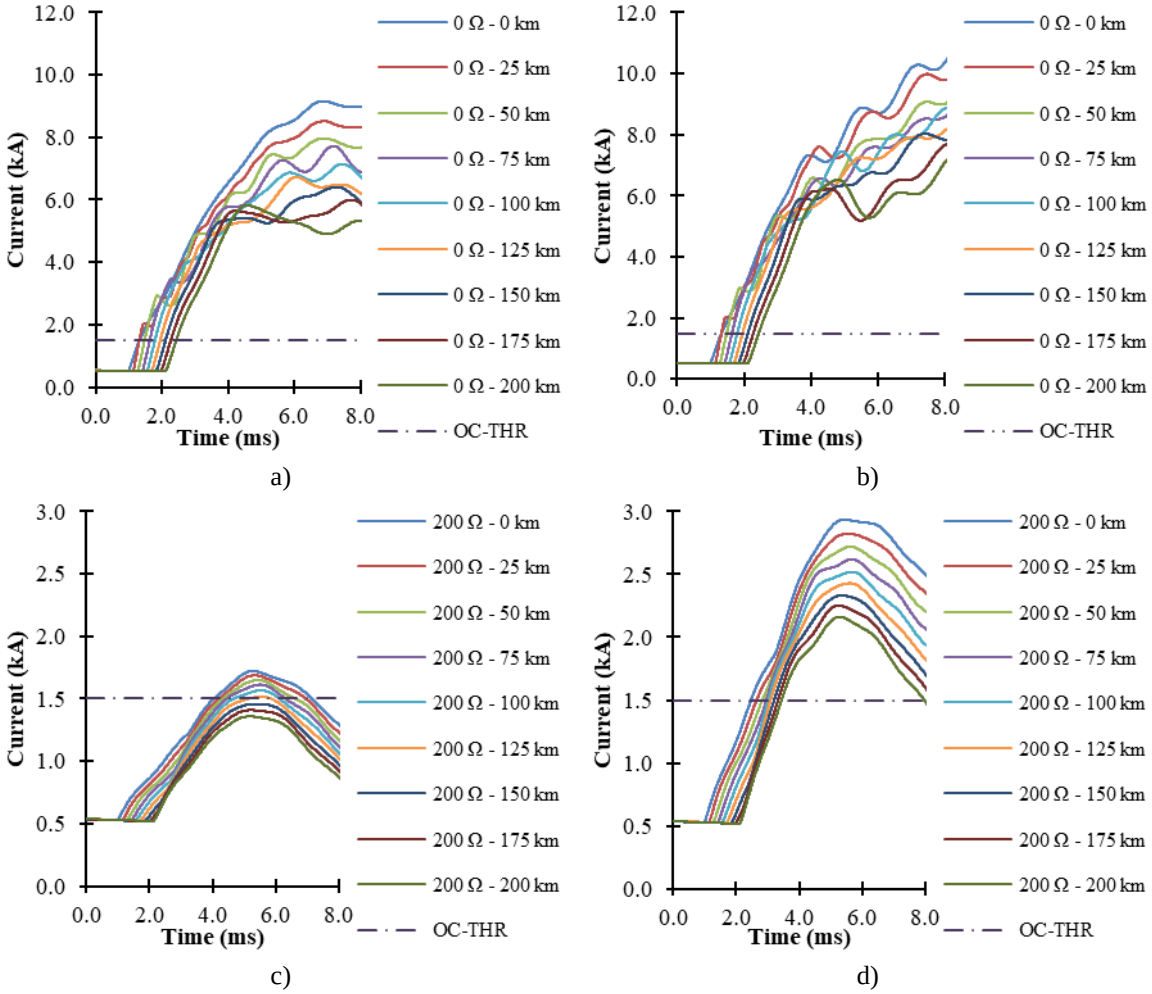


Figure 5.3.- OC threshold value and fault current measured by relay R14 during a), c) a PtG fault and b), d) a PtP for with different fault locations and resistances.

Moreover, the slower operation speed of the OC algorithm is emphasized for relay R41 since the current is flowing out of the cable through that end during normal conditions and it has to change its polarity when a fault in the link occurs. Therefore, the operation speed of relay R41 is slower than that of relay R14. Additionally, relay R41 presents a worse capability of detecting high resistance faults as it can be seen by comparing Figure 5.3-c and -d with Figure 5.5-c and -d. Relay R14 is able to detect all 200 Ω PtP faults and most of the 200 Ω PtG faults while relay R14 is only capable of detecting some of the simulated 200 Ω faults. No 200 Ω PtG faults are detected by relay R41.

Therefore, it can be concluded through this comparison that the proposed LIVRD algorithm presents better features and performance than the existing OC algorithm.

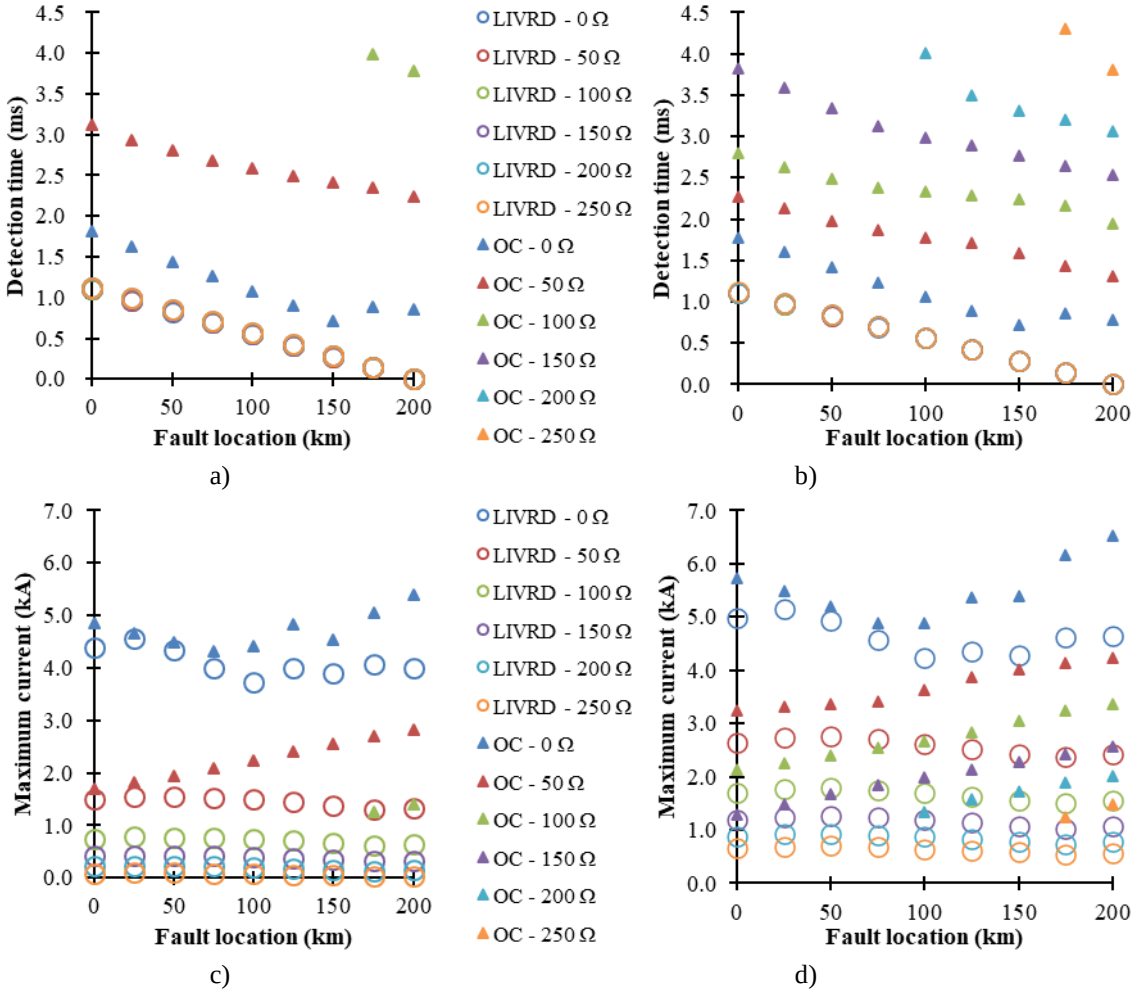


Figure 5.4.- Comparison of the OC and LIVRD algorithms (relay R41) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

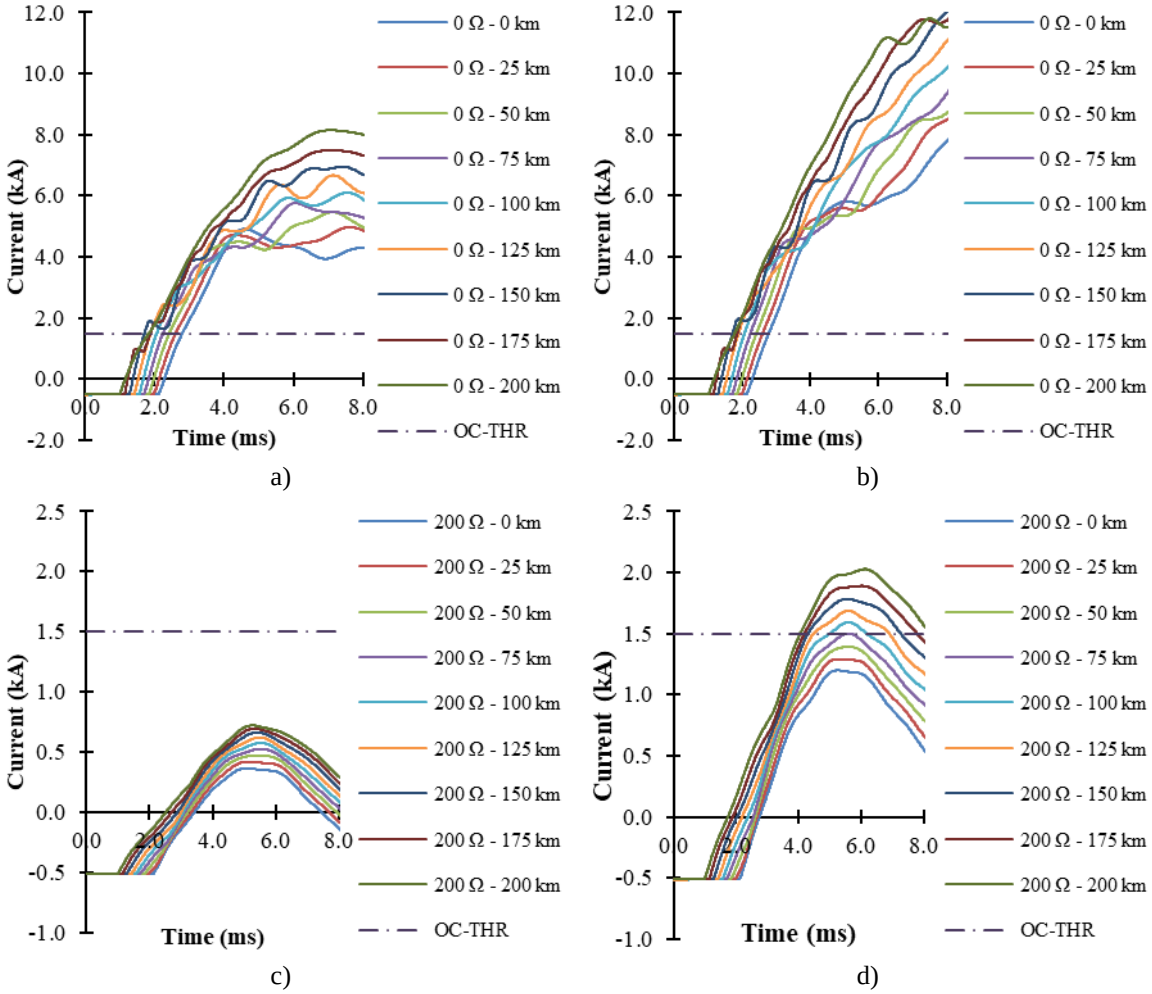


Figure 5.5.- OC threshold value and fault current measured by relay R41 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

5.1.2. Undervoltage algorithm

The proposed LIVRD algorithm is compared with the undervoltage algorithm, which is examined in subsection 2.6.2.1. The LIVRD algorithm employs the threshold values displayed in Table 4.1, while the UV algorithm uses a threshold value of 200 kV. The UV threshold value is selected in order to avoid nuisance operation of other relays located in healthy links, i.e., to ensure selectivity and sensitivity. This way, fault detection is achieved by the UV algorithm when the voltage drops under 200 kV, as it is shown in Figure 5.6.

Results of this comparison are summarized in Table B.2 of Appendix-B and are depicted in Figure 5.7 and Figure 5.8 for relay R14 and Figure 5.9 and Figure 5.10 for relay R41. Figure 5.7 and Figure 5.9 show the fault detection time and maximum interrupted fault current for different fault types, locations and resistances. The UV algorithm is represented by a triangle and the LIVRD algorithm is represented by a circle.

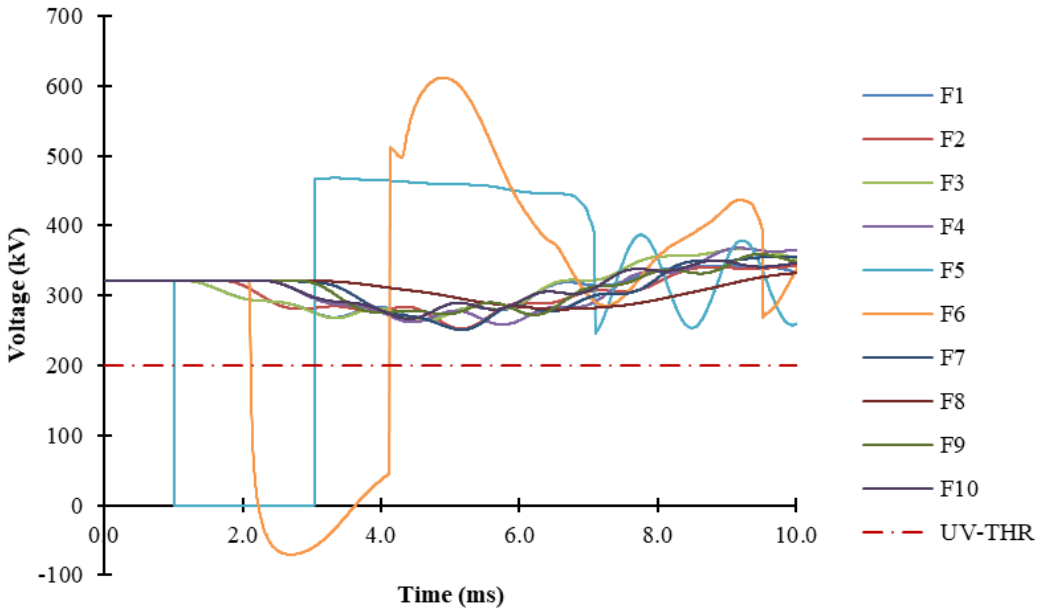


Figure 5.6.- Selection of threshold value for the UV algorithm (measured by relay R14).

Meanwhile, Figure 5.8 and Figure 5.10 show the fault-induced voltage signal for all the simulated cases, together with the UV threshold value for better visualization of the performance of the UV algorithm.

As it can be seen from the results, the UV algorithm presents a less sensitive operation than the LIVRD algorithm and even than the previously-analysed OC algorithm. It is capable of detecting all the simulated fault cases up to 50 Ω regardless of their location or fault type. However, it is not able to detect PtG and PtP fault cases with resistances above 100 Ω and 150 Ω, respectively.

High fault resistances attenuate the collapse of the voltage, so it does not drop under the selected threshold value as it can be seen in Figure 5.8-c, -d and Figure 5.10-c and –d. On the other hand, the LIVRD algorithm presents a fast and proper operation against fault cases with resistances up to 250 Ω regardless of the fault type or location.

Thus, it is demonstrated that the LIVRD algorithm presents a more sensitive operation than the UV algorithm as well as a higher operation speed where the fault detection time barely varies regardless of the fault's features.

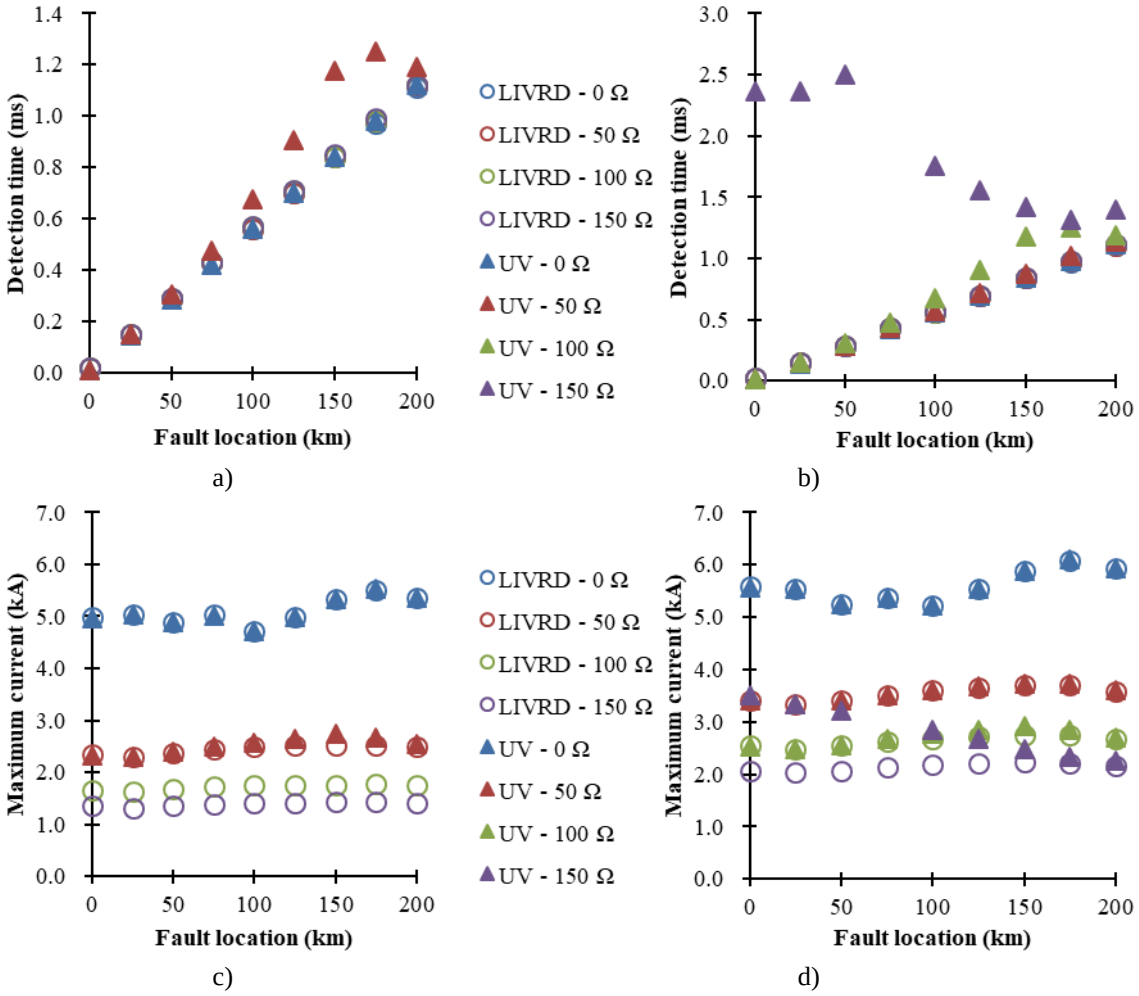


Figure 5.7.- Comparison of the UV and LIVRD algorithms (relay R14) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

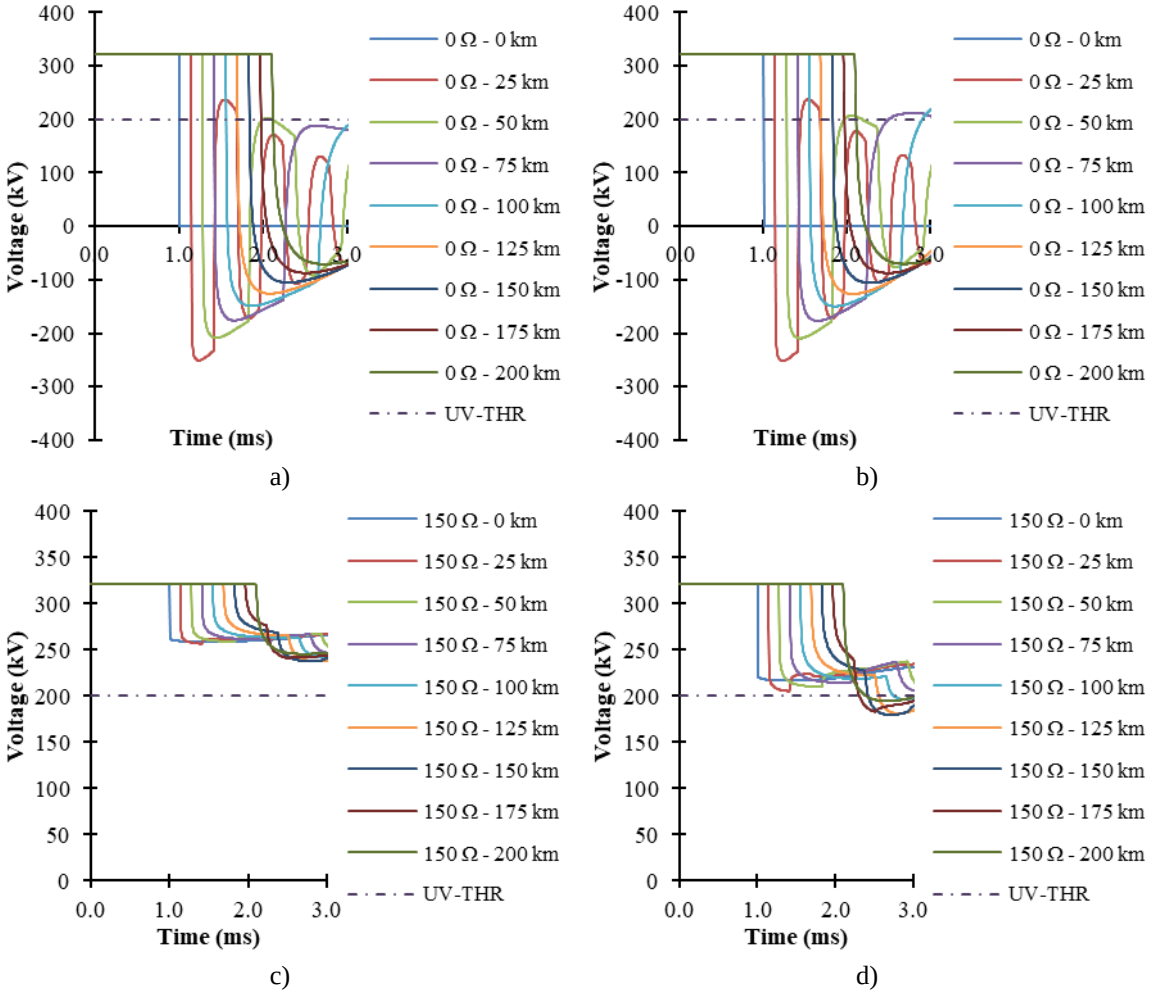


Figure 5.8.- UV threshold value and voltage measured by relay R14 during a), c) a PtG fault and b), d) a PtP fault with different fault locations and resistances.

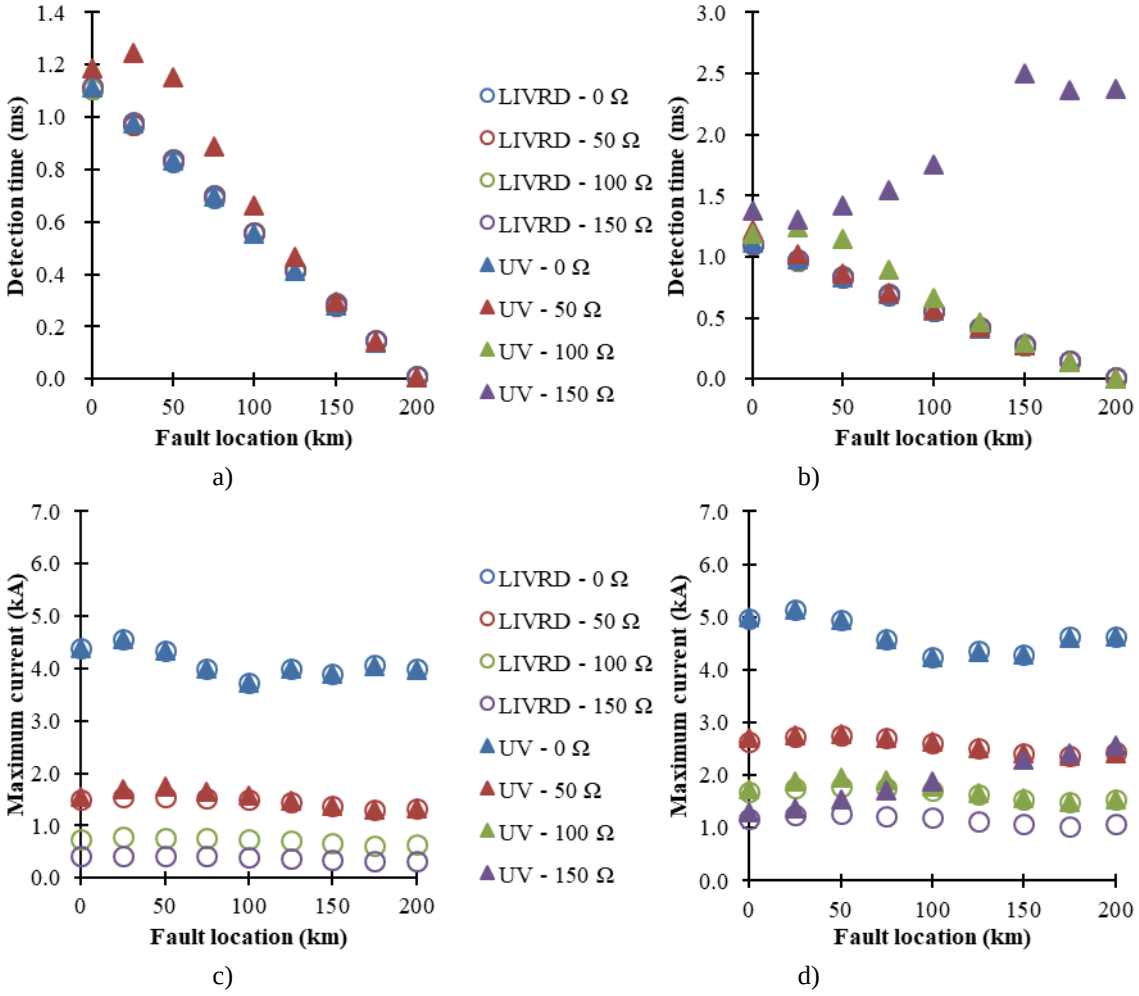


Figure 5.9.- Comparison of the UV and LIVRD algorithms (relay R41) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

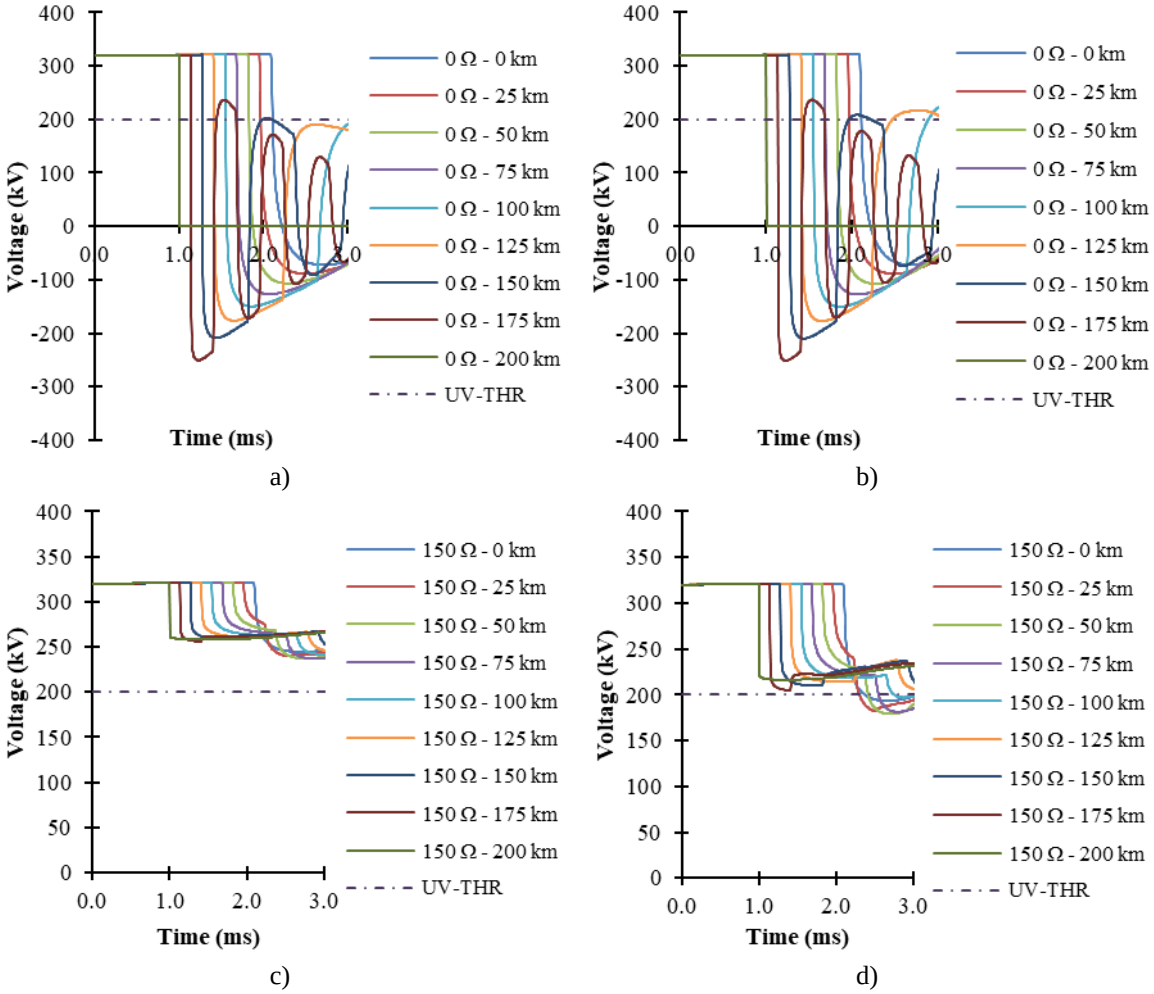


Figure 5.10.- UV threshold value and voltage measured by relay R41 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

5.1.3. Inductor-voltage algorithm

The inductor-voltage (LV) algorithm measures the voltage across the inductors located at the ends of the link as borders of the protection zone, i.e., the voltage across the limiting inductors. The measured voltage is compared with a threshold value so as to discriminate between normal operation conditions and fault conditions. Characteristics of the LV algorithm are presented in subsection 2.6.2.3. The proposed LIVRD algorithm is also an inductor-voltage-based algorithm since it compares the voltage measured at both sides of the limiting inductors by calculating its ratio and the ratio's derivative. Thus, two inductor-voltage-based algorithms are compared in this subsection.

A threshold value of 200 kV is employed by the common LV algorithm while the proposed one employs those presented in Table 4.1. Thus, the inductor-voltage algorithm detects a fault condition when the voltage across the inductor overcomes the selected threshold value. The selected LV threshold value enables selective and sensitive fault detection avoiding nuisance operation of unaffected relays as it is shown in Figure 5.11.

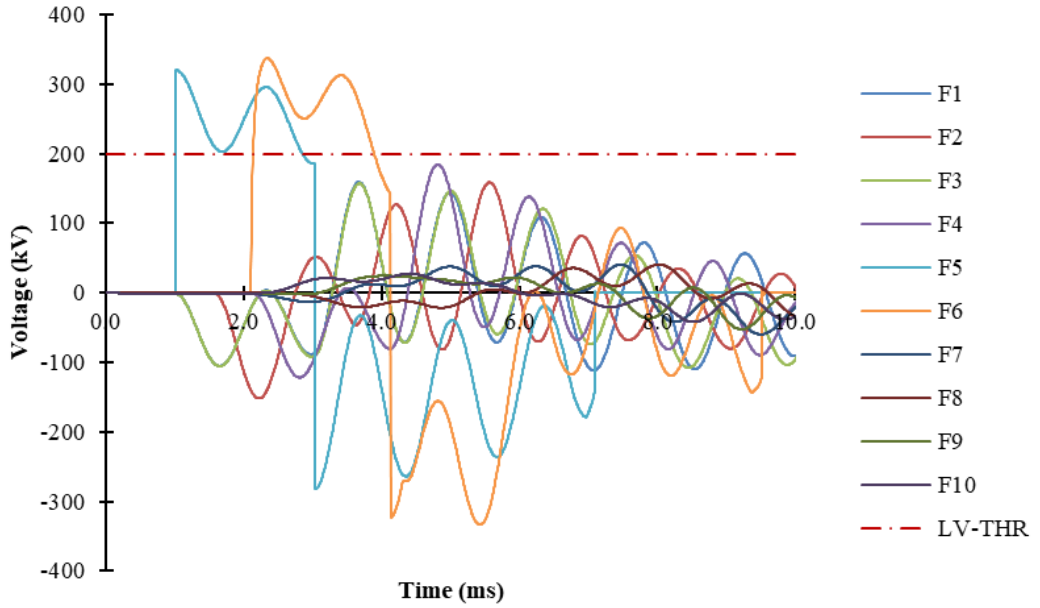


Figure 5.11.- Selection of threshold value for the LV algorithm (measured by relay R14).

Table B.3 (Appendix-B) summarizes the results of this comparison by presenting the fault detection time of both algorithms and the maximum interrupted current by the circuit breaker in case of operation after fault detection by both algorithms. These results are also illustrated in Figure 5.12 and Figure 5.14 regarding relays R14 and R41, respectively. The proposed LIVRD algorithm is represented with a circle and the common LV algorithm with a triangle.

On the other hand, the voltage measurements across the inductor are represented in Figure 5.13 and Figure 5.15 regarding relays R14 and R41, respectively. The LV threshold value is also represented in these figures in order to visualise the performance of the LV algorithm.

The LV algorithm is able to properly detect solid faults regardless of the fault type while it is not sensitive enough to detect high-resistance faults. The voltage across the inductor during high-resistance faults does not increase as much as it does during solid faults. This attenuation is emphasized if PtG and PtP faults are compared. PtG faults are more difficult to detect which is challenging for the LV algorithm since this type of faults are more common in cable-base systems. This attenuation is depicted in Figure 5.13 and Figure 5.15, where the voltage across the limiting inductor induced by solid and 50 Ω faults is illustrated.

Hence, the proposed LIVRD algorithm presents a better performance against high-resistance faults than the common LV algorithm.

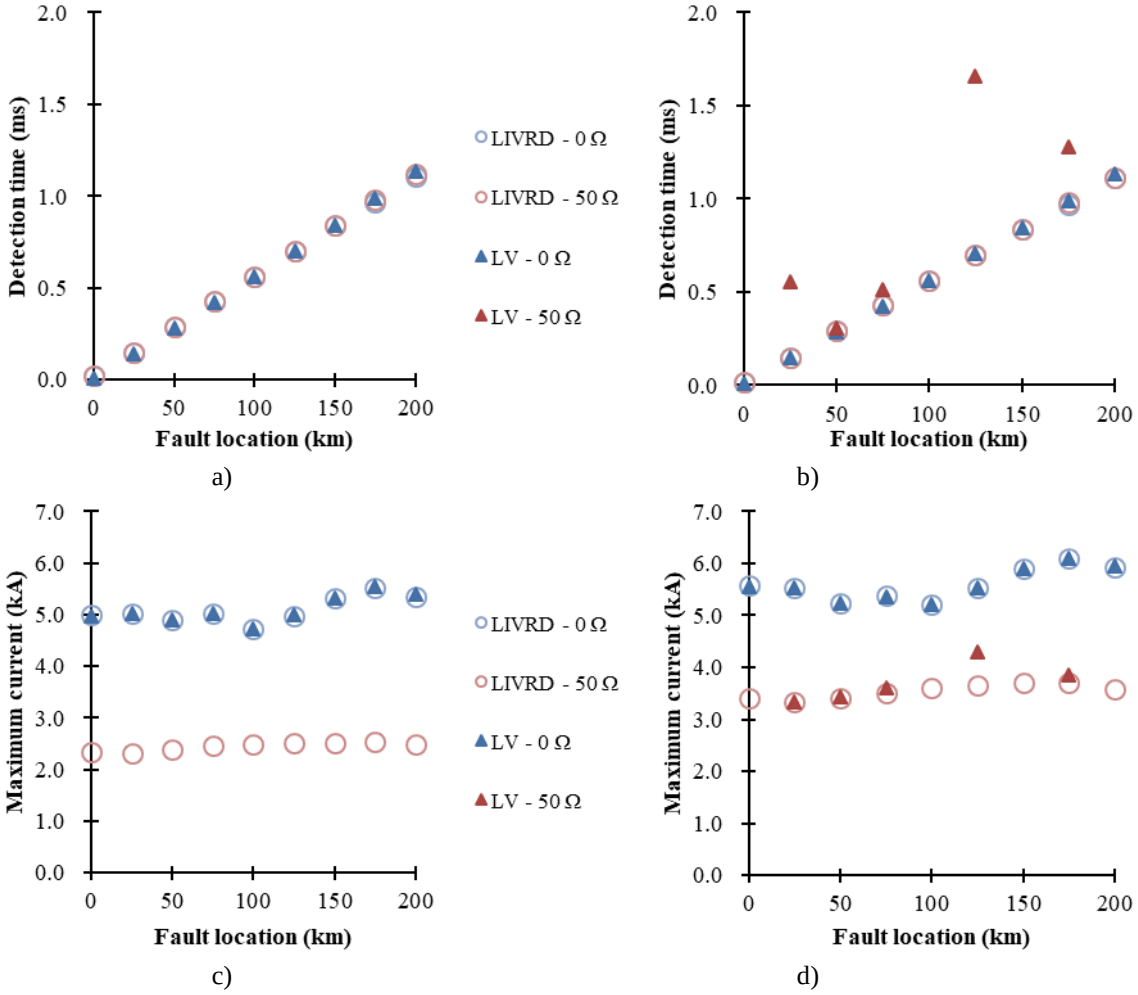


Figure 5.12.- Comparison of the LV and LIVRD algorithms (relay R14) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

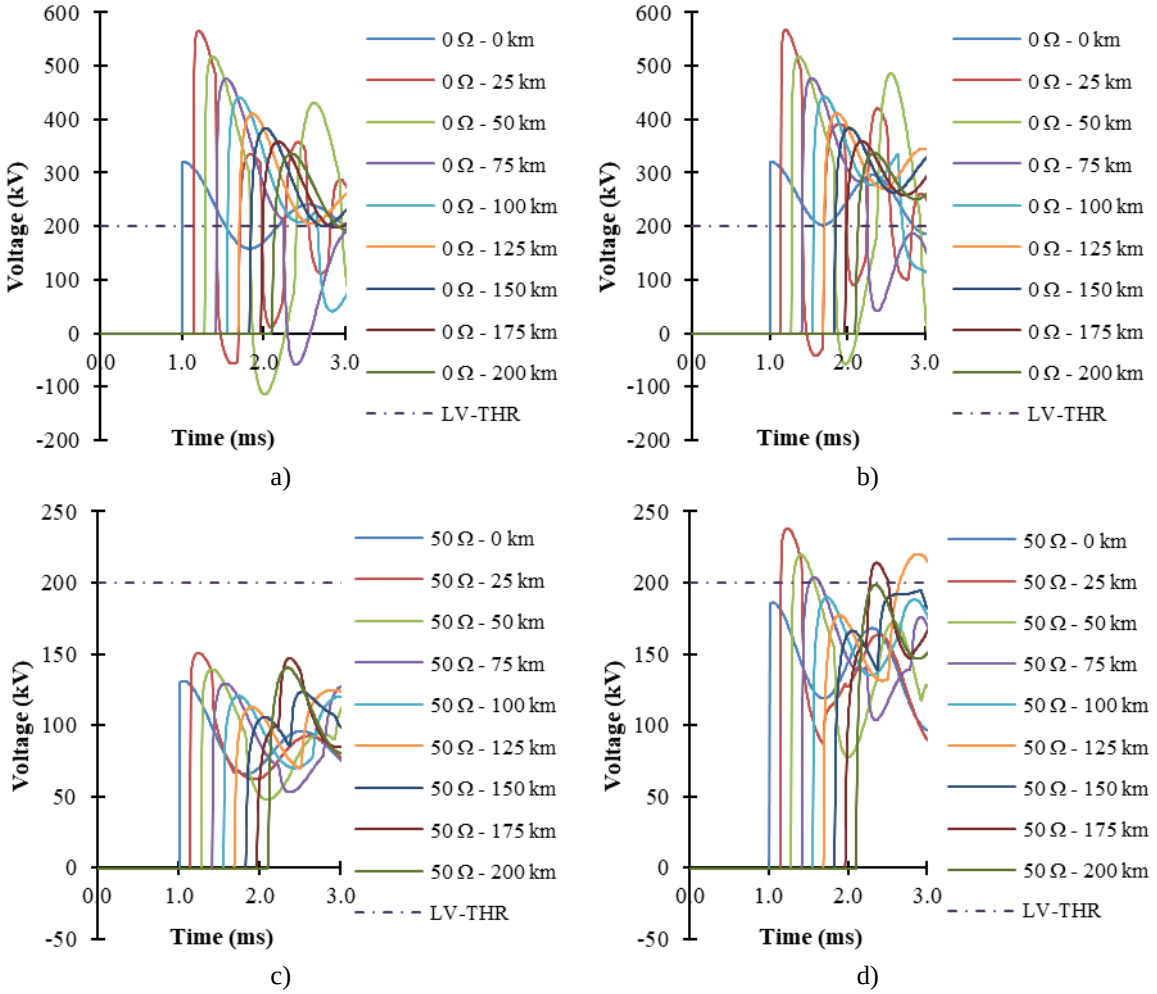


Figure 5.13.- LV threshold value and inductor-voltage measured by relay R14 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

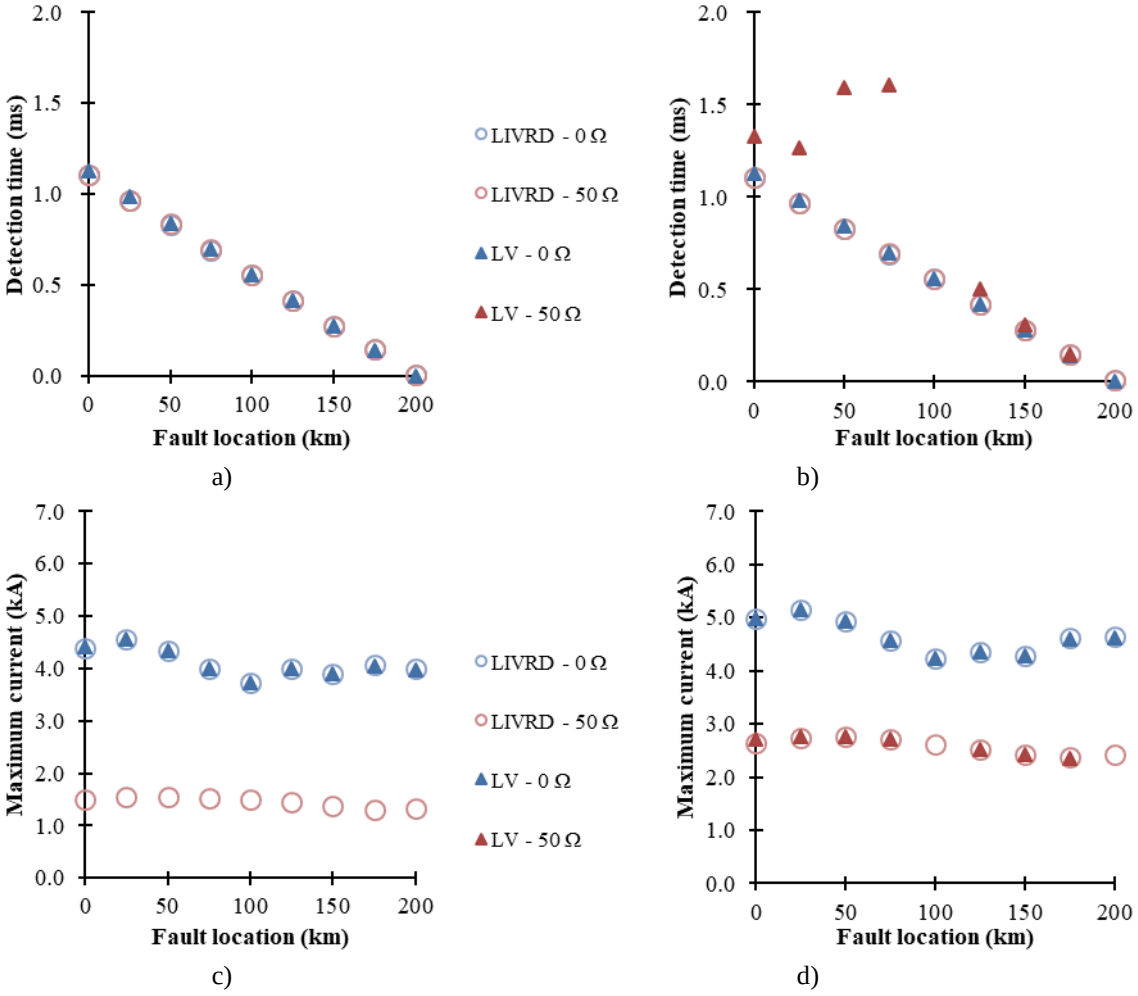


Figure 5.14.- Comparison of the LV and LIVRD algorithms (relay R41) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

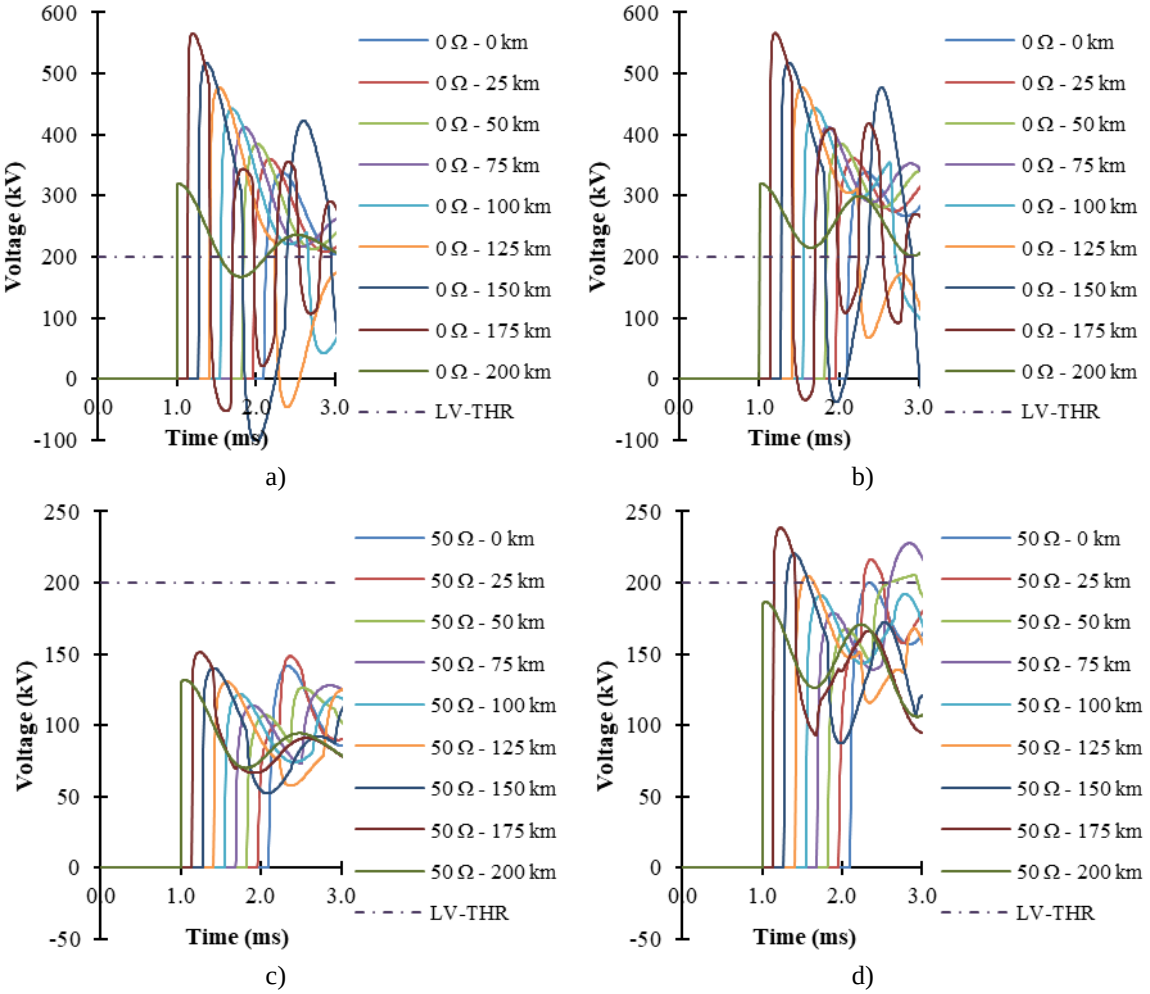


Figure 5.15.- LV threshold value and inductor-voltage measured by relay R41 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

5.1.4. Rate-of-change-of-current algorithm

The proposed LIVRD algorithm is compared with the rate-of-change-of-current algorithm, explained in subsection 2.6.1.2. The ROCOC algorithm is compared with the proposed LIVRD algorithm via simulations in link 14. A threshold value of 2 kA/ms is selected for the ROCOC algorithm operation in order to achieve selective and sensitive operation; fault detection is achieved when the threshold value is overcome as it shown in Figure 5.16. Meanwhile, the LIVRD algorithm uses the threshold values presented in Table 4.1.

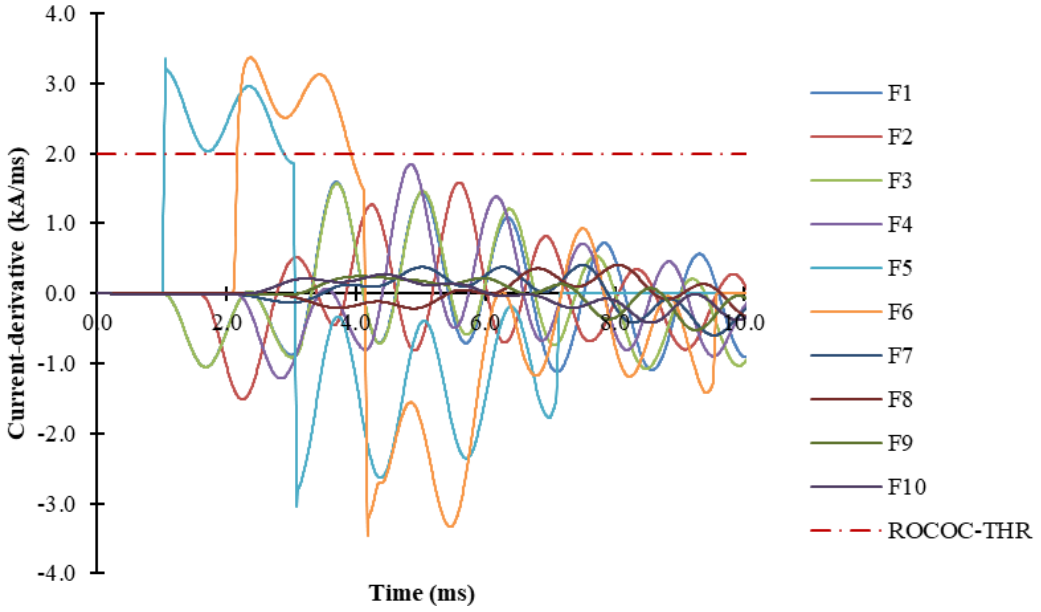


Figure 5.16.- Selection of threshold value for ROCOC algorithm (measured by relay R14).

The results of the comparison are shown in Table B.4 of Appendix-B, Figure 5.17 and Figure 5.19, i.e., fault detection times and maximum interrupted fault currents for relays R14 and R41 regarding both algorithms. Figure 5.18 and Figure 5.20 show the current-derivative values for the simulated cases and the ROCOC threshold value so the performance of the ROCOC algorithm can be visualised.

The ROCOC algorithm is a derivative-based algorithm, so it presents a fast operation against solid faults, just slightly slower than the proposed LIVRD algorithm. However, it is based on calculating the current-derivative, i.e., the rate-of-rise of the current which is greatly affected by the fault resistance as it was demonstrated in subsection 5.1.1. The attenuation of the fault current during high-resistance faults makes fault detection more complex. Therefore, high-resistance faults produce lower current-derivative values which do not overcome the selected threshold value as it can be seen in Figure 5.18 and Figure 5.20.

The results show how the ROCOC algorithm cannot detect any PtG faults with resistances of 50 Ω or higher and it also starts having problems detecting 50 Ω PtP

faults. Nevertheless, the ROCOC algorithm presents a feature that differentiates it from the overcurrent algorithm; relay R41 presents an operation as fast as that of relay R14 regardless of the polarity of the current. The ROCOC algorithm can quickly detect the presence of a fault inside the protection zone even when the current has not yet completed polarity reversal.

However, the proposed LIVRD protection algorithm is able to quickly detect faults up to 250 Ω regardless of fault type and fault location, so it presents a better performance than the ROCOC algorithm.

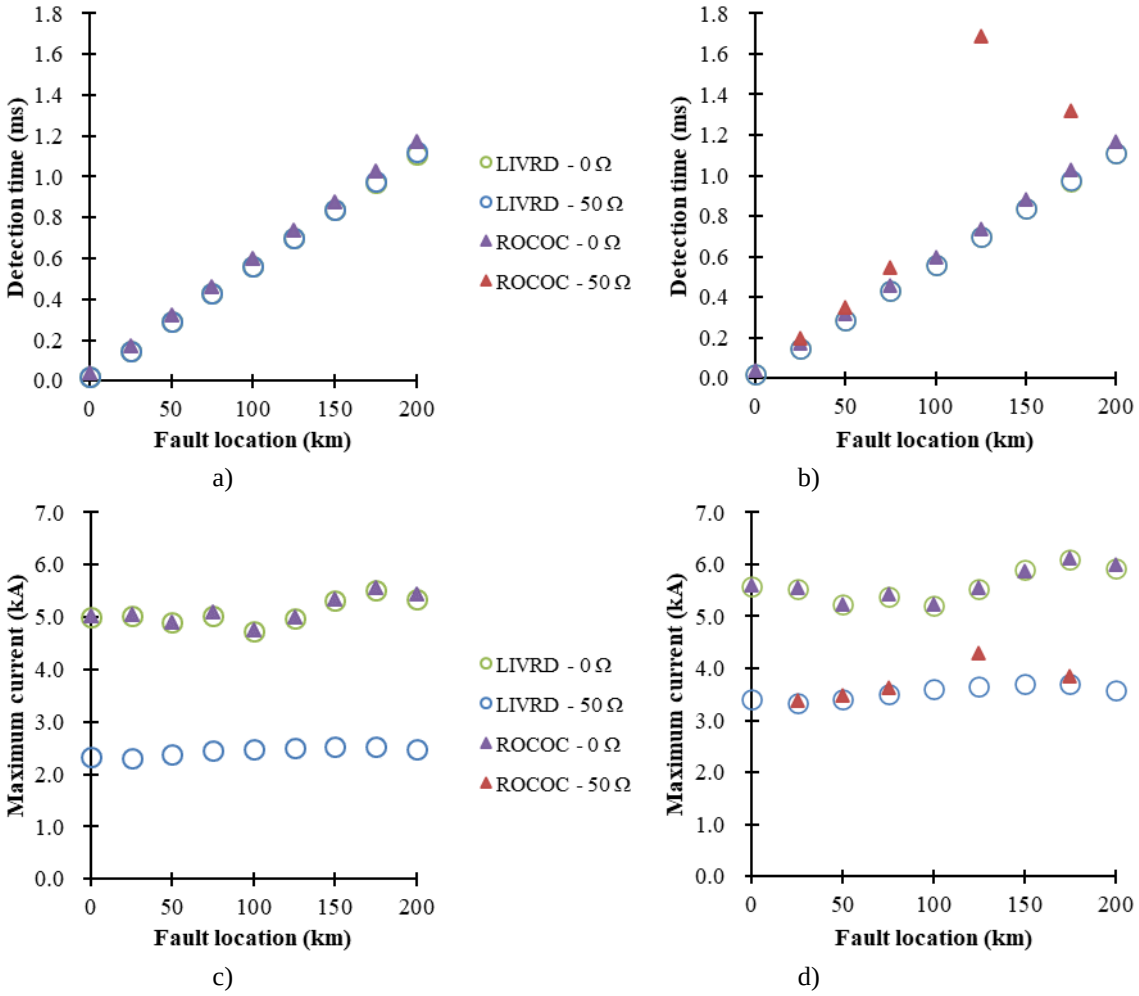


Figure 5.17.- Comparison of ROCOC and LIVRD algorithms (relay R14) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

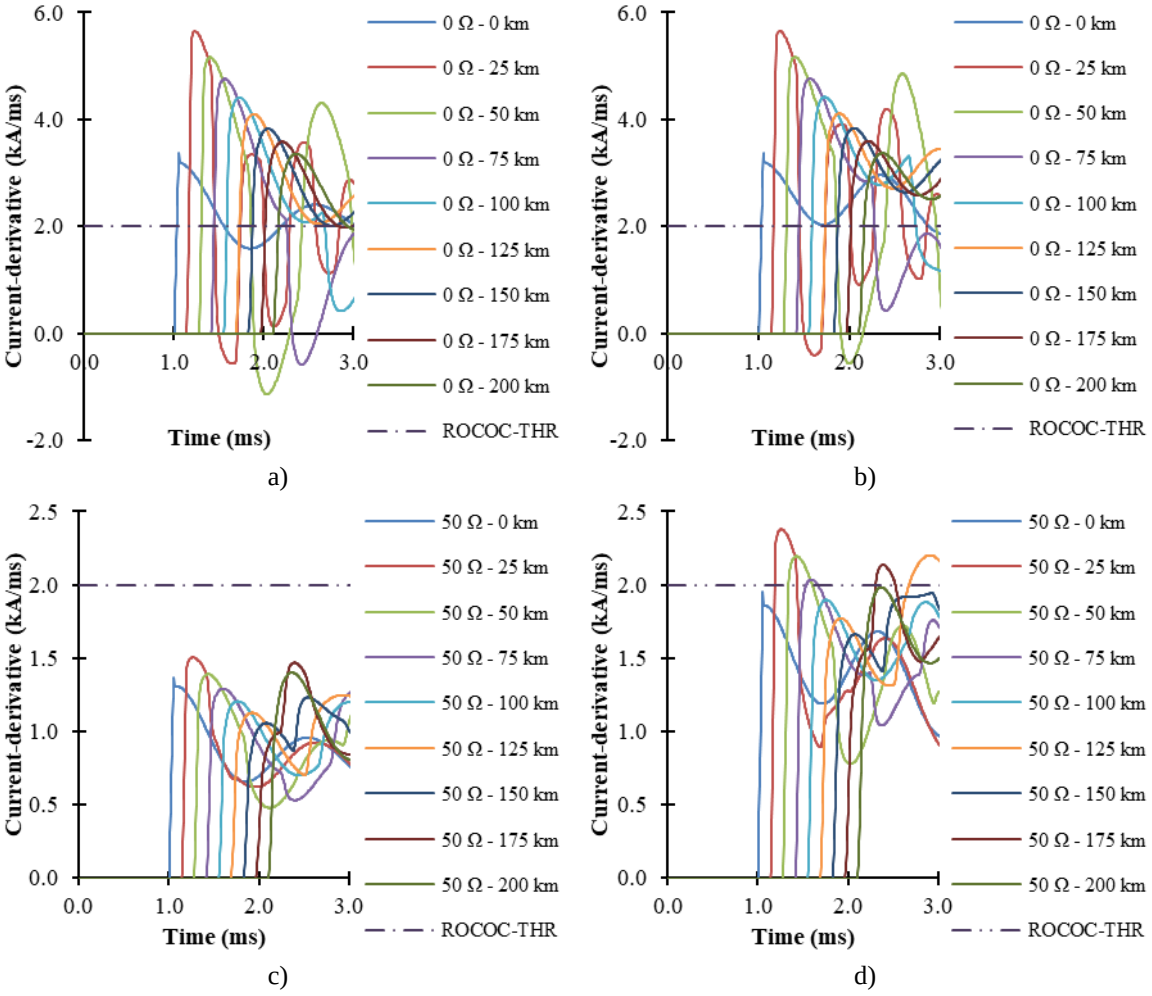


Figure 5.18.- ROCOC threshold value and current-derivative values measured by relay R14 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

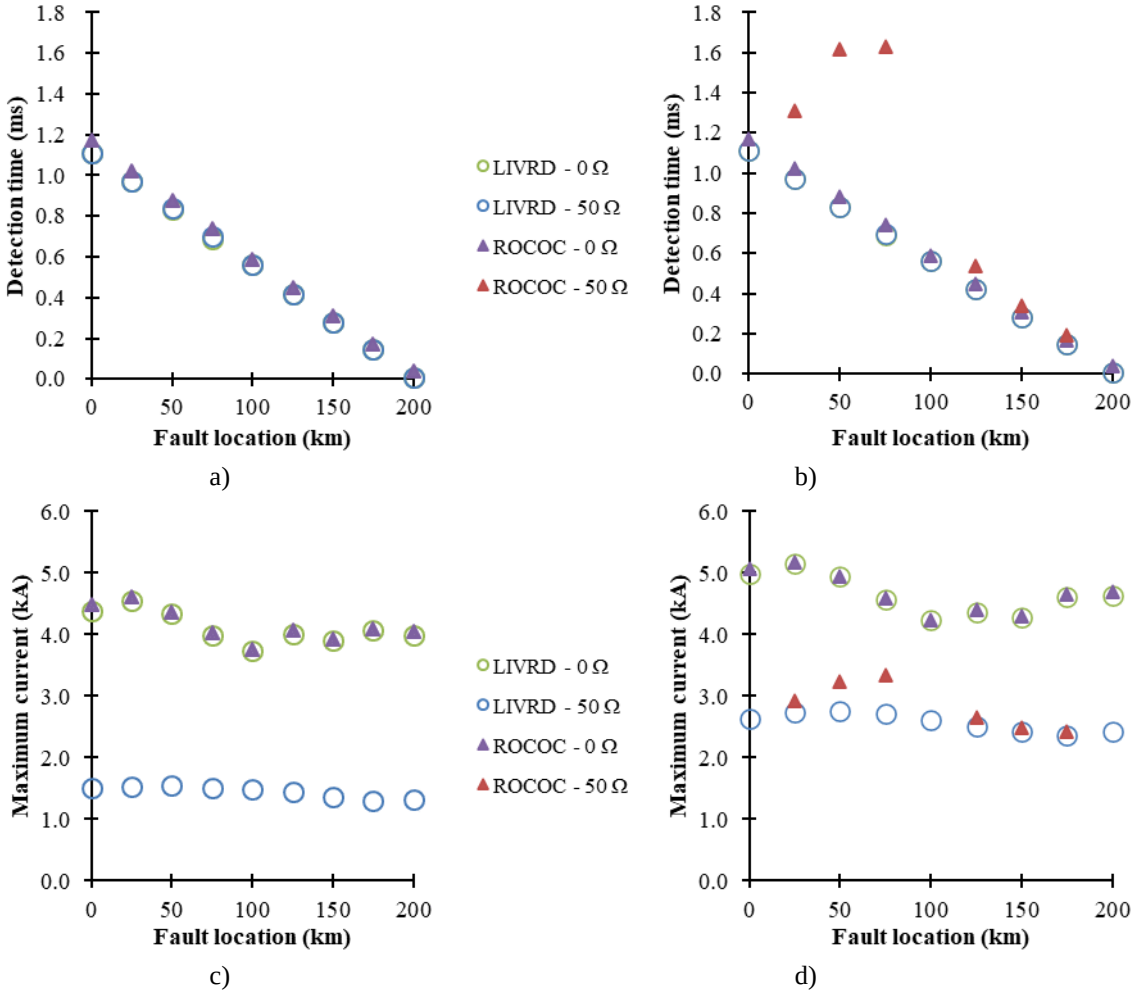


Figure 5.19.- Comparison of ROCOC and LIVRD algorithms (relay R41) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

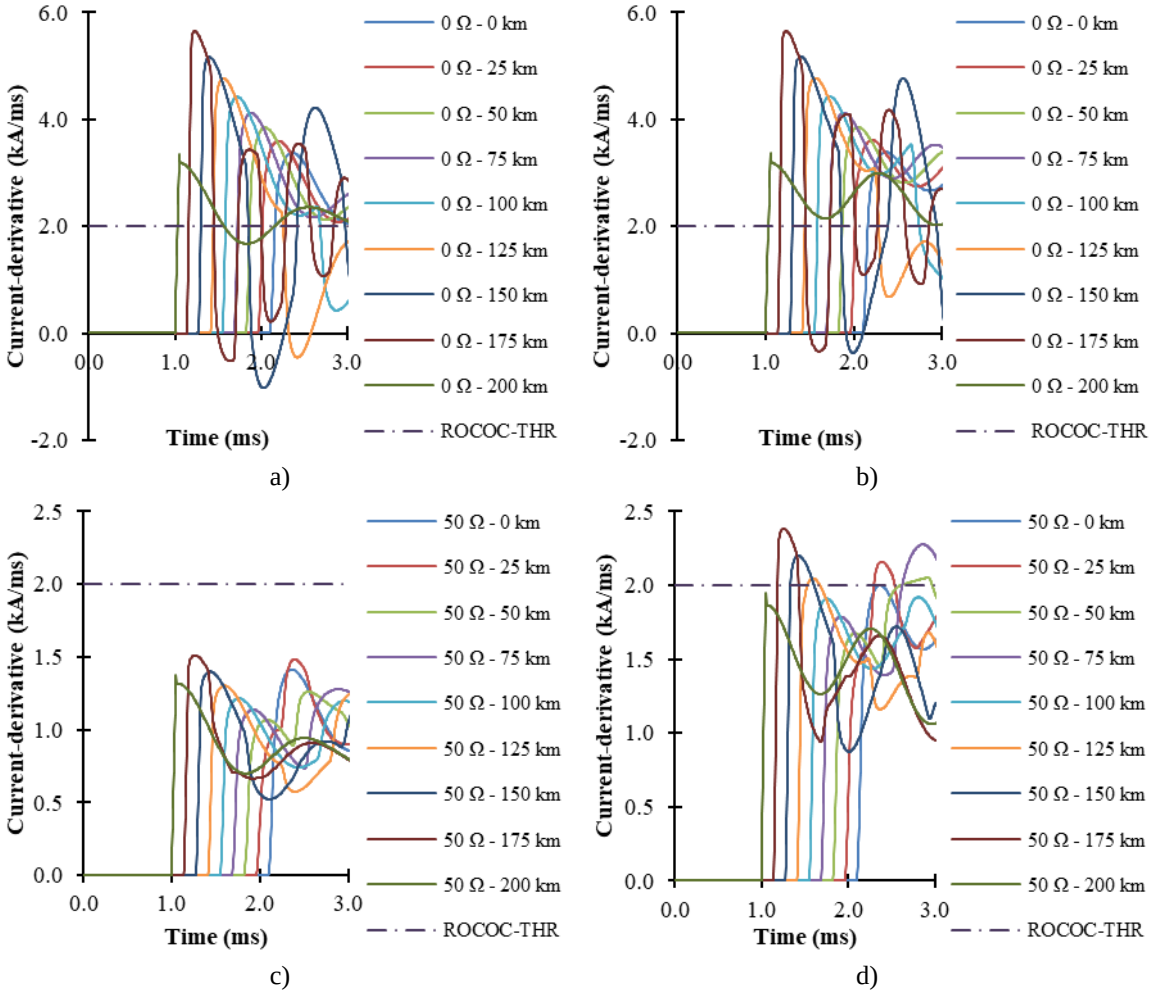


Figure 5.20.- ROCOC threshold value and current-derivative values measured by relay R41 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

5.1.5. Rate-of-change-of-voltage algorithm

The proposed LIVRD algorithm is compared with the rate-of-change-of-voltage algorithm, which is explained in subsection 2.6.2.2.

The ROCOV algorithm and the LIVRD algorithm are compared since they are local-measurement-based algorithms which present fast operation and high fault-resistance sensitivity. As in previous subsections, this comparison takes place in link 14; different fault cases are simulated while varying the fault type, location and resistance.

The LIVRD algorithm uses the threshold values presented in Table 4.1 while the ROCOV algorithm employs a -300 kV/ms threshold value [153], ensuring selective and sensitive operation when it is implemented in the grid model as it is shown in Figure 5.21.

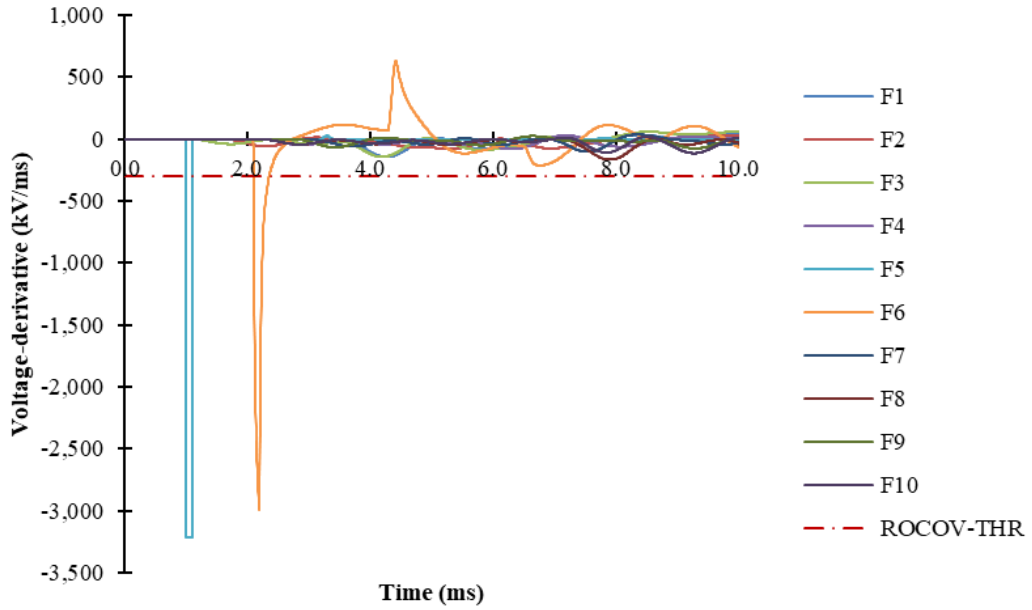


Figure 5.21.- Selection of threshold value for ROCOV algorithm (measured by relay R14).

Table B.5 (Appendix-B), Figure 5.22 and Figure 5.24 summarize the results of the comparison, i.e., fault detection times and maximum interrupted current for all the simulated cases regarding relays R14 and R41. Figure 5.23 and Figure 5.25 also depict the calculated voltage-derivatives for all fault cases.

As it can be seen in Table B.5 (Appendix-B), ROCOV algorithm presents the best performance of all existing local-measurement-based algorithms of this chapter. It presents better performance than the undervoltage algorithm, since, even when the collapse of the voltage is attenuated, the voltage drop is sharp enough to produce a high voltage-derivative value (in absolute value).

The ROCOV algorithm presents a fault detection speed almost as fast as that of the proposed LIVRD algorithm; it is only slower for high-resistance faults. Moreover, it is able to detect all the simulated PtP faults up to 250 Ω.

However, it presents problems with the detection of PtG faults with resistances over 150 Ω. As it can be demonstrated in subsection 5.1.2, high-resistance faults produce an attenuation in the voltage drop. Hence, the calculated voltage-derivative's peak value is also attenuated and does not cross the selected threshold value making impossible fault detection.

Therefore, it is concluded from the comparison that the LIVRD algorithm presents better operation against high-resistance faults than the ROCOV algorithm.

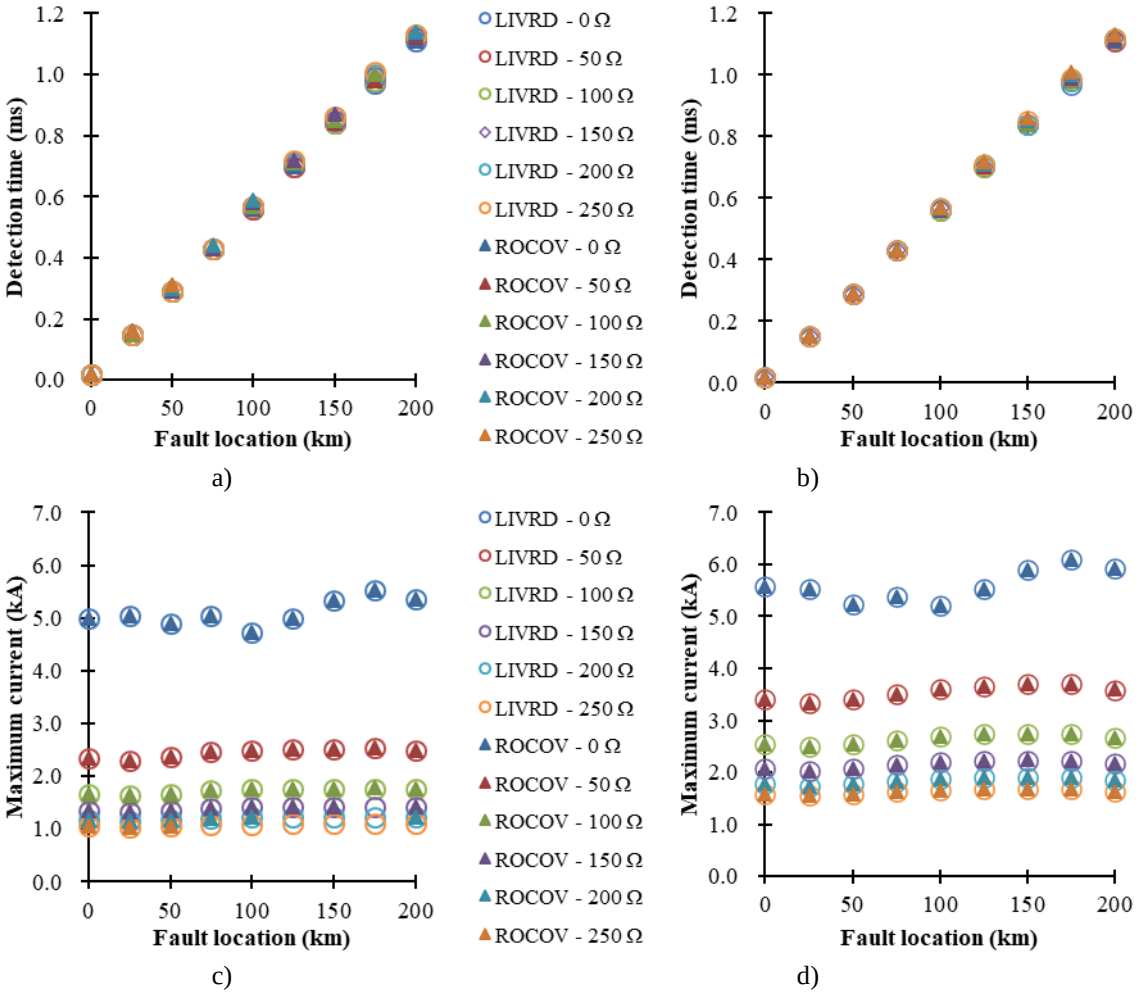


Figure 5.22.- Comparison of ROCOV and LIVRD algorithms (relay R14) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

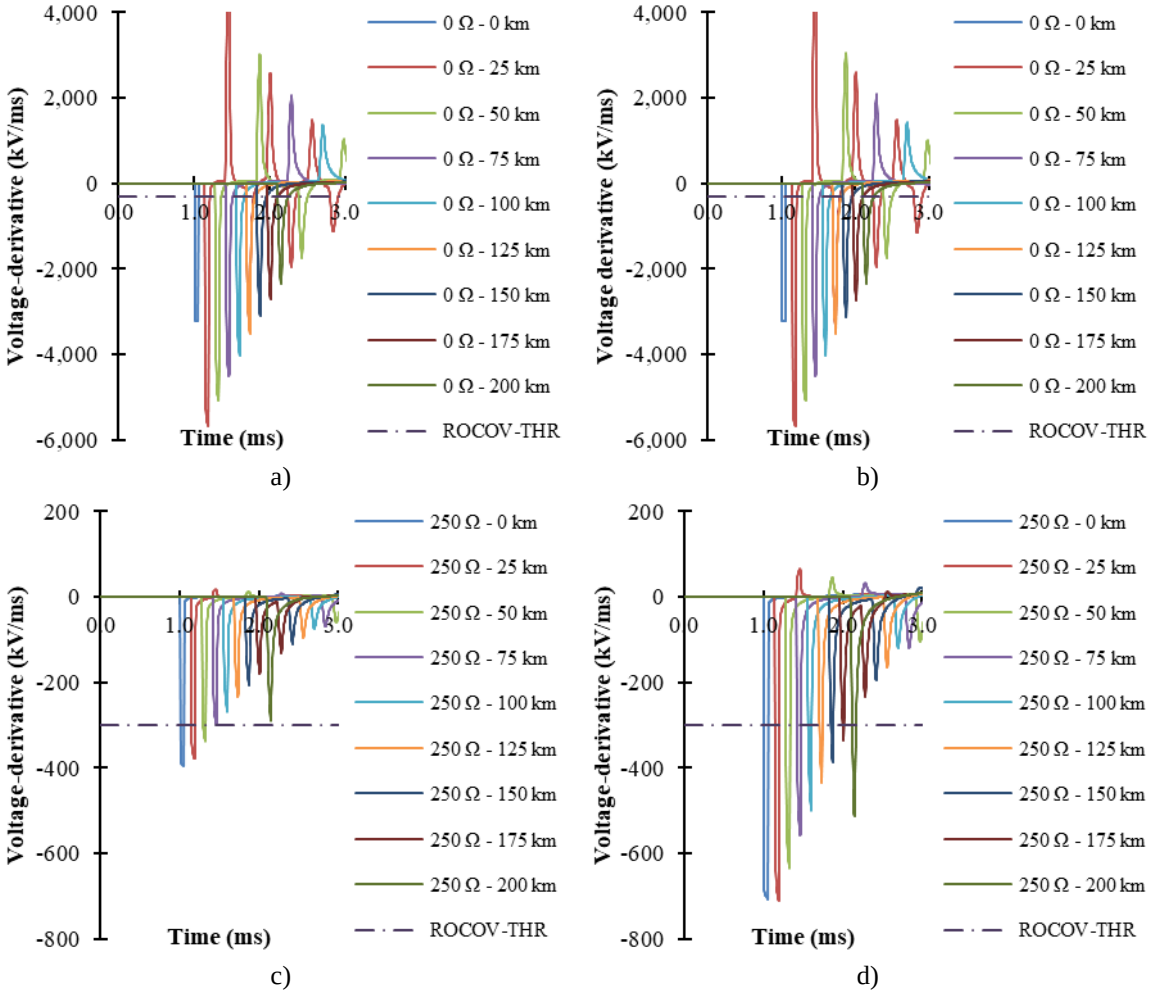


Figure 5.23.- ROCOV threshold value and voltage-derivative values measured by relay R14 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

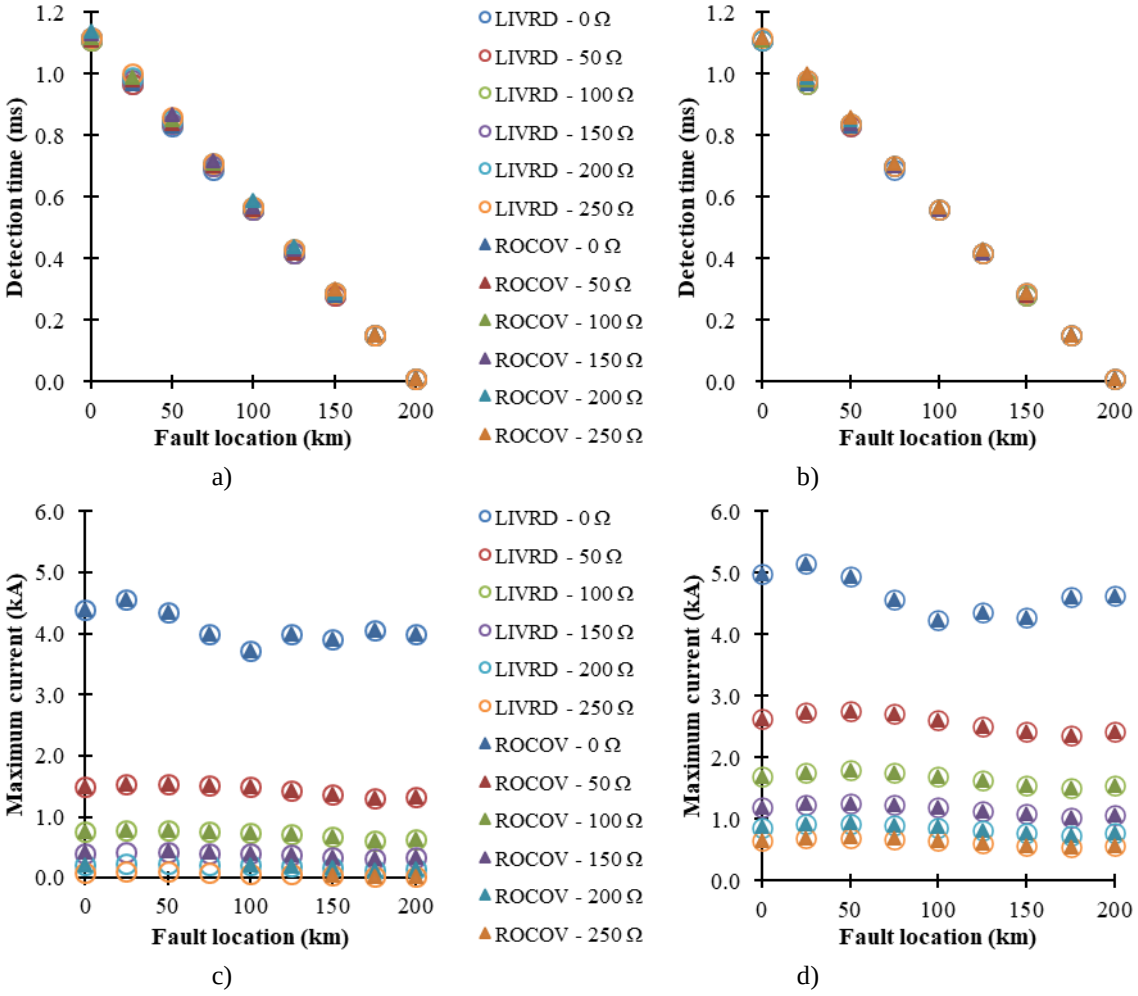


Figure 5.24.- Comparison of ROCOV and LIVRD algorithms (relay R41) for different fault locations and resistances for a), c) PtG faults and b), d) PtP faults.

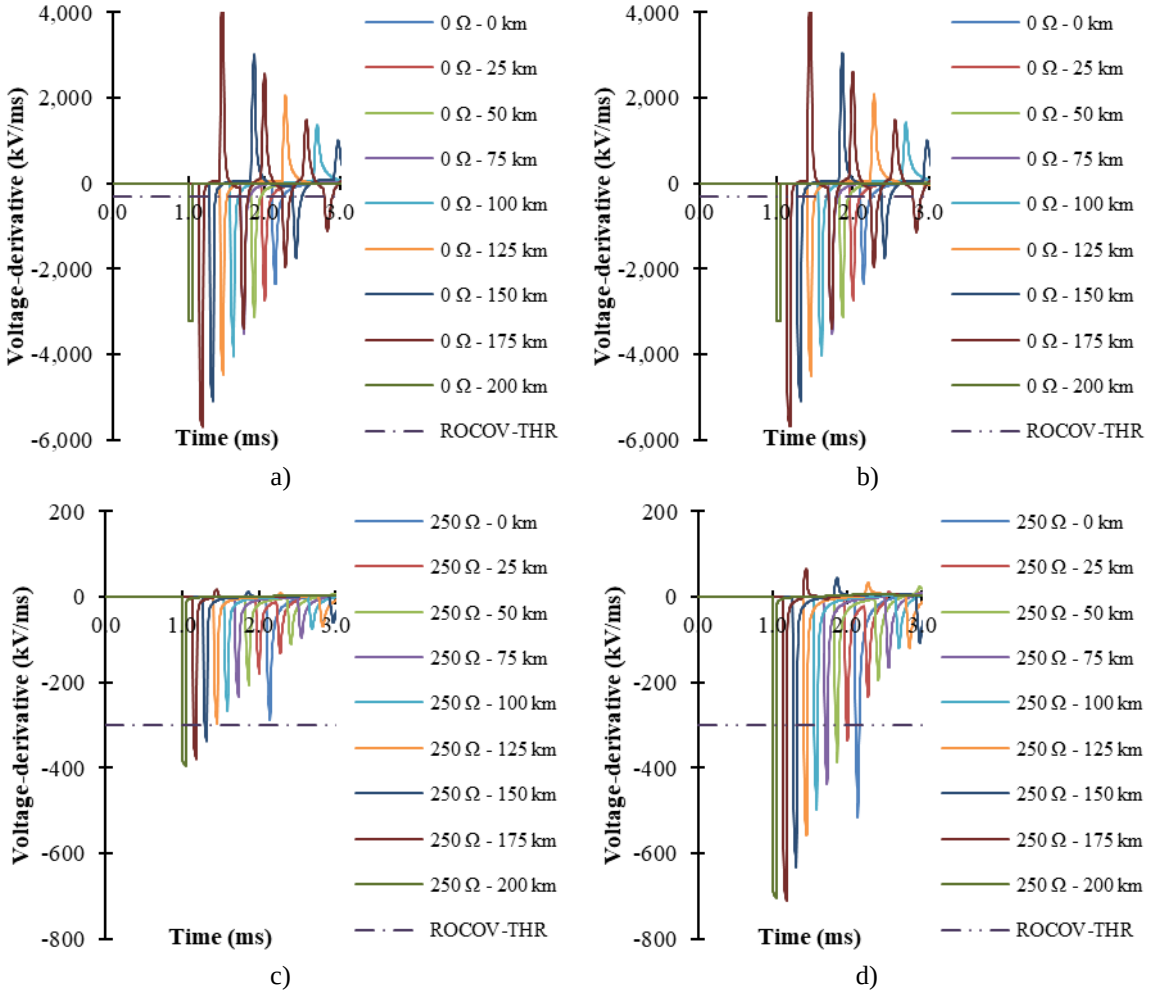


Figure 5.25.- ROCOV threshold value and voltage-derivative values measured by relay R41 during a), c) a PtG fault and b), d) a PtP fault for different fault locations and resistances.

5.2. Circuit breaker failure protection

The performance of the proposed LIVRD circuit breaker failure protection algorithm is evaluated by comparing it with a conventional circuit breaker failure protection. The proposed LIVRD circuit breaker failure protection is a local-measurement-based algorithm in order to satisfy the speed requirement associated to VSC-based grids. Moreover, the circuit breaker failure protection does not wait to operate until the estimated fault clearing time passes, as it is explained in subsection 3.3.3. This makes it faster than conventional circuit breaker failure protections and, therefore, suitable for VSC-based grids.

This way, the performance of the proposed LIVRD circuit breaker failure protection is thoroughly compared with a conventional circuit breaker failure protection in terms of operation speed and fault current interruption capability. Only solid PtP faults are analysed since they are the most constrictive in terms of fast rate-of-rise of the fault current. Hence, solid PtP faults are relatively more capable of putting the protection system at risk of not satisfying the operation speed requirement related to VSC-based systems.

The simulated fault case is F1, which is located in link 12, at the beginning of the cable, next to Bus 1. According to the proposed protection scheme, relay R12 operates as link primary protection while relay R13 (along with relay R14) operates as circuit breaker failure protection when circuit breaker DC-CB12 presents a failure in its operation.

Figure 5.26 depicts the fault current caused by a solid PtP F1 fault case (fault inception at 1 ms). Prospective fault current, operation of link primary protection and time steps regarding the circuit breaker protections are also included in the figure.

Relay R13 achieves backward fault detection and initiates the circuit breaker failure protection at time, t_{CBFi}, 1.100 ms (0.100 ms after fault inception as it is indicated in Table 4.7). Then, the circuit breaker failure protection keeps on standby during a time $t_{CBFstandby}$, equal to the operating time of the circuit breaker (2 ms for a H-CB) and then it starts the process of verifying the proper operation of the corresponding circuit breaker at instant 3.100 ms.

Relay R13 verifies the proper operation of circuit breaker DC-CB12 by checking the bus-side voltage-derivative, $ROCOV_{bus}$, within a time window $\Delta t_{CBF\_ROCOV_{bus}}$ of 150 μs (see Table 4.1). If the calculated $ROCOV_{bus}$ overcomes the corresponding threshold value THR_5 (200 kV/ms, see Table 4.1) during the time window, circuit breaker DC-CB12 has properly operated and the fault clearance process has started.

Otherwise, a failure in the operation of circuit breaker DC-CB12 is detected and a trip signal is sent to circuit breaker DC-CB13 (relay R14 operates similarly and sends a trip signal to circuit breaker DC-CB14).

For a solid PtP F1 fault, relay R13 detects a failure of circuit breaker DC-CB12 at time 3.250 ms ($t_{CBFd} = t_{CBFi} + t_{CBFstandby} + \Delta t_{CBF\_ROCOV_{bus}}$), i.e., 2.250 ms from fault inception. Circuit breaker DC-CB13 (and DC-CB14) operates after 2 ms at time (t_{CBFo}) 5.250 ms, interrupting a maximum fault current of 9.622 kA. Fault clearance is completed at time t_{CBFc}, around 10.550 ms (9.550 ms from fault inception).

On the other hand, a conventional circuit breaker failure protection must wait until the estimated fault clearing time of the link primary protection (t_{Pc}) has passed to verify if the circuit breaker has properly operated. For the simulated fault case depicted in Figure 5.26, the estimated fault clearing time is around 6.750 ms, at that instant (t_{CONVd}) the prospective fault current is above 12 kA. Moreover, the circuit breaker operates at 8.750 ms (t_{CONVo}), when the fault current is almost 15 kA.

Therefore, if a conventional circuit breaker failure protection is employed, a failure of the circuit breaker is detected when the proposed LIVRD circuit breaker failure protection is already completing the fault clearing process. The prospective fault current has reached a high magnitude at that time and continues rising until the circuit breaker operates, 2 ms after failure detection.

According to this, the fault clearing process by a conventional circuit breaker failure protection is completed at a much higher time than by employing the proposed LIVRD circuit breaker failure protection. Thus, it is demonstrated that the proposed LIVRD circuit breaker failure protection ensures a faster operation than conventional circuit breaker failure protections.

Moreover, a circuit breaker with lower fault current interruption capability can be chosen if the LIVRD circuit breaker failure protection is employed, in comparison with a conventional circuit breaker failure protection. The conventional circuit breaker failure protection must interrupt a much higher fault current than the one interrupted by the proposed LIVRD circuit breaker failure protection (9 kA vs 15 kA). This comparison is summarized in Table 5.1.

Similarly to the previously-explained fault case scenario, a solid PtP F1 fault measured by the relays located at the other end of link L12 is analysed. Contrary to the previous case, circuit breaker DC-CB12 operates properly, while circuit breaker DC-CB21 presents a failure in its operation.

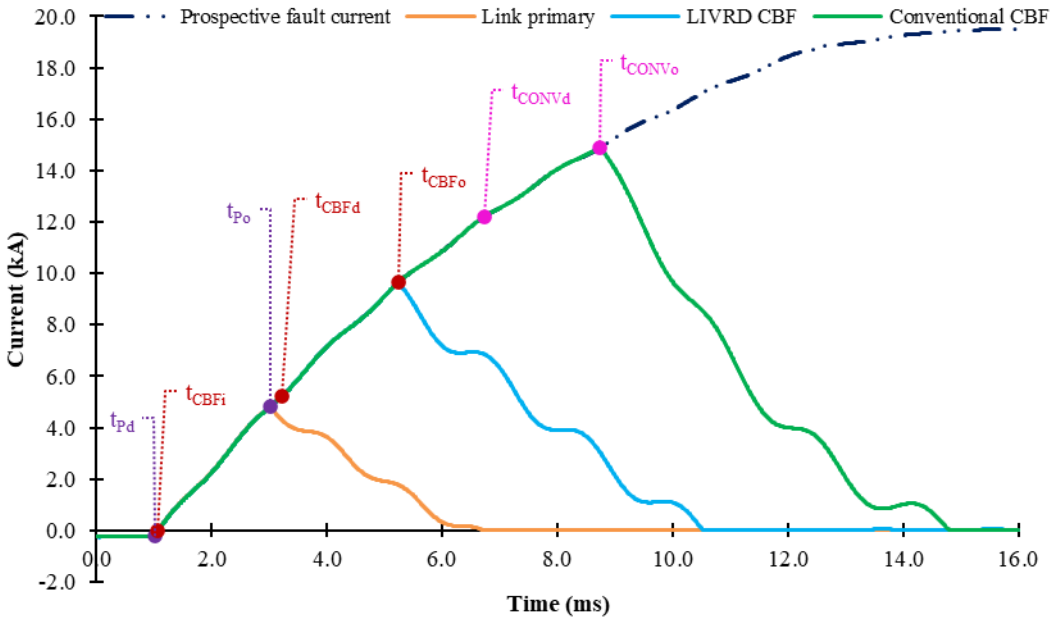


Figure 5.26.- Fault current induced by a solid PtP F1 fault with failure of DC-CB12 during operation of LIVRD link primary protection, LIVRD circuit breaker failure protection and conventional circuit breaker failure protection.

Table 5.1.- Comparison of the proposed LIVRD circuit breaker protection and a conventional circuit breaker failure protection for failure of DC-CB12 during a solid PtP F1 fault. Time steps (ms) and maximum fault current interrupted (kA).

Fault	**Failure of DC-CB**	**CBF protection Relay**	**LIVRD CBF protection**					**Conventional CBF protection**			
			t_{CBFi}	t_{CBFd}	t_{CBFo}	t_{CBFc}	I_{max}	t_{CBFd}	t_{CBFo}	t_{CBFc}	I_{max}
F1 PtP solid	DC-CB12	R13	1.100	3.250	5.250	10.550	9.622	6.750	8.750	14.850	14.909

Figure 5.27 shows the fault current regarding LIVRD link primary protection related to relay R21 and LIVRD circuit breaker failure protection related to relay R24. The LIVRD circuit breaker failure protection is initiated when relay R24 detects a backward fault at instant, t_{CBFi}, 1.650 ms, i.e., 0.650 ms after fault inception. Then, the proposed LIVRD circuit breaker failure protection keeps on standby until time $t_{CBFstandby}$ passes, when it verifies the proper operation of circuit breaker DC-CB21. The $ROCOV_{bus}$ signal is checked during a time window $\Delta t_{CBF\_ROCOV_{bus}}$ of 250 μs (see Table 4.1). The $ROCOV_{bus}$ does not cross threshold value THR_5 (100 kV/ms, see Table 4.1), so failure of circuit breaker DC-CB21 is detected at time (t_{CBFd}) 3.900 ms ($t_{CBFd} = t_{CBFi} + t_{CBFstandby} + \Delta t_{CBF\_ROCOV_{bus}}$), i.e., 2.900 ms from fault inception. Thus, trip signals are sent to circuit breaker DC-CB24 which operates at time, t_{CBFo}, 5.900 ms, interrupting a fault current of 7.826

kA. Fault clearance is completed at time (t_{CBFc}) 11.200 ms, i.e., 10.200 ms after fault inception.

On the other hand, a conventional circuit breaker failure protection detects a failure of circuit breaker DC-CB21 at a time t_{CONVd} slightly higher than the estimated fault clearing time of the link primary protection (t_{Pc}), i.e., around 8 ms (7 ms from fault inception) when the fault current reaches up to 10 kA. Therefore, circuit breaker DC-CB24 operates at approximately 10 ms (t_{CONVo}), interrupting a maximum current of more than 11 kA. Fault clearance is completed at 16.050 ms (15.050 ms from fault inception).

Once again, it is demonstrated the faster operation of the proposed LIVRD circuit breaker failure protection and how it allows employing a circuit breaker with lower fault current interruption capability, as it is summarized in Table 5.2.

Table 5.2.- Comparison of the proposed LIVRD circuit breaker protection and a conventional circuit breaker failure protection for failure of DC-CB21 during a solid PtP F1 fault. Time steps (ms) and maximum fault current interrupted (kA).

Fault	**Failure of DC-CB**	**CBF protection Relay**	**LIVRD CBF protection**					**Conventional CBF protection**			
			t_{CBFi}	**t_{CBFd}**	**t_{CBFo}**	**t_{CBFc}**	**I_{max}**	**t_{CBFd}**	**t_{CBFo}**	**t_{CBFc}**	**I_{max}**
F1 PtP solid	DC-CB21	R24	1.650	3.900	5.900	11.200	7.826	7.950	9.950	16.050	11.385

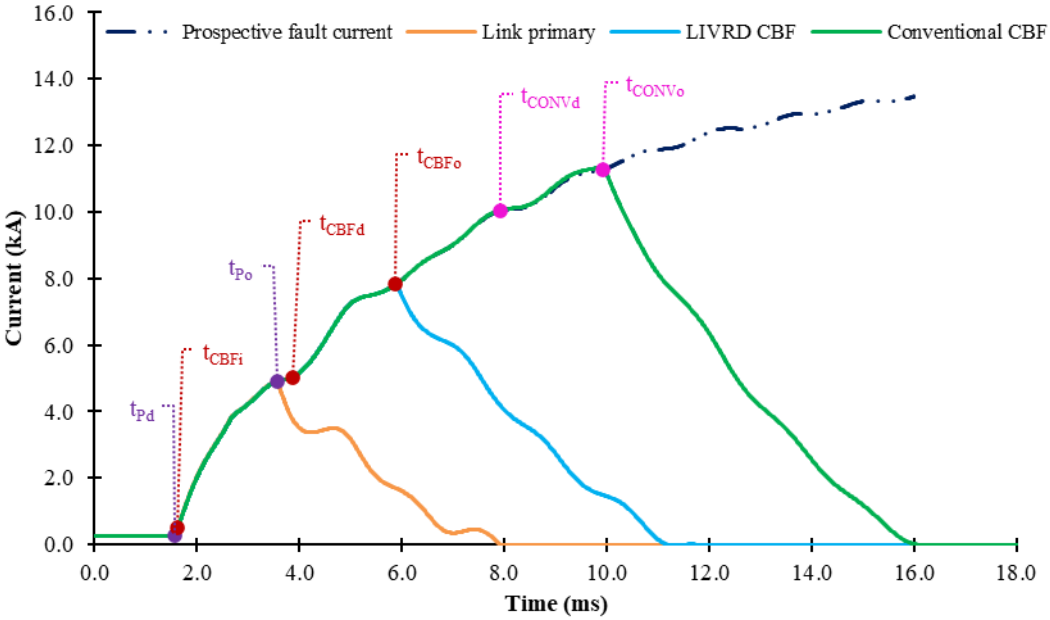


Figure 5.27.- Fault current induced by a solid PtP F1 fault with failure of DC-CB21 during operation of LIVRD link primary protection, LIVRD circuit breaker failure protection and conventional circuit breaker failure protection.

5.3. Conclusion

In this chapter, the proposed LIVRD protection scheme has been analysed in comparison with common local-measurement-based algorithms found in the literature. This way, primary link protection and circuit breaker failure protection are considered. The comparison outlines the benefits of the proposed LIVRD algorithm. Hereunder, the main conclusions of the link primary protection comparison are summarised.

The novel LIVRD algorithm proposed in this thesis is able to detect up to 250 Ω faults regardless of the fault type, resistance and location. Thus, it presents a fast, sensitive and selective performance against all the simulated fault cases. This comparison highlights the advantageous features of the proposed LIVRD link primary protection.

Table 5.3 shows a summary of the comparison between the LIVRD link primary protection and other existing local-measurement-based algorithms. The results indicate that the most similar algorithms to the proposed one in term of operation speed, are the derivative-based algorithms, i.e., the ROCOC and ROCOV algorithms. However, the ROCOC algorithm is not sensitive to high-resistance faults, while the ROCOV algorithm presents lower sensitivity to high-resistance PtG faults than the proposed LIVRD algorithm. On the other hand, the inductor-voltage algorithm presents fast operation against solid faults but low sensitivity to high-resistance faults. The undervoltage algorithm is more sensitive to high-resistance faults than the inductor-voltage algorithm but its detection speed is considerably affected during high-resistance faults. Meanwhile, the overcurrent algorithm presents better sensitivity to high-resistance faults than the two previously-mentioned voltage-measurement-based algorithms, while its operations speed is the slowest among the analysed algorithms. However, the overcurrent algorithm is not as sensitive to high-resistance faults as the proposed LIVRD algorithm. Therefore, it can be concluded that the proposed LIVRD link primary protection presents better attributes for fault detection regardless of the fault characteristics than existing local-measurement-based algorithms.

The performance of the novel LIVRD circuit breaker failure protection proposed in this thesis has also been compared with a conventional circuit breaker failure protection. Conventional circuit breaker failure protections commonly wait until the estimated fault clearing time of the link primary protection passes to evaluate if the fault has been cleared or remains affecting the system. Meanwhile, the proposed LIVRD circuit breaker failure protection is capable of detecting the proper or improper operation of a DC-CB in a time range of hundreds of microseconds after the operation time of the link primary protection by first detecting a backward fault and, then, analysing the voltage-derivative value. This feature makes the proposed LIVRD circuit breaker failure protection much faster than the conventional one. A

higher fault detection and operation speed allows interrupting lower fault currents and, thus, employing circuit breakers with lower fault current interruption capability which also reduces the installation costs of a MTDC grid.

Table 5.3.- Summary of the comparison between the proposed LIVRD link primary protection and other existing local-measurement-based algorithms.

Algorithm	**Fault resistance**		**Fault detection time**
	PtG faults	**PtP faults**	
Overcurrent algorithm	Up to 50 Ω	Up to 150 Ω	0.330-4.310 ms
Undervoltage algorithm	Up to 50 Ω	Up to 100 Ω	0.010-2.375 ms
Inductor-voltage algorithm	Solid faults	Solid faults	0.010-1.655 ms
ROCOC algorithm	Solid faults	Solid faults	0.050-1.200 ms
ROCOV algorithm	Up to 150 Ω	Up to 250 Ω	0.050-1.150 ms
LIVRD algorithm	***Up to 250 Ω***	***Up to 250 Ω***	***0.050-1.150 ms***

Chapter 6.

CONCLUSIONS AND FUTURE WORK

This chapter summarizes the main conclusions extracted from the work presented in this thesis. Moreover, several research lines for future work which have been identified during the progress of this thesis are also presented.

6.1. Conclusions

This thesis has been focused in analysing one of the most complex challenges related to the development of MTDC grids, i.e., fault protection. Therefore, the most relevant concepts regarding fault protection of MTDC grids have been presented and reviewed. This way, the state of the art of the research has been extracted from Chapter 2. Protection systems applied to MTDC grids tend to employ 100 mH limiting inductors, a full-selective strategy, H-CBs and local-measurement-based algorithms. Besides, MTDC grids are usually composed of half-bridge MMCs while the system could be configured as a bipole or as a symmetric-monopole. Moreover, the combined operation of different protection methods can benefit the performance of the protection system.

Accordingly, this thesis has proposed in Chapter 3 a novel fault protection algorithm, which has been theoretically defined and thoroughly evaluated through simulations in a four-terminal MTDC grid model. The proposed LIVRD algorithm is based on local voltage measurements, which are taken at both sides of the limiting inductors. This way, the proposed LIVRD algorithm is an inductor-voltage-based

protection method, which can satisfy the critical requirement of operation speed related to VSC-based grids. When a fault occurs, the damping characteristic of the limiting inductor produces a difference of voltage, which is used by the proposed LIVRD algorithm as a fault marker. The ratio between the voltage measurements at the link-side and at the bus-side of the limiting inductor and its derivative are calculated. Hence, the voltage-ratio-derivate, VRD, is in charge of fast fault detection while the voltage-ratio, VR, locates the fault, thus, confirming backward or forward fault detection to the corresponding protection zone.

Moreover, a threshold selection methodology for local-measurement-based fault protection algorithms has been proposed in this thesis. This methodology starts by analysing the worst fault case scenarios for the proposed LIVRD algorithm to extract the critical values and to select an initial threshold value. Then, transients induced by the opening of a circuit breaker have been taken into account in order to update the initial threshold value (if necessary). This way, adequate threshold values can be selected ensuring the selective operation of the corresponding local-measurement-based algorithm.

The proposed LIVRD algorithm is capable of quickly detecting faults while selectively discriminating between forward and backward faults as it has been demonstrated in Chapter 4. Additionally, it presents high sensitivity to high-resistance faults (up to 250 Ω). Moreover, the interesting features of the novel LIVRD algorithm proposed in this thesis have been employed to develop a complete protection scheme. It comprises link primary protection, link backup protection, busbar protection and circuit breaker failure protection.

- Link primary protection: fast and selective operation against all faults located in the link. It operates when the VRD algorithm detects a fault and the VR algorithm confirms it is a forward fault.

- Link backup protection: it operates when the link primary protection does not achieve fault detection due to a malfunctioning relay. It operates when all the neighbouring relays detect a backward fault. A trip signal is sent to the circuit breaker placed in the affected link, so the fault is properly cleared. Its operation speed is slightly slower than the link primary protection.

- Busbar protection: operation against internal busbar faults. It operates when a backward fault is detected by all the relays interconnected to the affected busbar. The operation is fast due to employing only local measurements.

- Circuit breaker failure protection: detection of improper operation of a circuit breaker. Besides the VR and VRD algorithms, it also employs the voltage-derivative ($ROCOV_{bus}$) calculation in order to verify the correct operation of the corresponding circuit breaker. Trip signals are sent to all the neighbouring

circuit breakers connected to the same bus of the malfunctioning circuit breaker in order to properly clear the fault.

Moreover, this thesis has also proposed a novel circuit breaker failure protection, applied to DC-CBs, which only uses local measurements and presents faster operation than conventional circuit breaker failure protections. The proposed LIVRD circuit breaker failure protection is able to detect the malfunctioning operation of a circuit breaker without waiting until link primary protection's estimated fault clearing time has passed. This feature implies important time savings and, thus, a reduction of the maximum fault current in the moment of interruption. This way, circuit breakers with lower current interruption capabilities can be implemented in the system, which also reduces the installation costs.

The fast, selective and sensitive operation of the proposed protection scheme has been demonstrated and the influence of relevant parameters in its performance has also been evaluated. These parameters include limiting inductor size, sampling frequency and measurement noise disturbance as well as fault location and fault resistance. The most important outcomes of the performed evaluation are cited hereunder. The effect of the inductor size is negligible, so the proposed protection scheme can accurately operate with typical 100 mH limiting inductors. Meanwhile, the effects of the fault resistance and sampling frequency are significant. High-resistance faults are more complex to detect due to attenuation; the fault protection algorithm's sensitivity to high-resistance faults and, thus, proper fault detection depends on the selected threshold value. Moreover, a high sampling frequency amplifies the difference between VRD values during internal fault conditions and during normal operation or external fault conditions. This way, fault detection can be more easily achieved with a high-sampling frequency. The fault location also affects its operation, but increasing the sampling frequency can adapt the LIVRD protection scheme to longer distances to fault. However, the LIVRD fault protection algorithm can correctly operate with a relatively low sampling frequency of 20 kHz. Additionally, the performance of the LIVRD protection scheme has also been validated for SNRs in the measured magnitudes above 40 dB for the link primary protection and above 50 dB for the reverse-reach-based algorithms (link backup, busbar and circuit breaker failure protection).

Therefore, the advantages of the LIVRD fault protection algorithm have been highlighted while it has been demonstrated that it overcomes the limitations found in the common and conventional fault protection algorithms. These advantageous features are fast, selective and sensitive operation regardless of the fault characteristics, i.e., fault type, fault resistance and fault location.

6.2. Future research lines

Some possible future research lines have been identified from the work carried out in this thesis:

- Application to fault type identification: The proposed LIVRD algorithm could be adapted in order to identify which type of fault is affecting the system since a protection system capable of distinguishing the different fault types presents a significant feature for its application in bipole systems. Discriminating between PtP and PtG faults is important for systems configured as a bipole, where only the affected pole (in case of a PtG fault) is isolated; power transmission continues through the healthy pole and the ground return cable as an asymmetric-monopole configuration.

- Application to H-CB with pro-active control: the novel LIVRD protection scheme proposed in this thesis can be implemented together with a H-CB with pro-active control. The joint operation of these two elements might be beneficial for the protection system in terms of operation speed, especially in the case of circuit breaker failure protection. The pro-active control can be initiated at the same time than the LIVRD circuit breaker failure protection, i.e., after backward fault detection. Then, the time needed for the H-CB to commutate the fault current to the main breaker branch can be employed by the LIVRD circuit breaker failure protection to verify the DC-CB operation. This way, the joint operation of the pro-active control and the LIVRD circuit breaker failure protection will save some milliseconds in the process of current interruption, improving the operation speed and reducing the maximum current interrupted.

- Real time/prototype implementation and testing of the proposed fault protection scheme.

- Interaction of the proposed fault protection scheme with other converter topologies, such as fault-blocking converters, and with converter control.

- Application to Medium Voltage (MV) DC systems: DC systems have been gaining relevance in distribution levels in recent years. Thus, the performance of protection systems in MVDC grids should be analysed as well as the application of different fault protection algorithms, since the ones employed in HVDC systems might present some limitations when applied to MVDC grids and not properly carry out their purpose.

APPENDICES

A. Four-terminal MMC-based grid model

This thesis validates the performance of the proposed LIVRD protection scheme through PSCAD simulations. The study cases have been simulated employing the system model presented in [187] and available in [226]. The four-terminal grid depicted in Figure A.1 is modelled in PSCAD.

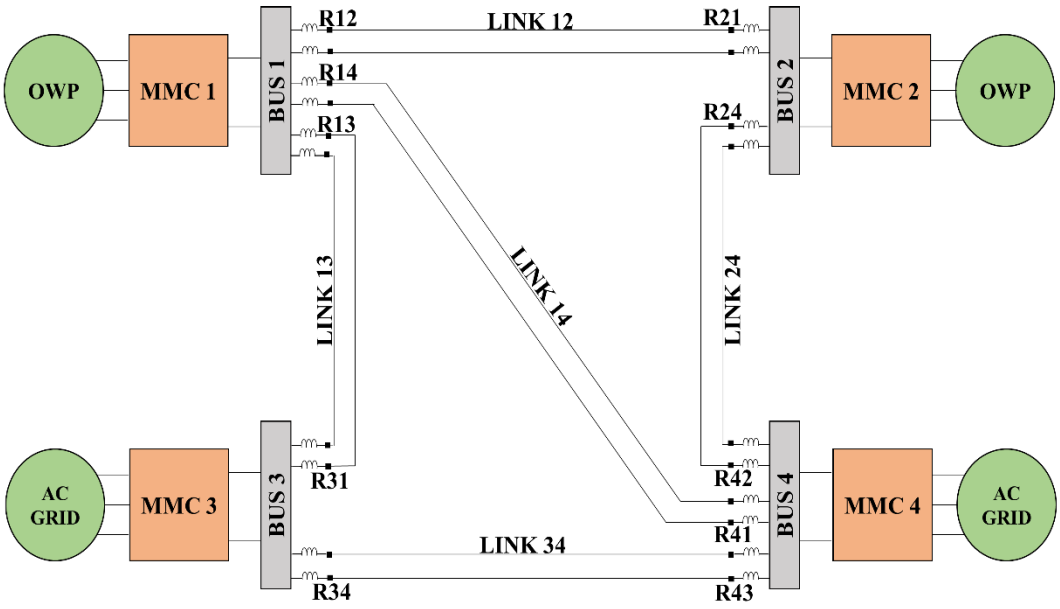


Figure A.1.- Scheme of the four-terminal grid modelled in PSCAD.

Two onshore AC grids are interconnected to two offshore wind power plants through five undersea cables, which are 320 kV XLPE insulated cables and are

modelled using frequency dependent models. Links 12 and 34 are 100 km long, links 13 and 14 have a length of 200 km while the length of link 34 is 150 km. The cables comprise a core conductor, a lead sheath and steel armor, with intermediate insulation layers. The constant resistivity of the ground return is 1 Ωm, the cable's surge impedance is 33.73 Ω and the wave propagation speed is 183.5 km/ms. Cable geometry and parameters are shown in Table A.1.

Table A.1.- Parameters of XLPE cables.

Parameters	Radius (mm)	Resistivity (Ωm)	Relative Permittivity	Relative Permeability
Core	19.5	$1.68 \cdot 10^{-8}$	-	1
Insulation	48.7	-	2.3	1
Sheath	51.7	$2.2 \cdot 10^{-7}$	-	1
Insulation	54.7	-	2.3	1
Armor	58.7	$1.8 \cdot 10^{-7}$	-	10
Insulation	63.7	-	2.3	1

Four HB-MMC converters are modelled and implemented in the MTDC system. HB-MMCs do not present fault-blocking capability, so if their internal overcurrent protection is triggered, the submodules are blocked and they become uncontrolled-rectifiers. MMCs 1, 2 and 3 present a rated power of 900 MVA while the rated power of MMC 4 is 1200 MVA. Table A.2 summarizes the most relevant parameters of each MMC.

Table A.2.- Parameters of half-bridge modular multilevel converters.

Parameters	MMC 1, 2, 3	MMC 4
Rated power (MVA)	900	1200
AC converter side voltage (kV)	380	380
Arm capacitance (μF)	29.3	39
Arm inductor (mH)	84.8	63.6
Arm resistance (Ω)	0.885	0.67
Bus filter inductor (mH)	10	10

The system is configured as a symmetric-monopole with a DC pole-to-ground voltage of 320 kV. A full-selective fault-clearing strategy is adopted; DC-CBs and 100 mH limiting inductors are located at both ends of each cable. The DC-CB model implemented in the system basically comprises a switch in parallel with a surge arrester since these components can simply represent the performance of a DC-CB, i.e., inserting a counter voltage in order to drive the fault current to zero and absorbing the system energy. An operating time of 2 ms is assumed, which is a

common operating time for H-CBs as it is found in the literature. The surge arrester presents a rated voltage of 480 kV which is 150% of the DC pole-to-ground voltage.

B. Comparison between the LIVRD algorithm and existing algorithms

This appendix shows additional results from the comparison carried out in Chapter 5. Hereunder, results from each comparison between the novel LIVRD algorithm proposed in this thesis and existing algorithms are summarized in Tables B.1 to B.5. Fault detection time of each algorithm is indicated from fault inception in milliseconds, e.g., a fault detection time of 0.5 ms means the fault has been detected at 1.5 ms (fault inception time + fault detection time). Moreover, the maximum fault current interrupted by the circuit breakers is displayed in the "Maximum current" column. Failure in detecting the fault case is represented by an "X".

B.1. Overcurrent algorithm

Table B.1.- Operation of the OC and LIVRD algorithms for different fault locations and resistances. [Part 1 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			OC		LIVRD		OC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
0 Ω	0 km	R14	0.340	5.569	0.050	4.990	0.330	6.194	0.050	5.578
		R41	1.810	4.851	1.150	4.386	1.780	5.727	1.150	4.978
	25 km	R14	0.330	5.198	0.150	5.033	0.330	5.727	0.150	5.535
		R41	1.620	4.667	1.000	4.551	1.600	5.483	1.000	5.149
	50 km	R14	0.490	4.959	0.300	4.899	0.490	5.365	0.300	5.238
		R41	1.440	4.492	0.850	4.348	1.420	5.211	0.850	4.940
	75 km	R14	0.640	5.446	0.450	5.029	0.640	5.680	0.450	5.373
		R41	1.260	4.321	0.700	3.992	1.240	4.897	0.700	4.576
	100 km	R14	0.800	4.949	0.600	4.726	0.800	5.277	0.600	5.217
		R41	1.080	4.419	0.600	3.730	1.070	4.884	0.600	4.232
	125 km	R14	0.960	5.141	0.700	4.982	0.960	5.589	0.700	5.542
		R41	0.900	4.825	0.450	4.001	0.890	5.377	0.450	4.356
	150 km	R14	1.120	5.371	0.850	5.323	1.120	5.876	0.850	5.892
		R41	0.720	4.535	0.300	3.912	0.720	5.392	0.300	4.287
	175 km	R14	1.280	5.640	1.000	5.516	1.280	6.168	1.000	6.091
		R41	0.890	5.049	0.150	4.063	0.860	6.170	0.150	4.622
	200 km	R14	1.450	5.791	1.150	5.346	1.440	6.334	1.150	5.922
		R41	0.850	5.397	0.050	3.994	0.780	6.516	0.050	4.634

Table B.1.- Operation of the OC and LIVRD algorithms for different fault locations and resistances. [Part 2 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			OC		LIVRD		OC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
50 Ω	0 km	R14	1.070	3.193	0.050	2.342	0.630	4.266	0.050	3.415
		R41	3.120	1.694	1.150	1.500	2.280	3.246	1.150	2.635
	25 km	R14	1.220	3.173	0.150	2.303	0.750	4.252	0.150	3.334
		R41	2.930	1.828	1.000	1.538	2.140	3.315	1.000	2.731
	50 km	R14	1.380	3.175	0.300	2.378	0.780	4.062	0.300	3.409
		R41	2.800	1.950	0.850	1.540	1.980	3.360	0.850	2.751
	75 km	R14	1.480	3.145	0.450	2.455	0.960	4.114	0.450	3.515
		R41	2.680	2.094	0.700	1.519	1.870	3.413	0.700	2.707
	100 km	R14	1.630	3.086	0.600	2.490	1.140	4.128	0.600	3.598
		R41	2.580	2.244	0.600	1.492	1.780	3.625	0.600	2.621
	125 km	R14	1.730	3.009	0.700	2.509	1.320	4.105	0.700	3.666
		R41	2.490	2.403	0.450	1.442	1.710	3.864	0.450	2.516
	150 km	R14	1.780	2.931	0.850	2.521	1.480	4.066	0.850	3.708
		R41	2.420	2.556	0.300	1.370	1.590	4.019	0.300	2.418
	175 km	R14	1.870	2.867	1.000	2.530	1.550	3.988	1.000	3.699
		R41	2.350	2.691	0.150	1.303	1.440	4.133	0.150	2.365
	200 km	R14	1.990	2.789	1.150	2.491	1.670	3.945	1.150	3.593
		R41	2.240	2.820	0.050	1.330	1.310	4.244	0.050	2.433

Table B.1.- Operation of the OC and LIVRD algorithms for different fault locations and resistances. [Part 3 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			OC		LIVRD		OC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
100 Ω	0 km	R14	1.710	2.471	0.050	1.664	0.960	3.546	0.050	2.544
		R41	X[d]	X	1.150	0.753	2.800	2.145	1.150	1.695
	25 km	R14	1.900	2.463	0.150	1.631	1.100	3.530	0.150	2.484
		R41	X	X	1.000	0.780	2.630	2.257	1.000	1.763
	50 km	R14	2.060	2.419	0.300	1.674	1.240	3.543	0.300	2.546
		R41	X	X	0.850	0.776	2.490	2.397	0.850	1.791
	75 km	R14	2.130	2.342	0.450	1.724	1.350	3.497	0.450	2.630
		R41	X	X	0.700	0.760	2.380	2.543	0.700	1.761
	100 km	R14	2.190	2.269	0.600	1.751	1.530	3.418	0.600	2.688
		R41	X	X	0.600	0.742	2.330	2.676	0.600	1.703
	125 km	R14	2.260	2.196	0.750	1.763	1.670	3.299	0.700	2.733
		R41	X	X	0.450	0.710	2.290	2.835	0.450	1.626
	150 km	R14	2.390	2.116	0.850	1.765	1.740	3.194	0.850	2.754
		R41	X	X	0.300	0.672	2.240	3.043	0.300	1.548
	175 km	R14	2.520	2.030	1.000	1.772	1.830	3.131	1.000	2.739
		R41	3.990	1.260	0.150	0.625	2.160	3.237	0.150	1.498
	200 km	R14	2.640	1.942	1.150	1.752	1.940	3.053	1.150	2.669
		R41	3.780	1.414	0.050	0.647	1.950	3.361	0.050	1.550

Table B.1.- Operation of the OC and LIVRD algorithms for different fault locations and resistances. [Part 4 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			OC		LIVRD		OC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
150 Ω	0 km	R14	2.420	2.044	0.050	1.352	1.220	3.030	0.050	2.075
		R41	X	X	1.150	0.415	3.820	1.289	1.150	1.188
	25 km	R14	2.520	1.993	0.150	1.325	1.380	3.021	0.150	2.028
		R41	X	X	1.000	0.430	3.590	1.485	1.000	1.245
	50 km	R14	2.620	1.941	0.300	1.354	1.550	3.016	0.300	2.075
		R41	X	X	0.850	0.427	3.340	1.683	0.850	1.263
	75 km	R14	2.710	1.887	0.450	1.391	1.700	2.968	0.450	2.140
		R41	X	X	0.700	0.412	3.130	1.838	0.700	1.237
	100 km	R14	2.820	1.818	0.600	1.410	1.810	2.862	0.600	2.190
		R41	X	X	0.600	0.399	2.990	1.988	0.600	1.192
	125 km	R14	2.950	1.742	0.750	1.419	1.890	2.753	0.700	2.218
		R41	X	X	0.450	0.376	2.890	2.131	0.450	1.135
	150 km	R14	3.080	1.659	0.850	1.424	1.970	2.680	0.850	2.234
		R41	X	X	0.300	0.350	2.770	2.288	0.300	1.081
	175 km	R14	3.250	1.570	1.000	1.430	2.100	2.622	1.000	2.223
		R41	X	X	0.150	0.316	2.650	2.434	0.150	1.033
	200 km	R14	3.500	1.442	1.150	1.414	2.210	2.531	1.150	2.167
		R41	X	X	0.050	0.333	2.540	2.578	0.050	1.074

Table B.1.- Operation of the OC and LIVRD algorithms for different fault locations and resistances. [Part 5 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			OC		LIVRD		OC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
200 Ω	0 km	R14	3.050	1.661	0.050	1.173	1.480	2.674	0.050	1.781
		R41	X	X	1.150	0.219	X	X	1.150	0.871
	25 km	R14	3.200	1.603	0.150	1.150	1.660	2.664	0.150	1.742
		R41	X	X	1.000	0.233	X	X	1.000	0.917
	50 km	R14	3.340	1.537	0.300	1.172	1.840	2.623	0.300	1.780
		R41	X	X	0.850	0.230	X	X	0.850	0.932
	75 km	R14	3.460	1.475	0.450	1.201	1.960	2.548	0.450	1.833
		R41	X	X	0.750	0.218	X	X	0.700	0.908
	100 km	R14	3.670	1.392	0.600	1.215	2.030	2.466	0.600	1.872
		R41	X	X	0.600	0.206	4.010	1.331	0.600	0.871
	125 km	R14	4.150	1.235	0.750	1.222	2.100	2.389	0.750	1.899
		R41	X	X	0.450	0.190	3.490	1.577	0.450	0.826
	150 km	R14	X	X	0.900	1.229	2.220	2.328	0.850	1.909
		R41	X	X	0.300	0.166	3.310	1.734	0.300	0.783
	175 km	R14	X	X	1.000	1.234	2.340	2.249	1.000	1.900
		R41	X	X	0.150	0.140	3.200	1.884	0.150	0.744
	200 km	R14	X	X	1.150	1.222	2.450	2.152	1.150	1.854
		R41	X	X	0.050	0.154	3.060	2.026	0.050	0.777

Table B.1.- Operation of the OC and LIVRD algorithms for different fault locations and resistances. [Part 6 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			OC		LIVRD		OC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
250 Ω	0 km	R14	4.100	1.325	0.050	1.055	1.800	2.444	0.050	1.581
		R41	X	X	1.150	0.093	X	X	1.150	0.656
	25 km	R14	X	X	0.150	1.037	2.030	2.417	0.150	1.547
		R41	X	X	1.000	0.105	X	X	1.000	0.693
	50 km	R14	X	X	0.300	1.054	2.150	2.338	0.300	1.578
		R41	X	X	0.900	0.103	X	X	0.850	0.705
	75 km	R14	X	X	0.450	1.078	2.200	2.258	0.450	1.623
		R41	X	X	0.750	0.089	X	X	0.700	0.683
	100 km	R14	X	X	0.600	1.089	2.270	2.194	0.600	1.654
		R41	X	X	0.600	0.080	X	X	0.600	0.651
	125 km	R14	X	X	0.750	1.098	2.350	2.133	0.750	1.678
		R41	X	X	0.450	0.066	X	X	0.450	0.614
	150 km	R14	X	X	0.900	1.101	2.470	2.056	0.850	1.690
		R41	X	X	0.300	0.047	X	X	0.300	0.579
	175 km	R14	X	X	1.050	1.107	2.580	1.965	1.000	1.682
		R41	X	X	0.150	0.027	4.310	1.253	0.150	0.546
	200 km	R14	X	X	1.150	1.096	2.720	1.865	1.150	1.640
		R41	X	X	0.050	0.037	3.810	1.487	0.050	0.574

[a]Fault location from relay R14

[b]Detection time is the time between fault inception and fault detection by the protection algorithm

[c]Maximum current interrupted by the circuit breaker

[d]Symbol “X” means fault detection is not achieved

B.2. Undervoltage algorithm

Table B.2.- Operation of the UV and LIVRD algorithms for different fault locations and resistances. [Part 1 of 4]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			UV		LIVRD		UV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
0 Ω	0 km	R14	0.010	4.970	0.050	4.990	0.010	5.559	0.050	5.578
		R41	1.115	4.396	1.150	4.386	1.115	4.986	1.150	4.978
	25 km	R14	0.145	5.027	0.150	5.033	0.145	5.530	0.150	5.535
		R41	0.975	4.557	1.000	4.551	0.975	5.149	1.000	5.149
	50 km	R14	0.285	4.899	0.300	4.899	0.285	5.238	0.300	5.238
		R41	0.835	4.350	0.850	4.348	0.835	4.940	0.850	4.940
	75 km	R14	0.420	5.004	0.450	5.029	0.420	5.357	0.450	5.373
		R41	0.695	3.995	0.700	3.992	0.695	4.577	0.700	4.576
	100 km	R14	0.560	4.726	0.600	4.726	0.560	5.217	0.600	5.217
		R41	0.555	3.725	0.600	3.730	0.555	4.231	0.600	4.232
	125 km	R14	0.700	4.982	0.700	4.982	0.700	5.542	0.700	5.542
		R41	0.415	3.987	0.450	4.001	0.415	4.347	0.450	4.356
	150 km	R14	0.840	5.323	0.850	5.323	0.840	5.892	0.850	5.892
		R41	0.280	3.912	0.300	3.912	0.280	4.287	0.300	4.287
	175 km	R14	0.980	5.528	1.000	5.516	0.980	6.099	1.000	6.091
		R41	0.140	4.050	0.150	4.063	0.140	4.608	0.150	4.622
	200 km	R14	1.120	5.363	1.150	5.346	1.120	5.936	1.150	5.922
		R41	0.005	3.984	0.050	3.994	0.005	4.624	0.050	4.634

Table B.2.- Operation of the UV and LIVRD algorithms for different fault locations and resistances. [Part 2 of 4]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			UV		LIVRD		UV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
50 Ω	0 km	R14	0.010	2.335	0.050	2.342	0.010	3.406	0.050	3.415
		R41	1.185	1.549	1.150	1.500	1.220	2.718	1.150	2.635
	25 km	R14	0.150	2.303	0.150	2.303	0.150	3.334	0.150	3.334
		R41	1.245	1.704	1.000	1.538	1.020	2.765	1.000	2.731
	50 km	R14	0.305	2.394	0.300	2.378	0.285	3.403	0.300	3.409
		R41	1.150	1.747	0.850	1.540	0.860	2.772	0.850	2.751
	75 km	R14	0.475	2.496	0.450	2.455	0.430	3.515	0.450	3.515
		R41	0.890	1.653	0.700	1.519	0.710	2.714	0.700	2.707
	100 km	R14	0.675	0.861	0.600	2.490	0.570	3.606	0.600	3.598
		R41	0.665	1.579	0.600	1.492	0.565	2.626	0.600	2.621
	125 km	R14	0.905	2.644	0.700	2.509	0.715	3.676	0.700	3.666
		R41	0.465	1.486	0.450	1.442	0.420	2.516	0.450	2.516
	150 km	R14	1.175	2.733	0.850	2.521	0.870	3.728	0.850	3.708
		R41	0.295	1.386	0.300	1.370	0.280	2.418	0.300	2.418
	175 km	R14	1.250	2.681	1.000	2.530	1.025	3.727	1.000	3.699
		R41	0.145	1.298	0.150	1.303	0.145	2.358	0.150	2.365
	200 km	R14	1.190	2.534	1.150	2.491	1.140	3.614	1.150	3.593
		R41	0.005	1.326	0.050	1.330	0.005	2.428	0.050	2.433

Table B.2.- Operation of the UV and LIVRD algorithms for different fault locations and resistances. [Part 3 of 4]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			UV		LIVRD		UV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
100 Ω	0 km	R14	X[d]	X	0.050	1.664	0.010	2.537	0.050	2.544
		R41	X	X	1.150	0.753	1.185	1.732	1.150	1.695
	25 km	R14	X	X	0.150	1.631	0.150	2.484	0.150	2.484
		R41	X	X	1.000	0.780	1.245	1.890	1.000	1.763
	50 km	R14	X	X	0.300	1.674	0.305	2.559	0.300	2.546
		R41	X	X	0.850	0.776	1.150	1.966	0.850	1.791
	75 km	R14	X	X	0.450	1.724	0.475	2.664	0.450	2.630
		R41	X	X	0.700	0.760	0.890	1.894	0.700	1.761
	100 km	R14	X	X	0.600	1.751	0.675	2.770	0.600	2.688
		R41	X	X	0.600	0.742	0.665	1.787	0.600	1.703
	125 km	R14	X	X	0.750	1.763	0.905	2.860	0.700	2.733
		R41	X	X	0.450	0.710	0.465	1.665	0.450	1.626
	150 km	R14	X	X	0.850	1.765	1.175	2.924	0.850	2.754
		R41	X	X	0.300	0.672	0.295	1.562	0.300	1.548
	175 km	R14	X	X	1.000	1.772	1.250	2.844	1.000	2.739
		R41	X	X	0.150	0.625	0.145	1.493	0.150	1.498
	200 km	R14	X	X	1.150	1.752	1.190	2.698	1.150	2.669
		R41	X	X	0.050	0.647	0.005	1.546	0.050	1.550

Table B.2.- Operation of the UV and LIVRD algorithms for different fault locations and resistances. [Part 4 of 4]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			UV		LIVRD		UV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
150 Ω	0 km	R14	X[d]	X	0.050	1.352	2.365	3.505	0.050	2.075
		R41	X	X	1.150	0.415	1.375	1.289	1.150	1.188
	25 km	R14	X	X	0.150	1.325	2.365	3.345	0.150	2.028
		R41	X	X	1.000	0.430	1.300	1.365	1.000	1.245
	50 km	R14	X	X	0.300	1.354	2.505	3.209	0.300	2.075
		R41	X	X	0.850	0.427	1.415	1.538	0.850	1.263
	75 km	R14	X	X	0.450	1.391	X	X	0.450	2.140
		R41	X	X	0.700	0.412	1.550	1.708	0.700	1.237
	100 km	R14	X	X	0.600	1.410	1.755	2.854	0.600	2.190
		R41	X	X	0.600	0.399	1.755	1.880	0.600	1.192
	125 km	R14	X	X	0.750	1.419	1.560	2.672	0.700	2.218
		R41	X	X	0.450	0.376	X	X	0.450	1.135
	150 km	R14	X	X	0.850	1.424	1.425	2.488	0.850	2.234
		R41	X	X	0.300	0.350	2.505	2.294	0.300	1.081
	175 km	R14	X	X	1.000	1.430	1.310	2.327	1.000	2.223
		R41	X	X	0.150	0.316	2.365	2.417	0.150	1.033
	200 km	R14	X	X	1.150	1.414	1.400	2.252	1.150	2.167
		R41	X	X	0.050	0.333	2.375	2.566	0.050	1.074

[a]Fault location from relay R14

[b]Detection time is the time between fault inception and fault detection by the protection algorithm

[c]Maximum current interrupted by the circuit breaker

[d]Symbol “X” means fault detection is not achieved

B.3. Inductor-voltage algorithm

Table B.3.- Operation of the LV and LIVRD algorithms for different fault locations and resistances. [Part 1 of 3]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			LV		LIVRD		LV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
0 Ω	0 km	R14	0.010	4.970	0.050	4.990	0.010	5.559	0.050	5.578
		R41	1.130	4.423	1.150	4.386	1.130	4.986	1.150	4.978
	25 km	R14	0.145	5.027	0.150	5.033	0.145	5.530	0.150	5.535
		R41	0.985	4.569	1.000	4.551	0.985	5.149	1.000	5.149
	50 km	R14	0.285	4.899	0.300	4.899	0.285	5.238	0.300	5.238
		R41	0.840	4.352	0.850	4.348	0.840	4.940	0.850	4.940
	75 km	R14	0.425	5.017	0.450	5.029	0.425	5.365	0.450	5.373
		R41	0.700	3.999	0.700	3.992	0.700	4.577	0.700	4.576
	100 km	R14	0.565	4.732	0.600	4.726	0.565	5.218	0.600	5.217
		R41	0.560	3.730	0.600	3.730	0.560	4.231	0.600	4.232
	125 km	R14	0.705	4.985	0.700	4.982	0.705	0.535	0.700	5.542
		R41	0.420	4.001	0.450	4.001	0.420	4.347	0.450	4.356
	150 km	R14	0.845	5.325	0.850	5.323	0.845	5.891	0.850	5.892
		R41	0.280	3.912	0.300	3.912	0.280	4.287	0.300	4.287
	175 km	R14	0.990	5.539	1.000	5.516	0.990	6.106	1.000	6.091
		R41	0.140	4.050	0.150	4.063	0.140	4.608	0.150	4.622
	200 km	R14	1.135	5.390	1.150	5.346	1.135	5.957	1.150	5.922
		R41	0.005	3.984	0.050	3.994	0.005	4.624	0.050	4.634

Table B.3.- Operation of the LV and LIVRD algorithms for different fault locations and resistances. [Part 2 of 3]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			LV		LIVRD		LV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
50 Ω	0 km	R14	X[d]	X	0.050	2.342	X	X	0.050	3.415
		R41	X	X	1.150	1.500	1.330	2.718	1.150	2.635
	25 km	R14	X	X	0.150	2.303	0.555	3.340	0.150	3.334
		R41	X	X	1.000	1.538	1.270	2.765	1.000	2.731
	50 km	R14	X	X	0.300	2.378	0.310	3.431	0.300	3.409
		R41	X	X	0.850	1.540	1.590	2.772	0.850	2.751
	75 km	R14	X	X	0.450	2.455	0.515	3.598	0.450	3.515
		R41	X	X	0.700	1.519	1.605	2.714	0.700	2.707
	100 km	R14	X	X	0.600	2.490	X	X	0.600	3.598
		R41	X	X	0.600	1.492	X	X	0.600	2.621
	125 km	R14	X	X	0.700	2.509	1.655	4.291	0.700	3.666
		R41	X	X	0.450	1.442	0.500	2.516	0.450	2.516
	150 km	R14	X	X	0.850	2.521	X	X	0.850	3.708
		R41	X	X	0.300	1.370	0.305	2.418	0.300	2.418
	175 km	R14	X	X	1.000	2.530	1.280	3.843	1.000	3.699
		R41	X	X	0.150	1.303	0.150	2.358	0.150	2.365
	200 km	R14	X	X	1.150	2.491	X	X	1.150	3.593
		R41	X	X	0.050	1.330	X	X	0.050	2.433

Table B.3.- Operation of the LV and LIVRD algorithms for different fault locations and resistances. [Part 3 of 3]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			LV		LIVRD		LV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
100 Ω	0 km	R14	X	X	0.050	1.664	X	X	0.050	2.544
		R41	X	X	1.150	0.753	X	X	1.150	1.695
	25 km	R14	X	X	0.150	1.631	X	X	0.150	2.484
		R41	X	X	1.000	0.780	X	X	1.000	1.763
	50 km	R14	X	X	0.300	1.674	X	X	0.300	2.546
		R41	X	X	0.850	0.776	X	X	0.850	1.791
	75 km	R14	X	X	0.450	1.724	X	X	0.450	2.630
		R41	X	X	0.700	0.760	X	X	0.700	1.761
	100 km	R14	X	X	0.600	1.751	X	X	0.600	2.688
		R41	X	X	0.600	0.742	X	X	0.600	1.703
	125 km	R14	X	X	0.750	1.763	X	X	0.700	2.733
		R41	X	X	0.450	0.710	X	X	0.450	1.626
	150 km	R14	X	X	0.850	1.765	X	X	0.850	2.754
		R41	X	X	0.300	0.672	X	X	0.300	1.548
	175 km	R14	X	X	1.000	1.772	X	X	1.000	2.739
		R41	X	X	0.150	0.625	X	X	0.150	1.498
	200 km	R14	X	X	1.150	1.752	X	X	1.150	2.669
		R41	X	X	0.050	0.647	X	X	0.050	1.550

[a]Fault location from relay R14

[b]Detection time is the time between fault inception and fault detection by the protection algorithm

[c]Maximum current interrupted by the circuit breaker

[d]Symbol “X” means fault detection is not achieved

B.4. Rate-of-change-of-current algorithm

Table B.4.- Operation of the ROCOC and LIVRD algorithms for different fault locations and resistances. [Part 1 of 2]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOC		LIVRD		ROCOC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
0 Ω	0 km	R14	0.050	5.029	0.050	4.990	0.050	5.615	0.050	5.578
		R41	1.200	4.494	1.150	4.386	1.200	5.070	1.150	4.978
	25 km	R14	0.200	5.055	0.150	5.033	0.200	5.556	0.150	5.535
		R41	1.050	4.604	1.000	4.551	1.050	5.181	1.000	5.149
	50 km	R14	0.350	4.900	0.300	4.899	0.350	5.236	0.300	5.238
		R41	0.900	4.365	0.850	4.348	0.900	4.937	0.850	4.940
	75 km	R14	0.500	5.103	0.450	5.029	0.500	5.419	0.450	5.373
		R41	0.750	4.027	0.700	3.992	0.750	4.584	0.700	4.576
	100 km	R14	0.600	4.769	0.600	4.726	0.600	5.225	0.600	5.217
		R41	0.600	3.764	0.600	3.730	0.600	4.240	0.600	4.232
	125 km	R14	0.750	5.007	0.700	4.982	0.750	5.544	0.700	5.542
		R41	0.450	4.078	0.450	4.001	0.450	4.409	0.450	4.356
	150 km	R14	0.900	5.334	0.850	5.323	0.900	5.884	0.850	5.892
		R41	0.350	3.920	0.300	3.912	0.350	4.300	0.300	4.287
	175 km	R14	1.050	5.575	1.000	5.516	1.050	6.128	1.000	6.091
		R41	0.200	4.088	0.150	4.063	0.200	4.648	0.150	4.622
	200 km	R14	1.200	5.449	1.150	5.346	1.200	6.006	1.150	5.922
		R41	0.050	4.056	0.050	3.994	0.050	4.696	0.050	4.634

Table B.4.- Operation of the ROCOC and LIVRD algorithms for different fault locations and resistances. [Part 2 of 2]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOC		LIVRD		ROCOC		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
50 Ω	0 km	R14	X[d]	X	0.050	2.342	X	X	0.050	3.415
		R41	X	X	1.150	1.500	X	X	1.150	2.635
	25 km	R14	X	X	0.150	2.303	0.200	3.395	0.150	3.334
		R41	X	X	1.000	1.538	1.350	2.935	1.000	2.731
	50 km	R14	X	X	0.300	2.378	0.350	3.475	0.300	3.409
		R41	X	X	0.850	1.540	1.650	3.235	0.850	2.751
	75 km	R14	X	X	0.450	2.455	0.550	3.632	0.450	3.515
		R41	X	X	0.700	1.519	1.650	3.335	0.700	2.707
	100 km	R14	X	X	0.600	2.490	X	X	0.600	3.598
		R41	X	X	0.600	1.492	X	X	0.600	2.621
	125 km	R14	X	X	0.700	2.509	1.700	4.305	0.700	3.666
		R41	X	X	0.450	1.442	0.550	2.648	0.450	2.516
	150 km	R14	X	X	0.850	2.521	X	X	0.850	3.708
		R41	X	X	0.300	1.370	0.350	2.494	0.300	2.418
	175 km	R14	X	X	1.000	2.530	1.350	3.861	1.000	3.699
		R41	X	X	0.150	1.303	0.200	2.420	0.150	2.365
	200 km	R14	X	X	1.150	2.491	X	X	1.150	3.593
		R41	X	X	0.050	1.330	X	X	0.050	2.433

[a]Fault location from relay R14

[b]Detection time is the time between fault inception and fault detection by the protection algorithm

[c]Maximum current interrupted by the circuit breaker

[d]Symbol “X” means fault detection is not achieved

B.5. Rate-of-change-of-voltage algorithm

Table B.5.- Operation of the ROCOV and LIVRD algorithms for different fault locations and resistances. [Part 1 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOV		LIVRD		ROCOV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
0 Ω	0 km	R14	0.050	4.990	0.050	4.990	0.050	5.578	0.050	5.578
		R41	1.150	4.386	1.150	4.386	1.150	4.978	1.150	4.978
	25 km	R14	0.150	5.033	0.150	5.033	0.150	5.535	0.150	5.535
		R41	1.000	4.551	1.000	4.551	1.000	5.144	1.000	5.149
	50 km	R14	0.300	4.899	0.300	4.899	0.300	5.238	0.300	5.238
		R41	0.850	4.348	0.850	4.348	0.850	4.940	0.850	4.940
	75 km	R14	0.450	5.029	0.450	5.029	0.450	5.373	0.450	5.373
		R41	0.700	3.999	0.700	3.992	0.700	4.577	0.700	4.576
	100 km	R14	0.600	4.726	0.600	4.726	0.600	5.217	0.600	5.217
		R41	0.600	3.730	0.600	3.730	0.600	4.232	0.600	4.232
	125 km	R14	0.700	4.982	0.700	4.982	0.700	5.542	0.700	5.542
		R41	0.450	4.001	0.450	4.001	0.450	4.356	0.450	4.356
	150 km	R14	0.850	5.323	0.850	5.323	0.850	5.892	0.850	5.892
		R41	0.300	3.912	0.300	3.912	0.300	4.287	0.300	4.287
	175 km	R14	1.000	5.528	1.000	5.516	1.000	6.099	1.000	6.091
		R41	0.150	4.063	0.150	4.063	0.150	4.622	0.150	4.622
	200 km	R14	1.150	5.346	1.150	5.346	1.150	5.922	1.150	5.922
		R41	0.050	3.994	0.050	3.994	0.050	4.634	0.050	4.634

Table B.5.- Operation of the ROCOV and LIVRD algorithms for different fault locations and resistances. [Part 2 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOV		LIVRD		ROCOV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
50 Ω	0 km	R14	0.050	2.342	0.050	2.342	0.050	3.415	0.050	3.415
		R41	1.150	1.500	1.150	1.500	1.150	2.635	1.150	2.635
	25 km	R14	0.150	2.303	0.150	2.303	0.150	3.334	0.150	3.334
		R41	1.000	1.546	1.000	1.538	1.000	2.738	1.000	2.731
	50 km	R14	0.300	2.378	0.300	2.378	0.300	3.409	0.300	3.409
		R41	0.850	1.540	0.850	1.540	0.850	2.758	0.850	2.751
	75 km	R14	0.450	2.455	0.450	2.455	0.450	3.515	0.450	3.515
		R41	0.700	1.519	0.700	1.519	0.700	2.707	0.700	2.707
	100 km	R14	0.600	2.498	0.600	2.490	0.600	3.606	0.600	3.598
		R41	0.600	1.492	0.600	1.492	0.600	2.621	0.600	2.621
	125 km	R14	0.750	2.516	0.700	2.509	0.700	3.666	0.700	3.666
		R41	0.450	1.442	0.450	1.442	0.450	2.516	0.450	2.516
	150 km	R14	0.850	2.521	0.850	2.521	0.850	3.708	0.850	3.708
		R41	0.300	1.380	0.300	1.370	0.300	2.418	0.300	2.418
	175 km	R14	1.000	2.530	1.000	2.530	1.000	3.699	1.000	3.699
		R41	0.150	1.303	0.150	1.303	0.150	2.365	0.150	2.365
	200 km	R14	1.150	2.491	1.150	2.491	1.150	3.600	1.150	3.593
		R41	0.050	1.330	0.050	1.330	0.050	2.433	0.050	2.433

Table B.5.- Operation of the ROCOV and LIVRD algorithms against different for locations and resistances. [Part 3 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOV		LIVRD		ROCOV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
100 Ω	0 km	R14	0.050	1.664	0.050	1.664	0.050	2.544	0.050	2.544
		R41	1.150	0.758	1.150	0.753	1.150	1.695	1.150	1.695
	25 km	R14	0.150	1.631	0.150	1.631	0.150	2.484	0.150	2.484
		R41	1.000	0.784	1.000	0.780	1.000	1.768	1.000	1.763
	50 km	R14	0.300	1.674	0.300	1.674	0.300	2.546	0.300	2.546
		R41	0.850	0.781	0.850	0.776	0.850	1.791	0.850	1.791
	75 km	R14	0.450	1.724	0.450	1.724	0.450	2.630	0.450	2.630
		R41	0.750	0.765	0.700	0.760	0.700	1.761	0.700	1.761
	100 km	R14	0.600	1.751	0.600	1.751	0.600	2.696	0.600	2.688
		R41	0.600	0.748	0.600	0.742	0.600	1.703	0.600	1.703
	125 km	R14	0.750	1.763	0.750	1.763	0.750	2.739	0.700	2.733
		R41	0.450	0.717	0.450	0.710	0.450	1.626	0.450	1.626
	150 km	R14	0.850	1.770	0.850	1.765	0.850	2.754	0.850	2.754
		R41	0.300	0.672	0.300	0.672	0.300	1.557	0.300	1.548
	175 km	R14	1.000	1.781	1.000	1.772	1.000	2.739	1.000	2.739
		R41	0.150	0.625	0.150	0.625	0.150	1.498	0.150	1.498
	200 km	R14	1.150	1.756	1.150	1.752	1.150	2.669	1.150	2.669
		R41	0.050	0.647	0.050	0.647	0.050	1.550	0.050	1.550

Table B.5.- Operation of the ROCOV and LIVRD algorithms for different fault locations and resistances. [Part 4 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOV		LIVRD		ROCOV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
150 Ω	0 km	R14	0.050	1.352	0.050	1.352	0.050	2.075	0.050	2.075
		R41	1.150	0.418	1.150	0.415	1.150	1.191	1.150	1.188
	25 km	R14	0.200	1.330	0.150	1.325	0.150	2.028	0.150	2.028
		R41	X[d]	X	1.000	0.430	1.000	1.249	1.000	1.245
	50 km	R14	0.300	1.354	0.300	1.354	0.300	2.075	0.300	2.075
		R41	0.900	0.438	0.850	0.427	0.850	1.263	0.850	1.263
	75 km	R14	0.450	1.391	0.450	1.391	0.450	2.140	0.450	2.140
		R41	0.750	0.420	0.700	0.412	0.700	1.237	0.700	1.237
	100 km	R14	0.600	1.414	0.600	1.410	0.600	2.190	0.600	2.190
		R41	0.600	0.403	0.600	0.399	0.600	1.192	0.600	1.192
	125 km	R14	0.750	1.422	0.750	1.419	0.750	2.223	0.700	2.218
		R41	0.450	0.381	0.450	0.376	0.450	1.135	0.450	1.135
	150 km	R14	0.900	1.431	0.850	1.424	0.850	2.239	0.850	2.234
		R41	0.300	0.350	0.300	0.350	0.300	1.081	0.300	1.081
	175 km	R14	X	X	1.000	1.430	1.000	2.226	1.000	2.223
		R41	0.150	0.316	0.150	0.316	0.150	1.033	0.150	1.033
	200 km	R14	1.150	1.417	1.150	1.414	1.150	2.167	1.150	2.167
		R41	0.050	0.333	0.050	0.333	0.050	1.074	0.050	1.074

Table B.5.- Operation of the ROCOV and LIVRD algorithms for different fault locations and resistances. [Part 5 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOV		LIVRD		ROCOV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
200 Ω	0 km	R14	0.050	1.173	0.050	1.173	0.050	1.781	0.050	1.781
		R41	1.150	0.224	1.150	0.219	1.150	0.873	1.150	0.871
	25 km	R14	0.200	1.154	0.150	1.150	0.150	1.742	0.150	1.742
		R41	X	X	1.000	0.233	1.000	0.921	1.000	0.917
	50 km	R14	0.300	1.176	0.300	1.172	0.300	1.780	0.300	1.780
		R41	X	X	0.850	0.230	0.850	0.936	0.850	0.932
	75 km	R14	0.450	1.204	0.450	1.201	0.450	1.833	0.450	1.833
		R41	X	X	0.750	0.218	0.750	0.913	0.700	0.908
	100 km	R14	0.600	1.221	0.600	1.215	0.600	1.872	0.600	1.872
		R41	0.600	0.213	0.600	0.206	0.600	0.876	0.600	0.871
	125 km	R14	X	X	0.750	1.222	0.750	1.899	0.750	1.899
		R41	0.450	0.195	0.450	0.190	0.450	0.831	0.450	0.826
	150 km	R14	X	X	0.900	1.229	0.850	1.913	0.850	1.909
		R41	0.300	0.166	0.300	0.166	0.300	0.783	0.300	0.783
	175 km	R14	X	X	1.000	1.234	1.000	1.906	1.000	1.900
		R41	0.150	0.140	0.150	0.140	0.150	0.744	0.150	0.744
	200 km	R14	1.150	1.224	1.150	1.222	1.150	1.857	1.150	1.854
		R41	0.050	0.154	0.050	0.154	0.050	0.777	0.050	0.777

Table B.5.- Operation of the ROCOV and LIVRD algorithms for different fault locations and resistances. [Part 6 of 6]

Fault resistance (Ω)	Fault location[a] (km)	Relay	Pole-to-Ground fault				Pole-to-Pole fault			
			ROCOV		LIVRD		ROCOV		LIVRD	
			Detection time[b] (ms)	Maximum current[c] (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)	Detection time (ms)	Maximum current (kA)
250 Ω	0 km	R14	0.050	1.055	0.050	1.055	0.050	1.581	0.050	1.581
		R41	X	X	1.150	0.093	1.150	0.656	1.150	0.656
	25 km	R14	0.200	1.040	0.150	1.037	0.150	1.547	0.150	1.547
		R41	X	X	1.000	0.105	1.000	0.699	1.000	0.693
	50 km	R14	0.350	1.061	0.300	1.054	0.300	1.578	0.300	1.578
		R41	X	X	0.900	0.103	0.900	0.713	0.850	0.705
	75 km	R14	X	X	0.450	1.078	0.450	1.623	0.450	1.623
		R41	X	X	0.750	0.089	0.750	0.687	0.700	0.683
	100 km	R14	X	X	0.600	1.089	0.600	1.654	0.600	1.654
		R41	X	X	0.600	0.080	0.600	0.656	0.600	0.651
	125 km	R14	X	X	0.750	1.098	0.750	1.682	0.750	1.678
		R41	X	X	0.450	0.066	0.450	0.619	0.450	0.614
	150 km	R14	X	X	0.900	1.101	0.900	1.693	0.850	1.690
		R41	0.300	0.051	0.300	0.047	0.300	0.579	0.300	0.579
	175 km	R14	X	X	1.050	1.107	1.050	1.687	1.000	1.682
		R41	0.150	0.027	0.150	0.027	0.150	0.546	0.150	0.546
	200 km	R14	X	X	1.150	1.096	1.150	1.642	1.150	1.640
		R41	0.050	0.037	0.050	0.037	0.050	0.574	0.050	0.574

[a]Fault location from relay R14

[b]Detection time is the time between fault inception and fault detection by the protection algorithm

[c]Maximum current interrupted by the circuit breaker

[d]Symbol “X” means fault detection is not achieved

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