This is the accepted manuscript of the article that appeared in final form in **Renewable and Sustainable Energy Reviews** 113 (2019) // Article ID 109264, which has been published in final form at https://doi.org/10.1016/j.rser.2019.109264. © 2019 Elsevier under CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/)

Power module electronics in HEV/EV applications: new trends in wide-bandgap semiconductor technologies and design aspects

A. Matallana[a,*], E. Ibarra[a], I. López[a], J. Andreu[a], J. I. Garate[a], X. Jordà[b], J. Rebollo[b]

[a] *University of the Basque Country (UPV/EHU), Plaza Ing. Torres Quevedo 1, 48013 Bilbao, Spain*
[b] *IMB-CNM (CSIC), Cerdanyola del Vallès (Bellaterra), 08193 Barcelona, Spain*

Abstract

A large number of factors such as the increasingly stringent pollutant emission policies, fossil fuel scarcity and their price volatility have increased the interest towards the partial or total electrification of current vehicular technologies. These transition of the vehicle fleet into electric is being carried out progressively. In the last decades, several technological milestones have been achieved, which range from the development of basic components to the current integrated electric drives made of silicon (Si) based power modules. In this context, the automotive industry and political and social agents are forcing the current technology of electric drives to its limits. For example, the U.S Department of Energy's goals for 2020 include the development of power converter technologies with power densities higher than 14.1 kW/kg and efficiencies greater than 98%. Additionally, target price of power converters has been set below $3.3/kW. Thus, these goals could be only achieved by using advanced semiconductor technologies. Wide-bandgap (WBG) semiconductors, and, most notably, silicon carbide (SiC) based power electronic devices, have been proposed as the most promising alternative to Si devices due to their superior material properties.

As the power module is one of the most significant component of the traction power converter, this work focuses on an in-deep review of the state of the art concerning such element, identifying the electrical requirements for the modules and the power conversion topologies that will best suit future drives. Additionally, current WBG technology is reviewed and, after a market analysis, the most suitable power semiconductor devices are highlighted. Finally, this work focuses on practical design aspects of the module, such as the layout of the module and optimum WBG based die parallelization, placement and Direct Bonded Copper (DBC) routing.

Keywords: EV, WBG, SiC, GaN, power semiconductors, power module, parallelization, parasitic inductances, layout, gate-attack, DBC, connectors.

*Corresponding author

Email addresses: asier.matallana@ehu.eus, Tel. +0034 94 601 72 43 (A. Matallana), edorta.ibarra@ehu.eus (E. Ibarra), iraide.lopez@ehu.eus (I. López), jon.andreu@ehu.eus (J. Andreu), joseignacio.garate@ehu.eus (J. I. Garate), xavier.jorda@imb-cnm.csic.es (X. Jordà), jose.rebollo@imb-cnm.csic.es (J. Rebollo)

List of acronyms

2DEG	2-D electron gas
AC	Alternating current
AMB	Active metal brazing
BJT	Bipolar junction transistor
CHB	Cascade H-bridge
DBA	Direct bonded Aluminum
DBC	Direct bonded copper
DC	Direct current
DLC	Direct lead bonding
DOE	United States Department of Energy
DSP	Digital signal processor
D-mode	Depletion mode
EMC	Electromagnetic compatibility
EMF	Electromotive force
EMI	Electromagnetic Interference
E-mode	Enhancement mode
EV	Electric vehicle
FC	Flying capacitor
FCell	Fuel cell vehicle
GHG	Greenhouse gas
HEMT	High electron mobility transistor
HEV	Hybrid electric vehicle
HSEM	High speed electric machine
HV	High voltage
HVDC	High voltage direct current
ICE	Internal combustion engine
IEA	International Energy Agency
IGBT	Insulated gate bipolar transistor
JBS	Junction barrier schottky
JFET	Junction field effect transistor
LC_{JFET}	Lateral channel junction field effect transistor
MIS-HEMT	Metal insulator semiconductor gate field effect transistor
MOSFET	Metal oxide semiconductor field effect transistor
MPS	Merged PN schottky diode
MTBF	Mean time between failures
NPC	Neutral point clamped
p-HEMT	p-GaN gate Field effect transistor
OEM	Original equipment manufacturer
PCB	Printed circuit board
PHEV	Plug-in hybrid electric vehicle
PiN	p-n diode with intrinsic region
PM	Permanent magnet
PMSM	Permanent magnet synchronous machine
R&D	Research and development
RE	Range extended
SAE	Society of Automotive Engineers
SBD	Schottky barrier diode
SJT	Super junction transistor
TIM	Thermal interface material
UN ESCAP	United Nations Economic and Social Commission for Asia
USCAR	United States Council for Automotive Research
VT_{JFET}	Vertical trench junction field effect transistor
WBG	Wide-bandgap

List of symbols

Symbol	Description
α	Thermal expansion coefficient (K^{-1})
λ	Thermal conductivity ($W/(m \cdot K)$)
A	Area of a surface (m^2))
BD_{xy}	Body diode top or bottom (x) and number of branch (y) (-)
C_{DC}	DC-link capacitor (F)
d	Thickness of a layer (m)
D_{xy}	Diode top or bottom (x) and number of branch (y) (-)
D_b	Drain bottom connection (-)
D_t	Drain top connection (-)
G_b	Gate bottom connection (-)
G_t	Gate top connection (-)
I_{max}	Maximum semiconductor current (A)
I_{rr}	Recovery current (A)
L_o	Overall length of the material (m)
L_b	Equivalent parasitic inductance of bonding (H)
L_{bd}	Drain bottom equivalent inductance (H)
L_{bs}	Source bottom equivalent inductance (H)
L_d	Drain equivalent parasitic inductance (H)
L_{dBUS}	Drain DC-link equivalent inductance (H)
L_{DC^+x}	Equivalent parasitic inductance between x device and DC^+ power terminal (H)
L_g	Gate equivalent inductance (H)
L_{gate}	Gate loop total parasitic inductance (H)
$L_{p1-phase}$	Phase equivalent inductance of P-cell (H)
$L_{n1-phase}$	Phase equivalent inductance of N-cell (H)
L_{tg}	Gate top track equivalent inductance (H)
L_{tsaux}	Source auxiliary top track equivalent inductance (H)
L_{td}	Drain top equivalent inductance (H)
L_{ts}	Source top equivalent inductance (H)
L_s	Source auxiliary equivalent inductance (H)
L_{sBUS}	Source DC-link equivalent inductance (H)
L_{sw}	Power loop equivalent inductance (H)
L_w	Equivalent parasitic inductance of wire (H)
M_{effect}	Equivalent parasitic inductance due to mutual coupling effect (H)
M_{xj}	MOSFET top or bottom (x) and number of branch (y) (-)
n	Number of devices in parallel (-)
S_b	Source bottom connection (-)
S_{baux}	Source bottom auxiliary connection (-)
S_t	Source top connection (-)
S_{taux}	Source top auxiliary connection (-)
Q_c	Charge value of diode (C)
Q_g	Gate charge (C)
Q_{rr}	Reverse recovery charge (C)
R_{dson}	Equivalent resistance when the device is on (Ω)
R_g	Internal gate resistance (Ω)
Rg_{ext}	External gate resistance (Ω)
R_{th}	Thermal resistance (K/W)
$R_{th_{subs}}$	Substrate equivalent thermal resistance (K/W)
SW_{xy}	Switch top or bottom (x) and number of branch (y) (-)
T	Temperature (K)
t_f	Fall time of transistors (s)
T_{jmax}	Maximum junction temperature of semiconductor (K)
t_r	Rise time of transistors (s)
T_{vj}	Vehicle junction temperature (K)
V_{block}	Semiconductor maximum blocking voltage (V)
V_{DCbus}	DC-link voltage (V)
V_g	Gate voltage drop (V)
V_{gs}	Gate - source voltage (V)
V_s	Source voltage drop (V)
V_{th}	Semiconductor threshold voltage (V)

1. Introduction

The use of electric energy for propulsion is not new, as it dates back to the 19th century, when Robert Anderson designed the first non rechargeable battery powered electric vehicle. This invention was followed by other similar innovations, such as the vehicle known as "*Jamais contente*" (in the year 1899), which was the first electric vehicle (EV) able to reach 100 km/h [1]. Thus, at the dawn of road transportation, the primitive EV technology had a high market share. As a matter of fact, in the early 90s, there were more electric powered vehicles than petrol powered ones. Likewise, the first hybrid electric vehicle (HEV) was manufactured in 1911 by Woods Motor Vehicle Company. However, several factors such as the invention of the electric starter for petrol powered vehicles (which eliminated the need of a hand crank), the low price of petrol, and the continuous improvement of many relevant features of Internal Combustion Engine (ICE) based vehicles (autonomy, power, comfort, etc.) lead to the decline of electrified vehicles. Around 1935, there where practically no EVs on the road [1, 2], as the electrical technology available at the beginning of the 20th century was not developed enough to compete with the ICE. However, the reintroduction of HEV/EVs started in the late 90s thanks to the maturity of power electronics [3–5] and digital signal processor (DSP) [6, 7] technologies. Nevertheless, it was not until the beginning of the 21st century when HEV/EVs regained significant popularity [1].

The main reasons of its reintroduction where both an increasing environmental awareness and oil shortage, this last leading to high and fluctuating oil prices. the environmental forecasts are becoming more pessimistic from day to day. According to the projections of the International Energy Agency (IEA), greenhouse gas (GHG) emissions are expected to double in 2050 the 2005 levels, unless decisive actions in climate policies are taken immediately [8]. Provided that the transportation sector accounts for about 23 % of GHG emissions [9], transportation electrification is considered one of the main solutions to reduce GHG levels in the atmosphere and slow down the climate change [10]. In this context and attending to the IEA Energy Technology Perspective BLUE Map scenario, electrified vehicles (EVs and Plug-in HEVs) will contribute to reduce CO_2 emissions produced by light-duty vehicles approximately a 30 % by 2050 [8]. This implies that the sales of PHEVs and EVs vehicles are expected to reach 50 million units by 2050 (figure 1). According to the Electric Vehicle World Sales Database, the PHEV/EV global fleet reached around 5.4 million units in 2018, which represents an increase of 64 % over 2017. In [11], an additional growth of 52 % is expected by the end of 2019. Thus, the global PHEV/EV fleet would reach 8.5 million units in 2019. Therefore and up to date, these recent data and forecasts match with the long term fleet evolution prediction presented in figure 1.

In order to achieve the BLUE Map goals, the worldwide adoption of electrified vehicle technologies before 2050 is mandatory. Nevertheless, the penetration of PHEVs and EVs will depend on several factors, such as supplier technologies, retailer's offers and promotions, vehicle specifications, charging infrastructures, consumer's demand and government policies, among others [8]. Currently, government policies largely influence all the others [8]; in fact, many countries are implementing restrictive emission regulations to promote PHEVs and EVs. For instance, the Euro 6 emissions standard is mandatory in the European Union since 2014 [12, 13]. National and international programs such as Horizon 2020 [14, 15], or organizations such as the United States Council for Automo-

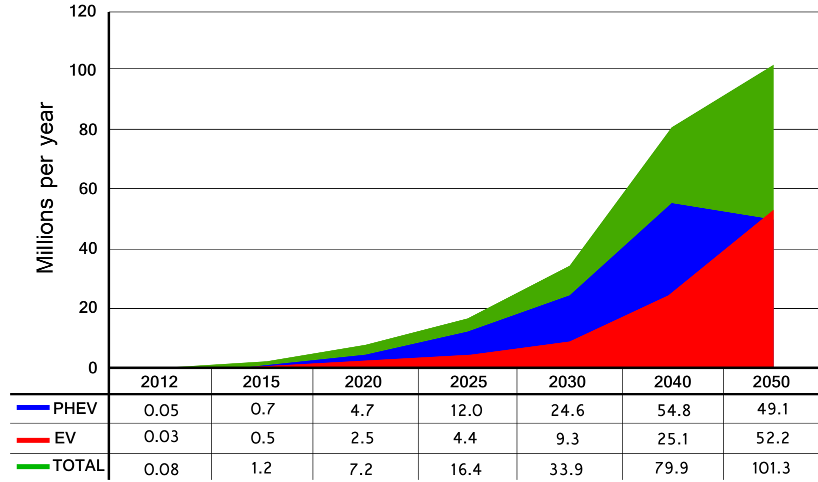


Figure 1: Worldwide EV and PHEV sales forecasted by the BLUE Map scenario (in millions per year) [8].

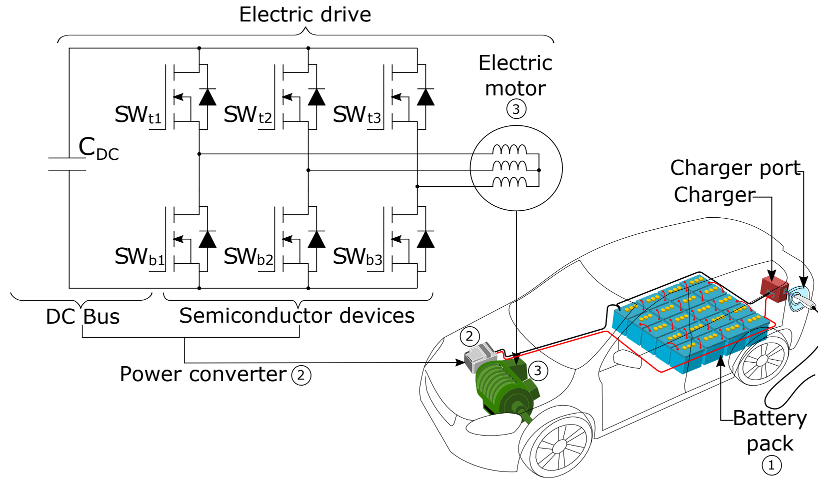


Figure 2: Explosion drawing of an automotive electric drive system main components.

tive Research (USCAR) [16, 17], the U.S Department of Energy (DOE) [18, 19] or the United Nations Economic and Social Commission for Asia (UN ESCAP) [20] establish qualitative and quantitative goals for the next generation of HEV/EVs.

From the previous reports, it can be concluded that current and future R&D efforts of the automotive HEV/EV industry should mainly be focused on electric drive technologies (i.e., the power converter, including DC-link capacitors and power semiconductors, the cooling systems and the electric motor), batteries and charging infrastructures. In this sense, figure 2 shows the general diagram of an EV, which includes the aforementioned elements. Among them, the power electronics that constitute the core of the propulsion

system can be considered of capital importance, as they are responsible of controlling the power flow between the batteries and the electric machine (in motoring operation mode), and vice versa (in regenerative braking operation mode) [21].

The technological targets proposed by Horizon 2020, USCAR, DOE and UN ESCAP regarding the power electronics are stringent (when compared to 2010-2012 data), and can be summarized in the following items:

1. An increase of the power density of the power conversion stage of around 50 % (from 8.7 kW/l up to 13.4 kW/l).
2. A reduction of power converter losses (conduction and switching losses) by 50 %.
3. Significant costs reductions (a reduction by four) for on-board power electronics (from $ 30/kW to $ 8/kW).
4. Simplification of thermal management systems by using on-board coolants minimizing, as possible, the usage of additional components.
5. Whole drive size and weight reductions of 35 % and 40 %, respectively (from 1.1 kW/kg and 2.6 kW/l up to 1.4 kW/kg and 4.0 kW/l).

Specifically, the U.S. DOE's goals for 2020 propose the development of power converter technologies with specific power of more than 14.1 kW/kg and efficiencies greater than 98 %. At the same time, the aforementioned goals aim for a significant cost reduction up to $ 3.3/kW.

Current market technologies cannot achieve all these previous figures. Consequently, an extensive research and development regarding key technologies that constitute the power converter (figure 2, ②) should be conducted, i.e. advanced thermal management systems [22–24], improved DC-link components and designs [25, 26], power semiconductor technology [27–30], optimized layouts and packaging [31–33] and alternative power conversion topologies [34–37], among others. Thus, it becomes clear that the research topics in this field are wide. In this context, this work will focus on the review of the solutions that could improve the following power conversion stage design aspects:

- **Alternative power conversion architectures.** The most suitable alternatives will be reviewed, and the ones that best suit the application will be identified based on the operational requirements of future HEV/EV drive systems. Finally, the fundamental constituting elements of such architectures will be derived, because they will be the fundamental power electronics units to be improved.
- **New power semiconductor devices.** The aforementioned technological goals could only be achieved by using advanced semiconductor technologies. Wide-bandgap (WBG) semiconductors, especially gallium nitride (GaN) and silicon carbide (SiC) based power electronic devices, have been proposed as the most promising alternative to silicon (Si) devices due to their superior material properties, allowing to improve thermal conductivity, increase the achievable maximum switching frequencies and/or reduce power losses. In this context, the article will study the usage of new WBG power semiconductors in automotive power converters. An in-deep market analysis will be conducted in order to provide a whole

picture of the current semiconductor technologies and their suitability for automotive applications.

- **WBG automotive power module design aspects.** As it will be justified in this paper, power modules, from different manufacturers or manufactured ad-hoc with available die technologies, will be the preferred option to achieve the automotive grade specifications. Considering the particularities of WBG technology, a review and discussion regarding possible power conversion stage layouts and parallelization schemes (required due to the high power ratings of the particular application) will be conducted, focusing on the available technologies and technical solutions that could be used.

Thus, the following sections will provide valuable information, not only for the research community, but also for practical power electronics engineers that are focused on the design of the hardware elements of the power conversion stage of HEV/EVs.

2. Power electronics in HEV/EV applications

The determination of the most appropriate power conversion alternatives for both current and next generation HEV/EV drive systems is a topic of relevant importance. The selection of a given architecture (figure 2) would depend on the electric parameters of the system (battery voltage and phase currents), and also on a variety of desired features such as high power density, fault tolerance, high frequency operation and cost effective thermal management, among others. The following items review all these aspects, providing a list of the most suitable power converter topologies and their design requirements.

2.1. Battery and power semiconductors: Electric operation conditions

Battery (figure 2, ①) voltage is one of the key electrical parameters that must be considered for the design of an HEV/EV power conversion stage. According to a number of automotive standards, such as LV 216-1, LV 216-2 and SAE J1654, the maximum battery voltage should not exceed the low-voltage limit of 1500 V due to the following reasons [38]:

(a) Exceeding this limit significantly increases the requirements related to operational safety.

(b) As voltages exceeding 1500 V are not present in the automotive industry, it is very difficult to find automotive grade components that could withstand such high voltages.

Nominal voltages in the range of 300-400 V are common in battery packs installed on small and medium vehicles [38–41], while voltages up to 870 V can be found in sport cars and heavy duty vehicles (table 1) [38, 39, 41]. In this context, table 1 shows, among other relevant parameters, the common battery voltage levels according to the type of vehicle (electrification degree and vehicle class). Such high voltages are also being considered, in general, for future HEV/EVs, because the section of power wires and battery charging times can be significantly reduced [38, 42].

Table 1: Electric mobility performance class overview for passenger vehicles and commercial vehicles/buses [39].

			Mild Hybrid			Full Hybrid/Plug-in		EV (Batt/RE(1)/FCell(2))			Unit
			12 V	48 V	HV	mid	Power	Small car	Medium car	Sport car	
Passenger vehicles	Max. EM Power		4	12	20	60	100	60	100	180	kW
	Max. EM Speed		50	150	150	200	300	200	300	500	Nm
	Voltage converter DC/DC		--	60/12	200/12	400/12	450/12	400/12	400/12	800/12 420/12	V
	Charger AC/DC		--	--	--	--	230/420	230/400	230/400	230/450 450/800	V
	Battery		15	60	200	400	420	400	400	420/800	V
	Max. current	DC(3)	333	333	167	200	400	200	333	550/280	A
		AC(4)	353	500	500	600	800	250	450	1000/500	A

			Mild Hybrid up to approx. 40 % internal combustion engine				Plug-in hybrid	EV (Batt/RE(1)/FCell(2))			Unit
			7.5 t	7.5-12 t	> 12 t	bus 18 t	7.5-12 t	7.5 t	7.5-12 t	bus 18 t	
Commercial vehicles/buses	Max. EM Power		50	65	120	120	90	100	120	2x120	kW
	Max. EM Speed		350	450	1000	1000	500	350	450	2x500	Nm
	Voltage converter DC/DC		400/12	400/24	420/24 800/24	420/24 800/24	420/24	420/12	800/24	800/24	V
	Charger AC/DC		--	--	--	--	3x400/420	3x400/420	400/420	3x400/800	V
	Battery		420	420	420/800	420/800	420	420	420	400/800	V
	Max. current	DC(3)	180	223	400/200	400/200	300	330	400	400	A
		AC(4)	300	350	450/250	450/250	450	450	450	2x500	A

Table notes:
(1) RE: Range Extended hybrid vehicle.
(2) FCell: Fuel Cell vehicle.
(3) Supplied by battery pack.
(4) On electric machine stator.

In regard to the current and power ratings that should withstand the HEV/EV drive system power conversion stages, they will depend on the maximum torque and power requirements of the vehicle, and also on the torque per ampere production capabilities of the installed electric machine(s) [43]. When using permanent magnet (PM) based machines, the extra current required during field weakening should also be considered [44–46]. In this context, currents up to 255 A are generally found in three-phase systems with power ratings between 50 kW and 70 kW [44, 47, 48], and up to 480 A for systems of 125 kW [49, 50]. These numbers could significantly increase for high power heavy duty vehicles. The Irizar ieTran (18 m version) is an illustrative example of this statement, as it has a nominal power of 235 kW. Similarly, the Green Power EV350 all electric bus features a maximum power of 300 kW. In this context and taking into account the current ratings of discrete power semiconductors and bare dies, the parallelization (figure 3) of power semiconductor devices (or the usage of power modules including parallelized devices) becomes mandatory for all vehicles.

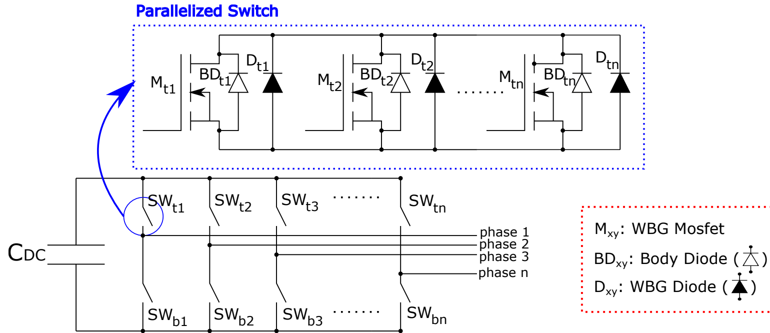
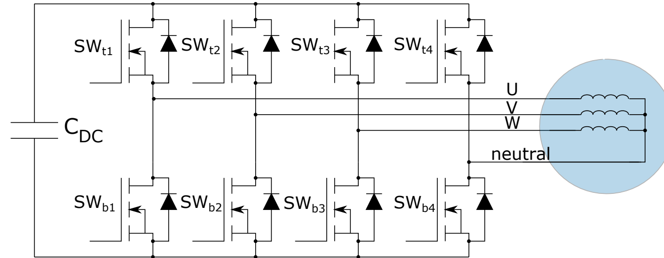


Figure 3: Generic power converter topology of future HEV/EV electric drives based on two-level multi-phase topologies and with parallelized power switches.

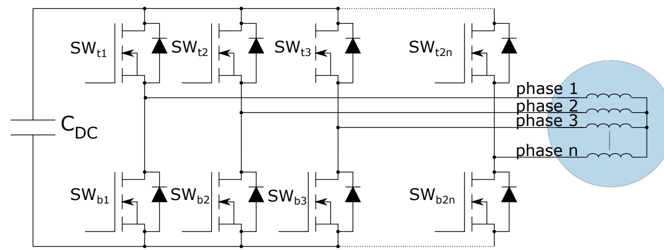
2.2. Power conversion topology

Efficient, compact, robust and safe power systems (figure 2, ②) are desirable for future HEV/EV drives [51]. In this context, it is relevant to identify the power conversion topologies that will best suit future HEV/EV applications. Two-level three-phase power conversion architectures (usually connected to synchronous machines -Toyota, Honda, Mercedes, BMW, Nissan, Volkswagen, etc.- or induction machines - Tesla, Hyundai, etc.) have become the standard in the current automotive industry [44, 48, 52–56]. Most relevant original equipment manufacturers (OEM), such as Tesla, Nissan, Audi, Toyota and Chevrolet rely on such architecture for their HEV and/or EVs [57, 58]. A number of Tier 1 and 2 automotive inverter suppliers such as Semikron (SKAI product family), Cascadia Motion LLC (former Rinehart Motion Systems, including the PM and RM inverter families) and Brusa Elektronik AG (DMC series), to name a few, provide complete two-level three-phase inverters for automotive use for both prototypes or industrialized vehicles. Power electronics suppliers such as Infineon (HybridPack modules), Semikron (SKIM, solderless sinter technology) and Fuji Electric (incorporating direct water cooling), among others, also provide automotive qualified two-level three-phase power modules [58–60]. Nevertheless, an increase on phase levels and number of phases could be considered.

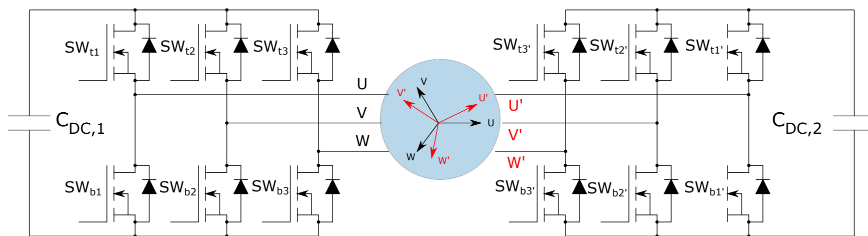
In high power traction applications such as railway transport, it is of common practice to use multilevel converters with medium power semiconductors [61–63], following the well known Neutral Point Clamped (NPC) [64], Flying Capacitor (FC) [65] or Cascade H-bridge (CHB) [66] configurations. A number of benefits can be obtained from their use, such as the improvement of the synthesized voltage and current waveforms and power handling capabilities [61, 67–69]. However, multilevel technology has significant drawbacks for the automotive industry, as voltage oscillations must be avoided in NPC configurations [70, 71], increasing the complexity and computational burden of the control algotithms. On the other hand, system hardware complexity and costs are also increased [61, 67–69, 72, 73]. Taking the latter into account and considering both the battery voltage levels adopted by the automotive industry (section 2.1) and current power semiconductor technology, it can be stated that future HEV/EVs will continue relying on two-level power conversion stages.



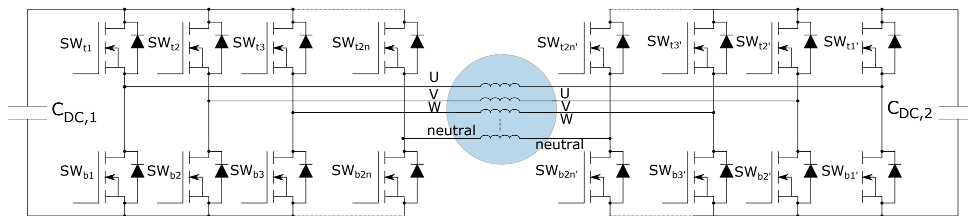
(a) Extension of the three-phase machine fault tolerance including access to the machine neutral.



(b) Multiphase topology with star connected windings and odd phase-number.



(c) Dual three-phase configuration with star connections in windings.



(d) Multiphase configuration for three-phase machine with open windings.

Figure 4: Alternative fault tolerant multiphase power conversion topologies for HEV/EV drives.

On the other hand, multiphase technologies (figure 4) include a number of relevant benefits that the automotive industry could exploit, such as power splitting (which allows greater power handling capabilities or a reduction of parallelization requirements), increased fault tolerance, high efficiency, high power density and lower torque ripple than equivalent three-phase systems [34–36]. Additionally, some specific multiphase topologies can be effectively reused for battery charging, eliminating the dedicated charge power converter and reducing the volume, weight and overall costs of the vehicle power electronics systems [37, 74]. Additionally, an equivalent n-phase machine can be easily derived from a three-phase machine with the same characteristics and performance [75]. For all these reasons, multiphase technologies are successfully being introduced in electrified transportation systems [76].

Taking into account the current safety requirements for commercial vehicles (refer to the international standard for functional safety ISO 26262), the power system must be designed and dimensioned in a way that the Mean Time Between Failures (MTBF) is maximized. However, as an operation free of faults cannot be guaranteed at 100 %, fault tolerance can be considered as crucial. An extensive research to provide fault tolerance to three-phase systems under open and short circuit faults has been conducted [77–80]. However and thanks to the additional degrees of freedom of multiphase topologies, fault tolerance can be greatly extended by using corrective control strategies, improving passengers' safety and post-fault operation [34, 35]. A number of fault tolerant architectures, such as neutral connected (figure 4(a)), star connected (figure 4(b)), dual three-phase (figure 4(c)) or open winding (figure 4(d)) multiphase configurations can be found in the scientific literature. Table 2 summarizes the most relevant features of each configuration, including a number of references regarding each alternative.

As a summary, it can be stated that although three-phase technologies have an industrial prevalence due to their maturity and simplicity, it is worth to explore the introduction of multiphase technologies beyond their usage in heavy duty vehicles. From the reviewed alternatives, the open winding multiphase configuration provides additional fault tolerance against machine winding short circuit faults [81, 82]. However, this additional fault tolerance is achieved at the cost of doubling the required power switches when compared to star connected multiphase topologies. Thus, the economical costs of this alternative could be high.

The dual three-phase configuration [83–85] has two significant advantages over the other two multiphase technologies. On the one hand, it can provide fault tolerance over power supply faults[1]. The second benefit is that three-phase solutions (power electronics and control algorithms) can be directly translated into the dual three-phase scenario, simplifying the transition between three-phase and multiphase technologies.

It is important to consider that the degrees of freedom (regarding current control) are the same for both dual three-phase and star connected five-phase machines. Thus, five-phase architectures can provide an appropriate fault tolerance against open circuit faults [35, 86] with one less phase when compared to dual three-phase technologies. Additionally, harmonic control capabilities of five-phase topologies must be considered [87], as well as their capabilities to cope with up to two open circuit phase faults, ensuring a

[1]Two separated battery packs could be necessary to take advantage of this feature, increasing the complexity of the vehicular architecture. Such feature can be better exploited in aerospace applications, where various independent high voltage direct current (HVDC) networks are available.

Table 2: Summary of the most relevant multiphase architectures suitable for HEV/EV drive systems, including their corresponding references and main features.

Topology	**Fig.**	**Number of elements**	**Fault tolerance**	**Refs.**[(1)]
3-phase with neutral[(2)]	4(a)	8 switches[(3)], 1 DC-link[(4)]	o.c. faults (control)	[77, 78]
5-phase	4(b)	10 switches[(3)], 1 DC-link[(4)]	Intrinsic or control (multiple o.c. faults)	[34–36, 76, 86, 88–96]
7-phase		14 switches[(3)], 1 DC-link[(4)]		[97]
9-phase		18 switches[(3)], 1 DC-link[(4)]		[98, 99]
11-phase		22 switches[(3)], 1 DC-link[(4)]		[100, 101]
Dual three-phase	4(c)	12 switches[(3)], 2 DC-link[(4)]	o.c. and s.c. faults[(6)]	[83–85, 102–105]
3-phase open winding	4(d)	12 switches[(3)], 2 DC-link[(4,5)]	o.c. and s.c. (control)	[77, 106]
4-phase open winding		16 switches[(3)], 2 DC-link[(4,5)]	o.c. and s.c. (intr./ctrl.)	[107]
5-phase open winding		20 switches[(3)], 2 DC-link[(4,5)]	o.c. and s.c. (intr./ctrl.)	[81, 82]

Table notes:
(1) Although some of these references do not strictly apply to HEV/EV applications, their underlying concepts can be easily extended to automotive applications.
(2) From the power converter point of view, this architecture can be considered as multiphase.
(3) The switch will be constituted by a number of power semiconductor devices in parallel (figure 4).
(4) The DC-link may be constituted by a single or multiple C_{DC} capacitors and the corresponding busbar (integrated or not).
(5) Additionally and at the cost of losing some modularity, a single DC-link can be used instead.
(6) In some particular cases, braking torque produced by a short circuit in one of the two three-phase inverters can be compensated by properly regulating the healthy one.

low torque ripple in the machine [88].

From the previous lines, it can be concluded that automotive power conversion topologies (figure 2) will rely on the two-level branch (figures 3 and 4) as a core constituting element. Thus, special focus on this element should be provided by automotive power electronics engineers to achieve an optimum design.

2.3. Influence of future electric machine design considerations on power electronics

The electric machine (figure 2, ③) technology and its requirements must be also considered for the power converter design. In this sense, weight reduction targets and HEV/EV space constraints have lead to the research and development of high power density drive systems [14, 16, 20]. Being this one of the most important aspects for the automotive industry, the power density of the machine can be significantly improved using multiphase technologies, as the additional control degrees of freedom allow to control the harmonic injection (generally fundamental and third harmonic), thus increasing torque production capabilities [75, 86, 87, 97]. As an illustrative example, a five-phase PMSM with a quasi-trapezoidal back-EMF distribution is controlled in [87] with fundamental and third harmonic injection, increasing the torque production by 14,5 %. Similarly, a torque enhancement of 20 % is claimed in [108]. For this reason, the use of multiphase topologies (section 2.2) is again justified.

Complementarily, power density can be further maximized increasing the operation speed of automotive electric machines, leading to High Speed Electric Machine (HSEM) desing concepts [48, 109–111]. A good example of how power density is improved by increasing the mechanical speed can be found in Toyota HEV IPMSMs. Both second and third generation Toyota IPMSMs have a rated power of 50 kW. The active volume of the second generation machine is of 4.78 l, with a maximum mechanical speed of

6000 rpm, while the third generation machine achieves the same power with an active volume of 2.74 l, as its maximum mechanical speed is significantly higher (13900 rpm) [48]. However and considering the future power density requirements, a great number of automotive machines with mechanical speeds higher than 15000 rpm are expected for the near future [110].

In such a high speed operation, torque control of automotive HSEMs can be challenging due to high fundamental-to-sampling frequency ratios (typical switching frequencies of IGBT based commercial automotive power inverters such as Semikron SKAI and Cascadia Motion PM families have typical switching frequencies ranging from 5 kHz to 12 kHz), which makes the stator current regulation and field weakening control difficult tasks [47, 112–115]. As a consequence, power electronics' switching frequencies should be significantly increased in order to achieve a satisfactory electric drive performance [116]. As, due to efficiency requirements, the power losses in the conversion stage should be kept low under such operation conditions, future HEV/EV power electronics should rely on Wide-bandgap (WBG) power semiconductors with low switching losses [30, 117–119].

2.4. Thermal management constraints

Appropriate thermal management is required to ensure the integrity (not exceeding the rated operation temperatures) and extend the lifetime (number of thermal cycles) of HEV/EV propulsion system critical elements such as battery packs [120–124], electric machines [125, 126] and power electronics [33, 127, 128], where liquid cooling or air cooling approaches are followed, being currently liquid cooling the preferred option for the OEMs [22].

Cost reduction is one of the main concerns for the automotive industry. In this context, a number of agents have focused on the simplification of the electric drive cooling systems to achieve the aforementioned goal [14, 16, 20]. Nowadays, most commercial HEV/EVs mount two separate liquid cooling circuits, a low temperature loop for power electronics cooling, and a high temperature loop for electric machine cooling (including ICE cooling in HEVs) [22, 33, 129, 130]. The nominal coolant temperatures are of around 65°C and 105°C for the low and high temperature loops, respectively. On the other hand, battery cooling should be provided separately, as the optimum operating temperature of a lithium-ion battery ranges between 20°C and 40°C [131].

Two approaches that have a considerable impact in power electronics cooling are being followed to simplify and reduce the costs of the aforementioned architecture:

(a) The elimination of the low temperature loop, sharing the high temperature cooling loop for both power electronics and electric machine/ICE [33, 130]. In this context, power converter cooling technologies must be very efficient in order to operate at such high coolant temperatures. Indirect water cooling [129] uses a thermal interface material (TIM) between the power module and the cold plate, simplifying the assembly process, but increasing the thermal resistance (R_{th}). Thus, direct cooling [128] should be preferred, as the TIM layer is removed, providing direct contact between the base plate of the power converter and the coolant. In order to further enhance heat transfer capabilities, recent advances in liquid cooling systems include double-sided cooling structures [129, 132], where new assembly and interconnection technologies must be developed (i,e. suppression of wire bonding). Regarding cold plate technologies, modifications on structure and materials can be

followed, increasing the surface area and improving the heat transfer. Two examples of these developments are the microchannel [133, 134] and pin-fin [135, 136] cold plate technologies.

(b) The substitution of the power converter cooling loop by a high performance air cooling architecture that makes use of the air flow generated during vehicle movement [22, 130, 137–140]. For example, this alternative can be effectively implemented for in-wheel power electronics/electric machine solutions [141]. It must be taken into account that, although optimized, the heat dissipation capabilities for air cooling are lower than for liquid cooling.

Both solutions are valid for the reduction of the system complexity and cost, as pumps, coolant lines, remote heat exchanger fans, and coolant fluid can be partially or totally removed from the vehicle [22, 142]. As a drawback, the operation temperature of the power semiconductor devices is increased, leading to possible reliability problems. This future thermal management scenario justifies again the introduction of WBG technologies, because they have lower power losses and better thermal conductivity than silicon based devices [30, 143, 144], leading to lower junction temperatures on the power switches.

Thus, once the selection of the semiconductor technology has been justified through the influence of the HSEMs (section 2.3) and thermal management constraints (section 2.4), it is important to analyse the real possibilities that these technologies offer, conducting a review of the available solutions in the market.

2.5. Electromagnetic interference constraints

The intrinsic characteristic of HEV/EV electronic systems constitute them as sources of both radiated and conducted electromagnetic emissions (EMI). On the other hand, those systems also suffer from EMI[2] that may affect their integrity [145]. Concerning HEV/EV vehicles using WBG technology, there are specific researches that review their EMI issues [146, 147]. The usage of WBG semiconductors implies that power devices operate at higher frequencies [146, 147]. Consequently, rise (t_r) and fall (t_f) times become shorter than for *Si* technology. Thus, the dv/dt and di/dt derivatives increase the number and order of harmonic components, and introduce high frequency currents that are distributed thorough the elements of the whole propulsion system.

The main sources of EMI, which are common to any type of electronic system, are the following [148]:

- Common mode interferences.
- Common ground.
- Capacitive coupling.
- Inductive coupling.

[2]The EMI affects HEV/EV low voltage equipment such as Electronic Control Units (ECU) and Battery Management Systems (BMS), and also high voltage electronics such as power converters and their corresponding driver circuitry.

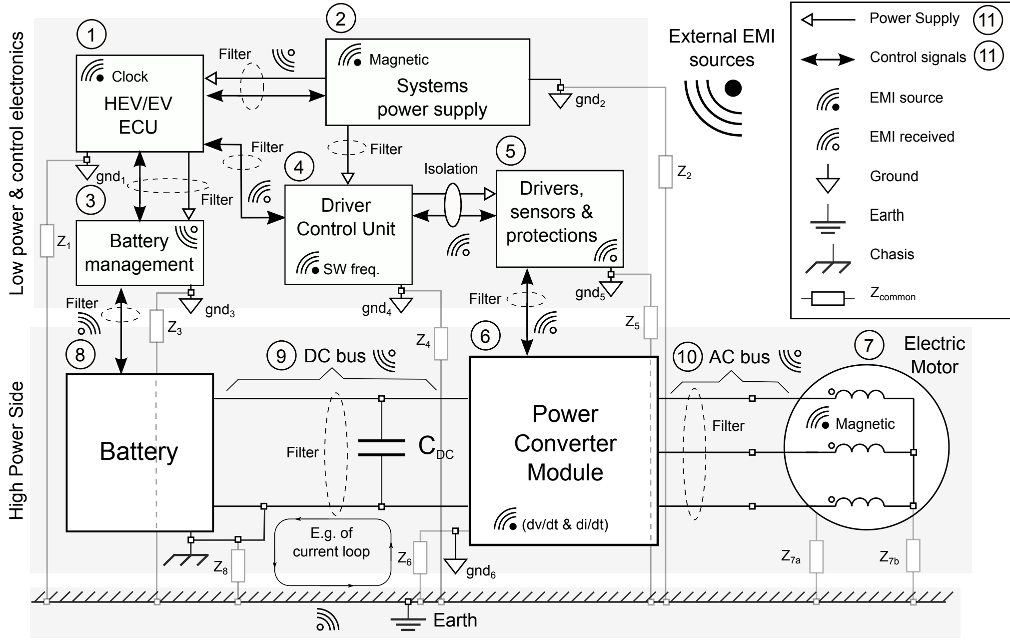


Figure 5: Identification of EMI sources in HEV/EV applications.

- Radiated and conducted electromagnetic fields.

To deal with the aforementioned issues, designers should follow PCB design guidelines for EMC (Electromagnetic Compatibility), and also check possible conducted and radiated EMI considering EMC regulations. The applicable regulation for HEV/EVs is the UNECE Regulation 10 [149]. Besides, IEC 61967 [150] (150 kHz to 1 GHz) and IEC 61851 [151] should also be considered.

Figure 5 shows the main sources and mechanism of EMI in HEV/EV traction systems. There are many techniques that can be used to deal with the different types of radiated and conducted EMI [148], such as the minimization of the size of current loops, the usage of uniform impedance reference ground plane without cuts to avoid common ground issues, shielding techniques of PCB and/or wires to minimize the radiated magnetic and/or electric fields, the minimization of the length of the wires and tracks, the usage of shielded wires and ferrite beads in power supply, signal and control lines, or CM filtering at both ends of wires to diminish the radiated and conducted interferences. As a summary, table 3 lists the specific EMI protection techniques that are applicable to HEV/EV electronic systems.

3. Wide BandGap power semiconductors for EV applications

As stated in the introduction, *Si* based Insulated Gate Bipolar Transistors (IGBTs) and diodes are the current industry standard for traction and HEV/EV systems [23, 58, 183]. Although they represent a mature technology, extensive researches have been

Table 3: Relationship between HEV/EV subsystems, EMI interferences and EMC techniques.

Block of figure 5	Subsystem	Main sources and EMI mechaninms	EMC specific techniques	Refs.
①	Electronics Control Unit (ECU)	• Radiated and conducted EMI of CPU main clock frequency and harmonics.	• Digital filtering in the ADCs	[152–155]
②	Low power supply	• Magnetic fields in unshielded inductances of switched DC-DC converters and filters	• CM power line filtering or ferrite beads at both ends • Use toroidal or shielded inductances	[156–159]
③	Battery management	• Commom EMI issues	• EMI filtering	[156, 157] [160]
④	Drivers Control Unit	• Interferences from the dv/dt and di/dt.	• Layout design	[161–163]
⑤	Driver	• Radiated and conducted EMI from the dv/dt and di/dt. •Insuficient isolation produce electric coupling EMI.	• Minimum track clearance adjusted to the maximum voltage levels and the electrical strength of the PCB or DBC substrates. • Control signals in differential mode (DM) • Optocopled control signals • Fiber optic for control signals	[164–168]
⑥	Power module	• Specially in WBG devices EMI from dv/dt and di/dt of the PWM switching frequency and its harmonics. • Power devices feedback loops with self resonant frequencies cause oscillations in the power ramp-up of the devices. • Distributed parasitic inductances and capacitances in the power and control lines.	• Snubbers. RC filters and RF tramps for attenuation of the overshooting frequencies and damping the transfer response of feedback loops within the power devices. • Modulation techniques for harmonic suppression. • Substrates with higher electric strength. • Increase the thickness of PCB conductive layers and tracks to improves the current distribution and reduce the parasitic distributed impedances.	[161–163] [169–177]
⑦	Motor	• Electromagnetic fields produced in the winding	• Winding techniques and stator configuration	[178]
⑧	Battery	• Commom EMI issues	•EMI filtering	[156, 157] [179]
⑨	Power DC Bus	• Discontinuous load currents Voltage drops in the wires due to their equivalent series resistance. • Coupled or radiated EMI into the wires. • Current density distribution in conductors.	• Voltage ripple reduction with capacitors and filtering. • Filtering inductances shielded or with toroidal cores. • Type of wires: laminated or multifilar) • Laminated bus structure minimize distributed inductance and equivalent bus resistance.	[164] [180–182]
⑩	Power AC Bus	• EMI coupled or radiated into the wires.	• RLC filtering for overvoltage suppression. • Type of wires (laminated, multibifilar)	[164, 178]
⑪	Control and power wires	• Commom EMI issues	•Twisted wires. •Ferrite beads in the wires.	[164]

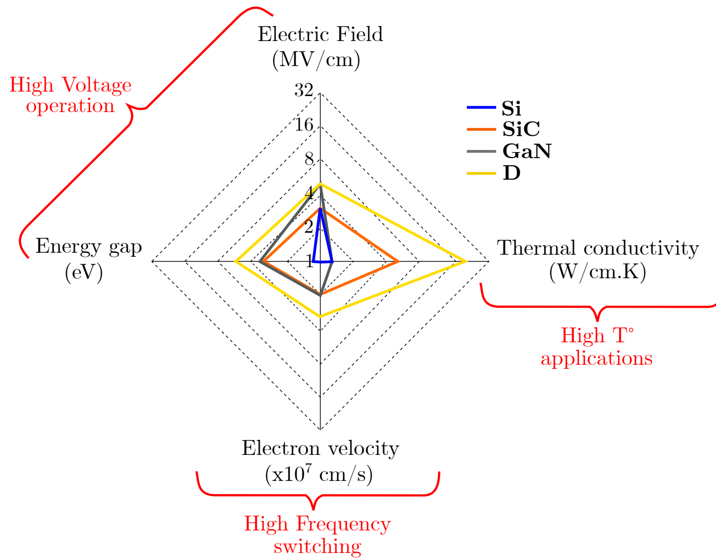


Figure 6: Current status of wide-bandgap materials.

carried out in the last two decades in order to improve their features. Such improvements have been mainly focused on the reduction of power losses (both static and dynamic), and minimization of reverse recovery currents and leakage currents, among others [184–187]. However, *Si* has physical limitations related to the intrinsic material physical properties, which are very difficult to overcome. For this reason, the use of new advanced materials is being further justified.

Taking the latter into account, WBG semiconductors are gaining popularity in the automotive market. Among them, *GaN* and *SiC* devices are considered as the most matured technologies, although other semiconductor materials such as Diamond and Gallium Oxide (Ga_2O_3) exhibit a high potential, and are currently under investigation in many laboratories [188, 189]. These new materials solve some well known *Si* limitations concerning blocking voltage, operating temperature and switching frequency, which are related with the main physical parameters involved in power device design: critical electric field, band-gap energy, charge carriers saturation velocity and thermal conductivity [30, 143, 144, 190–195]. Concerning these parameters, figure 6 compares graphically the *SiC* and *GaN* potential regarding blocking voltage, switching speed and high temperature operation, when compared to *Si*. Figure 6 includes Diamond's parameters, which is considered the ultimate semiconductor material. It is also worth to remark that, from a technical point of view, packaging aspects could limit the maximum figures achievable by the semiconductor device itself as, for example, specific packaging solutions allow *SiC* devices to operate in the -150°C to +300°C range [196]. Besides, as section 2.5 highlights, the design complexity of WBG technology increases, because it introduces new technical challenges that were less relevant in *Si* technology. The circuit parasitic capacitances [163] and inductances [162] become more critical, as higher switching speeds and faster turn ON/OFF transients generate interferences and oscillations that are source of EMI [147, 197], producing higher harmonic content [169], cross-talk effects [198] and

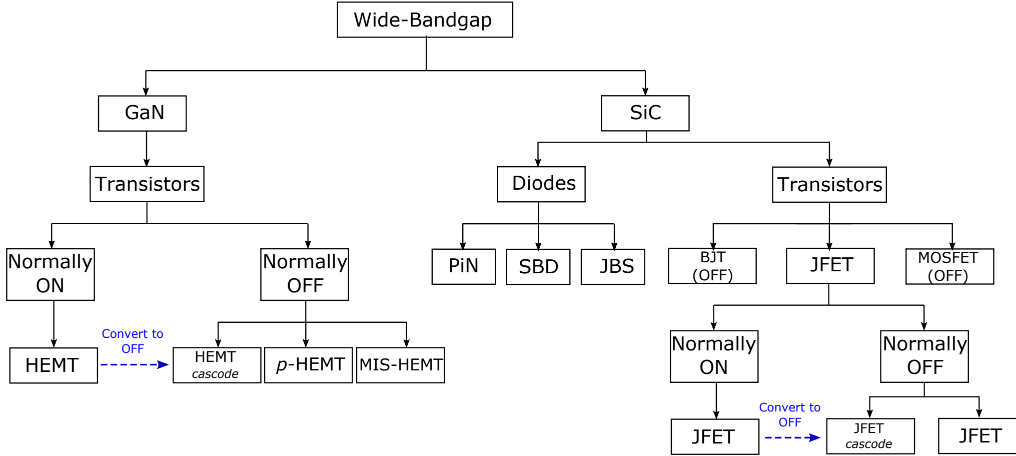


Figure 7: *GaN* and *SiC* power devices that could be exploited for the HEV/EV power electronics.

interaction between the converter and the load [199].

There is a significant number of commercial *GaN* and *SiC* devices (figure 7) whose electro-thermal characteristics must be analysed to be implemented in automotive power electronics. In the following items, a general overview of the commercially available *GaN* and *SiC* devices is carried out, and their suitability for HEV/EVs is studied.

3.1. Gallium nitride power semiconductors

Current *GaN* devices are based on *GaN* and *GaN* alloy thin layers epitaxially grown on various substrates (sapphire, *SiC* and *Si*), since high quality *GaN* mono-crystalline wafers are not yet available [200, 201]. The interface between such layers presents a very low resistance sheet, known as the 2-D electron gas (or 2DEG) layer, which allows optimum lateral electrical conduction due to a very high electron mobility. Up to date, the only commercially available *GaN* power devices are the High Electron Mobility Transistors (HEMT), which are based on such effect using *AlGaN/GaN* thin layers grown on *Si* wafers (*GaN*-on-*Si* technology). They are normally ON by nature, and their working principle is based on interrupting the 2DEG low resistance channel between Drain and Source terminals by acting on a third control or Gate terminal. Many efforts have been addressed to obtain normally OFF switches, because the safety requirements of HEV/EV applications make extremely important to rely on such kind of switches for the propulsion inverter [202]. One solution consists on connecting, inside the same package, the normally ON *GaN* HEMT with a normally OFF low voltage *Si* MOSFET in cascode configuration [203–205]. The main problems of this solution are the addition of the on-state resistances of both devices in series, and the maximum operation temperature limitation introduced by the *Si* MOSFET.

Another approach for obtaining a normally OFF HEMT consists on including additional gate structures in the device, depleting the conductive channel at zero gate bias. So far, nowadays there are two main technological approaches to do that. The first solution is based on a *p*-*n* junction structure between the gate and source, leading to

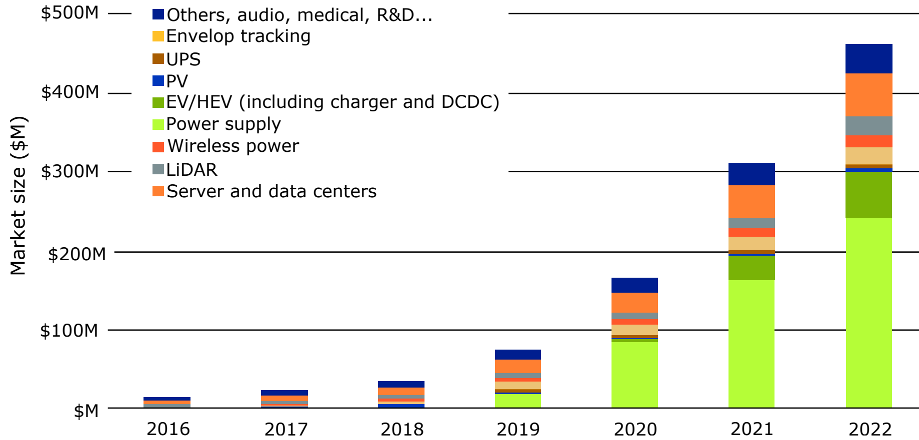


Figure 8: Current *GaN* market status and future prospects (source [214]).

the so called *p*-HEMT family of transistors [206–208]. The second option is based on the introduction of a metal-insulator-semiconductor (MIS) structure at the gate level, leading to the MIS-HEMT family [209–211]. In this sense, Figure 7 summarizes the commercially available *GaN* device options described above, showing their most relevant features considering the automotive market [30, 190, 212].

In principle, the very low ON-state resistance ($\sim$25 $m\Omega$) and fast switching speed achieved by 650 V *GaN* devices could make such devices good candidates for certain HEV/EV applications [144]. Nevertheless, HEMTs are lateral devices with very narrow gate fingers to ensure their blocking capability (either for normally ON and OFF devices, or for *p*-HEMTs and MIS-HEMTs). These structural characteristics lead to two facts that determine the behaviour of *GaN* HEMTs. Firstly, the narrow gates, the lateral current conduction scheme and the not too high *GaN* thermal conductivity are less favourable for heat dissipation (higher thermal resistance) than the common scenario found in vertical devices [213], limiting the maximum current ratings of *GaN* HEMTs. Secondly, the blocking voltage between drain and source must be withstood in the device surface (not in the semiconductor volume, as is the case in vertical devices). Due to the surface defects, the maximum theoretical breakdown voltage related with *GaN* properties cannot be achieved [203]. In addition, the breakdown mechanism in such lateral devices is destructive (another difference with vertical IGBTs and diodes), significantly limiting their reliability. Significant research efforts are now being carried out in order to obtain high quality *GaN* substrates, allowing the development of vertical devices (*GaN*-on-*GaN* technology) [200, 201].

Despite such drawbacks, *GaN* technology has high potential. In recent years, there have been various acquisitions/associations [214] between traditional *Si* power semiconductor manufacturers and high-tech and smaller companies specialized in *GaN* technology. This fact highlights the interest of the industry in *GaN*. To name some examples, Infineon has acquired International Rectifier, Fujitsu has done the same with Transphorm, Rhom has acquired *GaN* Systems, and ST Microelectronics has partnered with Leti CEA. Current technological applications for *GaN* are diverse, as they cover lighting systems (opto-LED), consumer equipments (opto-laser, power supplies, etc.),

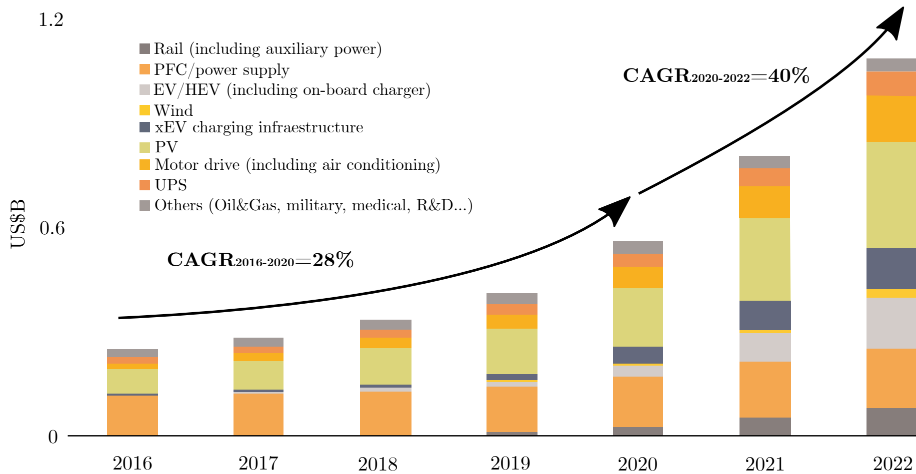


Figure 9: Current *SiC* market status and future prospects (source [218]).

radio-frequency, aerospace and defence, health and virtual reality (figure 8). Regarding power applications, there are several *GaN* technology companies (EPC, Exagan, GaN Systems, ST Microelectronics through Leti CEA, NTT, Panasonic and Transphorm) involved. In some references [201, 215–217], it is stated that *GaN* will be competitive with *Si* and *SiC* for future HEV/EV applications which will demand higher switching frequencies at medium voltage. However, currently commercial devices of a few tens/hundreds of kW are non-existent[3].

As a summary, it can be concluded that *GaN* could be an interesting option to manufacture power devices but, due to the technological problems described above, the current ranges and reliability are insufficient for their application in automotive propulsion inverters. Thus, it can be concluded that *GaN* technology is still not a valid option.

3.2. Silicon carbide power semiconductors

In recent years, *SiC* based devices have improved their performance (lower conduction voltage drop, higher operating temperature and better parameters stability) thanks to improvements in the bulk material growth process, device design and fabrication technology [30, 191]. Thus, they constitute a solution for high voltage/high power applications, since *SiC* physical material parameters allow the construction of smaller chips with lower parasitic capacitances and fast switching speed capabilities [28]. The power electronics industry also supports the introduction of this new technology, as it can be confirmed from the available market data and future prospects (figure 9). In this context, Table 4 summarizes various *SiC* and *Si* traction inverters, highlighting some of their more relevant features.

[3]As an example, EPC offers devices with 350 V@6.3 A; and 90 V@90 A; GaN Systems reaches 650 V@120 A; TI 600 V@12 A; Panasonic 600 V@10 A; and, finally, Transphorm reaches 600 V with a drain current of 20 A. Moreover, commercial *GaN* multichip power modules are not available.

Table 4: Examples of *SiC*/*Si* electric traction inverters for HEV/EV drive systems.

Full *SiC* inverter	**Power**	**Efficiency**(1)	**Power density**	**DC bus voltage**	**Refs.**
EV inverter	30 kW	99.5 % peak	15 kW/l	250-800 V	[219]
EV inverter	60 kW	-	34 kW/l	400 V	[146]
EV inverter 1200 V half bridge modules	110 kVA	Mean 96.3 % and peak 98.9 %	23.1 kVA/l (17 kW/l) 16.8 kVA/kg (12.4 kW/kg)	200-450 V	[146]
EV inverter	100 kW peak	-	34 kW/l	400 V	[220]
EV inverter	80 kW	99.5 %	-	800 V	[221]
EV inverter	60 kW	92.3-99.1 %	160 kW/dm^3	800 V	[222]
EV inverter	120 kW	96.8-99.3 %	160 kW/dm^3	800 V	[222]
EV inverter	88 kW	-	21.5 kW/l	900 V	[223]

Commercial *Si* inverter	**Power**	**Specific power**(2)	**Power density**	**DC bus voltage**	**Refs.**
Motor inverter for 2004 Prius	50 kW	5.68 kW/kg	5.75 kW/l	200 V	[224]
Motor inverter for 2007 Camry	70 kW	9.33 kW/kg	11.67 kW/l	250 V	[224]
Motor inverter for 2008 LS 600h	110 kW	14.86 kW/kg	17.19 kW/l	288 V	[224]
Motor inverter for 2010 Prius	60 kW	16.67 kW/kg	11.11 kW/l	200 V	[224]
Motor inverter for Nissan leaf 2012	80 kW	4.9 kW/kg	5.7 kW/l	380 V	[225]

Table notes:
(1) Analysed literature does not provide specific power data.
(2) Consulted commercial solutions do not provide efficiency data.

In the following paragraphs, currently available *SiC* technologies are presented. Figures 10 and 11[4] show their voltage and current levels, while figures 12 and 13 identify the most significant parameters of a portfolio of current *SiC* devices for power modules. In this comparative study, almost all the analysed devices are encapsulated in TO-247 or D3PACK packages, with similar junction-to-case thermal resistance values. Concerning bare dies, the manufacturers provide nominal parameter values assuming a similar junction-to-case thermal resistance. Based on the chosen parameters, the charts provide the performance of the devices and the scope of their parameters[5], which can be summarized as follows:

- V_{block} (V), maximum blocking voltage of the power device during the OFF state. This parameter refers to $V_{DS_{max}}$ (maximum repetitive drain to source voltage) for MOSFETs, JFETs and BJTs, and V_{RRM} (maximum repetitive reverse voltage) for diodes. This voltage must be higher than the maximum HEV/EV battery voltage, including a given security margin (typically a 1.5x or 2x factor) due to voltage peaks produced across the devices during commutations (section 2.1).

[4] The present work only considers discrete semiconductors, and lefts aside bare dies, because manufacturers do not provide homogeneous specifications for the later. Consequently, a comparison of their parameters requires complex post-processing of the supplied data. Besides, discrete semiconductors are usually made of bare dies. Thus, the provided comparison would be enough for generic frameworks.

[5] The provided voltage and current ranges are for discrete *SiC* devices (CREE, Fuji Electric, GeneSiC, Global Power, Infineon, Microsemi, ROHM, ST and USC). The commercial power modules provided by power semiconductor manufactures have higher current levels because they mount power semiconductors in parallel to constitute each switch.

- I_{max} (A), maximum current of the semiconductor during the conduction state. This parameter refers to I_D (continuous ON-state DC drain current), provided by manufacturers for MOSFETs, JFETs and BJTs, and I_S/I_F for diodes. This parameter and the total current per phase of the power converter will define the number of power semiconductor devices to be paralleled for each switch (figure 3, SW_{XY}) of the inverter. Mainly, I_{max} is thermally limited, and it depends on the junction-to-case thermal resistance of the device.

- T_{jmax} (^{0}C), maximum operation junction temperature. This parameter determines the maximum allowable junction temperature of the device, and it is determined from manufacturers reliability data. Exceeding this temperature seriously decreases the nominal device lifetime [226]. The inverter must be electrically and thermally designed in such a way that the maximum application temperature is lower than T_{jmax} and T_{vop} (which is maximum temperature under switching conditions of the semiconductor).

- R_{dson} ($m\Omega$), drain to source ON-state resistance. This parameter refers to the R_{DSon} indicated by manufacturers for unipolar devices: MOSFETs and JFETs. Some BJT manufacturers neglect the collector-to-emitter offset voltage drop and provide also an equivalent R_{DSon} value as a main conduction parameter. This parameter, together with the instantaneous conduction current, defines the power conduction losses of the device. Targeting a balanced current distribution per each semiconductor in parallel (figure 3), the thermal coefficient of R_{DSon} must be positive.

- R_g (Ω), internal gate resistance. The manufacturers of MOSFETs, JFETs and BJTs provide this parameter as $R_{g_{int}}$. It depends on the semiconductor size, where a higher size is equivalent to a higher resistance value. For the same current, the *SiC* semiconductor area is smaller than for *Si*. On the other hand, gate devices must have a minimum gate resistance value to avoid their destruction, so an external resistance ($R_{g_{ext}}$) is commonly included in order to solve this problem. Both resistances $R_{g_{int}}$ and $R_{g_{ext}}$ have direct influence in other parameters such as in the switching speed and the switching losses.

- V_f (V), the forward voltage drop. This parameter applies to diodes and bipolar devices. It is provided in datasheets at fixed current and temperature values, as it strongly depends on both variables.

- Q_g (nC), total gate charge. This parameter specifies the charge stored in the parasitic input capacitances between gate and source terminals, and it affects to the dynamic behaviour of the device. Moreover, this parameter determines design aspects of the driver, as it must provide enough power for switching, as it can be derived from (1). For *SiC* devices, Q_g does not depend on temperature. Thus, this technology is more stable than *Si* during switching.

$$P_{g_{drv}} = Q_g \Delta f_{sw} V_{drv_{off}^{on}}. \tag{1}$$

- Q_{rr} (nC), reverse recovery charge of a diode (total stored charge). This is the charge level required to complete the semiconductor turn OFF process. The parameter

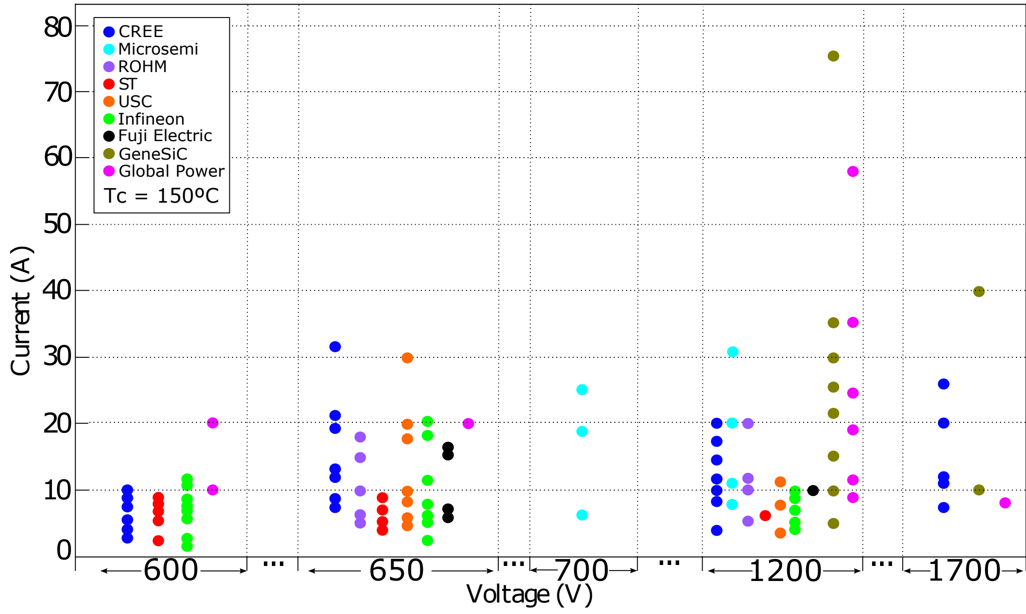
refers to Q_{rr} for bipolar junctions such as the MOSFET body diode and Q_c for Schottky (unipolar) diodes. This charge causes a current overshoot in the turn ON transition of the complementary transistor of the inverter, producing additional power losses.

With regard to *SiC* diodes, their main advantages when compared with their *Si* counterparts are their low reverse recovery charge (Q_{rr}) and low recovery current (I_{rr}), which produce lower switching power losses [227]. In addition, *SiC* diodes show also a positive conduction thermal coefficient [30, 228], which is critical for device parallelization (a requirement for HEV/EV applications). Additionally, when comparing *Si* and *SiC* diodes of the same size and thickness, blocking voltages are 10 times higher for *SiC* diodes. Current *SiC* diodes can be classified into three groups [28, 30, 229, 230]:

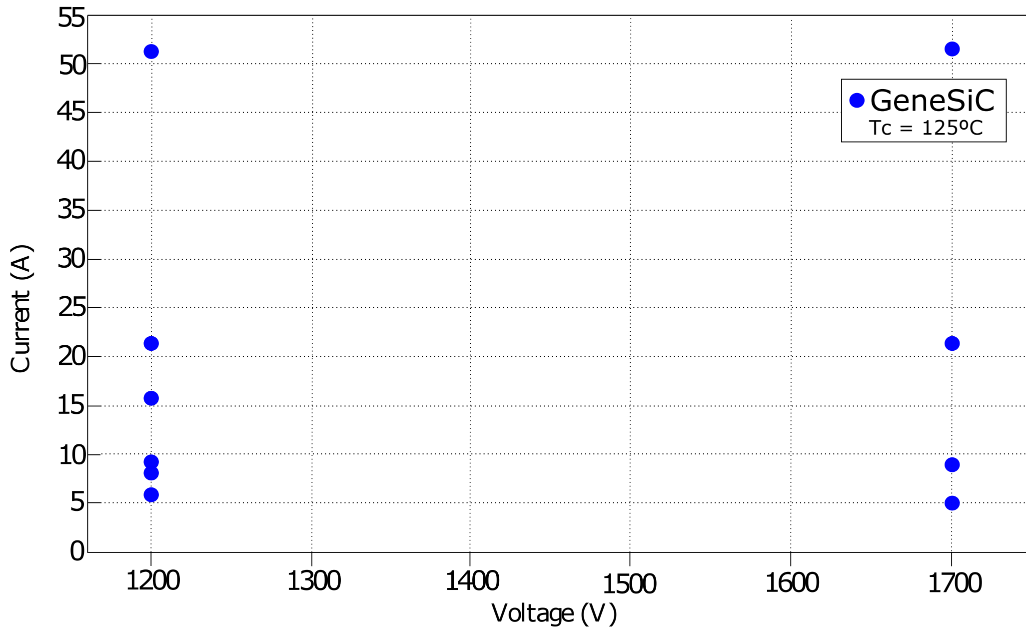
- **PiN diodes.** These bipolar devices are designed for very high voltage operation, typically above 3.3 kV. They exhibit a low voltage drop during ON state when compared to *Si* for such breakdown voltages, with a very small V_f or forward voltage drop. However, they have a higher Qrr than unipolar diodes, so their use in HEV/EV applications would decrease system efficiency, where high voltage values are not necessary. In addition, bipolar *SiC* devices are affected by a material degradation mechanism during forward current conduction associated with a kind of lattice defect called stacking fault. Recent improvements on material manufacturing have almost suppressed this limitation in practical applications [231].
- **Schottky barrier diodes (SBD).** These unipolar devices also feature a low ON state voltage drop and zero reverse recovery charge (Q_c), which produces a virtually null reverse recovery current (I_{rr}), allowing to switch very fast from ON to OFF. However, the leakage current is larger than for PiN diodes and increases quickly with temperature. Schottky diodes withstand much lower surge currents than PiN diodes.
- **Junction barrier schottky (JBS) or Merged PN Schottky diode (MPS).** This *SiC* diode has a hybrid structure. It combines the benefits of a low ON voltage drop and a low reverse recovery current of SBD diodes with the high surge current capability and low leakage currents of PiN diodes [227]. For these reasons, the JBS diode is the common solution for most commercial *SiC* power semiconductor manufactures. Typical voltage and current ranges of such devices are shown in figure 10(a), highlighting 600 V, 1200 V and 1700 V standard voltage ratings with a current range between 10 A and 50 A. Additionally, figure 12 highlights key advantages of JBS diode technology, such as low reverse recovery charge (3 nC@30 A - 370 nC@50 A), low forward voltage (1.35 V@30 A - 4 V@25 A) and relatively high maximum operation temperatures (175^{0}C). Thus, JBS diodes can be considered, among current solutions, as the best alternative for their application in automotive power converters.

As for *SiC* diodes, a number of *SiC* transistor technologies can be found in the market:

- ***SiC* Bipolar Junction Transistors (BJT).** They operate normally OFF, including high blocking voltage ranges (1200 V-1700 V) and wide current ranges (3 A-160 A) (figure 10(b)). These devices have low conduction voltage drops, thanks to

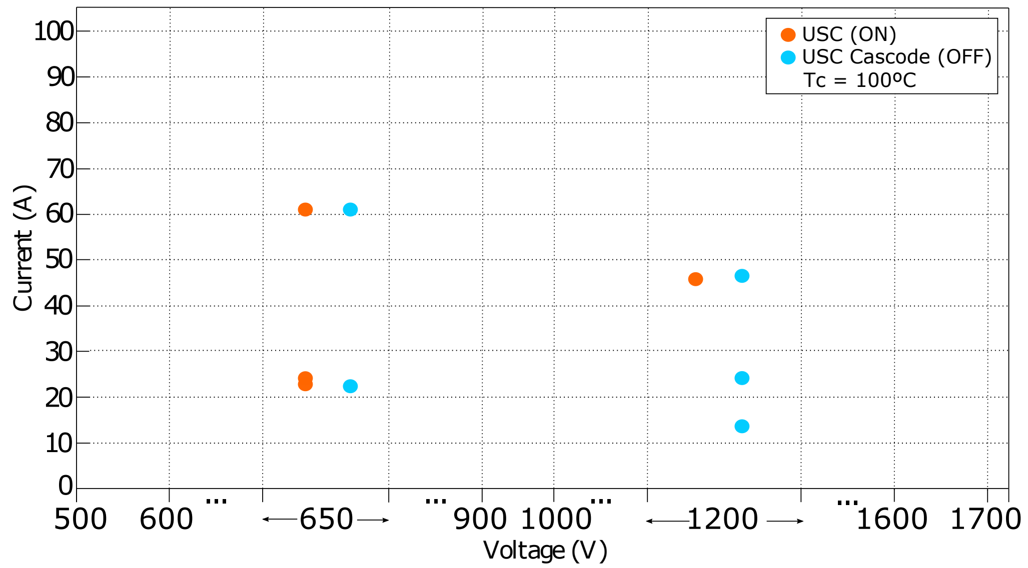


(a) *SiC* diodes voltage and current ranges.

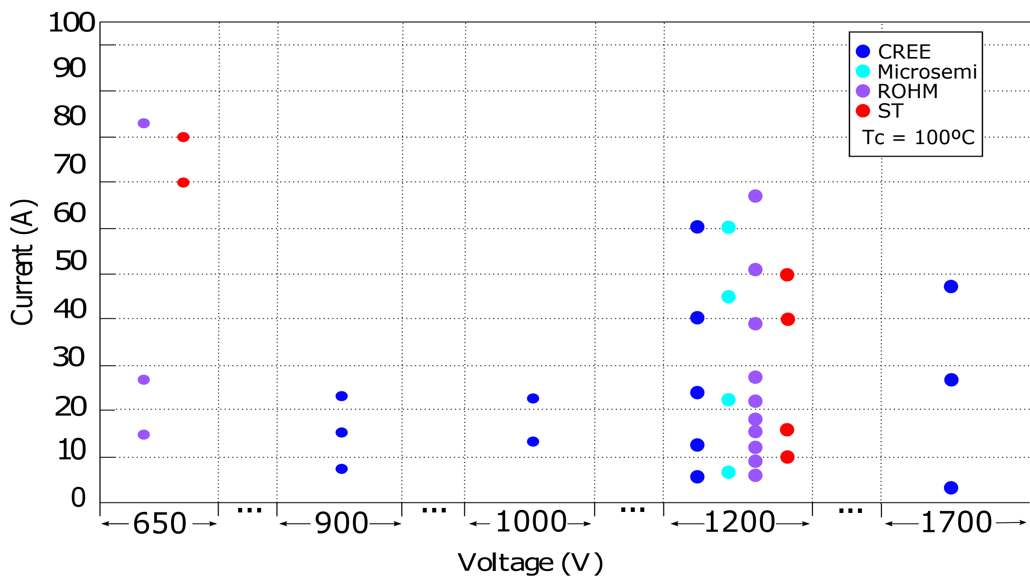


(b) *SiC* BJTs voltage and current ranges.

Figure 10: Voltage and current ratings of current *SiC* devices available on the market (I).

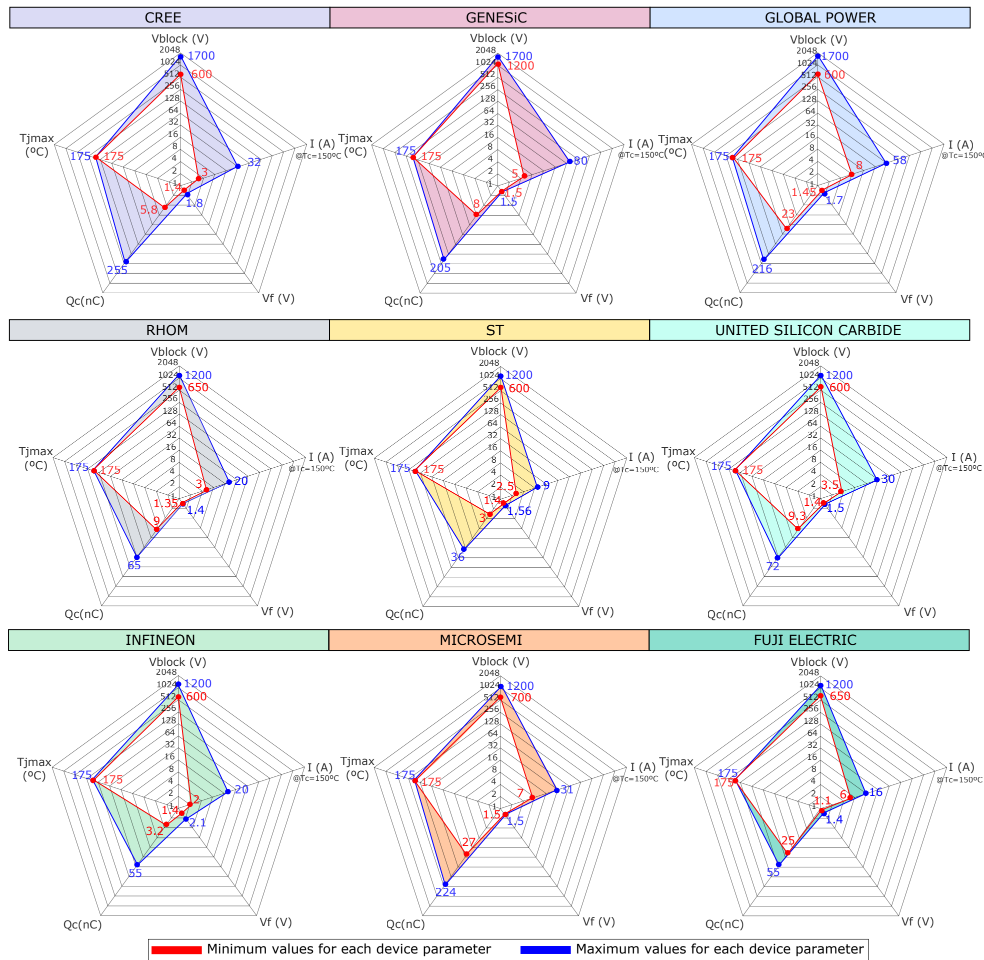


(a) *SiC* JFETs voltage and current ranges.



(b) *SiC* MOSFETs voltage and current ranges.

Figure 11: Voltage and current ratings of current *SiC* devices available on the market (II).

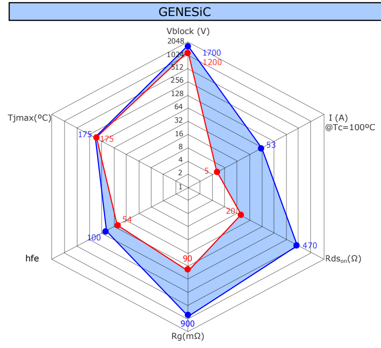


(*)The shaded area represents the possible values of the particular *SiC* diode parameters, while each colour represents a given manufacturer.

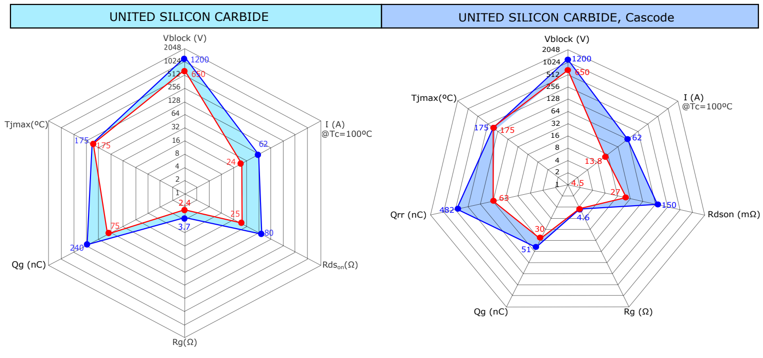
Figure 12: Maximum and minimum values of the most significant parameters of *SiC* devices (I)-DIODES.

an equivalent low ON state resistance (10 $m\Omega$-470 $m\Omega$), a positive R_{on} temperature coefficient and fast switching capabilities [232, 233] (figure 13(a)). However, they are current controlled devices, and have a negative current gain temperature coefficient. In addition, the design of the driver circuit becomes more complex than for voltage controlled devices.

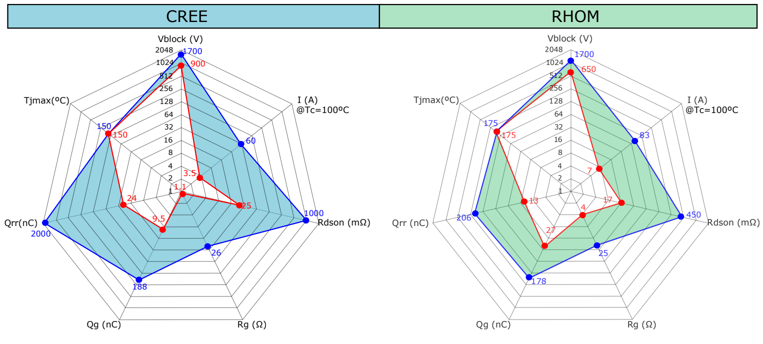
- ***SiC* Junction Field-Effect Transistors (JFET).** As basis, *SiC* JFETs can be considered as an excellent alternative for HEV/EV, because the lack of gate oxides allows to operate at high temperatures without stability problems (which occur in MOSFETs) [232, 234]. Moreover, the threshold voltage is independent of the junction temperature, and they exhibit an ultra low ON resistance [235, 236]. *SiC* JFETs are by default normally ON devices that are blocked when the gate-source p-n junction is reverse biased. In a similar way than for *GaN* HEMTs, normally

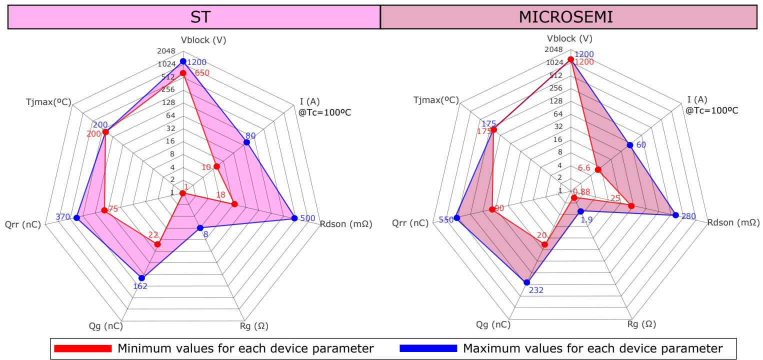


(a) SiC BJTs maximum and minimum values.



(b) SiC JFETs maximum and minimum values.





(c) SiC MOSFETs maximum and minimum values.

(*)The shaded area represents the possible values of the particular SiC device parameters, while each colour represents a given manufacturer.

Figure 13: Maximum and minimum values of the most significant parameters of SiC devices (II).

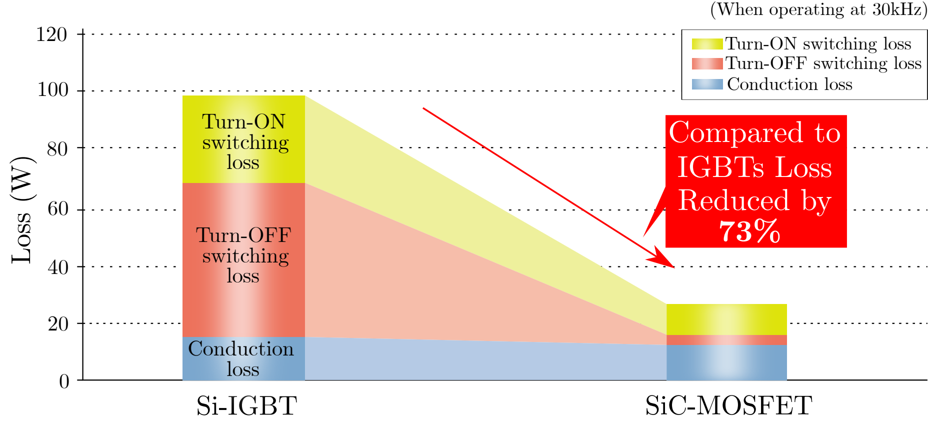


Figure 14: Power loss reduction achieved with *SiC* MOSFET compared to *Si* IGBT (source ROHM).

off devices can be obtained by connecting a low Ron *Si* MOSFET in cascode configuration with the *SiC* JFET (figure 13(b)). Nevertheless, the same effect can be obtained by modifying the JFET gate structure in a way that the channel region is interrupted (or depleted) at zero gate bias, although the subsequent threshold voltage is relatively low. Due to such a low threshold voltage, JFETs require specific driving circuits different from standard *Si* IGBT drivers. In both approaches, the price to pay for having a normally off behaviour increases R_{on}. *SiC* JFETs can be divided into two families, attending to the internal structure used for their design and fabrication [29, 30, 232]:

- Lateral channel component JFETs (LC_{JFET}). Although such devices are vertical, their channel shows a lateral component. They show higher on-state resistance than their vertical counterparts [237, 238].
- Vertical trench JFETs (VT_{JFET}). In this technology, the conduction channel is completely vertical, allowing a much higher level of integration and a lower on-state resistance [239].

Overall, it can be concluded that normally OFF *SiC* JFETs are still not mature enough for HEV/EV applications. In spite of their voltage and current levels (figure 11(a)), high current modules have not yet been commercialized.

- ***SiC* Metal Oxide Semiconductor Field Effect Transistors (MOSFET).** These devices have the same vertical structure than *Si* MOSFETs, are normally OFF, and provide a good balance between conduction and switching losses [28] due to their low ON resistance and $Q_g$charge (figure 13(c)). In this context, figure 14 shows the theoretical power loss reduction that could be achieved when substituting *Si* IGBTs by *SiC* MOSFETs of similar ratings.

  Another relevant feature is that they can be fired using the same driver circuitry as for *Si* IGBTs (the referent for current power converters in HEV/EV propulsion systems), making the transition between both technologies easier. Additionally,

Table 5: *SiC* semiconductor technologies, listing their most relevant advantages and disadvantages [29, 30, 228, 229, 233, 235, 240, 241].

Device	Main advantages	Main disadvantages
SiC diodes	Lower reverse recovery charge than *Si*	
	Lower switching losses than *Si*	
	Positive temp. coefficient$^{(1)}$	
PiN	High Voltage (>3,3 kV)	High reverse recovery current
	Low leakage current (Temp. independent)	High reverse recover charge
	Low conduction resistance	
SBD	Typical voltage abour 600 V	Higher leakage current
	Low reverse recovery current	High variation with temperature
	Low reverse recovery charge	
JBS	Hybrid device (SBD and PiN) 600 V-3.3 kV	
SiC BJT	Normally OFF	Current controlled
	Low conduction voltage drop	Complexity of the driver$^{(2)}$
	Gate-emitter low conduction voltage	
	Fast switching dynamics	
SiC JFET	High operation temp.	Lateral JFET normally ON$^{(3)}$
(lateral, vertical)	Threshold voltage no temp. dependency.	VT_{JFET} normally ON $^{(4)}$
	Vertical JFET without parasitic diode$^{(5)}$	
	Low conduction resistance	
SiC MOSFET	Normally OFF	Low robustness
	Gate charge similar to *Si* IGBTs	(gate reliability)
	Same drivers as for *Si* IGBTs can be used$^{(6)}$	
	Ratings similar to *Si* IGBTs$^{(7)}$	
	Higher switching frequencies	
	Positive temperature coefficient$^{(1)}$	
	Higher thermal conductivity	

Notes:
(1) Required for easy device parallelization.
(2) Compared with the voltage controlled devices.
(3) Compromising converter safety under transistor firing control malfunctions.
(4) VTJFET normally ON appears in cascode configuration to be normally OFF.
(5) Such parasitic diodes exhibit low performance, including high conduction losses.
(6) Simplifying the migration from *Si* to WBG power conversion technology.
(7) Taking into account that *SiC* Mosfet is compared with IGBT structure

they can operate without an external antiparallel diode, due to the body diode present in the transistor structure [28, 242, 243]. Nevertheless, this solution must be analysed for each application, because better results will be probably obtained with external and optimized JBS diodes. Charge (Q_{rr}) values are very similar to the gate MOSFET charge (Q_g) (figure 13(c)). In general, *SiC* MOSFETs are at this moment the devices receiving more research efforts for high power applications (for example, for improving the long term threshold voltage stability) and significant improvements are continuously reported [230, 233, 234]. For example, a major breakthrough was the introduction of the ultra-low R_{on} *SiC* MOSFETs based on a trench gate structure.

Regarding voltage and current ratings of such devices (between 400 V-1700 V and 2.6 A-100 A, figure 11(b)), their implementation in HEV/EV propulsion applications is feasible using the devices with the higher current range. In this sense, a

number of manufacturers are producing full *SiC* MOSFET modules[6]. Considering the figures determined in section 2.1, HEV/EV propulsion inverters could be manufactured by an affordable parallelization of modules, discrete devices or dies.

From the reviewed literature and considering all the aforementioned merits of *SiC* MOSFETs, it can be concluded that these devices offer the best features for HEV/EV applications among WBG transistors.

As a summary, table 5 shows the main features of *SiC* based technologies that can be found on the market. *SiC* based IGBTs have not been considered, because they are in early research stages and they are not commercialized [244]. As it has been previously justified, *SiC* JBS diodes and MOSFETs are the most adequate devices to substitute traditional *Si* FRD diodes and *Si* IGBTs. However, the current ratings of discrete semiconductors are not high enough to cope with the actual requirements of electric vehicles. Thus, parallelization through discrete elements or bare dies (constituting a power module) is mandatory in order to get higher current levels and other power requirements of HEV/EV applications (section 2.1). In this context, the implementation of ad hoc power modules (using bare dies) could provide a better performance, because it will be feasible to manufacture power converters with low parasitic inductances, improved thermal characteristics and higher power densities, desirable features for automotive power applications. In the following, the most relevant aspects regarding the design of future automotive *SiC* power modules will be reviewed.

4. Automotive *SiC* power module: constituting parts, design process and criteria

In general, two approaches are followed by the industry to implement the power switches of an automotive converter:

- Discrete IGBT devices. This approach is being followed by Tesla in most of their vehicles [57], where International Rectifier discrete IGBTs (AUIR family, TO-247 package) are mounted over a power PCB. The advantage of this approach is that the power ratings of the converter can be easily upgraded over the existing design (without significant modifications) by means of substituting the discrete devices.
- Power modules. For example, Nissan, BMW, Audi, Toyota and Chevrolet have adopted half-bridge or six-pack IGBT modules with their specific layout and cooling technologies [57]. However, *SiC* MOSFET power modules are also being adopted for next generation vehicles. In this context, Tesla has integrated a full *SiC* power converter with 24 1-in-1 power modules over a pin-fin heatsink in his Model 3 vehicle [245].

Thus, it can be concluded that major automotive OEMs have generally adopted power module technology to constitute the traction inverters, which is in concordance with the conclusions provided at the end of the previous section.

[6]These modules include *SiC* JBS diodes in anti-parallel to the transistors in order to improve the properties of the module, as the performance of the body diode of a *SiC* MOSFET is inferior than the preformance of the JBS [240].

Bearing in mind that the preferred power conversion topologies for HEV/EV applications would be based on the half bridge branch configuration (section 2.2), the power stage could be modular, i.e. made of independent or single phase modules, or and standalone power module that groups all the required converter phases. Regardless of the selected solution, both approaches share the same constituting elements.

In this context, ideas and design criteria reviewed from commercial and research solutions will be provided for the design of automotive *SiC* power modules, as their design can be more challenging (sections 2.5 and 3) than for *Si* technologies. Prior to focusing on the automotive *SiC* (MOSFETs and JBS diodes) power module design process, it is important to describe and understand such constituting elements.

In general, it can be stated that a bare die based power module can be divided into five key parts (figure 15), i.e., mechanics (encapsulation), substrate (stack-up), gate attack (for control and monitoring signals), power layout (for high current circulation) and terminals (power and control). Although, apparently, such parts can be considered separated blocks, they are interrelated, and the design of each part affects the others. Thus, a global vision of the problem is required when designing the whole module. In the following items, the most significant aspects of such fundamental parts are reviewed.

4.1. Power module mechanics

The mechanical part of the module (figure 15-A) is related to the particular encapsulation (standard or custom) and to the layout of the power connectors and auxiliary terminals (control and monitoring signals). This part imposes the main constraints on the design of the rest of the elements, as it sets the available space and terminals placement [246].

There is a wide portfolio of standard cases in the market. Some well-known transport solutions such as PrimePACK modules rely on the placement of the power connectors in the central part of the module, while other solutions place such terminals on the edges [59] (figure 16). Particularly, the most of current *Si* based automotive grade power modules such as the Infineon hybridPACK and Semikron SKIM 606 and 909 families adopt the border power terminal placement, as it allows to use integrated MKP-type DC-link capacitors, significantly reducing the parasitic inductances of the capacitor/module group [247]. Such modules assemble the driver board on top of the power module, providing a compact solution.

Extreme thermal variations (ΔT_{vj}) within the module during vehicle driving profiles have also a great impact in the design of the case and connectors. For example, a vehicle that is parked in extreme weather conditions (bellow -20°C) preheats its power converter cooling system to its nominal coolant temperature (of between 65°C-85°C) and, during driving, the junction temperature T_{vj} reaches high values. When the vehicle stops all the systems cool again. As a result, an extreme ΔT_{vj} of 150°C (or greater) can be easily generated. This phenomena affects the joints between elements of different materials with different dilatation coefficients. If the module design does not take all this into account, premature failures can occur within the module, although the maximum junction temperature has not been reached. In this sense, the automotive design must ensure a minimum number of such extreme operation cycles. The innovative solution provided by Semikron for the SKIM family can be highlighted, where the connectors and the plastic elements are solderless and are hold in their position by applying an specific pressure on the module screws [59, 248].

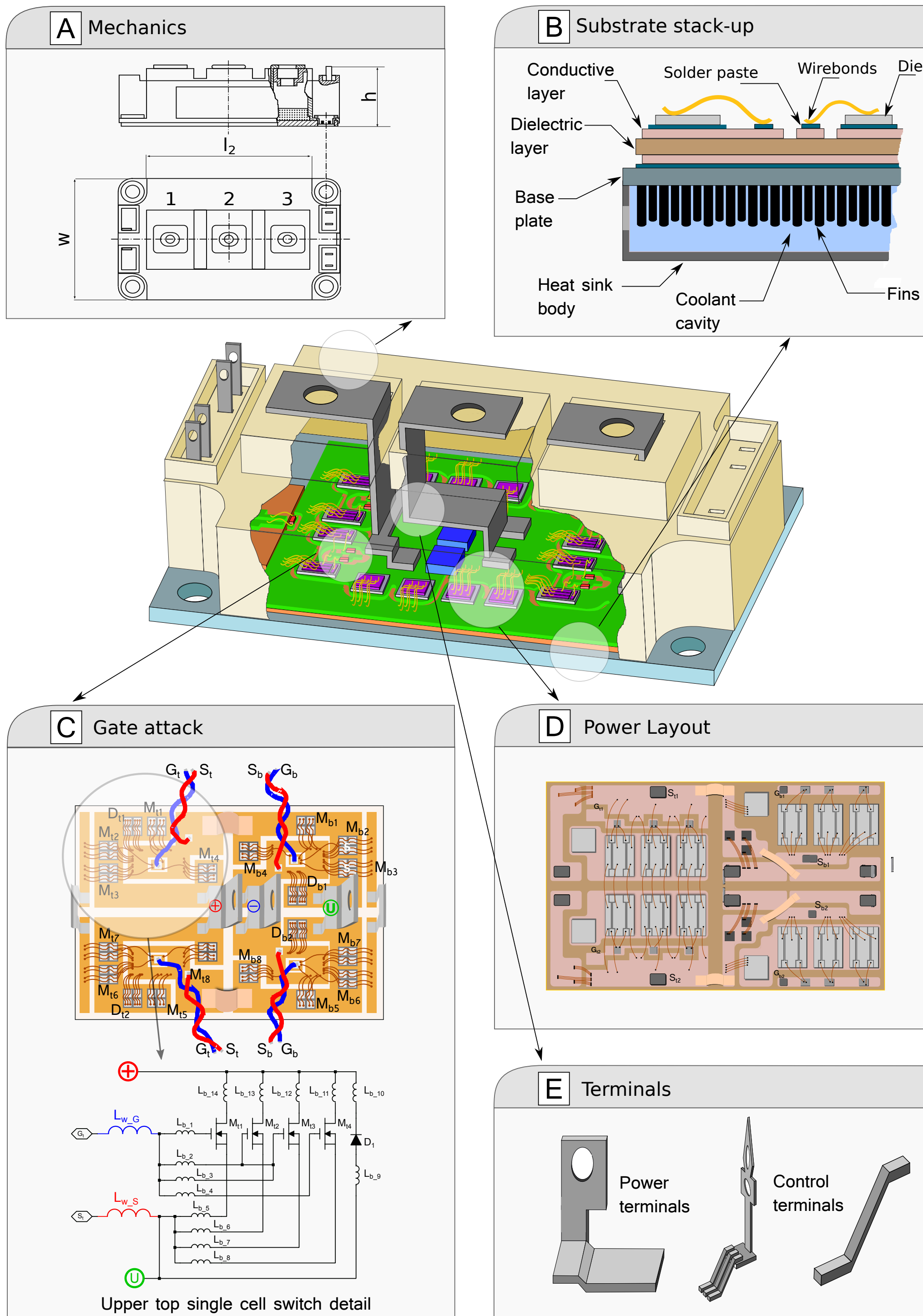
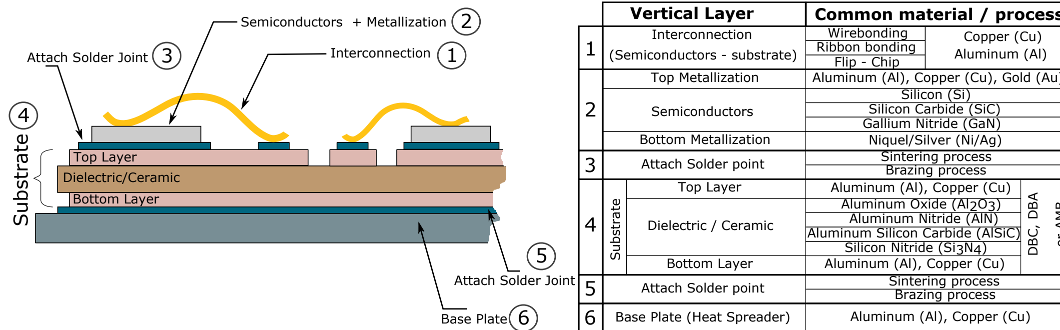


Figure 15: Main parts that constitute a bare die based power module.

	Phase leg / Half Bridge	Full Inverter
Semikron	Semitrans 2: Main power and DC Bus terminals; Auxiliary terminals; Baseplate	Semix 13: Auxiliary terminals; Main power terminals; DC bus terminals; Baseplate
Semikron	Semitop 3: Mounting hole; Mounting post; No baseplate; main power and auxiliary connectors (soldered)	SKiM 93: Main power terminals; Pressure part; DC bus terminals; No baseplate; Springs to driver auxiliary terminals
Infineon	Econodual 3: DC bus terminals; Main power terminal; Baseplate; Auxiliary terminals	EconoPack E3: DC bus terminals; Main power terminals; Baseplate; Auxiliary terminals
CREE	Half Bridge module: Main power and DC Bus terminals; Auxiliary terminals; Baseplate	Six-Pack: Main power terminals; DC bus terminals; Auxiliary terminals; DC bus terminals; Baseplate

Figure 16: Examples of standard power module encapsulations.



	Vertical Layer		Common material / process		
1	Interconnection (Semiconductors - substrate)		Wirebonding Ribbon bonding Flip - Chip	Copper (Cu) Aluminum (Al)	
2	Top Metallization		Aluminum (Al), Copper (Cu), Gold (Au)		
2	Semiconductors		Silicon (Si) Silicon Carbide (SiC) Gallium Nitride (GaN)		
2	Bottom Metallization		Niquel/Silver (Ni/Ag)		
3	Attach Solder point		Sintering process Brazing process		
4	Substrate	Top Layer	Aluminum (Al), Copper (Cu)		DBC, DBA or AMB
4	Substrate	Dielectric / Ceramic	Aluminum Oxide (Al_2O_3) Aluminum Nitride (AlN) Aluminum Silicon Carbide (AlSiC) Silicon Nitride (Si_3N_4)		DBC, DBA or AMB
4	Substrate	Bottom Layer	Aluminum (Al), Copper (Cu)		DBC, DBA or AMB
5	Attach Solder point		Sintering process Brazing process		
6	Base Plate (Heat Spreader)		Aluminum (Al), Copper (Cu)		

Figure 17: General substrate structure for a power application.

4.2. Substrate stack-up

The substrate (figure 15-B) provides a surface where power semiconductors and other components, such as passive elements and control and power terminals, are placed and interconnected allowing their electrical connection and isolation with a good thermal conductivity [249]. A variety of technological solutions can be found in the literature and the industry, specially when WBG devices are incorporated, being good examples various advanced solutions such as the SKiN structure, the SiPLIT solution, and other embedded structures of multiple layers [250–252]. All the aforementioned require non-conventional materials, processes and design concepts, incorporating novel attach materials, interconnections and advanced heat transfer cooling systems [253, 254]. Considering that the automotive industry is cost sensitive, inorganic substrates such as Direct Bonding Copper (DBC), Direct Bonding Aluminum (DBA) or Active Metal Brazing (AMB) could be preferred [255].

In DBCs and DBAs, the union between copper and ceramic layers is an eutectic bond. In AMB, copper and ceramic layers are joined by a brazing process [255]. For illustration purposes, figure 17 shows the interconnections and layers generally present on a DBC substrate based design [256, 257]. The most common interconnection technology is the wirebonding [258], even though other solutions such as ribbon bonding and flip-chip can be also found to connect the semiconductors with the top layer of the substrate. On the other hand, semiconductors have metallization layers on both surfaces in order to assembly the top surface with the wirebondings and the bottom surface with the substrate. Finally, it is also important to point out that the attaches between semiconductors-substrate and substrate-base plate are based on sintering or brazing processes [259].

All these substrate layers (figure 17) determine the vertical thermal behaviour between the power semiconductors and the base plate. The material of each layer must have a high thermal conductivity (λ) to achieve a low thermal resistance (R_{th}), which is given by [250, 257, 260]:

$$R_{th} = \frac{d}{\lambda \cdot A}, \tag{2}$$

where d and A are the thickness and the area of the layer, respectively. On the other hand, the equivalent thermal resistance $R_{th_{subs}}$ substrate is the sum of the R_{th} of each layer:

$$R_{th_{subs}} = R_{th_1} + R_{th2} + R_{th_3} + ... + R_{th_N}. \quad (3)$$

Regarding mechanical aspects, the thermal expansion coefficients (CTE or α) of the different materials that constitute the substrate (4) are relevant parameters, as they indicate the dilatation/contraction of materials due to temperature variations. Such coefficients must be as close as possible in order to prevent mechanical fatigue between layer, which could significantly reduce the lifetime of the power module [250, 257].

$$\alpha = \frac{\Delta L}{L_0 \cdot \Delta T}, \quad (4)$$

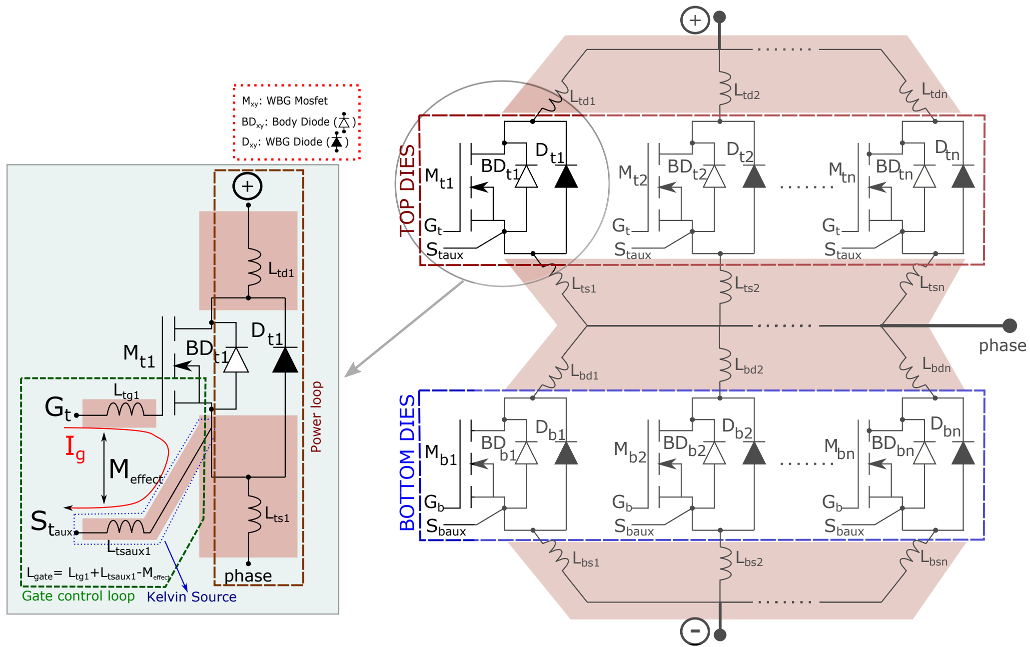
where L_0 is the overall length of the material, ΔL is the linear deformation with respect to L_0 and ΔT is the temperature variation with respect to temperature from which L_0 has been determined.

4.3. Gate Attack

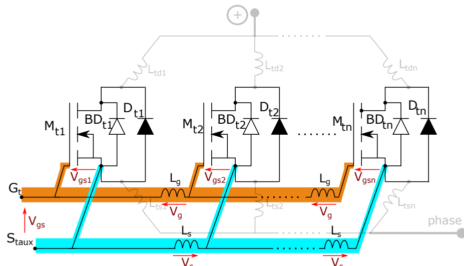
The elements that constitute the gate attack (figure 15-C) manage and distribute the control signals that drive the power transistors. In modules with more than one parallelized power semiconductor per switch. (figure 3), imbalances in the gate control signals can be produced [261]. Such imbalances are generated, among other things, due to different stray inductances between gate control loops (figure 18(a)), whose effects produce turn ON/OFF delays, and also variations of power losses among paralleled semiconductors. All this can produce uneven current distributions among the paralleled elements, leading to possible hot spots and thermal runaway which, in some situations, could produce module failures [262–264].

Other significant problem produced by an inadequate gate attack design is the generation of high electromagnetic interferences (EMI). This aspect is more relevant when *SiC* devices with high speed commutation capabilities are used instead of slower *Si* devices. As a solution, minimizing and matching gate loops [265] decreases such harmful electromagnetic interference (EMI) effects [266]. Thus, an adequate gate attack design must be carried out. As a general rule of thumb, it can be said that control signal tracks must be as short as possible to reduce equivalent parasitic impedance of gate loops. However, more specific issues regarding the gate attack design must be considered in order to achieve an adequate solution:

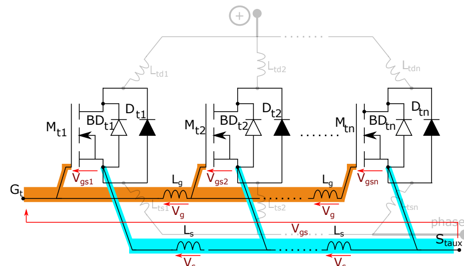
- The power and gate control loops must be independent in order to avoid feedback effects. For that reason, an auxiliary connection S_{taux} (figure 18(a)) is required to control the commutations of the transistors [261, 267–269]. This type of connection is known as Kelvin connection. The control signals, which are applied between the transistor gate (G_t) and source (S_{taux}) contacts, have their own tracks with a low parasitic impedance, being decoupled from the power signals, specially from the stray impedance L_{ts1} (source inductance) of the power loop (figure 18(a)).
- The control signals are differential, consisting on two tracks, gate and source (figure 18(a)). These tracks must be as close as possible between them, reducing the length of the gate loop, and improving their mutual coupling effect. All these reduces the parasitic gate loop inductance (5), improving the robustness of the differential signal to external noise sources (EMI) [268, 270].



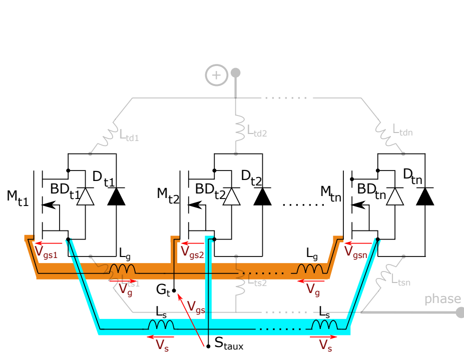
(a) Half-Bridge of n semiconductors in parallel with the detail of gate loop.



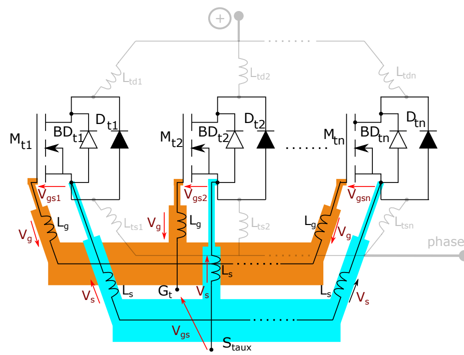
(b) Negative asymmetry feedback effect.



(c) Positive asymmetry feedback effect.



(d) Negative-positive asymmetry feedback effect.



(e) Negative symmetry feedback effect.

Figure 18: Gate current loop and feedback effects.

$$L_{gate} = L_{tg1} + L_{tsaux1} - M_{effect}, \tag{5}$$

where L_{gate} is the whole inductance of the gate loop, L_{tg1} is the equivalent inductance of the gate track, L_{tsaux1} is the equivalent inductance of the auxiliary track, and M_{effect} is the mutual coupling effect between both tracks. It is important to consider that the inductance value of transistor gate track L_{tg1} (which can produce voltage drops in the control signals, and oscillations that are able to produce unexpected turn ONs [271]) must be minimized [268].

- Each paralleled transistor (figure 18(a)) must have its own gate control loop. The gate tracks of all the paralleled devices must have the same length and width to have an equal stray impedance. This is of paramount importance to obtain a good turn ON synchronization between devices[7]. Thus, a symmetrical gate attack design should be followed [261, 272, 273]. The next examples summarise various feedback effects over gate attack depending on the specific parasitic inductances derived from given layouts [274, 275]:

  (a) When the gate (G_t) and source (S_{taux}) control terminals are placed one next to the other in one side of the switch (figure 18(b)), a negative feedback effect is introduced in the gate signals. As a result, transistor 1 turns ON faster than transistor n, as:

  $$V_{gsn} = V_{gs} - n \cdot (V_g + V_s) < V_{gs2} = V_{gs} - (V_g + V_s) < V_{gs1} = V_{gs}, \tag{6}$$

  where V_{gsj} is the gate-source voltage of the transistors, being $j = \{1, 2...n\}$ and n the number of paralleled devices per switch, V_g is the voltage drop of the equivalent gate inductance and V_s is the voltage drop of the equivalent source track inductance.

  (b) When the G_t and S_{taux} terminals are located in the opposite sides of the switch (figure 18(c)) and the gate track equivalent inductance (L_g) is significantly smaller than the source track equivalent inductance (L_s), a positive feedback effect is generated in the gate signals. As a consequence, transistor n turns ON faster than transistor 1, as:

  $$V_{gsn} = V_{gs} - n \cdot V_g > V_{gs2} = V_{gs} - V_g - (n-1) \cdot V_s > V_{gs1} = V_{gs} - n \cdot V_s. \tag{7}$$

  (c) When G_t and S_{taux} are located in the center of the switch (figure 18(d), a negative and positive feedback effect are simultaneously generated in the gate signals. In this situation, transistor 2 turns ON faster than transistor 1 and n, as:

[7] If the paralleled semiconductors do not switch ON at the same instant, there is a small period of time along which the whole phase current is shared by less semiconductors than expected, leading to overheating.

$$V_{gs2} = V_{gs} > V_{gs1} = V_{gs} - (V_g + V_s) > V_{gsn} = V_{gs} - n \cdot (V_g + V_s), \quad (8)$$

where $n \cdot (V_g + V_s) >> (V_g + V_s)$.

(d) When each parallel transistor has its own gate loop connected to gate-source control terminals in a symmetrical distribution to match the parasitic inductances (figure 18(e)), a negative feedback effect is produced in the gate signals, but all the transistors turn ON at the same time, as:

$$V_{gs1} = V_{gs} - (V_g + V_s) = V_{gs2} = V_{gs} - (V_g + V_s) = V_{gsn} = V_{gs} - (V_g + V_s). \quad (9)$$

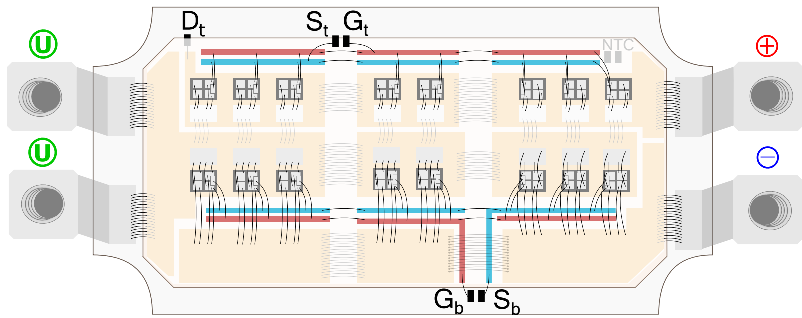
It becomes clear that this should be the design target that should be followed by the power module designer. However, a perfect symmetry is not always feasible, because the mechanical constraints of the power module may not allow to perfectly match the desired gate attack layout.

Once the ideal design criteria have been reviewed, these concepts can be implemented in different ways. The following three real industrial examples are the mainly commercial implementations of gate attack that will be analysed, focusing on the particularities of the design concepts carried out by each designer team. Such solutions can be summarized as:

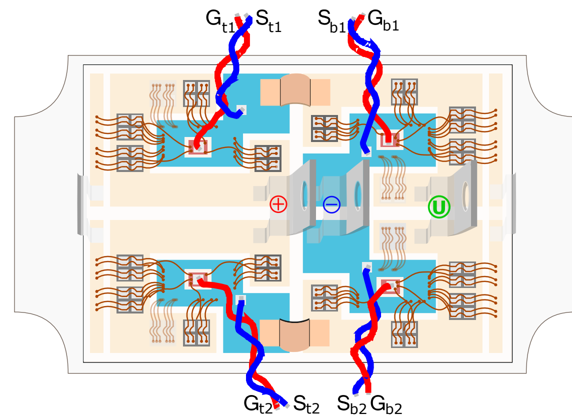
1. **Gate control signals over the power layout area.** In this solution, gate control loops (gate and source tracks) are positioned over the conduction layer of the substrate (power layout), i.e. the first layer of the DBC (figure 19(a)). The power and gate loops share the same substrate layer which may introduce interferences through the coupling between the power and control signal tracks [276]. The main drawback of this alternative is that the power module has an specific routing area, defined by the mechanical constraints, where a variety of components such as the power semiconductors, control and power terminals, and passive elements (i.e. gate resistances to protect parallel *SiC* MOSFETs) must be assembled. Consequently, the routing area that is exclusivelly dedicated to the power layout is reduced. Additionally, the design routing process becomes more complicated, since there are more electrical connections in a single surface (i.e. the number of wire bonding connections are increased in order to make all the electrical connections).

   As a conclusion, it can be stated that this solution increases the total parasitic impedance of the power module, since the area dedicated to the power signals is reduced [277].

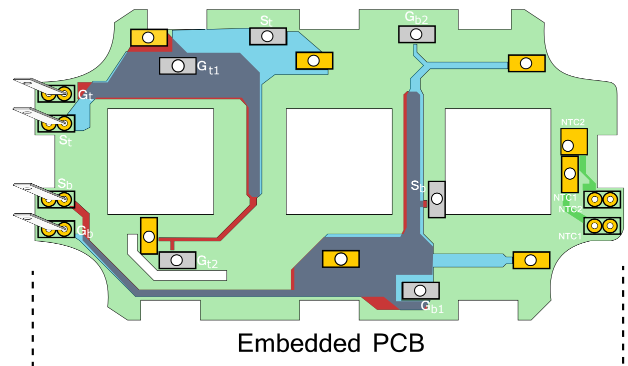
2. **Gate control signals through twisted wires connected to the power layout.** This solution allows to use the full DBC area for power connections, overcoming the problems generated by the previous design example. Wires (control signals) can be connected close to the transistor control contacts (figure 19(b)), reducing the parasitic impedance of the gate loop [59]. All the required wires are manufactured with the same length, avoiding previously explained imbalance problems.

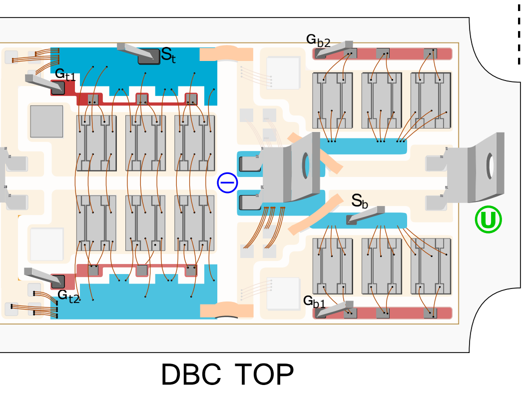


(a) Gate signals over power layout.



(b) Gate signals with twisted wires.





(c) Gate signals through PCB embedded.

Figure 19: Different gate attack options in commercial Half-Bridge power modules.

The twisted configuration provides a reduction of the gate loop stray inductance L_{gate} because the wire coupling effect M_{effect} is greater, as it can be seen from (5). This twisting also provides a higher robustness against EMI.

However, this solution does not allow to mount protection circuits directly in the gate loops, because the passive and active components (i.e. capacitors, resistances and diodes) required for such protections only can be implemented on the DBC, which reduces the power signals area and increases the design complexity.

3. **Gate control signals routed through an embedded PCB.** This option increases the degrees of freedom of the design (figure 19(c)), because the gate control loop protections (or other additional circuitry) could be mounted over the power module in the embedded PCB [272, 278] . The embedded PCB can be connected in vertical with the transistor gate-source contacts, minimizing the gate loop [268, 278].

   This embedded PCB based design leads to a multilayer structure, where the parasitic impedance L_{gate} decreases as the coupling effect M_{effect} is increased in the gate-source loop (opposite current directions). Using symmetric strategies for the gate-source tracks together with wide track areas, round squares and anti-copper pours, it is feasible to balance the currents of each paralleled gate transistor [261]. Finally, it is also possible to mount capacitors that reduce the track between the gate-source connection (limiting the current circulating through the gate).

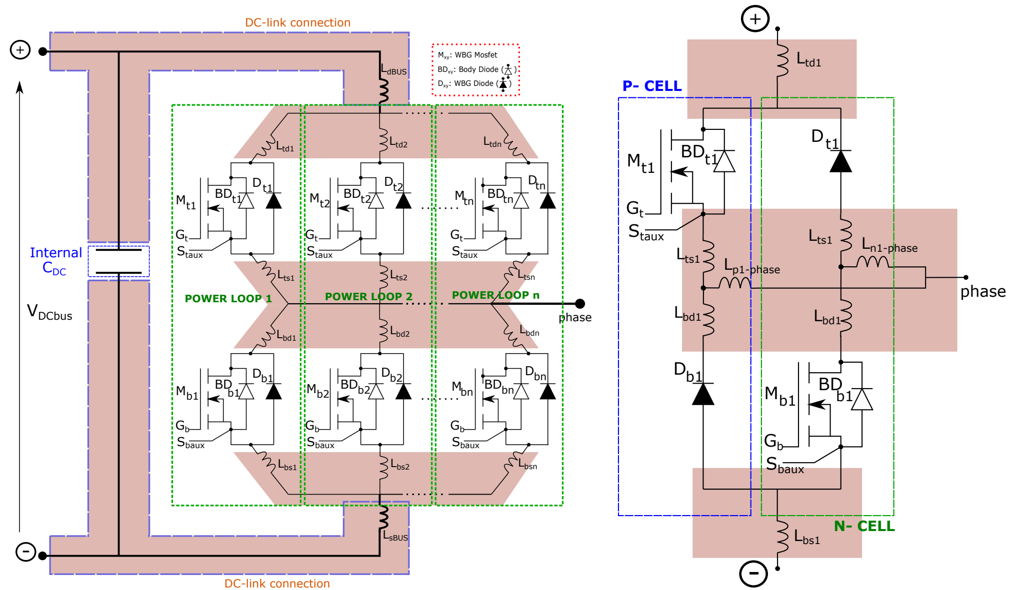
4.4. Power layout

The power layout (figure 15-D) constitutes the larger area of DBC (substrate) from which the high currents flow. As the switches are constituted by various paralleled dies, the design of the power layout should be conducted in a way that such circulating currents become balanced through all the paralleled devices. This arrangement improves the power module lifetime, performance and efficiency [279–282]. Taking all the latter into account, the power layout should be designed according to the following steps:

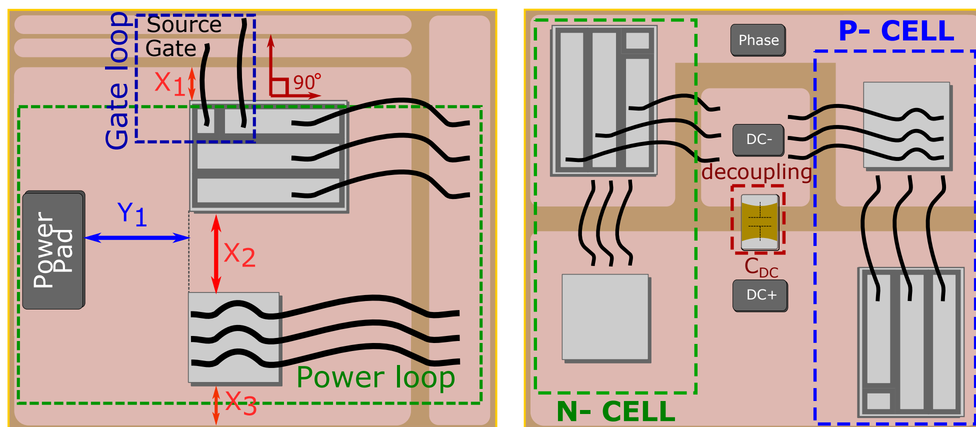
- The characteristics of the selected power semiconductor must be previously analysed in order to understand how they behave in parallel. Differences in parameters such as conduction resistance (R_{dson}) and threshold voltage (V_{th}) of paralleled dies can introduce significant current imbalance problems [274, 283–285]. In order to reduce such deviations, it is highly recommended to use devices with the positive thermal coefficient and same bare code [257].

- The available space is one of the most significant constraints during the power layout routing process. In general, the less devices to place, the easier is the routing process, because there is more space available to balance the tracks between the power semiconductors (power loops, figure 20(a)) [286].

  A *SiC* MOSFET based half-bridge with a given blocking voltage and current handling capability can be designed in a variety of ways. For example, the number of required dies can be reduced by using the body diodes of the MOSFET dies instead of external *SiC* JBS diodes. However, this approach reduces the efficiency of the module (worse performance of), as the resistance of the body diode is higher than of the JBS diode.



(a) Power loops of Half-Bridge of N semiconductors. (b) Cell power loop schematic.



(c) Wide and length variations. (d) Cell power loop layout.

Figure 20: Power loop device interconnection and stray inductance variation.

When using external SiC diodes, the routing process becomes more complicate, but overall efficiency can be further improved because SiC MOSFETs and SiC JBS diodes could be placed close together, forming a switch cell with a low stray inductance (figure 20(b)) [287, 288].

- In order to configure the electrical connections, the position and orientation of power semiconductor dies over the DBC layer (including their contacts ,i.e. gate, drain and source for SiC MOSFETs) must be considered [277]. A convenient placement allows to cancel electromagnetic fields between the power and gate loops. For example, wirebonding based electrical connections between control (gate-source) and power (drain-source) contacts must be perpendicular to avoid coupling (figure 20(c)) [268, 289].
- Before beginning to route the power layout connections, the areas that provide electrical insulation (clearance and creepage areas) must be defined to avoid possible short circuits. For this, it is important to consider the operating voltage, temperature and environment of the power application. The insulation area will depend on the pollution degree ratings of the specific application, which depends on the amount of dryness and condensation of the environment [290, 291].
- The electrical connections between the parallel power loops (figure 20(a)) must be defined. At this design stage, the total stray inductance of each power loop (L_{sw}) must be balanced (symmetric design) and reduced between the devices and the DC-link [267, 283, 285, 292, 293]. If a perfect symmetry is achieved, the total stray inductances of each power loop is:

$$\begin{aligned} L_{sw1} &= L_{td1} + L_{ts1} + L_{bd1} + L_{ds1} = \\ = L_{sw2} &= L_{td2} + L_{ts2} + L_{bd2} + L_{ds2} = \\ = ... = L_{swn} &= L_{tdn} + L_{tsn} + L_{bdn} + L_{dsn}, \end{aligned} \tag{10}$$

where L_{td} and L_{bd} are, respectively, the top and bottom equivalent parasitic inductances of drain connections, and L_{ts} and L_{bs} are, respectively, the top and bottom equivalent parasitic inductances of source connections subject to the following conditions:

$$\begin{aligned} L_{td1} &= L_{td2} = ... = L_{tdn}, \\ L_{ts1} &= L_{ts2} = ... = L_{tsn}, \\ L_{bd1} &= L_{bd2} = ... = L_{bdn}, \\ L_{bs1} &= L_{bs2} = ... = L_{bsn}. \end{aligned} \tag{11}$$

However, in practice it is not possible to meet a perfect match, but the design should try to approximate, as much as possible, to the result indicated in (10).

- For each single power loop, the connection between top and bottom devices must be defined to generate a power loop unit with the lowest L_{sw} possible. There are a great number of possibilities to connect top and bottom devices [269], among them, the cell or split option is generally adopted to achieve this goal [268, 285, 286, 294].

Figures 20(b) and 20(d) show the connections between a top SiC MOSFET and a bottom SiC JBS diode (P-Cell), and viceversa (N-Cell), following the cell concept. This configuration produces a reduction of L_{sw} because the physical switching routing is shorter [268, 273, 283]. The output (phase) inductance is increased, but this does not produce a drawback effect, because the load (electric machine) has a significantly higher inductive value.

- Adjusting the track dimensions of the switching loops can also help to reduce the stray impedance, because the parasitic inductance of the power layout depends on the width and length of the tracks [268, 269]. In this context, figure 20(c) illustrates the effects produced when changing track dimensions:
  - If X_1, X_2 and X_3 (specially X_2) distances are increased, a reduction of the parasitic inductance of the area is achieved, since the power loop is widen.
  - Increasing the length Y_1 increases the power loop stray inductance, since the distance between the power terminal and the semiconductors is increased.
- The application of symmetric design concepts help to balance the tracks of the electrical connections, obtaining similar parasitic impedances [269], providing currents flowing in opposite directions (which helps to reduce the parasitic inductances) [267, 268].

  For example, if an asymmetric design (figure 21(a)) is conducted, unequal lengths between power semiconductors and terminals are obtained, since the equivalent parasitic inductances between the positive main terminal and the switching cells (L_{DC^+1}, L_{DC^+2}, L_{DC^+3} and L_{DC^+4}) are:

$$\begin{aligned} L_{DC^+1} &= L_{d1} + L_{d2} + L_{d3} + L_{d4} \neq \\ \neq L_{DC^+2} &= L_{d2} + L_{d3} + L_{d4} \neq \\ \neq L_{DC^+3} &= L_{d3} + L_{d4} \neq \\ \neq L_{DC^+4} &= L_{d4}, \end{aligned} \tag{12}$$

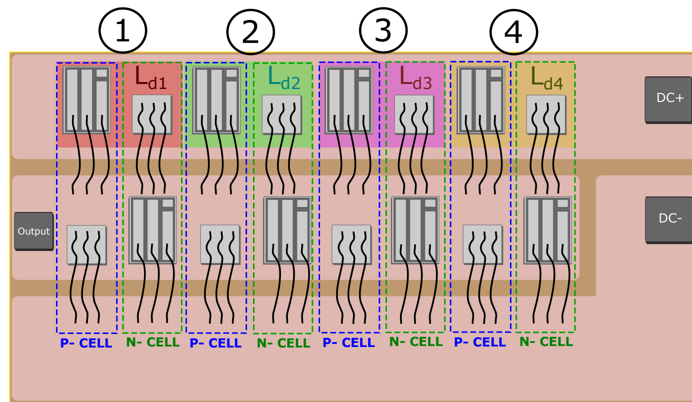
  where L_{d1}, L_{d2}, L_{d3} and L_{d4} are the equivalent parasitic inductances of each switching cell in drain connection.

  The previous can be greatly improved applying the concept of symmetry over one dimension [294] (figure 21(b)), where:

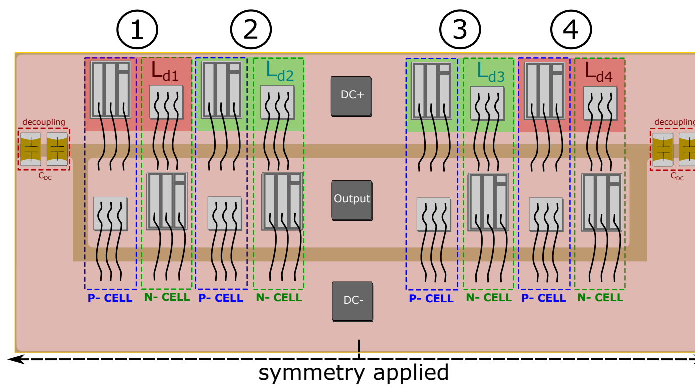
$$\begin{aligned} L_{DC^+1} = L_{d1} + L_{d2} = L_{DC^+4} = L_{d3} + L_{d4} \neq \\ \neq L_{DC^+2} = L_{d2} = L_{DC^+3} = L_{d3}. \end{aligned} \tag{13}$$

  The symmetry concept can be also applied in two dimensions [294], as shown in figure 21(c), improving the balance results and making a scalable power layout, where:

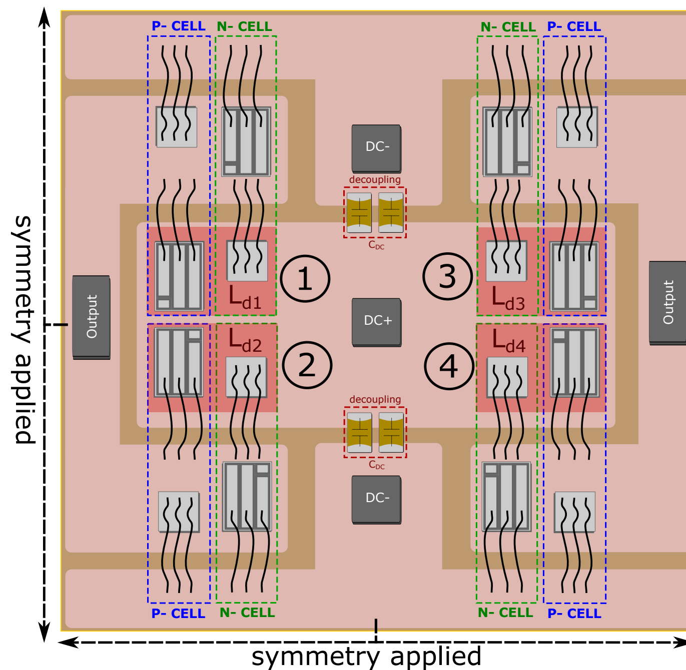
$$L_{DC^+1} = L_{d1} = L_{DC^+2} = L_{d2} = L_{DC^+3} = L_{d3} = L_{DC^+4} = L_{d4}. \tag{14}$$



(a) Asymetric design.



(b) Symmetry applied in one dimension.



(c) Symmetry applied in two dimensions.

Figure 21: Examples of applying symmetry over a DBC design.

Finally, it is interesting to consider that symmetry can be further improved following the design philosophy inherited from radio frequency (RF) and microwave design techniques used for power amplifiers, because both pursues similar goals [295]. According to these ideas, implementing round tracks, special cuts, edges and passive components (capacitors, figures 21(b) and 21(c)) can help to further balance and reduce power loops [292].

- Reducing the number of interconnections, particularly wirebondings, can be beneficial, since they introduce significant parasitic impedances and EMI to the circuit, aside from being the main source of failures due to mechanical stress [267, 287, 296]. As a general rule, wirebondings should only be used when another routing solutions are not possible in the design [246]. When using them, they must be as short as possible, and must be placed in an array configuration to reduce the parasitic inductance (generated due to parallel connection and coupling effects).

4.5. Terminals

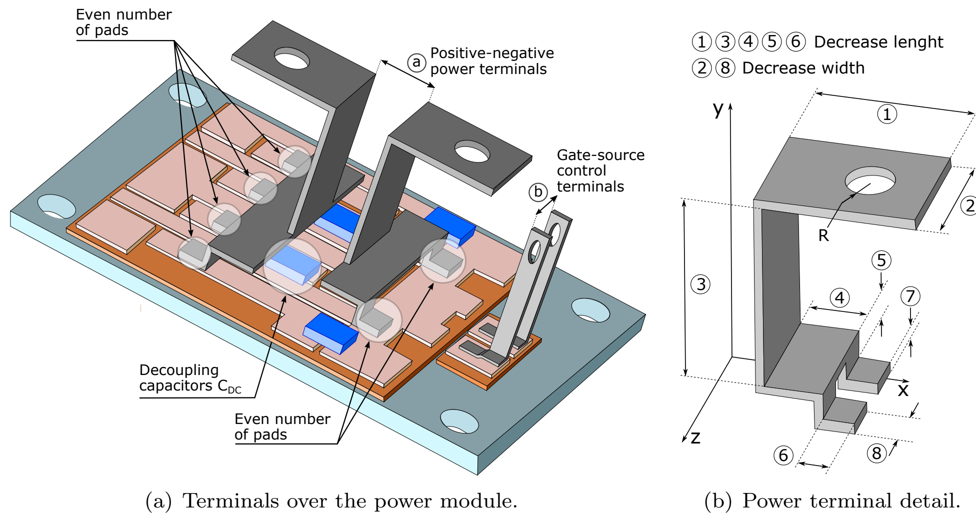
The power and control terminals (figure 15-E) connect the DBC substrate with the outside of the power module enclosure [297]. In general, these terminals are long and narrow, which significantly increases the total parasitic inductance of the module. Thus, the selection of the most appropriate connectors is a relevant aspect for automotive WBG modules. In order to improve their design, the following concepts could be adopted:

- The amount of terminals must be minimized, if possible, to avoid complex and long current loops [261]. However, there are some exceptions regarding control terminals. When the gate attack follows the embedded PCB design (section 4.3), the use of more control terminals over the DBC conduction layer could be beneficial, as it would reduce the length of gate loops, improving the inductance balance. This is due to the fact that the gate-source contacts of the dies are directly (vertically) connected.

- The pads of the terminals are the linking points between the terminals and the substrate conduction layer. Usually, the terminals have two pads to provide a good mechanical robustness and balance the current distribution in the connector (figure 22(a))[8]. The gate and power tracks must be designed to flow equal currents through the multiple pads that constitute the terminal, in order to minimize possible current distribution imbalances [297]. According to this symmetric concept, the terminals should be designed with a minimum even number of pads.

- Ideally, the terminals should be as width and short as possible to reduce their parasitic inductances (figure 22(b)), because they take part into the gate control and power loops. Also, differential signals must place their connectors as close as possible to reduce the stray inductance [257]. If the differential connectors (figure 22(a)) are close enough, it is possible to internally assemble a decoupling capacitor (C_{DC}) between the positive and negative power terminals [298], providing a reduction on the parasitic inductance.

[8] There are some particular exceptions, such as control terminals with only one pad.



(a) Terminals over the power module.

(b) Power terminal detail.

Figure 22: Examples of control and power terminals over a power module.

As a conclusion, it is remarkable that the terminals are sometimes forgotten during the design process. This represents a design flaw as, in some specific cases, they may introduce up to 50 % of the total inductance of power loop [267, 285].

4.6. Design steps of the SiC power module

Once the parts that constitute the module, their most significant design aspects and the interrelation between them have been clarified, it is important to point out which steps should be carried out in order to achieve a successful automotive power module design. It must be bear in mind that a well organized and appropriate design flow will allow to simplify and accelerate the whole design process of the module. This topic has been addressed in the scientific literature [251, 276, 289, 297]. However, this paper particularizes such work-flows to the WBG context and to the automotive application. As a summary, the design steps are depicted in figure 23.

5. Conclusions

The scientific literature and a number of agencies from Europe, United States and Asia support the idea that transport electrification would help to reduce current greenhouse gas emissions, which are responsible for some of severe environmental problems. In order to widespread the penetration of HEV/EV technologies, great research efforts should be conducted by the scientific community, leading to investigations on novel power conversion architectures, state of the art WBG power semiconductors, and particularized power module designs, to name a few.

Regarding the identification of the most appropriate power conversion topology, it can be concluded that there is not an unique optimum solution. The following points should be considered in order to select the topology for a given HEV/EV application:

1) In the near future, battery voltage will not exceed 1500 V (typically will be between 300-870 V), because operational safety requirements would significantly increase if such voltage is exceeded. Considering both blocking voltage capabilities of current semiconductor technology and cost efficiency, it becomes evident that two-level technologies will be the preferred option for HEV/EV propulsion system inverters.

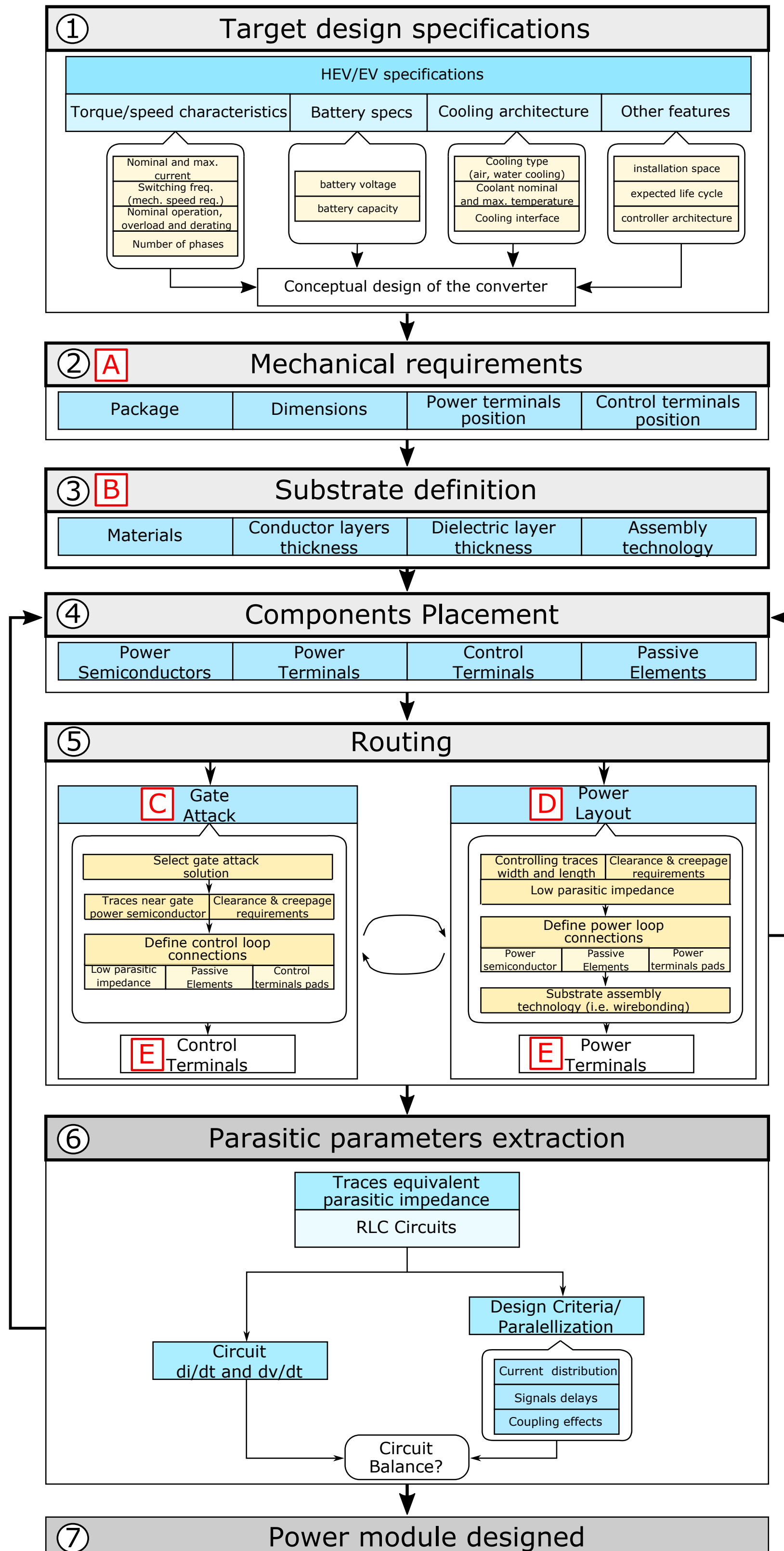


Figure 23: General design process for a power module based on standard solution.

2) Considering HEV/EV typical current and power ratings, parallelization of power semiconductor devices becomes mandatory, in the form of bare dies (constituting a power module) or discrete semiconductors.

3) The two-level three-phase topology is generally applied in current light to medium HEV/EVs, as it represents a cost effective solution. However, the introduction of multiphase technologies should be considered, not only for high power applications (trucks, electric buses or sport cars), but also when relevant propulsion system features such as efficiency, reliability and power and torque density need to be improved. On the other hand, it is important to remark that multiphase topologies could also be used to remove the need of a dedicated power converter for battery charging.

3) The progressive introduction of HSEM technologies will require to progressively increase the switching frequency of the power inverter. For this reason, the introduction of WBG technologies with reduced switching losses becomes crucial for the future. As these new semiconductors can operate at higher junction temperatures, another benefit derived form their introduction would be a reduction of the complexity and cost of the cooling system.

Regarding WBG technologies, the scientific literature shows that *GaN* and *SiC* devices are gaining popularity in the automotive market, as they overcome the limitations of traditional *Si* based technology. In this context, the following can be concluded:

4) Current *GaN* technology provides various diodes and HEMT transistors with blocking voltages of around 600-650 V, which, theoretically, could be applied for HEV/EV propulsion systems. However, up to date, they are not a valid option, because their current handling capabilities are highly limited (10-15 A), requiring the parallelization of too many devices. Moreover, there are no vertical devices (lateral devices) at the moment, which are necessary to manufacture compact power module designs with optimized thermal performance.

5) Currently, *SiC* power technology represents a real solution for HEV/EV applications, as a significant variety of matured vertical devices can be found in the market. Among them, it can be concluded that JBS diodes and MOSFETs are the most adequate for this application, because they can substitute traditional *Si* FRD diodes and *Si* IGBTs, providing lower power losses and higher operation temperatures. The migration from *Si* IGBTs to the aforementioned technologies would be simpler than expected, as the same firing circuitry (with minor modifications) can be reused.

The constituting element of the HEV/EV propulsion converter, with independence of the number of phases, would be (in the great majority of cases) the half-bridge configuration. In general, power modules are preferred over discrete devices due to their superior features. Considering, on the one hand, the demanding requirements of the automotive industry and, on the other, that parasitic inductances must be minimized as much as possible when incorporating WBG devices with high switching speeds, the following conclusions regarding design aspects can be highlighted:

6) The mechanics (power module encapsulation and layout of power and auxiliary terminals) imposes the main constraints for the design of the other elements that constitute the power module. Thus, special attention is required when designing such critical part. In the automotive context, the mechanical design must support extreme thermal variations during driving profiles, ensuring a minimum number of operating cycles in such extreme conditions.

7) A great number substrate alternatives, specially for modules incorporating *SiC* technologies, can be found in the scientific literature. However, the standard substrate technology, based on inorganic substrate and wirebonding interconnections, is a valid option, because it provides a sufficient thermal conductivity and is a cost effective solution.

8) As a general design consideration, gate attacks should be implemented with Kelvin connections in order to avoid feedback effects between control and power signals. Their tracks (i.e., gate and source) should be placed as close as possible, improving mutual coupling effects and avoiding EMI problems. It could also be suitable that each parallel transistor could have its own gate-source connection. This connection should be as short as possible, in order to reduce the equivalent parasitic impedance, and equal to other transistor connections in order to avoid delay problems that produce current imbalances. Finally, it is important to remark that symmetry design should be also conducted, as it helps to balance the control tracks.

9) Application requirements impose device parallelization in a significant number. Thus, the power semiconductor should be as similar as possible in order to avoid ON/OFF delays issues. Thus, it is convenient to use devices with the same bare code within a module.

10) Regarding the power layout, the number of elements implemented over the substrate should be also minimized in order to obtain more space to balance the electrical connections. Another important aspect when designing the layout is the position and orientation of the dies, as it helps to cancel electromagnetic fields between control and power loops. The equivalent parasitic inductance of the power loops must be reduced by controlling the dimensions of the tracks. The concept of symmetric design (achieving a unit, the cell or split, where coupling effect reduce the parasitic inductances and current imbalances) could be also convenient, resulting in a scalable power layout.

11) According to the literature, terminals can introduce up to 50 % of the whole parasitic inductance of the power module. For this reason, this drawback must be mitigated minimizing their number, controlling their dimensions (being the connectors as width and short as possible), and dividing the current in an even number of pads for balancing.

Following such design criteria, the performance of the automotive modules would be enhanced, improving the overall features of the propulsion system and, consequently, of the vehicle. As a general conclusion, it can be stated that next generation WBG based power systems will have a relevant role in the development of future HEV/EVs.

6. Acknowledgements

This work has been supported by the Department of Education, Linguistic Policy and Culture of the Basque Government within the fund for research groups of the Basque university system IT978-16, and by the Government of the Basque Country within the research program ELKARTEK as the project ENSOL (KK-2018/00040) and the Generalitat de Catalunya under AGAUR Grant 2017-SGR-1384. As well as, the program to support the education of researches of the Basque Country PRE_2017_2_0008.

References

[1] Guía del vehículo eléctrico, Tech. rep., Consejería de Economía y Hacienda, organización Dirección General de Indutria, Energía y Minas (2015).

[2] J. Y. Yong, V. K. Ramachandaramurthy, K. M. Tan, N. Mithulananthan, A review on the state-of-the-art technologies of electric vehicle, its impacts and prospects, Renewable and Sustainable Energy Reviews 49 (2015) 365 – 385 (2015).

[3] B. K. Bose, Energy, Environment, and Advances in Power Electronics, IEEE Transactions on Power Electronics 15 (4) (2000) 688–701 (2000).

[4] A. Kawahashi, A New-generation hybrid electric vehicle and its supporting power semiconductor devices, in: Proc. of the International Symposium on Power Semiconductor Devices & ICs, 2004, pp. 23–29 (2004).

[5] B. K. Bose, Golbal Warming: Emergy, Environmental Pollution, and the Impact of Power Electronics, IEEE Industrial Electronics Magazine (2010) 6–17 (2010).

[6] P. M. Menghal, A. Jaya, Real time control of electrical machine drives: A review, in: Proc. of the International Conference on Power, Control and Embedded Systems, 2010, pp. 1–6 (2010).

[7] R. Bojoi, M. Lazzari, F. Profumo, A. Tenconi, Digital field oriented control for dual three-phase induction motor drives, in: Proc. of the Conference Record of the IEEE Industri Aplications Conference (IAS), 2002, pp. 818–825 (2002).

[8] Technology Roadmap, Electric and plug-in hybrid electric vehicles, Tech. rep., International Energy Agency (IEA) (2011).

[9] Global EV Outlook 2016. Beyond one million electric cars, Tech. rep., International Energy Agency (IEA) (2016).

[10] V. Katic, B. Dumnic, Z. Corba, D. Milievi, Electrification of The Vehicle Propulsion System An Overview, Facta Universitatis Series:Electronics and Energetics 27 (2014) 299–316 (2014).

[11] Electric Vehicle World Sales Database: Global EV Sales for 2018 Final Results. [link].
URL http://www.ev-volumes.com/country/total-world-plug-in-vehicle-volumes/

[12] A technical summary of Euro 6/VI vehicle emission standards, Tech. rep., The International Council on Clean Transportation (2016).

[13] Global High-Performance Electric Vehicle Market 2017-2021, Tech. rep., Technavio (2017).

[14] Horizon 2020, The EU framework programme for research and innovation. [link].
URL https://ec.europa.eu/programmes/horizon2020

[15] European Commission, Horizon 2020 Work Programme 2016-2017: Smart, green and integrated transport, Tech. rep., European Commission.

[16] United States Council for Automotive Rresearch LLC. [link].
URL http://www.uscar.org/guest/index.php

[17] Energy Efficiency & Renewable Energy, Multi-Year Program Plan 2011-2015: Vehicle Technologies Program, Tech. rep., Office of Energy Efficiency & Renewable Energy (2010).

[18] EV Everywhere grand challenge blueprint, Tech. rep., U.S. Department of Energy (2013).

[19] U.S Department of Energy, Overview of the DOE VTO Electric Drive Technologies R&D Program, Tech. rep., U.S Department of Energy: Energy Efficiency and renewable energy.

[20] United nations economical and social commission for Asia and the Pacific. [link].
URL http://www.unescap.org/

[21] A. Emadi, Y. J. Lee, K. Rajashekara, Power Electronics and Motor Drives in Electric, Hybrid Electric, and plug-In Hybrid Electric Vehicles, IEEE Transactions on Industrial Electronics 55 (6) (2008) 2237–2245 (2008).

[22] S. Waye, High temperature air-cooled power electronics thermal design, Tech. rep., National Renewable Energy Laboratory (2016).

[23] I. Aranzabal, I. Martinez de Alegria, J. I. Garate, J. Andreu, N. Delmonte, Two-phase liquid cooling for electric vehicle IGBT power module thermal management, in: Proc. of the International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), 2017, pp. 495–500 (2017).

[24] M. Schneider-Ramelow, T. Baumann, E. Hoene, Design and assembly of power semiconductors with double-sided water cooling, in: Proc. of the International Conference on Integrated Power Electronics Systems, 2008, pp. 1–7 (2008).

[25] C. Neeb, J. Teichrib, R. De Donker, L. Boettcher, A. Ostmann, A 50 kW IGBT power module for automotive applications with extremely low dc-link inductance, in: Proc. of the European Power Electronics and Applications Conference (EPE-ECCE), 2014, pp. 1–10 (2014).

[26] H. Wen, W. Xiao, X. Wen, P. Armstrong, Analysis and evaluation of dc-link capacitors for high powerdensity electric vehicle drive systems, IEEE Transactions on Vehicular Technology 61 (7) (2012) 2950–2964 (2012).

[27] A. Stefanskyi, L. Starzak, A. Napieralski, Silicon carbide power electronics for electric vehicles, in: Proc. of the Ecological Vehicles and Renewable Energies (EVER), 2015, pp. 1–9 (2015).

[28] X. She, A. Q. Huang, . Luca, B. Ozpineci, Review of Silicon Carbide Power Devices and Their Applications, IEEE Transactions on Industrial Electronics 64 (10) (2017) 8193–8205 (2017).

[29] J. Rabkowski, D. Peftitsis, H. P. Nee, Silicon Carbide Power Transistors: A New Era in Power Electronics Is Initiated, IEEE Industrial Electronics Magazine 6 (2) (2012) 17 – 26 (2012).

[30] J. Millán, P. Godignon, X. Perpina, A. Perez-Tomas, J. Rebollo, A Survey of Wide Bandgap Power Semiconductor Devices, IEEE Transactions on Power Electronics 29 (5) (2014) 2155–2163 (2014).

[31] T. Stockmeier, From Packaging to Un-Packagin - Trends in Power Semiconductor Modules, in: Proc. of the International Symposium on Power Semiconductor Devices & ICs, 2008, pp. 12–19 (2008).

[32] S. E. Schulz, Exploring the High-Power Inverter: reviewing critical design elements for electric vehicle applications, IEEE Electrification Magazine (2017) 2325–5987 (2017).

[33] Y. Wang, X. Dai, G. Liu, D. Li, S. Jones, An Overview of Advanced Power Semiconductor Packaging for Automotive System, in: Proc. of the Conference on Integrated Power Electronics Systems (CIPS), 2016, pp. 1–6 (2016).

[34] F. Barrero, J. Duran, Recent Advances in the Design, Modeling, and Control of Multiphase Machines - Part I, IEEE Transactions on Industrial Electronics 63 (1) (2016) 449–458 (2016).

[35] F. Barrero, J. Duran, Recent Advances in the Design, Modeling, and Control of Multiphase Machines - Part II, IEEE Transactions on Industrial Electronics 63 (1) (2016) 459–468 (2016).

[36] P. Zheng, Y. Sui, Z. Fu, P. Tang, F. Wu, P. Wang, Investigation of a Five-Phase 20-Slot/18-Pole PMSM for Electric Vehicles, in: Proc. of the International Conference on Electrical Machines and Systems (ICEMS), 2014, pp. 1168–1172 (2014).

[37] I. Subotic, N. Bodo, E. Levi, M. Jones, V. Levi, Isolated Chargers for EVs incorporating six-phase machines, IEEE Transactions on Industrial Electronics 63 (1) (2016) 653–663 (2016).

[38] C. Jung, Power Up with 800-V Systems, IEEE Electrification Magazine (2017) 53–58 (2017).

[39] H. M. Fischer, Voltage Casses for Electric Mobility, Tech. rep., ZVEI - German Electrical and Electronic Manufacturers Association (2013).

[40] W. Junping, G. Jingang, D. Lei, An adaptive Kalman filtering based State of Charge combined estimator for electric vehicle battery pack, Energy Conversion and Management 50 (2009) 3182–3186 (2009).

[41] M. Kerler, P. Burda, M. Baumann, M. Lienkamp, A concept of a high-energy, low-voltage EV battery pack, in: Proc. of the IEEE International Electric Vehicle Conference (IEVC), 2014 (2014).

[42] N. Sridhar, Driving the future of HEV/EV with high-voltage solutions, Tech. rep., Texas Instruments, Automotive and Isolated Driver Solutions (2017).

[43] Z. Q. Zhu, D. Howe, Electrical Machines and Drives for Electric, Hybrid and Fuel Cell Vehicles, Proceedings of the IEEE 95 (4) (2007) 746–765 (2007).

[44] S. Y. Jung, J. Hong, K. Nam, Current Minimizing Torque Control of the IPMSM Using Ferrari's Method, IEEE Transactions on Power Electronics 28 (12) (2013) 5603–5617 (2013).

[45] S. Morimoto, Y. Takeda, T. Hirasa, K. Taniguchi, Expansion of Operating Limits for Permanent Magnet Morot by Current Vector Control Considering Inverter Capacity, IEEE Transactions on Industry Applications 26 (5) (1990) 866–871 (1990).

[46] S. Morimoto, S. Ooi, Y. Inoue, M. Sanada, Experimental Evaluation of a Rare-Earth-Free PMASynRM With Ferrite Magnets for Automotive Applications, IEEE Transactions on Industrial Electronics 61 (10) (2014) 5749–5756 (2014).

[47] E. Trancho, E. Ibarra, A. Arias, I. Kortabarria, J. Jurgens, L. Marengo, A. Fricasse, J. V. Gag-

ger, PM-Assisted Synchronous Reluctance Machine Flux Weakening Control for EV and HEV Applications, IEEE Transactions on Industrial Electronics 65 (4) (2018) 2986–2995 (2018).
[48] I. Boldea, L. N. Tutelea, L. Parsa, D. Dorrell, Automotive Electric Propulsion Systems with Reduced or No Permanent Magnet: An Overview, IEEE Transactions on Industrial Electronics 61 (10) (2014) 5696–5711 (2014).
[49] Q. K. Nguyen, M. Petrich, J. Roth-Stielow, Implementation of the MTPA and MTPV control with online parameter identification for a high speed IPMSM used as traction drive, in: Proc. of the International Power Electronics Conference, 2014, pp. 318–323 (2014).
[50] B. H. Nguyen, H. V. Do, C. Minh, High Performance Current Control of IPMSM for Electric Vehicles Drives Using Disturbance Observer, in: Proc. of the Vehicle Power Propulsion Conference (VPPC), 2015, pp. 1–5 (2015).
[51] R. Bojoi, A. Cavagnino, A. Tenconi, A. Tessarolo, S. Vaschetto, Multiphase Electrical Machines and Drives in the Transportation Electrification, in: Proc. of the Research and Technologies for Society and Industry Leveraging a better tomorrow (RTSI), 2015, pp. 1–8 (2015).
[52] T. Finken, M. Hombitzer, K. Hameyer, Study and Comparison of several Permanent-Magnet excited Rotor Types regarding their Applicability in Electric Vehicles, in: Proc. of the Electrical Power Train Conference (Emobility), 2010 (2010).
[53] E. Trancho, E. Ibarra, A. Arias, C. Salazar, I. López, A. Díaz de Guereñu, A. Peña, IPMSM Torque Control Strategies based on LUTs and VCT feedback for Robust Control under Machine Parameter Variations, in: Proc. of the IEEE Industrial Electronics Conference (IECON), 2016, pp. 2833–2838 (2016).
[54] Y. Inoue, S. Morimoto, M. Sanada, Control Scheme for Wide-Speed-Range Operation of Synchronous Reluctance Motor in M-T Frame Synchronized with Stator Flux Linkage, IEEE Journal of Industry Applications 2 (2) (2013) 98–105 (2013).
[55] S. Ooi, S. Morimoto, M. Sanada, Y. Inoue, Performance Evaluation of a high power density PMASynRM with ferrite magnets, IEEE Transactions on Industry Applications 49 (3) (2013) 1308–1315 (2013).
[56] A. M. Bazi, Electric Machines and Energy Storage Technologies in EVs and HEVs for Over a Century, in: Proc. of the International Electric Machines and Drives Conference, 2013, pp. 212–219 (2013).
[57] J. Reimers, L. Dorn-Bomba, C. Mak, A. Emadi, Automotive traction inverters: current status and future trends, IEEE Transactions on Vehicular Technology 68 (4) (2019) 3337–3350 (2019).
[58] Z. Liang, Status and trend of automotive power packaging, in: Proc. of the International Symposium on Power Semiconductor Devices and ICs, 2012, pp. 325–331 (2012).
[59] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, Application Manual Power Semiconductors, SEMIKRON International GmbH, 2nd Edition (2015).
[60] A. Uhlemann, E. Hymon, Directly cooled HybridPACK power modules with ribbon bonded cooling structures, in: Proc. of PCIM Europe, 2018, pp. 582–587 (2018).
[61] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M. A. M. Prats, The age of multilevel converters arrives, IEEE Industrial Electronics Magazine 2 (2) (2008) 28–39 (2008).
[62] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives, IEEE Transactions on Industrial Electronics 54 (6) (2007) 2930–2945 (2007).
[63] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, J. I. Leon, Recent Advances and Industrial Applications of Multilevel Converters, IEEE Transactions on Industrial Electronics 57 (8) (2010) 2553–2580 (2010).
[64] A. Nabae, I. Takahashi, H. Akagi, A New Neutral-Point-Clamped PWM Inverter, IEEE Transactions on Industry Applications IA-17 (5) (1981) 518–523 (1981).
[65] T. A. Meynard, H. Foch, Multi-level conversion: high voltage choppers and voltage-source inverters, in: Proc. of the Power Electronics Specialists Conference (PESC), Vol. 1, 1992, pp. 397–403 (1992).
[66] M. Marchesoni, M. Mazzucchelli, S. Tenconi, A nonconventional power converter for plasma stabilization, IEEE Transactions on Power Electronics 5 (2) (1990) 212–219 (1990).
[67] J. Rodriguez, J. S. Lai, F. Z. Peng, Multilevel inverters: a survey of topologies, controls, and applications, IEEE Transactions on Industrial Electronics 49 (4) (2002) 724–738 (2002).
[68] S. C. Recio, Mejora en la fiabilidad y en el control de tensión de punto neutro en convertidores de fijacióon por diodos de tres niveles, Ph.D. thesis, Escuela Técnica Superior de Ingeniería de Bilbao (2008).
[69] J. Rodríguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. M. Prats, M. A. Pérez,

Multilevel Converters: An Enabling Technology for High-Power Applications, Proceedings of the IEEE 97 (11) (2009) 1786–1817 (2009).

[70] I. López, S. Ceballos, J. Andreu, I. Martnez de Alegra, I. Kortabarria, Review of modulation algorithms for neutral-point-clamped multilevel converter, in: Proc. of the International Conference on Renewable Energies and Power Quality (ICREPQ), 2013, pp. 507–512 (2013).

[71] J. Pou, J. Zaragoza, P. Rodríguez, S. Ceballos, V. Sala, R. Burgos, D. Boroyevich, Fast-proccesing modulation strategy for the neutral-point-clamped converter with total elimination of the low-frequency voltage oscillations in the neutral point, IEEE Transactions on Industrial Electronics 54 (4) (2017) 2288–2299 (2017).

[72] J. Pou, D. Boroyevich, R. Pindado, Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter, IEEE Transactions on Power Electronics 20 (1) (2005) 123–131 (2005).

[73] J. Pou, R. Pindado, D. Boroyevich, P. Rodriguez, Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter, IEEE Transactions on Industrial Electronics 52 (6) (2005) 1582–1588 (2005).

[74] I. Subotic, N. Bodo, E. Levi, M. Jones, On-board integrated battery charger for EVs using an asymmetrical nine-phase machine, IEEE Transactions on Industrial Electronics 62 (5) (2015) 3285–3295 (2015).

[75] A. S. Abdel-Khalik, M. I. Masoud, S. Ahmed, A. M. Massoud, Effect of Current Harmonic Injection on Constant Rotor Volume Multiphase Induction Machine Stators: A Comparative Study, IEEE Transactions on Industry Applications 48 (6) (2012) 2002–2013 (2012).

[76] H. Guzman, I. Gonzalez, F. Barrero, M. Durán, Induction Motors - Aplications, Control and Fault Diagnostics. Chapter 12: Open-phase fault operation on multiphase induction motor drives, Intech, 2015 (2015).

[77] L. De Lillo, L. Emrpingham, P. Wheeler, S. Khwan-On, C. Gerada, N. Othman, X. Huang, Multiphase Power Converter Drive for Fault-Tolerant Machine Development in Aerospace Applications, IEEE Transactions on Industrial Electronics 57 (2) (2010) 575–583 (2010).

[78] B. Mirafzal, Survey of Fault-Tolerance Techniques for Three-Phase Voltage Source Inverters, IEEE Transactions on Industrial Electronics 61 (10) (2014) 5192–5202 (2014).

[79] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, H. S. Krishanamoorthy, Survey on Fault-Tolerant Techniques for Power Electronic Converters, IEEE Transactions on Power Electronics 29 (12) (2014) 6319–6331 (2014).

[80] C. Cecati, O. Di Tommaso, F. Genduso, R. Miceli, G. R. Galluzzo, Comprehensive Modeling and Experimental Testing of Fault Detection and Management of a Nonredundant Fault-Tolerant VSI, IEEE Transactions on Industrial Electronics 62 (6) (2015) 3945–3954 (2015).

[81] G. Fabri, E. Della Loggia, M. Tursini, Fault-Tolerant Design of Motor-Drives for High Reliability Applications, in: Proc. of the Research and Technologies for Society and Industry Leveraging a better tomorrow (RTSI), 2015, pp. 1–7 (2015).

[82] M. Villani, M. Tursini, G. Fabri, L. Castellini, High Reliability Permanent Magnet Brushless Motor Drive for Aircraft Application, IEEE Transactions on Industrial Electronics 59 (5) (2012) 2073–2081 (2012).

[83] J. Karttunen, S. Kallio, P. Peltoniemi, P. Silventoinen, O. Pyrhonen, Decoupled Vector Control Scheme for Dual Three-Phase Permanent Magnet Synchronous Machines, IEEE Transactions on Industrial Electronics 61 (5) (2013) 2185–2196 (2013).

[84] S. Kallio, M. Andriollo, A. Tortella, J. Karttunen, Decoupled dq Model of Double-Star Interior-Permanent-Magnet Synchronous Machines, IEEE Transactions on Industrial Electronics 60 (6) (2013) 2486–2494 (2013).

[85] D. Gerada, Z. Xu, M. Galea, C. Gerada, S. Pickerig, High Torque-Density In-Wheel Electrical Machine for an Electric Bus, in: Proc. of the Vehicle Power and Propulsion Conference (VPPC), 2016, pp. 1–6 (2016).

[86] O. Fall, N. K. Nguyen, J. F. Charpentier, P. Letellier, Variable speed control of a 5-phase permanent magnet synchronous generator including voltage and current limits in healthy and open-circuited modes, Electric Power Systems Research 140 (2016) 507–516 (2016).

[87] L. Parsa, H. A. Toliyat, Five-phase permanent-magnet motor drives, IEEE Transactions on Industry Application 4 (1) (2005) 30–37 (2005).

[88] A. Mohammadpour, L. Parsa, Global Fault-Tolerant Control Technique for Multiphase Permanent-Magnet Machines, IEEE Transactions on Industry Applications 51 (1) (2015) 178–186 (2015).

[89] Y. Sui, P. Zheng, Y. Fan, Zhao, Research on the vector control strategy of five-phase permanent-magnet synchronous machine based on third-harmonic current injection, in: Proc. of the Interna-

tional Electric Machines and Drives Conference (IEMDC), 2017, pp. 1–8 (2017).
[90] C. S. Lim, E. Levi, M. Jones, N. A. Rahim, W. P. Hew, FCS-MPC-Based Current Control of a Five-Phase Induction Motor and its Comparison with PI-PWM Control, IEEE Transactions on Industrial Electronics 61 (1) (2014) 149–163 (2014).
[91] G. Liu, Z. Lin, W. Zhao, Q. Chen, G. Xu, Third Harmonic Current Injection in fault-tolerant five-phase permanent-magnet motor drive, IEEE Transactions on Power Electronics 33 (8) (2018) 6970–6979 (2018).
[92] F. Baudart, B. Dehez, F. Labrique, E. Matagne, Optimal sinusoidal currents for avoiding torque pulsations after the loss of one phase in polyphase SMPM synchronous motor, in: Proc. of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2010, pp. 13–18 (2010).
[93] I. Gonzalez-Prieto, M. J. Duran, N. Rios-Garcia, F. Barrero, C. Martin, Open-switch Fault Detection in Five-phase Induction Motor Drives using Model Predictive Control, IEEE Transactions on Industrial Electronics 65 (4) (2018) 3045–3055 (2018).
[94] L. Zheng, J. E. Fletcher, B. W. Williams, X. He, Dual-Plane Vector Control of a Five-Phase Induction Machine for an Improved Flux Pattern, IEEE Transactions on Industrial Electronics 55 (5) (2008) 1996–2005 (2008).
[95] A. A. Rockhill, T. A. Lipo, A Simplified Model of a Nine Phase Synchronous Machine Using Vector Space Decomposition, in: Proc. of the Power Electronics and Machines in Wind Applications (PEMWA), 2009, pp. 1–5 (2009).
[96] D. Casadei, M. Mengoni, G. Serra, A. Tani, L. Zarri, Optimal Fault-Tolerant Control Strategy for Multi-Phase Motor Drives Under an Open Circuit Phase Fault Condition, in: Proc. of the International Conference on Electrical Machines, 2008, pp. 1–6 (2008).
[97] M. Mengoni, L. Zarri, A. Tani, L. Parsa, G. Serra, D. Casadei, High-Torque-Density Control of Multiphase Induction Motor Drives Operating Over a Wide Speed Range, IEEE Transactions on Industrial Electronics 62 (2) (2015) 814–825 (2015).
[98] M. Cheng, F. Yu, K. T. Chau, W. Hua, Dynamic Performance Evaluation of a Nine-Phase Flux-Switching Permanent-Magnet Motor Drive With Model Predictive Control, IEEE Transactions on Industrial Electronics 63 (7) (2016) 4539–4549 (2016).
[99] M. M. Wogari, O. Ojo, Nine-Phase Interior Permanent Magnet Motor for Electric Vehicle Drive, in: Proc. of the Power and Energy Society General Meeting, 2011, pp. 1–8 (2011).
[100] L. Jing, S. Norrga, H. Zhang, O. Wallmark, Evaluation of a Multiphase Drive System in EV and HEV Applications, in: Proc. of the International Electric Machines & Drives Conference (IEMDC), 2015, pp. 941–945 (2015).
[101] A. S. Abdel-Khalik, M. I. Masoud, B. W. Williams, Improved Flux Pattern With Third Harmonic Injection for Multiphase Induction Machines, IEEE Transactions on Power Electronics 27 (3) (2012) 1563–1578 (2012).
[102] Y. Hu, Z. Zhu, K. Liu, Current Control for Dual Three-Phase Permanent Magnet Synchronous Motors Accounting for Current Unbalance and Harmonics, IEEE Journal of Emerging and Selected Topics in Power Electronics 2 (2) (2014) 272–284 (2014).
[103] H. S. Che, E. Levi, M. Jones, W. P. Hew, N. A. Rahim, Current Control Methods for an Asymmetrical Six-Phase Induction Motor Drive, IEEE Transactions on Power Electronics 29 (1) (2014) 407–417 (2014).
[104] V. Patel, J. Wang, D. Nugraha, R. Vuletic, J. Tousen, Enhanced Availability of Drivetrain Through Novel Multiphase Permanent-Magnet Machine Drive, IEEE Transactions on Industrial Electronics 63 (1) (2015) 469–480 (2015).
[105] L. Alberti, N. Bianchi, Experimental tests of dual three-phase induction motor under faulty operating condition, IEEE Transactions on Industrial Electronics 59 (5) (2012) 2014–2048 (2012).
[106] J. W. Bennett, G. J. Atkinson, B. C. Mecrow, D. J. Atkinson, Fault-Tolerant Design Considerations and Control Strategies for Aerospace Drives, IEEE Transactions on Industrial Electronics 59 (5) (2012) 2049–2058 (2012).
[107] S. Binqiang, Z. Jihong, J. Jinghua, Remedial Operations of Permanent Magnet Fault Tolerant Motor for Short-Circuit Fault, in: Proc. of the IFAC Symposium on Mechatronic Systems, 2013, pp. 643–649 (2013).
[108] P. Zhao, G. Yang, Torque density improvement of five-phase PMSM drive for electric vehicles applications, Journal of Power Electronics 11 (4) (2011) 401–407 (2011).
[109] D. Fodorean, Study of a High-Speed Motorization With Improved Performances Dedicated for an Electric Vehicle, IEEE Transactions on Magnetics 50 (2) (2014) 921–924 (2014).
[110] D. Fodorean, L. Idoumghar, M. Brevilliers, P. Minciunescu, C. Irima, Hybrid Differential Evolution

Algorithm employed for the Optimum Design of a High-Speed PMSM used for EV propulsion, IEEE Transactions on Industrial Electronics 64 (12) (2017) 9824–9833 (2017).
[111] E. Sulaiman, T. Kosaka, N. Matsui, High Power Density Design of 6-Slot8-Pole Hybrid Excitation Flux Switching Machine for Hybrid Electric Vehicles, IEEE Transactions on Magnetics 47 (10) (2011) 4453–4456 (2011).
[112] L. Sepulchre, M. Fadel, M. Pietrzak-David, Improvement of the Digital Control of a High Speed PMSM for Vehicle Application, in: Proc. of the Ecological Vehicles and Renewable Energies (EVER), 2016 (2016).
[113] A. Altomare, A. Guagnano, F. Cupertino, D. Naso, Discrete-Time Control of High-Speed Salient Machines, IEEE Transactions on Industry Applications 52 (1) (2016) 293–301 (2016).
[114] M. Novak, Z. Novak, Stability Issues of High Speed PMSM Feedback Control Systems, in: Proc. of the European Conference on Power Electronics and Applications, 2013, pp. 1–9 (2013).
[115] A. Guagnano, F. Rizzello, G.and Cupertino, D. Naso, Robust Control of High-Speed Synchronous Reluctance Machines, IEEE Transactions on Industry Applications 52 (5) (2016) 3990–4000 (2016).
[116] B. P. Jeppesen, A. Crosland, Controlling high-speed motors with an FPGA, Tech. rep., Altera (2017).
[117] A. Bindra, Wide-Bandgap Power Devices: Adoption Gathers Momentum,, IEEE Power Electronics Magazine 5 (1) (2018) 22–27 (2018).
[118] T. M. Jahns, H. Dai, The past, present, and future of power electronics integration technology in motor drives,, CPSS Transactions on Power Electronics and Applications 2 (3) (2017) 197–216 (2017).
[119] A. Morya, M. Moosavi, M. C. Gardner, H. A. Toliyat, Applications of Wide Bandgap (WBG) devices in AC electric drives: A technology status review,, in: Proc. of the International Electric Machines and Drives Conference (IEMDC), 2017, pp. 1–8 (2017).
[120] A. A. Pesaran, Battery Thermal Management in EVs and HEVs : Issues and Solutions, 2001 (2001).
[121] W. Weixiong, W. Shuangfeng, W. Wei, C. Kai, H. Sihui, L. Yongxin, A critical review of battery thermal performance and liquid based battery thermal management, Energy Conversion and Management 182 (2019) 262 – 281 (2019).
[122] M. Shen, Q. Gao, A review on battery management system from the modeling efforts to its multiapplication and integration, International Journal of Energy Research (2019).
[123] P. Xiongbin, M. Chong, G. Akhil, B. Nengsheng, L. Xiangping, Thermal performance investigation of an air-cooled lithium-ion battery pack considering the inconsistency of battery cells, Applied Thermal Engineering 153 (2019) 596 – 603 (2019).
[124] S. Zhuangzhuang, Q. Hongzhong, L. Xintian, O. Chenzhi, W. Yansong, Structural optimization of lithium-ion battery for improving thermal performance based on a liquid cooling system, International Journal of Heat and Mass Transfer 130 (2019) 33 – 41 (2019).
[125] J. Juergens, A. Fricasse, L. Marengo, M. De Gennaro, B. Ponick, Innovative design of an air cooled ferrite permanent magnet assisted synchronous reluctance machine for automotive traction application, in: Proc. of the International Conference on Electric Machines (ICEM), 2016, pp. 803–810 (2016).
[126] Y. Karnavas, I. Chasiotis, E. Peponakis, Cooling System Design and Thermal Analysis of an Electric Vehicles In-Wheel PMSM, in: Proc. of the International Conference on Electric Machines (ICEM), 2016, pp. 1439–1445 (2016).
[127] O. Burak, Oak ridge national laboratory annual progress report for the electric drive technologies program, Tech. rep., Oak Ridge National Laboratory, Electrical and Electronics Systems Research Division (2016).
[128] T. Hitachi, H. Gohara, F. Naganue, Direct Liguid Cooling IGBT Module for Automotive Applications, Fuji Electric Review 57 (2012) 55–59 (2012).
[129] J. Schulz-Harder, Review of highly integrated solutions for power electronic devices, in: Conference on Integrated power systems (CIPS), 2008, pp. 1–7 (2008).
[130] FreedomCAR Power Electronics and Electrical Machines, Electrical and electronics technical team roadmap, Tech. rep., FreedomCAR Power Electronics and Electrical Machines (2013).
[131] K. Li, J. Yan, H. Chen, Q. Wang, Water cooling based strategy for lithium ion battery pack dynamic cycling for thermal management system, Applied Thermal Engineering 132 (2018) 575–585 (2018).
[132] J. Marcinkowski, Dual-sided Cooling of Power Semiconductor Modules, in: International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), 2014, pp. 1–7 (2014).

[133] D. Faulkner, M. Khotan, R. Shekarriz, Practical design of a 1000 w/cm2 cooling system [high power electronics, in: Annual IEEE Semiconductor Thermal Measurement and Management Symposium, 2003, pp. 223–230 (2003).
[134] E. Laloya, O. Lucía, H. Sarnago, J. M. Burdío, Heat amangement in power converters: fro, state of the art to future ultrahigh efficiency systems, IEEE transactions on power electronics 31 (11) (2016) 7896–7908 (2016).
[135] Z. Liang, L. Li, HybridPACK2 - advanced cooling concept and package technology for Hybrid Electric Vehicles, in: IEEE Vehicle Power and Propulsion Conference, 2008, pp. 1–5 (2008).
[136] A. Uhlemann, Investigation on AlCu-clad base plates and a new by-pass cooler for pin fin power modules, in: Conference on Integrated Power Electronics Systems (CIPS), 2014, pp. 1–4 (2014).
[137] K. J. Kelly, T. Abraham, K. Bennion, D. Bharathan, S. Narumachi, M. O'keefe, Assesment of thermal control technologies for cooling electric vehicle power electronics, in: Proc. of the Electric Vehicle Symposium (EVS), 2007, pp. 1–6 (2007).
[138] M. O'keefe, K. Bennion, Comparison of hybrid electric vehicle power electronics cooling options, in: Proc. of the Vehicle power and propulsion conference, 2007, pp. 1–6 (2007).
[139] S. S. Kang, T. Aavid, Advanced cooling for power electronics, in: Proc. of the Conference on integrated power electronics systems (CIPS), 2012, pp. 1–8 (2012).
[140] R. H. Staunton, T. A. Burress, L. D. Marlino, Evaluation of 2005 honda accord hybrid electric drive system, Tech. rep., Oak Ridge National Laboratory (2006).
[141] A. Peña, Final report summary - EUNICE (eco-design and validation of in-wheel concept for electric vehicles), Tech. rep. (2015).
[142] J. Hsu, R. Staunton, M. Starke, Barriers to the Application of High-Temperature Coolants in Hybrid Electric Vehicles, Tech. rep., Oak Ridge National Laboratory Technical Report ORNL/TM-2006/514 (2006).
[143] J. Millán, P. Godignon, Wide Band Gap power semiconductor devices, in: Proc. of the Conference on Electron Devices, 2013, pp. 293–296 (2013).
[144] K. S. Boutros, R. Chu, B. Hughes, GaN power electronics for automotive application, in: Proc. of the IEEE Energytech, 2012, pp. 1–4 (2012).
[145] L. Zhai, L. Lin, X. Zhang, C. Song, The effect of distributed parameters on conducted emi from dc-fed motor drive systems in electric vehicles, Energies 10 (1) (2017).
[146] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, H. A. Toliyat, Wide Bandgap Devices in AC Electric Drives: Opportunities and Challenges, IEEE Transactions on Transportation Electrification 5 (1) (2019) 3–20 (2019).
[147] X. Yuan, Application of silicon carbide (SiC) power devices: Opportunities, challenges and potential solutions, in: Annual Conference of the IEEE Industrial Electronics Society, 2017, pp. 893–900 (2017).
[148] C. R. Paul, Introduction to Electromagnetic Compatibility, John Wiley & Sons, Inc., 2006 (2006).
[149] United Nations, Regulation 10: Vehicle Radiated Emissions & Immunity Testing (Annexes 4, 5 and 6), Tech. rep., UNECE (2014).
[150] R. Carlton, IEC 61967 Integrated circuits - Measurement of electromagnetic emissions, Tech. rep., EDN Network (2003).
[151] Electric vehicle conductive charging system, Tech. rep., IEC (2001).
[152] D. Hamza, M. Pahlevaninezhad, P. K. Jain, Implementation of a Novel Digital Active EMI Technique in a DSP-Based DCDC Digital Controller Used in Electric Vehicle (EV), IEEE Transactions on Power Electronics 28 (7) (2013) 3126–3137 (2013).
[153] H. Huribayashi, T. Kajita, Area-Efficient Decimation Filter with 50/60Hz Power-Line Noise Suppression for $\Delta\Sigma$ A/D Converters, SICE Journal of Control, Measurement, and System Integration 10 (3) (2017) 165–169 (2017).
[154] J. Jun, C. Rhee, S. Kim, A 386-uW, 15.2-bit Programmable-Gain Embedded Delta-Sigma ADC for Sensor Applications, in: International Symposium on Low Power Electronics and Design, 2016, pp. 278–283 (2016).
[155] J. Jun, C. Rhee, M. Kim, J. Kang, S. Kim, A 21.8b sub-100Hz 1/f corner 2.4V-offset programmable-gain read-out IC for bridge measurement systems, IEEE International Solid - State Circuits Conference (2018) 330–332 (2018).
[156] X. Gong, J. A. Ferreira, Comparison and reduction of conducted emi in sic jfet and si igbt-based motor drives, IEEE Transactions on Power Electronics 29 (4) (2014) 1757–1767 (2014).
[157] F. Maislinger, H. Ertl, G. Stojcic, C. Lagler, F. Holzner, Design of a 100khz wide bandgap inverter for motor applications with active damped sine wave filter, The Journal of Engineering (2019).
[158] A. Bhargava, D. Pommerenke, K. W. Kam, F. Centola, C. W. Lam, DC-DC Buck Converter EMI

Reduction Using PCB Layout Modification, IEEE Transactions on Electromagnetic Compatibility 53 (3) (2011) 806–813 (2011).

[159] K. Kam, D. Pommerenke, F. Centola, C. Lam, R. Steinfeld, EMC guideline for synchronous buck converter design, in: IEEE International Symposium on Electromagnetic Compatibility, 2009, pp. 47–52 (2009).

[160] T. M. North, J. Muccioli, Automotive EMC testing The challenges of testing battery systems for electric and hybrid vehicles, IEEE Electromagnetic Compatibility Magazine 1 (1) (2012) 97–100 (2012).

[161] B. Zhang, S. Wang, An Overview of Wide Bandgap Power Semiconductor Device Packaging Techniques for EMI Reduction, in: IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity, 2018, pp. 297–301 (2018).

[162] A. Dutta, S. S. Ang, Electromagnetic Interference Simulations for Wide-Bandgap Power Electronic Modules, IEEE Journal of Emerging and Selected Topics in Power Electronics 4 (3) (2016) 757–766 (2016).

[163] Z. Dong, X. Wu, K. Sheng, Suppressing Methods of Parasitic Capacitance Caused Interference in a SiC MOSFET Integrated Power Module, IEEE Journal of Emerging and Selected Topics in Power Electronics 7 (2) (2019) 745–752 (2019).

[164] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, M. S. Mazzola, Methodology for Characterization of Common-Mode Conducted Electromagnetic Emissions in Wide-Bandgap Converters for Ungrounded Shipboard Applications, IEEE Journal of Emerging and Selected Topics in Power Electronics 6 (1) (2018) 300–314 (2018).

[165] I. Echeverria, F. Arteche, M. Iglesias, A. Pradas, J. Piedrafita, F. J. Arcega, Common Mode Noise Propagation and Effects in a Four-Wheel Drive Electric Vehicle, IEEE Transactions on Electromagnetic Compatibility 60 (1) (2018) 132–139 (2018).

[166] W. Qing-yu, Z. Xiao-dong, W. Lei, Z. Xi, EMC Design for HEV Drive System, in: International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, 2007, pp. 1361–1364 (2007).

[167] I. Hoda, J. Li, H. Funato, EMC Design and Development Methodology for Traction Power Inverters of Electric Vehicles, in: International Power Electronics Conference, 2018, pp. 2073–2077 (2018).

[168] L. Zhai, C. Song, Conducted EMI from motor drive system of electric vehicle under load operation, in: International Symposium on Electromagnetic Compatibility (APEMC), 2017, pp. 181–183 (2017).

[169] Y. Shi, Y. Zhang, L. Wang, H. Li, Reduction of emi noise due to nonideal interleaving in a 100 kw sic pv converter, IEEE Transactions on Power Electronics 34 (1) (2019) 13–19 (2019).

[170] L. Wang, Y. Shi, H. Li, Anti-EMI Noise Digital Filter Design for a 60-kW Five-Level SiC Inverter Without Fiber Isolation, IEEE Transactions on Power Electronics 3 (1) (2018) 13–17 (2018).

[171] N. Oswald, P. Anthony, N. McNeill, B. H. Stark, An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations, IEEE Transactions on Power Electronics 29 (5) (2014) 2393–2407 (2014).

[172] D. Stepins, An Improved Control Technique of Switching-Frequency-Modulated Power Factor Correctors for Low THD and High Power Factor, IEEE Transactions on Power Electronics 31 (7) (2016) 5201–5214 (2016).

[173] F. Pareschi, R. Rovatti, G. Setti, EMI Reduction via Spread Spectrum in DC/DC Converters: State of the Art, Optimization, and Tradeoffs, IEEE Access 3 (2015) 2857–2874 (2015).

[174] S. Kapat, Reconfigurable Periodic Bifrequency DPWM With Custom Harmonic Reduction in DCDC Converters, IEEE Transactions on Power Electronics 31 (4) (2016) 3380–3388 (2016).

[175] J. Mon, J. Gago, D. Gonzalez, J. Balcells, R. Fernandez, I. Gil, P. Bogonez, EMI reduction by means of switching frequency modulation with variable delay in power supplies, International Journal of Electronics 99 (1) (2012) 103–112 (2012).

[176] L. Zhai, X. Zhang, N. Bondarenko, D. Loken, T. P. Van Doren, D. G. Beetner, Mitigation Emission Strategy Based on Resonances from a Power Inverter System in Electric Vehicles, Energies 9 (6) (2016).

[177] V. Sangwan, D. Kapoor, C. M. Tan, C. H. Lin, H. Chiu, High-Frequency Electromagnetic Simulation and Optimization for GaN-HEMT Power Amplifier IC, IEEE Transactions on Electromagnetic Compatibility 61 (2) (2019) 564–571 (2019).

[178] A. Frikha, M. Bensetti, L. Pichon, F. Lafon, F. Duval, N. Benjelloun, Magnetic shielding effectiveness of enclosures in near field at low frequency for automotive applications, IEEE Transactions on Electromagnetic Compatibility 57 (6) (2015) 1481–1490 (2015).

[179] Designing EMI/EMC SafeBattery Pack, Tech. rep., Texas Instruments (2016).

[180] D. Shin, S. Jeong, Y. Baek, C. Park, G. Park, J. Kim, A Balanced Feedforward Current-Sense Current-Compensation Active EMI Filter for Common-Mode Noise Reduction, IEEE Transactions on Electromagnetic Compatibility (2019) 1–12 (2019).

[181] M. Troscher, T. Haschberger, Emission Reduction by Optimizing Current Return Paths in Electric Vehicles, in: Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI PI), 2018, pp. 460–460 (2018).

[182] T. Weber, Emc filters in high voltage traction drive systems, in: International Symposium on Electromagnetic Compatibility - EMC Europe, 2008, pp. 1–6 (2008).

[183] Y. Li, Z. Li, S. Zhu, M. Jiao, C. Wu, Junction temperature post-fault analysis of single IGBT short-circuit for double-side cooling inverter used for electric vehicle, in: Proc. of the International Electric Machines and Drives Conference (IEMDC), 2017, pp. 1–6 (2017).

[184] A. Mauder, T. Laska, L. Lorenz, Dynamic behaviour and ruggedness of advanced fast switching IGBTs and diodes, in: Proc. of the Conference Record of the Industry Applications, 2003, pp. 995–999 (2003).

[185] M. Mori, K. Oyama, T. Arai, J. Sakano, Y. Nishimura, K. Masuda, K. Saito, Y. Uchino, H. Homma, A Planar-Gate High-Conductivity IGBT (HiGT) With Hole-Barrier Layer, IEEE Transactions on Electron Devices 54 (6) (2007) 1515–1520 (2007).

[186] K. Xiaosong, A. Caiafa, E. Santi, J. L. Hudgins, P. R. Palmer, Characterization and modeling of high-voltage field-stop IGBTs, IEEE Transactions on Industry Applications 39 (4) (2003) 922–928 (2003).

[187] H. Ruthing, F. Umbach, O. Hellmund, P. Kanschat, G. Schmidt, 600V-IGBT3: trench field stop technology in 70 um ultra thin wafer technology, IEE Circuits, Devices and Systems 151 (3) (2004) 211–214 (2004).

[188] P. Godignon, V. Soler, M. Cabello, J. Montserrat, J. Rebollo, L. Knoll, E. Bianda, A. Mihaila, New trends in high voltage MOSFET based on wide band gap materials, in: Proc. of the International Semiconductor Conference (CAS), 2017, pp. 3–10 (2017).

[189] P. Godignon, G. Rius, M. Cabello, V. Soler, J. Montserrat, Gallium Oxide as the next semiconductor for power devices, in: Proc. of the Seminario Anual de Automtica, Electrnica Industrial e Instrumentacin (SAAEI), 2018, pp. 1–6 (2018).

[190] S. Araujo, M. Kazanbas, M. Wendt, T. Kleeb, P. Zacharias, Prospects of GaN devices in automotive electrification, in: Proc. of the PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2014, pp. 1–8 (2014).

[191] J. Biela, M. Schweizer, S. Waffler, J. W. Kolar, SiC versus Si - Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors, IEEE Transactions on Industrial Electronics 58 (7) (2011) 2872–2882 (2011).

[192] J. C. Balda, A. Mantooth, Power-Semiconductor Devices and Components for New Power Converter Developments: A key enabler for ultrahigh efficiency power electronics, IEEE Power Electronics Magazine 3 (2) (2016) 53–56 (2016).

[193] K. Shenai, The Figure of Merit of a Semiconductor Power Electronics Switch, IEEE Transactions on Electron Devices 65 (10) (2018) 4216–4224 (2018).

[194] A. S. Abdelrahman, Z. Erdem, Y. Attia, M. Z. Youssef, Wide Bandgap Devices in Electric Vehicle Converters: A Performance Survey, Canadian Journal of Electrical and Computer Engineering 41 (1) (2018) 45–54 (2018).

[195] P. Friedrichs, J. Milln, T. Harder, N. Kaminski, A. Lindemann, L. Lorenz, L. Schindele, P. Ward, Next Generation Power Electronics based on Wide Bandgap Devices - Challenges and Opportunities for Europe (ECPE Position Paper), Tech. rep., ECPE (2016).

[196] P. Godignon, X. Jorda, M. Vellvehi, X. Perpina, V. Banu, D. Lopez, J. Barbero, P. Brosselard, S. Massetti, SiC Schottky Diodes for Harsh Environment Space Applications, IEEE Transactions on Industrial Electronics 58 (7) (2011) 2582–2590 (2011).

[197] F. Zare, D. Kumar, M. Lungeanu, A. Andreas, Electromagnetic interference issues of power, electronics systems with wide band gap, semiconductor devices, in: IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 5946–5951 (2015).

[198] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, D. Costinett, Understanding the limitations and impact factors of wide bandgap devices' high switching-speed capability in a voltage source converter, in: IEEE Workshop on Wide Bandgap Power Devices and Applications, 2014, pp. 7–12 (2014).

[199] D. Han, S. Li, Y. Wu, W. Choi, B. Sarlioglu, Comparative Analysis on Conducted CM EMI Emission of Motor Drives: WBG Versus Si Devices, IEEE Transactions on Industrial Electronics

64 (10) (2017) 8353–8363 (2017).
[200] H. Nie, Q. Diduck, B. Alvarez, A. P. Edwards, B. M. Kayes, M. Zhang, G. Ye, T. Prunty, D. Bour, I. C. Kizilyalli, 1.5-kV and 2.2-mΩ-cm^{2}Vertical GaN Transistors on Bulk-GaN Substrates, IEEE Electron Device Letters 35 (9) (2014) 939–941 (2014).
[201] H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P. R. Chalker, M. Charles, K. J. Chen, N. Chowdhury, R. Chu, C. D. Santi, M. M. D. Souza, S. Decoutere, L. D. Cioccio, B. Eckardt, T. Egawa, P. Fay, J. J. Freedsman, L. Guido, O. Hberlen, G. Haynes, T. Heckel, D. Hemakumara, P. Houston, J. Hu, M. Hua, Q. Huang, A. Huang, S. Jiang, H. Kawai, D. Kinzer, M. Kuball, A. Kumar, K. B. Lee, X. Li, D. Marcon, M. Mrz, R. McCarthy, G. Meneghesso, M. Meneghini, E. Morvan, A. Nakajima, E. M. S. Narayanan, S. Oliver, T. Palacios, D. Piedra, M. Plissonnier, R. Reddy, M. Sun, I. Thayne, A. Torres, N. Trivellin, V. Unni, M. J. Uren, M. V. Hove, D. J. Wallis, J. Wang, J. Xie, S. Yagi, S. Yang, C. Youtsey, R. Yu, E. Zanoni, S. Zeltner, Y. Zhang, The 2018 GaN power electronics roadmap, Journal of Physics D: Applied Physics 51 (16) (2018) 163001 (2018).
[202] T. Uesugi, T. Kachi, Which are the future GaN power devices for automotive applications, lateral structures or vertical strucutres?, in: Proc. of the C MANTECH Conference, 2011, pp. 307–310 (2011).
[203] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, G. Meneghesso, AlGaN/GaN-Based HEMTs Failure Physics and Reliability: Mechanisms Affecting Gate Edge and Schottky Junction, IEEE Transactions on Electron Devices 60 (10) (2013) 3119–3131 (2013).
[204] D. C. Sheridan, D. Y. Lee, A. Ritenour, V. Bondarenko, J. Yang, C. Coleman, Ultra-Low Loss 600V - 1200V GaN Power Transistors for High Efficiency Applications, in: Proc. of the PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2014, pp. 1–7 (2014).
[205] K. Shirabe, M. M. Swamy, K. Jun-Koo, M. Hisatsune, W. Yifeng, D. Kebort, J. Honea, Efficiency Comparison Between Si-IGBT-Based Drive and GaN-Based Drive, IEEE Transactions on Industry Applications 50 (1) (2014) 566–572 (2014).
[206] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, Gate Injection Transistor (GIT) 2014;A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation, IEEE Transactions on Electron Devices 54 (12) (2007) 3393–3399 (2007).
[207] M. Su, C. Chen, S. Rajan, Prospects for the application of GaN power devices in hybrid electric vehicle drive systems, Semiconductor Science and Technology 28 (7) (2013) 074012 (2013).
[208] A. Lidow, J. Strydom, M. D. Rooij, D. Reusch, GaN Transistors for Efficient Power Conversion, 2nd Edition, Wiley, 2014 (2014).
[209] H. S. Kim, S. W. Han, W. H. Jang, C. H. Cho, K. S. Seo, J. Oh, H. Y. Cha, Normally-Off GaN-on-Si MISFET Using PECVD SiON Gate Dielectric, IEEE Electron Device Letters 38 (8) (2017) 1090–1093 (2017).
[210] K. J. Chen, O. Hberlen, A. Lidow, C. l. Tsai, T. Ueda, Y. Uemoto, Y. Wu, GaN-on-Si Power Technology: Devices and Applications, IEEE Transactions on Electron Devices 64 (3) (2017) 779–795 (2017).
[211] H. Li, C. Yao, L. Fu, X. Zhang, J. Wang, Evaluations and applications of GaN HEMTs for power electronics, in: Proc. of the International Power Electronics and Motion Control Conference, 2016, pp. 563–569 (2016).
[212] N. Kaminski, O. Hilt, SiC and GaN devices - wide bandgap is not all the same, IET Circuits, Devices Systems 8 (3) (2014) 227–236 (2014).
[213] X. Jorda, X. Perpina, M. Vellvehi, D. Sanchez, A. Garcia, A. Avila, Analysis of Natural Convection Cooling Solutions for GaN HEMT Transistors, in: Proc. of the European Conference on Power Electronics and Applications, 2018, pp. 1–9 (2018).
[214] A. Villamor, Z. Zong, Power GaN 2017: Epitaxy, devices, applications, and technology trends 2017, Tech. rep., Yole Developpment (2017).
[215] T. J. Anderson, S. Chowdhury, O. Aktas, M. Bockowski, J. K. Hite, GaN Power Devices Current Status and Future Directions, The Electrochemical Society Interface 27 (4) (2018) 43–47 (2018).
[216] F. Roccaforte, P. Fiorenza, G. Greco, R. L. Nigro, F. Giannazzo, F. Iucolano, M. Saggio, Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices, Microelectronic Engineering 187-188 (2018) 66 – 77 (2018).
[217] G. Longobardi, L. Efthymiou, M. Arnold, GaN power devices for Electric Vehicles State-of-the-art and future perspective, in: IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference,

2018, pp. 1–6 (2018).
[218] H. Li, SiC technologies adoption is going to accelerate with a tipping point in 2019 - Power SiC 2017: Materials, Devices, Modules, And Applications report, Tech. rep., Yole Developpement (2017).
[219] J. Zhu, H. Kim, H. Chen, R. Erickson, D. Maksimovi, High efficiency SiC traction inverter for electric vehicle applications, in: Applied Power Electronics Conference and Exposition (APEC), 2018, pp. 1428–1433 (2018).
[220] C. Zhang, S. Srdic, S. Lukic, Y. Kang, E. Choi, E. Tafti, A SiC-Based 100 kW High-Power-Density (34 kW/L) Electric Vehicle Traction Inverter, in: Energy Conversion Congress and Exposition (ECCE), 2018, pp. 3880–3885 (2018).
[221] H. Kim, H. Chen, J. Zhu, D. Maksimovi, R. Erickson, Impact of 1.2kV SiC-MOSFET EV traction inverter on urban driving, in: Wide Bandgap Power Devices and Applications (WiPDA), 2016, pp. 78–83 (2016).
[222] Fraunhofer IISB: department vehicle electronics, Potential of SiC for Automotive Power Electronics , Tech. rep.
[223] J. Casady, K. Olejniczak, T. McNutt, D. Simco, B. Passmore, R. Shaw, D. Martin, A. Curbow, B. Hull, J. Palmour, 88 kilowatt automotive inverter with new 900 Volt silicon carbide MOSFET technology (2017).
[224] B. Sarlioglu, C. T. Morris, D. Han, S. Li, Driving Toward Accessibility: A Review of Technological Improvements for Electric Machines, Power Electronics, and Batteries for Electric and Hybrid Vehicles, IEEE Industry Applications Magazine 23 (1) (2017) 14–25 (2017).
[225] Oak Ridge National Laboratory, Benchmarking EV and HEV Technologies, Tech. rep., Oak Ridge National Laboratory.
[226] J. Lutz, H. Schlangenotto, U. Scheuermann, R. D. Donker, Semiconductor Power Devices: Physics, Characteristics, Reliability, Springer, 2011 (2011).
[227] P. Brosselard, X. Jorda, M. Vellvehi, A. Perez-Tomas, P. Godignon, J. Millan, 1.2 kV Rectifiers Thermal Behaviour: comparison between Si PiN, 4H-SiC Schottky and JBS diodes, in: Proc. of the European Conference on Power Electronics and Applications, 2007, pp. 1–9 (2007).
[228] M. S. Lee, J. H. Lee, B. S. Jin, J. B. Lee, D. W. Chung, W. Frank, New intelligent power module with silicon carbide diode, in: Proc. of the International Conference on Power Electronics and ECCE (ICPE ECCE), 2011, pp. 1083–1086 (2011).
[229] J. Millán, A review of WBG power semiconductor devices, in: Proc. of the Semiconductor Conference (CAS), 2012, pp. 57–66 (2012).
[230] H. A. Mantooth, K. Peng, E. Santi, J. L. Hudgins, Modeling of Wide Bandgap Power Semiconductor Devices - Part I, IEEE Transactions on Electron Devices 62 (2) (2015) 423–433 (2015).
[231] R. E. Stahlbush, K. X. Liu, M. E. Twigg, Effects of Dislocations and Stacking Faults on the Reliability of 4H-SiC PiN Diodes, in: Proc. of the International Reliability Physics Symposium Proceedings, 2006, pp. 90–94 (2006).
[232] E. Santi, K. Peng, H. A. Mantooth, J. L. Hudgins, Modeling of Wide-Bandgap Power Semiconductor Devices - Part II, IEEE Transactions on Electron Devices 62 (2) (2015) 434–442 (2015).
[233] M. Ostling, R. Ghandi, C. M. Zetterling, SiC power devices ; Present status, applications and future perspective, in: Proc. of the Symposium on Power Semiconductor Devices and ICs (ISPSD), 2011, pp. 10–15 (2011).
[234] R. Green, A. Lelis, D. Habersat, Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs, Japanese Journal of Applied Physics 55 (4S) (2016) 04EA03 (2016).
[235] P. Friedrichs, R. Rupp, Silicon carbide power devices - current developments and potential applications, in: Proc. of the European Conference on Power Electronics and Applications, 2005, pp. 11–22 (2005).
[236] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, Y. Yokotsuji, High performance SiC trench devices with ultra-low Ron, in: Proc. of the International Electron Devices Meeting, 2011, pp. 26.5.1–26.5.3 (2011).
[237] M. Treu, R. Rupp, P. Blaschitz, K. Ruschenschmidt, T. Sekinger, P. Friedrichs, R. Elpelt, D. Peters, Strategic Considerations for Unipolar SiC Switch Options: JFET vs. MOSFET, in: Proc. of the Industry Applications Annual Meeting, 2007, pp. 324–330 (2007).
[238] E. Cereceda, D. Snchez, X. Perpi, M. Vellveh, J. Rebollo, P. Godignon, X. Jord, Estimation of electron mobility in lateral cannel SiC junction field effect transistor, in: Proc. of the Seminario Annual de Automtica, Electrnica Industrial e Instrumentacin (SAAEI), 2018, pp. 1–6 (2018).
[239] R. K. Malhan, Y. Takeuchi, M. Kataoka, A. P. Mihaila, S. J. Rashid, F. Udrea, G. A. J. Amaratunga, Normally-off trench JFET technology in 4H silicon carbide, Microelectronic Engineering

83 (1) (2006) 107 – 111,) (2006).
[240] H. Mirzaee, A. De, A. Tripathi, S. Bhattacharya, Design Comparison of High-Power Medium-Voltage Converters Based on a 6.5-kV Si-IGBT/Si-PiN Diode, a 6.5-kV Si-IGBT/SiC-JBS Diode, and a 10-kV SiC-MOSFET/SiC-JBS Diode, IEEE Transactions on Industry Applications 50 (4) (2014) 2728–2740 (2014).
[241] H. Yu, J. Lai, X. Li, Y. Luo, L. Fursin, J. H. Zhao, P. Alexandrov, B. Wright, M. Weiner, An IGBT and MOSFET gated SiC bipolar junction transistor, in: Proc. of the Conference Record of the Industry Applications Conference, 2002, pp. 2609–2613 (2002).
[242] V. Soler, M. Cabello, M. Berthou, J. Montserrat, J. Rebollo, P. Godignon, A. Mihaila, M. R. Rogina, A. Rodrguez, J. Sebastin, High-Voltage 4H-SiC Power MOSFETs With Boron-Doped Gate Oxide, IEEE Transactions on Industrial Electronics 64 (11) (2017) 8962–8970 (2017).
[243] V. Pala, E. V. Brunt, S. H. Ryu, B. Hull, S. Allen, J. Palmour, A. Hefner, Physics of bipolar, unipolar and intermediate conduction modes in Silicon Carbide MOSFET body diodes, in: Proc. of the International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2016, pp. 227–230 (2016).
[244] S. Ryu, C. Capell, C. Jonas, L. Cheng, M. O'Loughlin, A. Burk, A. Agarwal, J. Palmour, A. Hefner, Ultra high voltage (¿12 kV), high performance 4H-SiC IGBTs, in: 2012 24th International Symposium on Power Semiconductor Devices and ICs, 2012, pp. 257–260 (2012).
[245] E. Barbarini, STMicroelectronics SiC Module. Tesla Model 3 inverter, Tech. rep. (2018).
[246] A. De, A. J. Morgan, V. M. Iyer, H. Ke, X. Zhao, K. Vechalapu, S. Bhattacharya, D. C. Hopkins, Design, Package, and Hardware Verification of a High-Voltage Current Switch, IEEE Journal of Emerging and Selected Topics in Power Electronics 6 (1) (2018) 441–450 (2018).
[247] Infineon Technologies, Hybrid Kit for HybridPACK 2 (2014).
[248] M. Sprenger, R. Alvarez, I. Staudt, S. Bernet, Characterization of a new 1.2 kV IGBT 3L-NPC phase-leg module for low voltage applications, in: Proc. of the European Conference on Power Electronics and Applications, 2011 (2011).
[249] K. Wang, Z. Qi, F. Li, L. Wang, X. Yang, Review of state-of-the-art integration technologies in power electronic systems, CPSS Transactions on Power Electronics and Applications 2 (4) (2017) 292–305 (2017).
[250] C. Qian, A. M. Gheitaghy, J. Fan, H. Tang, B. Sun, H. Ye, G. Zhang, Thermal Management on IGBT Power Electronic Devices and Modules, IEEE Access 6 (2018) 12868–12884 (2018).
[251] P. Ning, X. Wen, L. Li, H. Cao, An improved planar module automatic layout method for large number of dies, CES Transactions on Electrical Machines and Systems 1 (4) (2017) 411–417 (2017).
[252] C. Neeb, L. Boettcher, M. Conrad, R. W. D. Doncker, Innovative and Reliable Power Modules: A Future Trend and Evolution of Technologies, IEEE Industrial Electronics Magazine 8 (3) (2014) 6–16 (2014).
[253] B. S. Passmore, A. B. Lostetter, A review of SiC power module packaging technologies: Attaches, interconnections, and advanced heat transfer, in: Proc. of the IEEE International Workshop On Integrated Power Packaging (IWIPP), 2017, pp. 1–5 (2017).
[254] C. Chen, F. Luo, Y. Kang, A review of SiC power module packaging: Layout, material system and integration, CPSS Transactions on Power Electronics and Applications 2 (3) (2017) 170–186 (2017).
[255] P. D. Anton Miric, Inorganic Substrates for Power Electronics Appliations, Tech. rep., Heraeus Deutscland GmbH (2015).
[256] B. Mouawad, B. Thollin, C. Buttay, L. Dupont, V. Bley, D. Fabrgue, M. Soueidan, B. Schlegel, J. Pezard, J. Crebier, Direct Copper Bonding for Power Interconnects: Design, Manufacturing, and Test, IEEE Transactions on Components, Packaging and Manufacturing Technology 5 (1) (2015) 143–150 (2015).
[257] A. Volke, M. Hornjamp, IGBT Modules - Technologies, Driver and Application, Infineon Technologies AG, Munich, 2012 (2012).
[258] C. C. Jung, c. Silber, J. Scheible, Heat Generation in Bond Wires, IEEE Transactions on Components, Packaging and Manufacturing Technology 5 (10) (2015) 1465–1476 (2015).
[259] L. A. Navarro, X. Perpi, P. Godignon, J. Montserrat, V. Banu, M. Vellvehi, X. Jord, Thermomechanical Assessment of Die-Attach Materials for Wide Bandgap Semiconductor Devices and Harsh Environment Applications, IEEE Transactions on Power Electronics 29 (5) (2014) 2261–2271 (2014).
[260] X. Jorda, X. Perpina, M. Vellvehi, J. Coleto, Power-Substrate Static Thermal Characterization Based on a Test Chip, IEEE Transactions on Device and Materials Reliability 8 (4) (2008) 671–679 (2008).

[261] C. Martin, J. Guichon, J. Schanen, R. Pasterczyk, Gate Circuit Layout Optimization of Power Module Regarding Transient Current Imbalance, IEEE Transactions on Power Electronics 21 (5) (2006) 1176–1184 (2006).

[262] H. Li, W. Zhou, X. Wang, S. Munk-Nielsen, D. Li, Y. Wang, X. Dai, Influence of Paralleling Dies and Paralleling Half-Bridges on Transient Current Distribution in Multichip Power Modules, IEEE Transactions on Power Electronics 33 (8) (2018) 6483–6487 (2018).

[263] Q. Haihong, Z. Ying, Z. Ziyue, W. Dan, F. Dafeng, W. Shishan, Z. Chaohui, Influences of circuit mismatch on paralleling silicon carbide MOSFETs, in: Proc. of the Conference on Industrial Electronics and Applications (ICIEA), 2017, pp. 556–561 (2017).

[264] S. L. Mantia, L. Abbatelli, C. Brusca, M. Melito, M. Nania, Design Rules for Paralleling of Silicon Carbide Power MOSFETs, in: Proc. of the PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2017, pp. 1–6 (2017).

[265] X. Wang, Z. Zhao, Y. Zhu, K. Chen, L. Yuan, A comprehensive study on the gate-loop stability of the SiC MOSFET, in: Proc. of the Energy Conversion Congress and Exposition (ECCE), 2017, pp. 3012–3018 (2017).

[266] A. Dutta, S. S. Ang, Electromagnetic Interference Simulations for Wide-Bandgap Power Electronic Modules, IEEE Journal of Emerging and Selected Topics in Power Electronics 4 (3) (2016) 757–766 (2016).

[267] G. Regnat, P. Jeannin, D. Frey, J. Ewanchuk, S. V. Mollov, J. Ferrieux, Optimized Power Modules for Silicon Carbide MOSFET, IEEE Transactions on Industry Applications 54 (2) (2018) 1634–1644 (2018).

[268] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, Y. Kang, An SiC-Based Half-Bridge Module With an Improved Hybrid Packaging Method for High Power Density Applications, IEEE Transactions on Industrial Electronics 64 (11) (2017) 8980–8991 (2017).

[269] P. D. Reigosa, F. Iannuzzo, S. Munk-Nielsen, F. Blaabjerg, New layout concepts in MW-scale IGBT modules for higher robustness during normal and abnormal operations, in: Proc. of the Applied Power Electronics Conference and Exposition (APEC), 2016, pp. 288–294 (2016).

[270] A. Cataliotti, D. D. Cara, G. Marsala, A. Pecoraro, A. Ragusa, G. Tinè, High-Frequency Experimental Characterization and Modeling of Six Pack IGBTs Power Modules, IEEE Transactions on Industrial Electronics 63 (11) (2016) 6664–6673 (2016).

[271] A. Lemmon, M. Mazzola, J. Gafford, C. Parker, Instability in Half-Bridge Circuits Switched With Wide Band-Gap Transistors, IEEE Transactions on Power Electronics 29 (5) (2014) 2380–2392 (2014).

[272] M. Guacci, D. Bortis, I. F. Kovacevic-Badstbner, U. Grossner, J. W. Kolar, Analysis and design of a 1200 V All-SiC planar interconnection power module for next generation more electrical aircraft power electronic building blocks, CPSS Transactions on Power Electronics and Applications 2 (4) (2017) 320–330 (2017).

[273] W. Jakobi, A. Uhlemann, M. Thoben, C. Schweikert, C. Strenger, A. P. Pai, L. Beaurenaut, M. Muenzer, Benefits of new CoolSiCTM MOSFET in HybridPACKTM Drive package for electrical drive train applications., in: Proc. of the Conference on Integrated Power Electronics Systems (CIPS), 2018, pp. 1–9 (2018).

[274] A. Matallana, J. Andreu, J. I. Garate, I. Aretxabaleta, E. Planas, Analysis and modelling of igbts parallelization fundamentals, in: Proc. of the IEEE Industrial Electronics Society (IECON), 2016, pp. 3247–3252 (2016).

[275] A. Matallana, J. Andreu, J. I. Garate, I. M. de Alegra, I. Kortabarria, Analysis of impedance and current distributions in parallel IGBT design, in: Proc. of the International Symposium on Industrial Electronics (ISIE), 2017, pp. 616–621 (2017).

[276] M. Kegeleers, J. Koerner, S. Matlok, M. Hofmann, M. Maerz, Parasitic Inductance Analysis of a Fast Switching 100 kW Full SiC Inverter, in: Proc. of the PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2017, pp. 1–7 (2017).

[277] S. Kicin, F. Traub, S. Hartmann, E. Bianda, C. Bernhard, S. Skibin, F. Canales, A new concept of a high-current power module allowing paralleling of many SiC devices assembled exploiting conventional packaging technologies, in: Proc. of the International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2016, pp. 467–470 (2016).

[278] J. Marchesini, P. Jeannin, Y. Avenas, J. Delaine, C. Buttay, R. Riva, Implementation and Switching Behavior of a PCB-DBC IGBT Module Based on the Power Chip-on-Chip 3-D Concept, IEEE Transactions on Industry Applications 53 (1) (2017) 362–370 (2017).

[279] C. Martin, J. L. Schanen, J. M. Guichon, R. Pasterczyk, Analysis of Electromagnetic Coupling and Current Distribution Inside a Power Module, IEEE Transactions on Industry Applications 43 (4) (2007) 893–901 (2007).

[280] R. Azar, F. Udrea, W. T. Ng, F. Dawson, W. Findlay, P. Waind, The Current Sharing Optimization of Paralleled IGBTs in a Power Module Tile Using a PSpice Frequency Dependent Impedance Model, IEEE Transactions on Power Electronics 23 (1) (2008) 206–217 (2008).

[281] P. Jeannin, J.-L. Schanen, E. Clavel, Original cabling conditions to insure balanced current during switching transitions between paralleled semiconductors, IEEE Transactions on Industry Applications 38 (1) (2002) 181–188 (2002).

[282] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, H. Li, A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DCDC Converter, IEEE Transactions on Power Electronics 32 (6) (2017) 4728–4740 (2017).

[283] H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt, W. T. Franke, Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs, IEEE Transactions on Power Electronics 31 (1) (2016) 621–634 (2016).

[284] J. Wang, H. S. Chung, R. T. Li, Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance, IEEE Transactions on Power Electronics 28 (1) (2013) 573–590 (2013).

[285] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, K. Rajashekara, A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications, IEEE Transactions on Power Electronics 29 (5) (2014) 2307–2320 (2014).

[286] Q. Yan, X. Yuan, Y. Geng, A. Charalambous, X. Wu, Performance Evaluation of Split Output Converters With SiC MOSFETs and SiC Schottky Diodes, IEEE Transactions on Power Electronics 32 (1) (2017) 406–422 (2017).

[287] M. Wang, F. Luo, L. Xu, A Double-End Sourced Wire-Bonded Multichip SiC MOSFET Power Module With Improved Dynamic Current Sharing, IEEE Journal of Emerging and Selected Topics in Power Electronics 5 (4) (2017) 1828–1836 (2017).

[288] H. Li, S. Munk-Nielsen, S. Beczkowski, X. Wang, A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules, IEEE Transactions on Power Electronics 31 (12) (2016) 8042–8045 (2016).

[289] S. Fu, Y. Mei, X. Li, C. Ma, G. Lu, A Multichip Phase-Leg IGBT Module Bonded by Pressureless Sintering of Nanosilver Paste, IEEE Transactions on Device and Materials Reliability 17 (1) (2017) 146–156 (2017).

[290] T. Harder, ECPE Guideline AQG 324 - Qualification of Power Modules for Use in Power Electronics Converter Units (PCUs) in Motor Vehicles, Tech. rep., ECPE European Center for Power Electronics e.V. (2018).

[291] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, A. Emadi, Bus Bar Design for High-Power Inverters, IEEE Transactions on Power Electronics 33 (3) (2018) 2354–2367 (2018).

[292] Y. Ren, X. Yang, F. Zhang, L. Tan, X. Zeng, Analysis of a low-inductance packaging layout for Full-SiC power module embedding split damping, in: Proc. of the Applied Power Electronics Conference and Exposition (APEC), 2016, pp. 2102–2107 (2016).

[293] A. Kopta, M. Rahimo, C. Corvasce, M. Andenna, F. Dugal, F. Fischer, S. Hartmann, A. Baschnagel, Next Generation IGBT and Package Technologies for High Voltage Applications, IEEE Transactions on Electron Devices 64 (3) (2017) 753–759 (2017).

[294] F. Yang, Z. Wang, Z. Liang, F. Wang, Electrical Performance Advancement in SiC Power Module Package Design with Kelvin Drain Connection and Low Parasitic Inductance, IEEE Journal of Emerging and Selected Topics in Power Electronics (2018) 1–1 (2018).

[295] S. C. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 2006 (2006).

[296] S. Seal, H. A. Mantooth, High Performance Silicon Carbide Power PackagingPast Trends, Present Practices, and Future Directions, Energies 10 (3) (2017).

[297] P. Ning, F. Wang, K. D. T. Ngo, Automatic layout design for power module, IEEE Transactions on Power Electronics 28 (1) (2013) 481–487 (2013).

[298] L. Yang, K. Li, J. Dai, M. Corfield, A. Harris, K. Paciura, J. O'Brien, C. M. Johnson, Electrical Performance and Reliability Characterization of a SiC MOSFET Power Module With Embedded Decoupling Capacitors, IEEE Transactions on Power Electronics 33 (12) (2018) 10594–10601 (2018).