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# *Impact of a Resistive Superconductive Fault Current Limiter in a Multi-Terminal HVDC Grid*

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*Abstract— The relevance of multi-terminal HVDC grids is expected to increase in next years. However, there are still several technical, economical and legal limitations that interfere with the construction of those multi-terminal links. One of the main technical obstacles is the handling of DC fault currents, because the interruption of DC currents in HVDC systems is nowadays a challenge. Among other proposals, the application of Superconducting Fault Current Limiters (SFCLs) combined with a mechanical Circuit Breaker (CB) solves technically that issue, according to the analysis and simulation results presented in this paper.*

**Keywords—DC fault, HVDC, multi-terminal, VSC-HVDC, PSCAD/EMTDC, resistive fault current limiter, superconductive material.**

## I. INTRODUCTION

Currently, HVDC links are being used mainly for two purposes: to connect off-shore wind farms and gas platforms with the bulk power system and to interconnect power grids for the reinforcement of existing AC grids. As the number of these point-to-point HVDC links increases, it is evident that it would be beneficial to connect them directly, building multi-terminal HVDC grids. However, there are still several technical, economical and legal limitations that interfere with the construction of those multi-terminal links.

The protection of HVDC grids is a major technical constraint. Particularly, the DC fault protection of voltage sourced converter (VSC) technology is one of the main issues that must be addressed. Regarding the causes of DC faults [1], it is assumed that DC faults in cables are due to mechanical stress, which makes the faults permanent. Besides, DC faults in overhead lines are caused by lightning and pollution, thus, they are supposed to be transient ones.

DC faults provoke a fast voltage drop and a current increase, which is enlarged by the contribution of the AC grid to the fault through the freewheeling diodes. As a consequence, DC faults are able to cause great damage [1].

Besides, DC current has no natural zero current crossing, unlike AC current. HVDC circuit breakers (CB) must bring current to zero as well as dissipate the extensive amount of energy stored in the system inductances [2]. There are several types of HVDC CBs. The interruption with mechanical DC CBs is too slow for VSC-HVDC systems, about 20-50 ms. The operation speed of Solid State DC CB is very fast, but these devices have high on-state losses. A combination of both types called hybrid CB has also been proposed, that benefits of both technologies but nowadays it is still under development. Some corporations have presented prototypes [3-4]. It is also possible to use double thyristor switches to clear the DC faults effectively, but this technique leaves the system isolated [5] and selectivity is required for a reliable protection.

Currently, the interruption of DC faults in HVDC systems is mainly performed from the AC side, which is only suitable for point-to-point transmissions. For a trustworthy protection of HVDC grids high fault currents must be managed. Since DC current interruption is still an unsolved issue, a possible approach is to reduce the fault currents and afterwards, interrupt those lower currents with conventional CBs. For that aim, superconductive fault current limiters (SFCL) can be employed [6]. SFCLs, which are based on superconducting materials, limit fault currents to a more manageable level during faults and do not have a significant impact on the electrical system in permanent operation.

Potentially, superconductivity is more suitable for DC systems than for AC systems as superconducting materials are sensitive to magnetic fields in movement. Therefore, the magnetic field distributions inside superconducting strips cause AC hysteresis losses [7]. The performance of SFCLs in HVDC systems is studied in several papers [8-12].

The main contribution of this paper regards the study of a resistive SFCL integrated in a four-terminal HVDC grid. Thus, in Section 2 the modelling approaches for resistive SFCLs are reviewed, in order to identify the most suitable option. Section 3 studies the impact of a resistive SFCL in an

HVDC grid. First, the modelling and parameterization of a resistive SFCL is proposed and finally the performance of the SFCL model is analysed in a multi-terminal HVDC grid. The impact of the SFCL is determined for several DC faults.

## II. Modelling of Resistive SFCLs

Essentially, there are four types of SFCLs: resistive, inductive, saturated-core and magnetic-shield SFCL. Resistive SFCLs show several advantages, such as a simpler structure, smaller size and lower cost [13]. Therefore, nowadays resistive SFCLs are regularly the selected option, also in DC grids [10,14-15].

When the current, the operating temperature or the external magnetic field are smaller than a threshold, resistive SFCLs operate under a *superconducting* state and offer no resistance for current. Under faults, the superconductor resistance increases highly because of the rise of the superconductor temperature. This stage is usually called the *flux-flow* state. When the superconducting material is completely quenched, the SFCL operates in *normal conducting state*. After the fault is cleared, the resistive SFCL needs a recovery time for cooling until it returns to its *superconducting* state.

Different types of simulation models for SFCLs have been presented, from simple models to more complex ones. The resistive SFCL models consist of the superconducting material (Rsc in Fig. 1) and a parallel resistor (Rp in Fig. 1), which is required for avoiding the overheating of the superconducting material. This parallel resistor reduces overvoltage during faults and diverts the fault current [16].

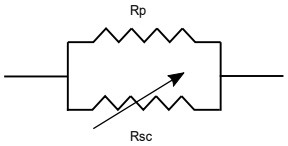


Fig. 1. Resistive SFCL model

There are two options for the parallel resistor (Rp). This resistance (or inductance) can be external, that is, installed in parallel outside the cryogenic environment to reduce the energy dissipated in the superconductor [17]. The other option is to enclose the resistance to the superconductor [18]. Thus, hot spot issues are reduced during the manufacturing process [19]. The parallel resistance can also result from the combination of the external resistance and a confined resistance.

The resistance of the superconducting material varies with current density, and hence, with temperature. Depending on the application, this resistance can be modelled by a simple time-dependent equation (a step, linear or exponential function) or by a thermo-electric model, which can also vary in complexity [20]. The detail of the required model depends on the purpose of the study.

The application of resistive SFCLs in DC systems has been considered in a number of references [7,10-11]. In [12], it has been verified that resistive SFCLs improve the robustness of a wind plant, suppressing the DC fault current, compensating the DC voltage sags and reducing the power fluctuations. The impact of a resistive SFCL on four types of HVDC CBs is analysed in [6].

## III. SFCL Implementation in an HVDC Grid

### A. Description of the Test Grid

The test grid used in the present paper, shown in Fig. 2, is provided by CIGRE [21] and has been developed in PSCAD™/EMTDC™. This configuration, called DCS2, represents a multi-terminal symmetric monopole HVDC link (±200 kV). A 500 MW Wind Farm (Converter F) and a 33 MW offshore load i.e. Oil and Gas platform (Converter E), are linked by a 200 km cable. There are two points of connection with AC grids (Converters B2 and B3), which are modelled connected by a 200 km cable. The short-circuit power of B2 and B3 AC grids is 30 GVA. Onshore and offshore elements are linked with 100 km overhead lines connected in series with a 100 km cable.

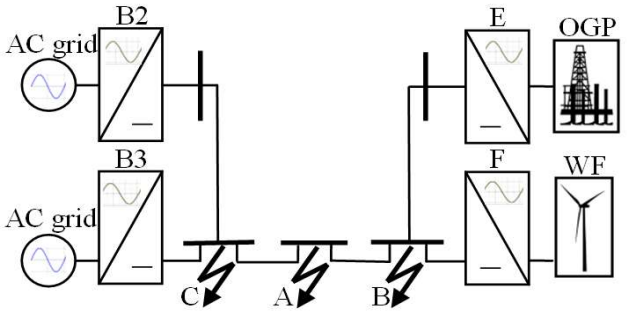


Fig. 2. Four-terminal symmetric monopole test grid.

Converters B2 and B3 (grid side) are controlled by the voltage and active power/reactive power control method (400 MW/0 MVAr into DC grid and 800 MW/0 MVAr into AC grid respectively), whereas the Converter F (WF) is controlled by active and reactive power and Converter E (load) is controlled by voltage and frequency.

### B. Design of SFCL

In the test grid, a SFCL is placed in each pole of the DC buses. This configuration is used in all converters except at the load side, due to its null current contribution in case of fault as it does not include active elements.

In this paper, the SFCL has been represented by an exponential model. The exponential evolution of resistance over the time has been implemented through a transfer function, as shown in Figure 3. $G$ is the gain, or the resistance final value, and $T$ is the time needed to develop the resistance final value. $G$ is set as 30 Ω for grid converters (B2 and B3) and 50 Ω for the Wind Farm converter (F), and $T$ is assumed to be 4 ms. The *Timed Fault Logic* block activates the fault at the specified time and the *Monostable* block keeps it activated for a period of time.

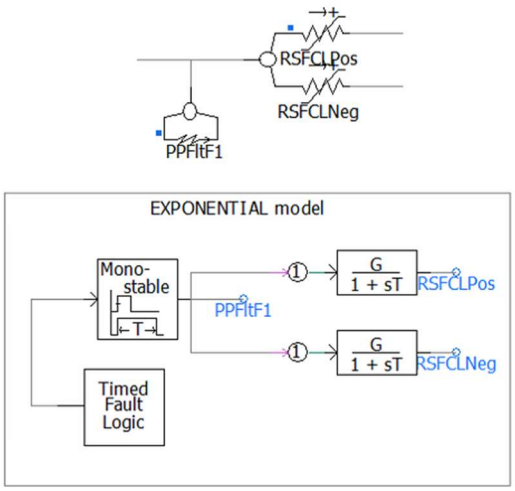


Fig. 3. Implementation of exponential model.

The sizing of the SFCL resistance has been selected based on equations (1), (2) and (3).

$$R_{Conv} = V_{DC} / I_p \tag{1}$$

$$R_{totSFCL} = (V_{DC} / I_{pSFCL} - R_{Conv}) \tag{2}$$

$$R_{SFCL} = R_{totSFCL} / 2 \tag{3}$$

$$LF = \left(I_{pSFCL} / I_p\right) \cdot 100 \tag{4}$$

Where $R_{Conv}$ is the equivalent resistance added by the VSC converter to the circuit in fault state, $V_{DC}$ is the voltage of the DC bus set in 400 kV because of the symmetric configuration, $I_p$ is the prospective peak value of short-circuit current, $R_{totSFCL}$ is the total resistance to install in the circuit, $I_{pSFCL}$ is the peak value of limited current (with SFCL), $R_{SFCL}$ is the resistance for each SFCL, half of $R_{totSFCL}$ for installing one in each pole and LF is the limiting factor in presence of the SFCL device.

### C. *Simulations and Results*

In order to investigate the performance of the multi-terminal VSC-HVDC system in Fig. 2 with the designed SFCL model, several DC permanent fault simulation cases have been carried out on different sections. Thus, the impact of SFCL operation has been studied for pole-to-pole faults for being the most dangerous ones due to high overcurrents, whereas pole-to-ground faults are characterised by the overvoltage in the non-affected pole.

Namely, pole-to-pole faults in the connection of B3-F overhead line and B3-F cable (Position A), DC side of Converter F (Position B) and in the DC side of converter B3 (Position C) have been simulated. The faults have been simulated with and without the SFCLs, in order to analyze the impact of the limiters. Faults are applied at 2 s.

Simulation results when the fault is located in Position A are shown in Fig. 4. These results show the current (kA) for each converter. Without SFCLs, when the fault is applied, current increases very quickly due to the discharge of capacitors. Then, the current sources are mainly the AC grids, therefore the current increase is slower. Afterwards, the fault is in the steady-state, which is characterized by the L/R time constant. Finally, the operation of AC CB in the converters reduces the current exponentially to zero. When SFCLs operate, currents present similar waveforms. However, peak currents are reduced.

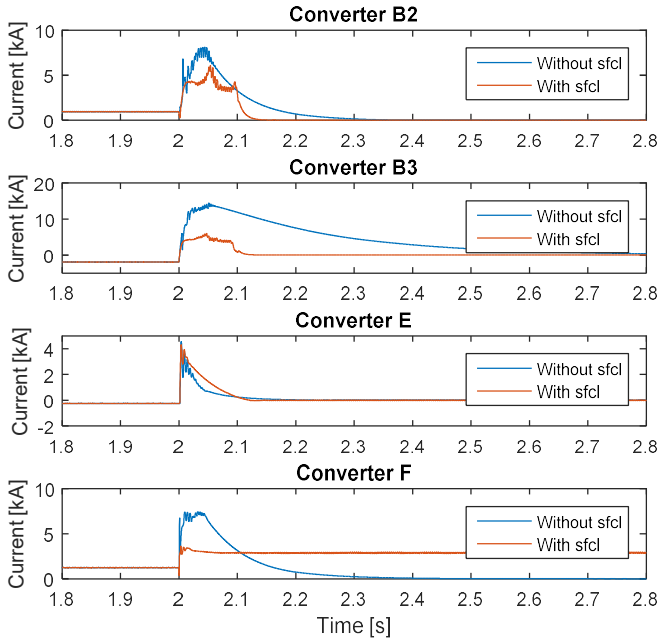


Fig. 4. Pole to pole fault in midline B3-F (position A).

TABLE I. LIMITING FACTOR

| | Without SFCL [kA] | With FCL [kA] | Limiting Factor |
|---|---|---|---|
| **Converter B2 (grid)** | 8.12 | 6.06 | 25.37 % |
| **Converter B3 (grid)** | 14.50 | 6.02 | 58.48 % |
| **Converter E (load)** | 4.57 | 4.70 | -2.80 % |
| **Converter F (WF)** | 7.42 | 6.35 | 14.42 % |

The first instants after fault occurrence are considered the critical ones as a great current is flowing until the protections are activated. The peak value of those currents and the limiting factors are shown in Table I. As depicted, the peak fault current can reach up approximately 9 times of the normal DC current in some points of the circuit. Highest currents are found in converter B3, because it is close to the fault and connected to an AC grid that feeds the fault. With SFCLs applied at B2, B3 and F converters a limiting factor up to 58.45% can be achieved. However, in this case there is a slight increase of circulating current to the load, as there is no SFCL in this converter. Nevertheless, the current increase is almost negligible.

The performances of SFCLs when the fault is located in Position B are shown in Fig. 5 and limiting factors are in Table II.

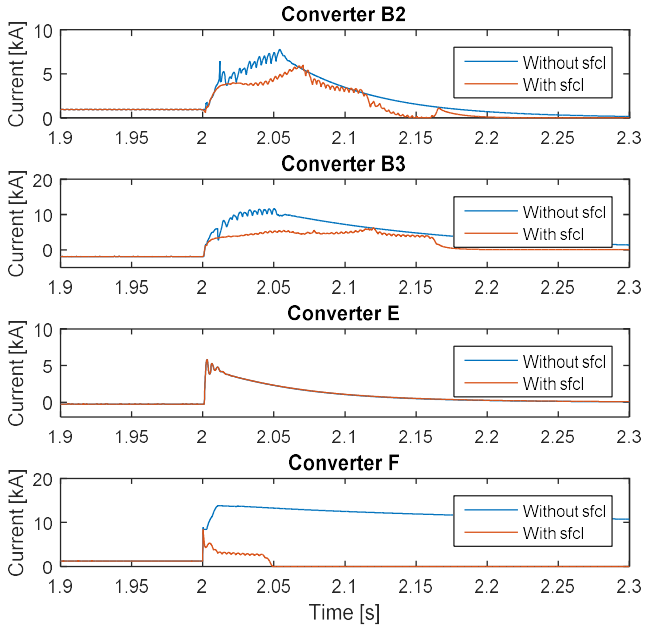


Fig. 5. Pole-to-pole fault in the DC side near Converter F (position B)..

TABLE II. LIMITING FACTOR

| | Without SFCL [kA] | With FCL [kA] | Limiting Factor |
|---|---|---|---|
| **Converter B2 (grid)** | 7.76 | 6.00 | 22.68 % |
| **Converter B3 (grid)** | 11.65 | 6.20 | 46.78 % |
| **Converter E (load)** | 5.85 | 5.85 | 0.00% |
| **Converter F (WF)** | 13.80 | 8.42 | 38.99 % |

This is the worst case for the electronic devices installed in Converter F (WF), given that they are supposed to bear the highest current they are designed for. The maximum fault current appears when the cable that connects the converter to the fault has a lower inductance. It can be seen in Fig. 5 that bigger currents lead to more damped currents. Without SFCLs 13.80 kA would flow through this converter, being able to be reduced to 8.42 kA with SFCLs, these results in a limiting factor of 38.99 %. The highest advantage in this case is for the Converter B3 with a limiting factor of 46.78 %.

The behaviour of the system when the fault is applied near Converter B3 (Position C) is also shown in Fig. 6 and limiting factors are indicated in Table III.

The worst case for the grid converters (B2 and B3) and all the elements associated to them is presented in Fig. 6, where the peak current can be approximately 15 times the normal value. In absolute values, the peak current in Converter B2 is reduced from 9.68 kA to 6.43 kA and in Converter B3 from 31.63 kA to 9.27 kA. A limiting factor of 33.57 % and 70.69 % can be achieved respectively after the implementation of SFCLs, being the last one the largest one.

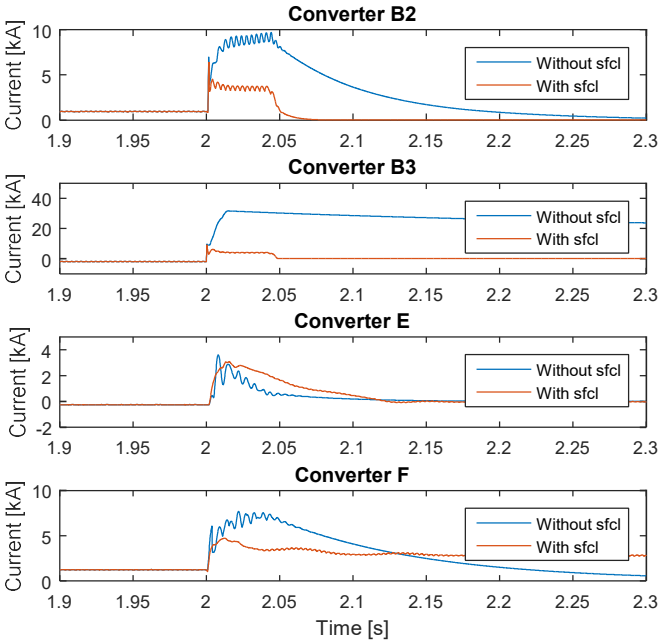


Fig. 6. Pole-to-pole fault in the DC side near Converter B3 (position C).

TABLE III. LIMITING FACTOR

| | Without SFCL [kA] | With FCL [kA] | Limiting Factor |
|---|---|---|---|
| **Converter B2 (grid)** | 9.68 | 6.43 | 33.57 % |
| **Converter B3 (grid)** | 31.63 | 9.27 | 70.69 % |
| **Converter E (load)** | 3.59 | 3.07 | 14.48 % |
| **Converter F (WF)** | 7.68 | 4.73 | 38.41 % |

## IV. CONCLUSIONS.

Resistive SFCLs are a promising technology able to limit the excessive fault levels caused by the expansion of power grids and the integration of renewable energy sources. Moreover, SFCLs can provide a technical solution for DC fault interruption, in combination with conventional CBs. Therefore, in the present paper, the performance of a resistive SFCL has been analysed in a four-terminal HVDC grid. Several faults in different locations have been applied in order to evaluate the impact of the limiter.

In HVDC systems the DC fault current evolution is more aggressive, and the steady value is significantly higher than AC faults. In case of fault, all current sources must be separated from every active powering end. Therefore, it is more difficult to control a meshed grid than a point-to-point link. In this scenario, SFCLs possess a great implantation potential, as proved in this paper.

In the present paper, the impact of SFCL operation has been studied for pole-to-pole faults for being the most dangerous ones due to high overcurrents. Based on the simulation results, it can be concluded that through resistive SFCLs fault currents can be reduced up to 70 %. In addition,

in normal operation limiter losses are minimum since the resistance is almost zero. In contrast, as SFCL resistance is not developed immediately after the fault occurrence, the first current peak corresponding to the discharge of capacitors may not be limited.

Thus, the combination of SFCLs with CBs proves to be a technically feasible option for DC fault interruption in multi-terminal HVDC grids. Namely, fault current are limited to fault breaking capacity values of commercially available CB models. Even more, the rest of electronic devices could also be designed for being protected against lower fault currents, leading to an economical savage. However, economic aspects are out of the scope of the present paper, but should be carefully studied in future projects, as well as necessary cooling systems.

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