IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

IEEE POWER & ENERGY SOCIETY SECTION

Received 18 November 2023, accepted 16 January 2024, date of publication 23 January 2024, date of current version 1 February 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3357614

RESEARCH ARTICLE

Optimal Connection Voltage of Soft Open Point and Shore-to-Ship Power Converters for Enhanced Capacitive Reactive Power Operation

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This work was supported by GISEL Research Group IT1522, Basque Country Government.

ABSTRACT Soft Open Point and Shore-to-Ship Power applications permit to deploy smart grid infrastructure into distribution and port networks. Both are based on power electronics converters that require an optimal integration to maximize capacitive reactive power limits at minimum impact over costs and efficiency. To meet this objective, the paper defines a methodology to calculate the optimal connection voltage of power converters used in these applications. The proposed methodology is based on three novelties related to capacitive reactive power limits definition. Firstly, all affecting variables from positive and negative sequences are jointly considered completing partial approaches identified in previous works. Secondly, the impact of negative sequence affecting multiple converter terminals is considered, adding accuracy to reactive power limit calculation of Soft Open Point converters. Thirdly, the influence of two main constraints affecting modulation limits in real converters is described, quantifying its impact over maximum capacitive reactive power limits. These constraints are related to semiconductor characteristics and to digital implementation; usually not considered for dimensioning purposes at application level, but which can have a key impact on capacitive operation. At this point, the authors provide explicit details of industrially available converter designs to support calculations and evaluate its impact over the final solution. Considering the above, the proposed methodology is implemented on a real 20 MW 6.6 kV medium voltage converter design and results are quantified and compared from a reactive power capacity, efficiency and cost perspective.

INDEX TERMS Modulation limits, reactive power capability, shore-to-ship power, soft open point.

I. INTRODUCTION

Soft Open Point (SOP) and Shore-to-Ship Power (S2SP) are Power Electronics (PE) based applications that play an increasingly important role in global electrification strategies. Both use Back-to-Back (B2B) converters that electrically connect two AC grids through an intermediate DC bus (Fig. 1). Whereas the use of SOP is oriented to transforming modern distribution grids into Active Distribution Networks, S2SP is a key application for the decarbonization of maritime transport.

On the one hand, the existence of ageing distribution infrastructure combined with the need of supplying reliable power to ever-increasing electricity consumers, define some of the challenges that Distribution System Operators (DSO) must face at present. To confront them, distribution grids must be equipped with assets that allow for functionalities such as:

- Voltage profile and power flow control to increase hosting capacity [1], [2].

The associate editor coordinating the review of this manuscript and approving it for publication was Shafi K. Khadem.

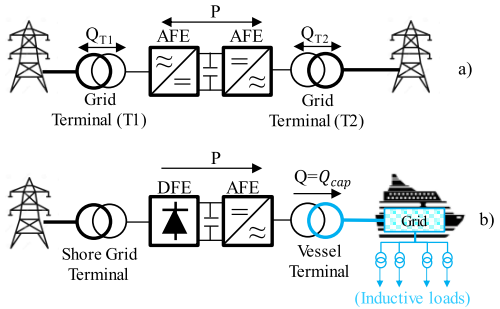


FIGURE 1. Representation of a two terminal SOP application (a), and a two terminal DFE grid interfaced S2SP application (b).

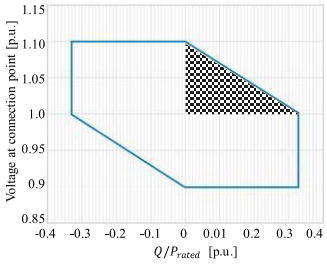


FIGURE 2. Reactive power delivery curve at rated active power conditions, represented as a function of the grid voltage, based on [23] .

- Network re-configuration for enhanced system resiliency and supply continuity [3].
- Voltage and feeder load balancing to ensure power quality and supply security [4], [5]
- Power supply restoration for supply continuity [6].

Thanks to PE, SOP applications can offer all these functionalities in one single power converter, therefore, are already considered by DSOs in their planning strategies. In this sense, pioneering utility scale SOP projects have gone through their first years of commercial operation [2]. A summary of this and other projects that have been deployed in the field can be found in [7] (focused on utility projects). Additionally, information on real converter designs oriented to SOP applications can be found in [2] and [7]. To finalize, review works on the topic offer an overall view of SOP applications and related functionalities that complement previous references [8], [9].

On the other hand, S2SP is an application that contributes to electrifying ports by means of 50/60 Hz frequency converters that connect berthed vessel on-board grids with port networks [10]. Aligned with toughening policies on polluting gas emissions, S2SP applications are called to accelerate their roll out in the coming years [11], [12]. The study presented in [13] provides a detailed review of converter topologies used in S2SP systems, an information that can be complemented with [10], [14], [15], [16]. Additionally, research on converter control [17], [18] and protection structures [19], [20], [21] are two of the main technical topics covered on S2SP applications.

From a converter sizing perspective, SOP and S2SP share similar rating requirements. According to [22], most demanding S2SP applications used for supplying cruise vessels must be sized to at least 16 MVA (20 MVA recommended). In contrast, size of SOP applications is not predetermined nevertheless, a typical approach is to match SOP size with MV distribution power line ratings which typically are in the range of 10-20 MVA [2], [7]. When it comes to converter types, SOP applications are built upon Active Front End (AFE) PE bridges to ensure bidirectional power flow between SOP terminals. Compared to this, due to unidirectional power flow requirements, S2SP applications can use lower cost Diode Front End (DFE) PE bridges at the shore connection. On the contrary, AFE PE bridges are required at the vessel terminal to permit active (P) and reactive (Q) power control [13] (Fig. 1).

Power requirements alongside space constraints in either electrical substations or ports, make Medium Voltage (MV) power converters most suitable for building SOP and S2SP applications. A comparison of pros and cons of different converter topologies oriented to S2SP is presented in [13] providing black-box type information that is valid for assessing SOP applications too (e.g., PE characteristics, control complexity or costs, among others). In this comparative study, MV three level Neutral-Point-Clamp (MV 3L NPC) and Modular Multilevel Converters (MMC) are highlighted as outstanding topologies. According to [13], MV 3L NPC presents lower cost and complexity and is proven in use in the mature drive industry. Nevertheless, intermediate DC bus and output AC voltages are limited by voltage rating of semiconductors and configuration thereof inside PE phase modules (i.e., series connection of semiconductors Fig. 3). On the contrary, MMC topologies permit to increase output voltages thanks to higher converter DC bus values achieved through multiple series-connected semiconductor modules.

Considering the above, the dimensioning of SOP and S2SP applications based on MV 3L NPC topologies require specific attention when operation points that maximize converter output voltage requirements are imposed. The latter correspond to operation points that require high values of Q to be delivered by the converter into the grid (i.e., capacitive reactive power, Q_{cap}).

In such operation points is when the MV 3L NPC converter, operated at its maximum permissible DC bus voltage can reach the maximum synthesizable AC output voltage and therefore limit its power capacity despite not having reached its current limitation yet. Capacitive reactive power operation requirements get most demanding when imposed simultaneously at rated active power (P_{rated}) and within the positive tolerance band of grid voltage. The operation of a SOP within the hatched area shown in Fig. 2, representing the requirements imposed by modern grid codes [23], corresponds to a practical application example in this sense. Additionally, the following applications are also potential use cases that would benefit from maximizing the Q_{cap} in SOP converters:

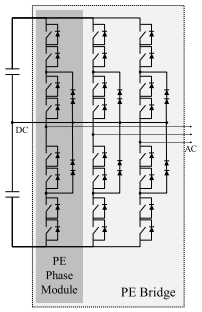


FIGURE 3. Serialized IGBT 3L NPC [26] – detail of PE bridge and PE phase module.

- Participation of DSOs in Reactive Power markets using SOP converters' maximum Q capacity [24].
- Fulfillment of standards that regulate Q exchange between transmission (T) and distribution (D) grids [25] (i.e., need to compensate the excess or lack of Q flowing from D to T to meet required limits).

Face to such requirements, MMC topology has similar theoretical limitations but can avoid them by oversizing the converter DC bus voltage with additional semiconductor modules installed in it.

On the other hand, converters used in S2SP applications operate by purpose in these precise conditions, i.e., delivering active and reactive power to vessel loads which are predominantly inductive. Operation constraints for supplying power to cruise vessels impose active power ratings beyond 10 MW at capacitive power factor values in the range of 0.8-0.9 p.u. (Q delivered to the vessel loads). Moreover, S2SP converters must be able to reach these operation points at higher-than-rated AC output voltages at vessel terminal. This can be necessary to compensate voltage drop in long cable connections in cases where the S2SP converter location at port is distant from the vessel. Finally, it must be highlighted that all these requirements become more restrictive in SPSP applications that are built upon DFE PE due to lower DC bus operation voltages compared to AFE PE designs.

Considering the above, the optimal design of SOP and S2SP applications using converter topologies that present DC bus limitations (e.g., MV 3L NPC) demands a joint assessment of application requirements and converter constraints. Assuming that converter hardware (HW) cannot be modified but used as an existing building block, optimal design of SOP and S2SP applications must come from a system integration perspective. In this sense, it is necessary to define the adequate converter connection voltage that maximizes P_{rated} and Q_{cap} simultaneous operation whilst minimizing the impact over cost and efficiency. To the authors' best knowledge, this topic has not been addressed by literature and is the main contribution of this paper where a calculation method valid for any converter topology is defined.

For the definition of this method, firstly, converter maximum Q_{cap} (Q_{cap_max}) must be formulated considering all variables affecting it. Basic theoretical formulation on this topic can be found in [27], [28], [29], and [30] for balanced grid conditions (i.e. positive sequence). A more in-detail approach studying the effect of negative sequence over Q_{cap_max} is presented in [31]. Nevertheless, the latter does not analyze the impact of negative sequence over converter's DC bus ripple therefore, over reactive power limits. This aspect is quantified by [32] for static reactive compensators (STATCOM) which are not directly comparable to SOP or S2SP due to single terminal construction and obvious differences in P flow. These publications provide each a partial view on how individual variables can affect Q_{cap_max} but the lack of a one-stop approach that provides a joint assessment of all possible constraints is still identified.

As a second contribution, this paper overcomes this gap by gathering all positive and negative sequence related variables into the equations that permit to calculate Q_{cap_max}. Moreover, for the first time, the paper adapts this calculation to SOP applications which, unlike other cases (e.g., renewable B2B converters), can be affected by negative sequence constraints at both grid terminals.

A third contribution is done in the paper providing specific details of converter modulation as a key parameter that influences Q_{cap_max} limits. Literature related to Q_{cap_max} calculation methods [27], [28], [29], [30], [31], [32], adopt typical converter modulation parameters as by-default values without describing how real constraints that are intrinsic to semiconductors and to how modulation is implemented in industrial digital controllers can affect Q_{cap_max}. Bridging the gap between theory and industrial practice, this paper compares and quantifies the impact of three specific modulation techniques over Q_{cap_max}. This information is comprehensively integrated into the optimal connection voltage calculation method that is proposed and as an additional merit, specific values from real semiconductors and from an industrially available 6.6 kV 3L NPC 20 MW SOP converter are used to support all calculations.

Finally, all previous contributions are brought together proposing a methodology used to determine a cost comparison of S2SP applications built upon DFE or AFE type PE bridges. The comparison is done considering the Short-Circuit Current (SCC) injection requirement that is imposed over the vessel terminal for protection relay adjustment purposes. Based on a real application example derived from the authors' industrial experience and using data from the previously mentioned 6.6 kV 3L NPC 20 MW converter, a cost breakdown of DFE and AFE type S2SP converters is provided.

As a summary, the main contribution of the paper is:

- Definition of a methodology that determines the optimal SOP and S2SP converter connection voltage that maximizes Q_{cap_max} at P_{rated}, minimizing the impact over costs an efficiency.

To achieve this, the following points are considered as hierarchical contributions:

- Formulation of Q_{cap_max} considering all positive and negative sequence related variables in a joint manner, completing previous individualized approaches.
- Adaption of Q_{cap_max} calculation for SOP applications that are affected by negative sequence at both converter terminals.
- Description of specific modulation constraints affecting Q_{cap_max}, focused on three different modulation techniques and quantified with real data from a 20 MW MV 3L NPC SOP converter.
- Cost and efficiency comparison, based on industrial figures, of S2SP AFE and DFE type converters for different values of SCC.

Based on the above, the paper is structured as follows. Section II presents details for calculating SOP converter Q_{cap_max} limits. Section III provides details of converter modulation techniques affecting Q_{cap_max}. Section IV presents the method for calculating the optimal converter connection voltage in SOP and S2SP applications. It also presents a comparison based on technical and cost figures of DFE and AFE topologies used in S2SP applications. Finally, Section V presents the conclusion of the paper.

II. SOP CONVERTER LIMITS

SOP maximum capacity values are represented using PQV curves where simultaneous P and Q limits are shown in four operation quadrants as a function of the grid voltage V_{net}. All system impedances including transformer and converter design values, as well as control and modulation parameters, must be considered in these curves. An example of the latter is represented in Fig. 4 which represents PQV capacity curves of the 20 MW SOP (22.8 MVA) that is detailed in Table 1. Additionally, Fig. 4 also includes voltage and current phasor diagrams describing the operation of the SOP in each quadrant according to the equivalent circuits and impedance notations shown in Table 2. Note that current and voltage phasor sizes in Fig. 4 are not scaled but drawn only for representation purposes. Equivalent curves for a similar-size commercial SOP converter can be found in [2].

Three PQV curves are represented in Fig. 4 representing SOP's capacity for different grid voltages. Continuous traces of PQV curves represent SOP maximum capacity due to converter current limitation (i.e., thermal limitation) whereas dotted traces show capacity limits imposed by converter voltage saturation.

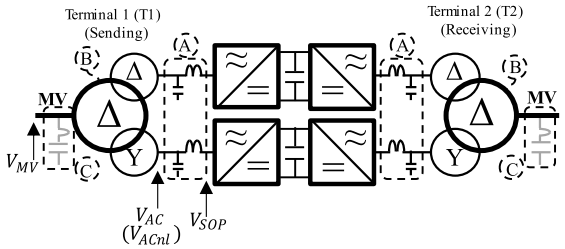
A. CONVERTER MAXIMUM REACTIVE POWER CAPACITY

SOP converter reactive power limits must be addressed with a special focus on maximum Q_{cap} boundaries, defining its relationship with converter voltage saturation and highlighting how is affected by design variables.

An extended view of already introduced two-dimensional PQV capacity curves is represented in Fig. 5-Fig. 7, by means of surface plots showing the evolution of Q_{cap} and Q_{ind} limits within the full range of grid voltage (±10%). Whereas inductive capacity limits show a continuous trend only limited by maximum current values, equivalent capacitive values present a non-linear shape in which voltage saturation

TABLE 1. 20MW (2 × 10MW) SOP data.

DETAILED DIAGRAM



(A): Converter in-built dV/dt filter; used to enhance insulation constraints by reducing converter's PWM voltage rising-edge steepness.

(B): Ddy 22 MVA grid-coupling transformer (U_{sc} = 15%, with two secondary windings connected).

(C): Harmonic filter for power quality purposes (when required).

SOP converter			
Data	Value	Data	Value
Topology	MV 3L NPC	AC voltage (Line-Line RMS)	6.6 kV
$V_{DC\text{-}SOP}$	10.2 kV	AC current (RMS) Short term Overload (2s)	2x 1000 A 1.5 p.u.

INDUSTRIAL CONVERTER MV900 - INGETEAM

10 MW MV-IGBT bidirectional SOP/S2SP converter [26], [33]

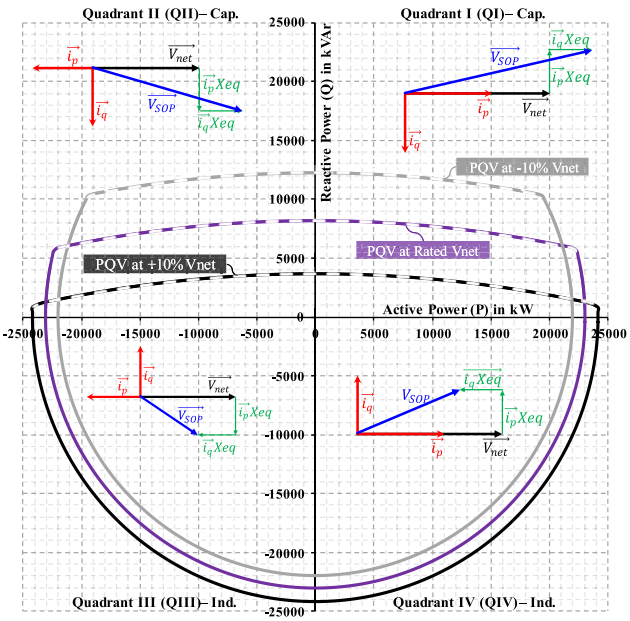
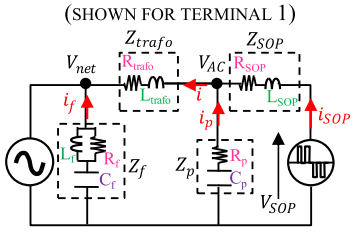
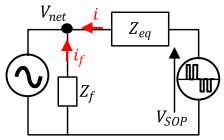


FIGURE 4. 20 MW SOP PQV capacity curves (sign convention as per [34]).

TABLE 2. SOP equivalent diagrams and impedance notations.

SOP IMPEDANCE DIAGRAM (SHOWN FOR TERMINAL 1)	EQUIVALENT SIMPLIFIED CIRCUIT (TERMINAL 1)
	

Where $V_{net} = V_{MV}\,K_{tr} \Longrightarrow K_{tr} = \frac{V_{ACnl}}{V_{MV(rated)}}$

IMPEDANCE NOTATIONS

Z_{SOP} represents the SOP output series impedance and Z_p the parallel branch representing the dV/dt filter circuit. With high-frequency dV/dt filters tuned at >50 kHz, Z_p could be considered as an open-circuit for fundamental frequency hence, $i \cong i_{SOP}$.

Z_{trafo} represents the transformer impedance which, for simplicity, is modeled with its short circuit impedance neglecting the magnetizing branch.

Z_{eq} corresponds to the equivalent impedance, represented in (1). Resistive values (R_{SOP}, R_{trafo}) are significantly lower compared to inductive impedances, thus, are dismissed to permit a simpler, yet valid, representation of formulas and phasor diagrams.

$$Z_{eq} = Z_{SOP} + Z_{trafo} = R_{eq}(\cong 0) + jX_{eq} \Rightarrow Z_{eq} \cong jX_{eq} \quad (1)$$

Z_f corresponds to the harmonic filter, which compared to dV/dt filters is tuned at much lower frequencies (<1 kHz). It means that i_f is not negligible at fundamental frequency and C_f contributes to the total reactive power capacity by supplying a capacitive Q_f that is proportional to the square of V_{net}.

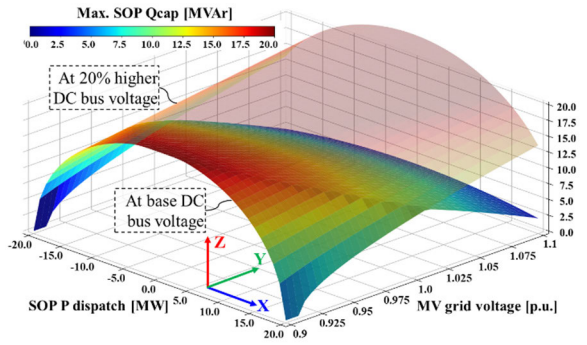


FIGURE 5. 20MW SOP Q_{cap} limits.

forces an almost flat decreasing Q_{cap} slope at increasing grid voltage values (Fig. 5). All values are calculated from base SOP characteristics indicated in Table 1.

Operation points at which the SOP converter reaches voltage saturation are highlighted by the flat surface represented in Fig. 6. The vertical axis (Z axis) represents the modulation index of the SOP converter (M), a magnitude that, indicates the ratio of the fundamental amplitude of the line-to-neutral output voltage at converter terminals (V_{SOP}) to one-half of V_{DC-SOP}.

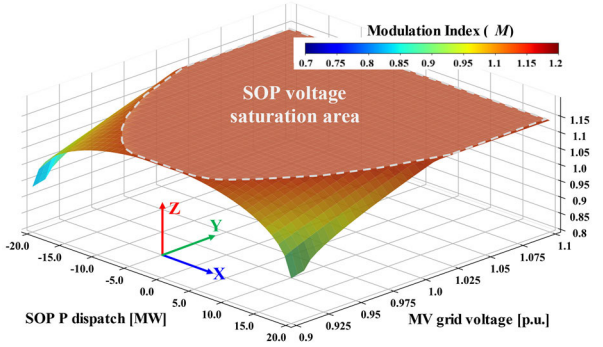


FIGURE 6. 20MW SOP modulation index when dispatched at maximum available Q_{cap} at base V_{DC-SOP}.

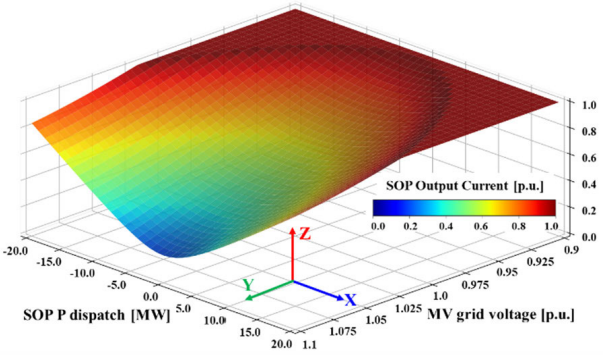


FIGURE 7. 20MW SOP output current when dispatched at maximum available Q_{cap} at base V_{DC-SOP}.

The expression of V_{SOP} linked with M can be found in (2) expressed in line-neutral peak instantaneous magnitude, where V_{DC-SOP} is the maximum DC bus voltage for permanent operation.

$$V_{SOP} = \frac{V_{DC-SOP}}{2} \times M \quad (2)$$

Once voltage saturation is reached, the SOP operates at its maximum capacity even when the output current is still lower than the limit. This is represented in Fig. 7 where, for displaying purposes, Y axis representing MV grid voltage in p.u. has been reverted compared to Fig. 6. Higher values of V_{DC-SOP} would permit to extend Q_{cap} limits until getting similar absolute values as for Q_{ind}, only limited by current (Fig. 5). Nevertheless, converter DC bus voltage is a predefined value, intrinsic to hardware elements that cannot be increased for steady-state operation.

The maximum value of Q_{cap} (Q_{cap_max}) is defined in (3) where the notation of the maximum capacitive reactive current available in a SOP converter is introduced (i_{qCap_max}). For interpreting equations (3)-(7), please refer to the phasor diagram described in Fig. 8 where all variables are represented in p.u.

$$Q = -i_{q(+)}V_{net(+)} \Rightarrow Q_{cap\_max} = -i_{qCap\_max}V_{net(+)} \quad (3)$$

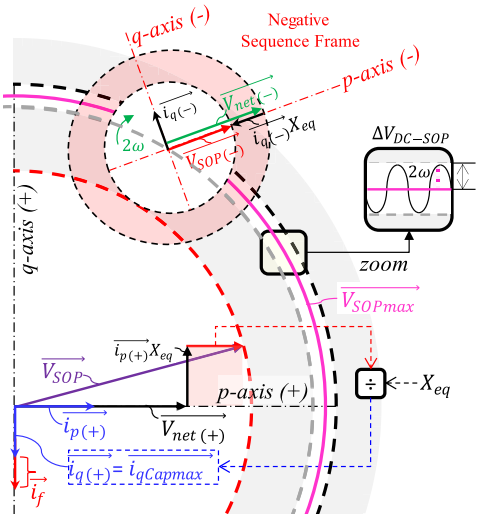


FIGURE 8. Positive and negative sequence frames and variables of SOP.

i_{qCap_max} is represented in (5) as calculated in [31] assuming the sign convention indicated in (4).

$$i_{q(+)} \begin{cases} < 0 \rightarrow (Q > 0) & cap \\ > 0 \rightarrow (Q < 0) & ind \end{cases} \tag{4}$$

$$i_{qCap\_max} = \left| \frac{\sqrt{\left(V_{SOP\_max} - V_{SOP(-)}\right)^2 - \left(X_{eq} i_{p(+)}\right)^2} - V_{net(+)}}{X_{eq}} \right| \tag{5}$$

V_{SOPmax} can be deduced from (1) by substituting M by its maximum limit; a value that depends on modulation techniques and other implementation constraints, as it will be further discussed in section III.

$V_{net(+)}$ and $V_{net(-)}$ represent respectively the amplitude of the positive and negative sequences of V_{net}. Negative sequence voltage in distribution grids is usually low, less than 0.02 p.u. of the rated value according to standards [35].

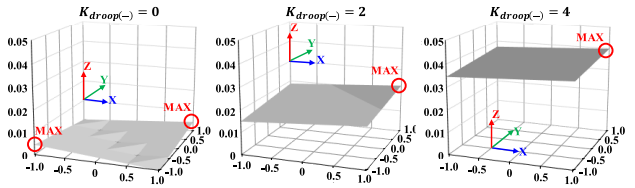
$i_{p(+)}$, $i_{q(+)}$ and $i_{p(-)}$, $i_{q(-)}$ represent respectively the active and reactive current amplitude of the positive and negative sequences of i. According to grid codes, $i_{p(-)}$ must be regulated to zero whereas $i_{q(-)}$ can adopt inductive values, proportional to $V_{net(-)}$ through a droop constant $K_{droop(-)}$ (6). As an example, European reference grid codes [36], [37], define a predetermined set of $K_{droop(-)}$ values to be considered in system integration studies, i.e., 2, 4 or 6.

$$i_{q(-)} = V_{net(-)} K_{droop(-)} \tag{6}$$

Inductive $i_{q(-)}$ flowing through X_{eq} will reduce the amplitude of the negative sequence voltage seen at SOP terminals $V_{SOP(-)}$.

$$V_{SOP(-)} = V_{net(-)} - \left| i_{q(-)} \right| X_{eq} \tag{7}$$

Besides, the existence of $V_{net(-)}$ and $i_{q(-)}$ create oscillating active power flows (P_{c2}, P_{s2}) (8), (9) that generate ripple at



X axis: Q_{SOP} at SOP T1 (-1.0 = Full inductive, 1.0: Full capacitive)
Y axis: Q_{SOP} at SOP T2 (-1.0 = Full inductive, 1.0: Full capacitive)
Z axis: ΔV_{DC-SOP} in p.u. over the rated value V_{DC-SOP}

FIGURE 9. ΔV_{DC-SOP} for different Q_{SOP} at T1 and T2 and different $K_{droop(-)}$.

the SOP DC bus voltage (ΔV_{DC-SOP}) (Fig. 8) [38]. Considering the positive and negative p-q reference frames shown in Fig. 8, $V_{net(+)q}$, $V_{net(-)q}$ and $i_{p(-)}$ are null.

$$P_{c2} = \left(V_{net(-)p} i_{p(+)} + V_{net(-)q} i_{p(+)} + V_{net(+)p} i_{p(-)} + V_{net(+)q} i_{q(-)}\right) \cos 2\omega t \tag{8}$$

$$P_{s2} = \left(V_{net(-)q} i_{p(+)} - V_{net(-)p} i_{q(+)} - V_{net(+)q} i_{p(-)} + V_{net(+)p} i_{q(-)}\right) \sin 2\omega t \tag{9}$$

Compared to single terminal PV converters or back-to-back wind converters in which the machine side terminal is not affected by unbalances, in SOP applications, the contribution to ΔV_{DC-SOP} by negative sequence may come from both converter terminals. Therefore, it is important to quantify the amplitude of this DC ripple and define its impact over Q_{cap_max}.

To simplify this exercise, an initial assumption is made considering that the amplitude of $V_{net(-)}$ seen at both SOP terminals (T1, T2) has the same value. Based on this and considering that $i_{p(+)}$ has the same magnitude but different sign at both terminals (neglecting SOP losses), it can be assumed that the power balance at the SOP DC bus generated by P_{c2} is null (i.e. $P_{c2\_T1} = -P_{c2\_T2}$) therefore, does not contribute to ΔV_{DC-SOP}.

As regards P_{s2}, capacitive $i_{q(+)}$ values will maximize its amplitude as shown in Fig. 9 where the evolution of ΔV_{DC-SOP} generated by P_{s2} is represented for three values of $K_{droop(-)}$. In all cases, $V_{net(-)}$ is considered 0.02 p.u. and P_{SOP} 20MW flowing from T1 to T2. Values in Z-axis represent ΔV_{DC-SOP} in p.u. over the rated value indicated in Table 1 (i.e., 10.2 kV). X and Y axis represent Q_{SOP} at T1 and T2 respectively, indicating operation at full inductive capacity when the axis value is -1.0 and full capacitive when the axis value is 1.0. Intermediate values show partial load operation in inductive (<0) or capacitive (>0) mode.

The formula used to calculate ΔV_{DC-SOP} is shown in (10). The total amplitude of P_{s2} is obtained adding magnitudes calculated at each terminal (P_{s2-T1}, P_{s2-T2}). C_{DC-SOP} is the SOP converter's DC bus capacitance and 2ω represents the frequency of P_{s2}, where ω is the angular frequency of the grid.

$$\Delta V_{DC-SOP} = \frac{|P_{s2-T1} + P_{s2-T2}|}{V_{DC-SOP}} \frac{1}{C_{DC-SOP} 2\omega} \tag{10}$$

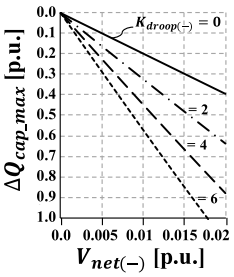


FIGURE 10. Loss of Q_{cap_max} due to grid negative sequence.

Finally, the effect over Q_{cap_max} of all negative sequence-related terms (i.e., $V_{net(-)}$, $i_{q(-)}$ and ΔV_{DC-SOP}) is quantified in Fig. 10. Note that $i_{q(-)}$ is represented by its equivalent term $K_{droop(-)}$ according to (6). The loss of Q_{cap} originated by negative sequence is named ΔQ_{cap_max} and represents in p.u. the reduction of Q_{cap} compared to rated conditions in absence of negative sequence. It can be noticed that for demanding negative sequence injection requirements ($K_{droop(-)} = 6$), the SOP can lose the capability to inject reactive power, even for low negative sequence voltage presence in the network, below 0.02 p.u.

III. MAXIMUM MODULATION INDEX

The maximum modulation index is a key parameter that defines the maximum synthesizable voltage limit of the SOP converter V_{SOP_max}, therefore, has a direct impact over Q_{cap_max}. It is completely influenced by two main constraints that are intrinsic to semiconductor switching characteristics and to how modulation is implemented in digital controllers.

A. SEMICONDUCTOR CONSTRAINTS

Dead time (t_{DT}) is the time applied in two complementary switches of the same branch to avoid a short-circuit in the DC bus. The method for calculating t_{DT} for IGBT type semiconductor modules is defined in [39] and it can be said that the value depends on data from semiconductor and driver datasheets as well as safety factors that are particular to each converter manufacturer.

Once a switching order needs to be effective, the semiconductor that must pass from ON to OFF receives the order instantaneously, while the OFF to ON switch transition is delayed for a t_{DT} time duration. During the time instant when both complementary switches are in OFF state, output voltage is achieved by means of the anti-parallel diodes; thus, output voltage is uncontrolled and completely dependent on the current sign. Due to the switching rise and fall times of commercial IGBT semiconductors and the switched voltage value, MV converters normally need a higher dead time, compared to LV converters. (Table 3). Many techniques to compensate dead time effects have been proposed in the specialized literature [40]. Its compensation is possible when the instantaneous current value is high enough to be measured precisely; however, it may be difficult to carry out an accurate compensation when instantaneous current is close to zero; since knowing the real sign of the current is critical to duly compensate t_{DT}.

TABLE 3. t_{DT} and t_{ON} values in real LV and MV megawatt size converters.

IGBT Reference	Ser*.	t_{ON} [µs]	t_{DT} [µs]	LV/ MV	Converter reference
FF1800R23IE7 [47]	No	5	6	LV	LV800 0.69 kV [33]
MBN1500FH45F [48]	No	10	12.5	MV	MV100 3.3 kV [33]
	Yes	10	20	MV	MV900 6.6 kV [33] [41]

Ser*: Serialized IGBTs in PE phase module, as represented in Fig. 3.

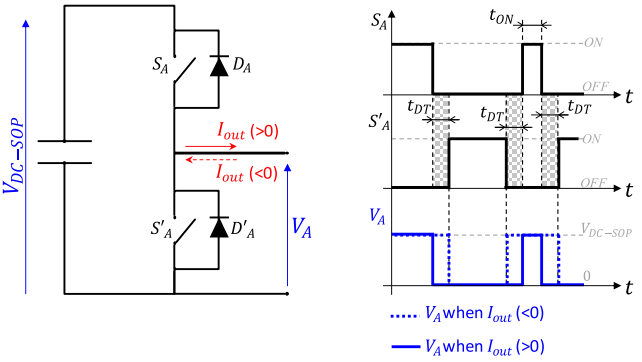


FIGURE 11. Minimum ON time (t_{ON}) and dead times (t_{DT}) in a two-level converter. Dashed (blue) and solid (red) lines represent output voltage depending on output current sign.

Additionally to t_{DT}, semiconductors need a minimum time in ON state (t_{ON}) to ensure that the desired switching transition has been made effective [41]. Nevertheless, beyond typical switching values available on semiconductor datasheets ($t_{d(on)}$, $t_{d(off)}$, t_r, t_f [42], [43]) there is another constraint that affects the minimum value of t_{ON}. The latter corresponds to the short circuit (SC) protection response time required by the semiconductor driver to detect such an anomaly. This value must be lower than the maximum time that a semiconductor can withstand a SC condition (referred as t_p or t_{psc} [42], [43]). Focused on MV IGBTs, as indicated in [42] and [43], this time is typically set to 10μs, a value that is longer than SC reaction time of state-of-the-art drivers for similar IGBTs (<6μs [44]). From a safety point of view, 10μs is typically considered a valid number for t_{ON} in MV IGBTs.

Fig. 11 shows t_{DT} and t_{ON} in a graphical way, represented for a two-level converter for simplicity. The information contained in Fig. 11 can be extrapolated to any multilevel converter that has two complementary switches. As it can be seen, t_{DT} always needs to be applied, while the minimum effective pulse needs to have a duration of t_{ON}. Dashed and solid lines in V_A signal represent the effect of dead times in the output voltage depending on the current sign.

The sum of both times ($t_{DT} + t_{ON}$) expresses the semiconductor time constraint that limits the maximum synthesizable voltage of the converter and, in consequence, Q_{cap_max} limits. Different semiconductor types as well as how they are

connected inside PE modules may imply different $t_{DT} + t_{ON}$ values. As an example, serialization of MV IGBTs in 6.6 kV 3L NPC converters requires additional circuitry at driver level that implies the use of different security margins. Table 3 shows details of t_{DT} and t_{ON} of commercially available megawatt size converters in LV and MV.

B. MODULATION CONSTRAINTS

The modulation technique used and how it is implemented in a real time controller is the key factor in the definition of the maximum synthesizable voltage and is closely related to the previously described semiconductor $t_{DT} + t_{ON}$ constraint.

MV converters usually use Space Vector Modulation (SVM) techniques, as they offer higher degrees of freedom for controlling floating capacitors or DC bus neutral points. MV high power converters tend also to use synchronous modulation methods, as it is the Selective Harmonic Elimination – PWM (SHE–PWM) and all its variants, [45], [46], in order to obtain high output waveform quality with low equivalent switching frequency.

Regarding SVM, asynchronous PWM can show similar behavior in terms of maximum synthesizable voltage; thus, henceforth it will be named as PWM. An important characteristic that needs to be taken into consideration is the updating frequency of the PWM, that is, the ratio of the control task actualization frequency (f_{act}) and the semiconductor switching frequency (f_{sw}).

Previously described $t_{DT} + t_{ON}$ constraint, defining the minimum ON to OFF transition time, must be always fulfilled at the first and the last switching transition of one control actualization period ($t_{act} = 1/f_{act}$). Applied to a three-phase converter, Fig. 12a) shows a generic example of a symmetrically sampled PWM which means that the reference is updated once per switching period ($t_{sw} = 1/f_{sw}$, peak or valley of the carrier). As it can be seen, to fulfill the $t_{DT} + t_{ON}$ constraint, the phase that switches first and last needs to keep the time constraint in one whole t_{act}. This constraint needs to be fulfilled at the first and last switching action of t_{act}. In the case of asymmetrical sampling, the f_{act} is twice the f_{sw} as shown in Fig. 12b). In this case, the reference could be updated at the beginning, in the middle and at the end of t_{sw}, having as drawback a lower output voltage synthesizing capacity.

The fulfillment of such time constraints implies a reduction in the maximum synthesizable voltage that is weighted by Y_{max}, the modulation constraint that adopts values between 0 and 1 and that can be defined as:

$$Y_{max} = 1 - (2 \cdot (t_{DT} + t_{ON}) \cdot f_{act}) \tag{11}$$

Consequently, the modulation constraint Y_{max}, must be included in the expression that defines V_{SOP}.

$$V_{SOP} = \frac{V_{DC-SOP}}{2} \cdot M \cdot Y_{max} \tag{12}$$

For calculating the maximum voltage (V_{SOP_max}) M should be substituted by $M = M_{max} = 2/\sqrt{3}$ if third harmonic injection is considered.

$$V_{SOPmax} = \frac{V_{DC-SOP}}{2} \cdot M_{max} \cdot Y_{max} \tag{15}$$

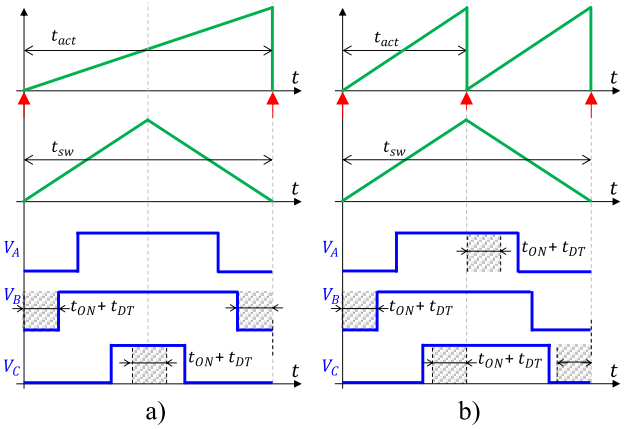


FIGURE 12. a) Symmetrical regular sampling (SRS–PWM), b) Asymmetrical regular sampling (ARS–PWM).

TABLE 4. Maximum modulation index constraint.

ARS—PWM	$Y_{max} = 1 - (4 \cdot (t_{DT} + t_{ON}) \cdot f_{sw})$	(13)
SRS—PWM	$Y_{max} = 1 - (2 \cdot (t_{DT} + t_{ON}) \cdot f_{sw})$	(14)

Substituting the sampling relation of f_{act} and f_{sw} in equation (11), the expressions of Y_{max} for ARS and SRS-PWM modulation techniques are summarized in Table 4. As stated, symmetrical sampled reaches higher output voltage, but will have lower reference updating reaction hence, worse dynamic performance.

On the contrary, synchronous modulation techniques are not synchronized by means of carrier triangular waveforms. This means that $t_{DT} + t_{ON}$ constraint needs to be considered in a different way. One example of this synchronous modulation is SHE–PWM considering all its variants. Those methods respect time constraint by ensuring the right distance between two consecutive switching angles, which is dependent on the output fundamental frequency. In general, synchronous modulation techniques reach higher Y_{max}, usually around 5% higher, as they do not need to switch each switching period as synchronous PWM techniques do. In the case of SHE–PWM, it completely depends on the used angle set. Main drawbacks are slower dynamic response than asynchronous modulations and difficulties to work with high amplitudes of negative sequence voltage.

Based on the characteristics of the 20 MW SOP MV 3L NPC that is considered in this paper, Table 5 shows maximum modulation index Y_{max} values using different modulation techniques and different sampling methods in asynchronous PWM techniques., Time constraint $t_{DT} + t_{ON}$ is considered to be 30 μs as set in [41] and Table 3. Carrier frequency is set to 900 Hz. For SHE–PWM modulation technique, the three-level nine angle set used in [49] is considered.

TABLE 5. Maximum modulation index for equivalent switching frequency of 900 Hz and $t_{DT} + t_{ON} = 30\ \mu s$.

Modulation Type	Modulation Constraint Y_{max}	Maximum Modulation Index $M_{max} \cdot Y_{max}$ Where $M_{max} = 2/\sqrt{3}$
ARS–PWM	0.892	1.03
SRS–PWM	0.946	1.092
SHE–PWM	1.0	1.154

With this number of angles, and considering fundamental frequency of 50 Hz, equivalent switching frequency of 900 Hz is achieved. Among the three modulation techniques, SHE–PWM shows superior performance showing Y_{max} values that are 12% and 5.7% higher than ARS-PWM and SRS-PWM respectively.

To conclude, the combination of semiconductor $t_{DT} + t_{ON}$ time alongside modulation type and actualization frequency, presents a non-negligible impact over Q_{cap_max} through the modulation constraint Y_{max}. Therefore, it must be considered to calculate realistic converter capacity limits.

IV. METHODOLOGY FOR CALCULATING THE OPTIMAL CONNECTION VOLTAGE SOP AND S2SP CONVERTERS

As formulated in section II, connecting converters to lower voltages permits to extend Q_{cap} limits. Nevertheless, this is possible at the cost of higher output current burden in all operation points. Considering this, the no-load voltage at the transformer secondary winding (V_{ACnl}) is the value to be optimized, looking for the highest possible value that permits to meet all application requirements at minimum loss of efficiency and least cost.

A. DEFINITION OF OPTIMAL CONNECTION VOLTAGE IN SOP CONVERTERS

The methodology for optimally sizing V_{ACnl} of bidirectional distribution SOP converters is illustrated in the flow chart that is shown in Fig. 13. It describes a methodology that can be split into three steps.

Firstly, different values of V_{ACnl} and $M \cdot Y_{max}$ are explored to calculate the Q_{cap_max} value that can be expected for each combination of both variables. Results are represented in a 2D surface where the absolute maximum values of Q_{cap_max} are located at the top edge that defines the boundary between current and voltage saturation limits of the SOP converter (hereinafter, referred as Limit Edge) (Fig. 14-a). It is observed that Q_{cap_max} values keep reducing steadily in the voltage saturation area until adopting negative values beyond the capacitive-inductive boundary line. Beyond this boundary, the sign of $i_{q(+)}$ must be inverted and the SOP can only operate in inductive mode.

Secondly, the intersection of the Limit Edge with the maximum modulation index limit ($M_{max} \cdot Y_{max}$) has to be calculated to obtain the optimal V_{ACnl} value at which the highest Q_{cap_max} is attained at minimum current needs (Fig. 14-b). As indicated in Table 5, $M_{max} \cdot Y_{max}$ values differ among

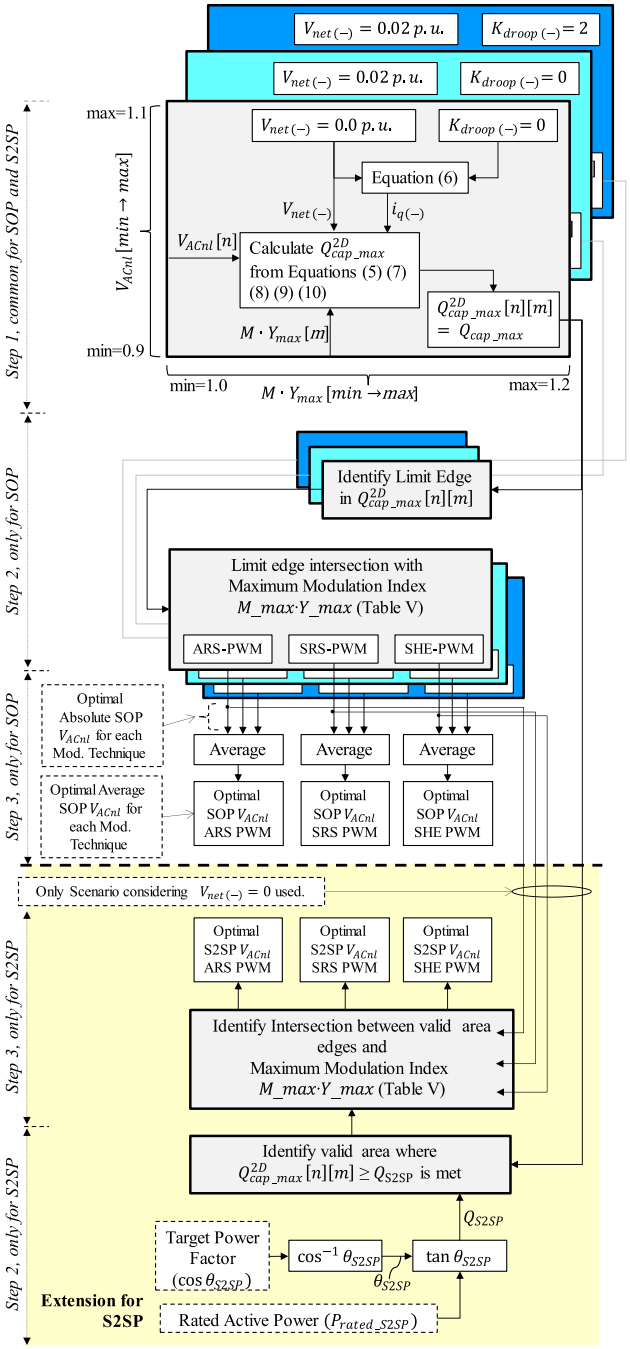


FIGURE 13. Flow chart of SOP optimal V_{ACnl} calculation methodology showing the extension for S2SP applications.

modulation techniques used therefore, so do the optimal V_{ACnl} values calculated from them.

Finally, the influence of negative sequence is analyzed iterating the previous two steps for different values of $V_{net(-)}$ and $i_{q(-)}$. Whereas $V_{net(-)}$ is set to its maximum allowed value of 0.02 p.u., $i_{q(-)}$ is obtained from (6) considering different values of $K_{droop(-)}$ (0 and 2). By doing so, equivalent Q_{cap_max} results are obtained for different combinations of $V_{net(-)}$ and $i_{q(-)}$ (represented in Fig. 15 and Fig. 16 respectively). Optimal V_{ACnl} values for these new grid scenarios

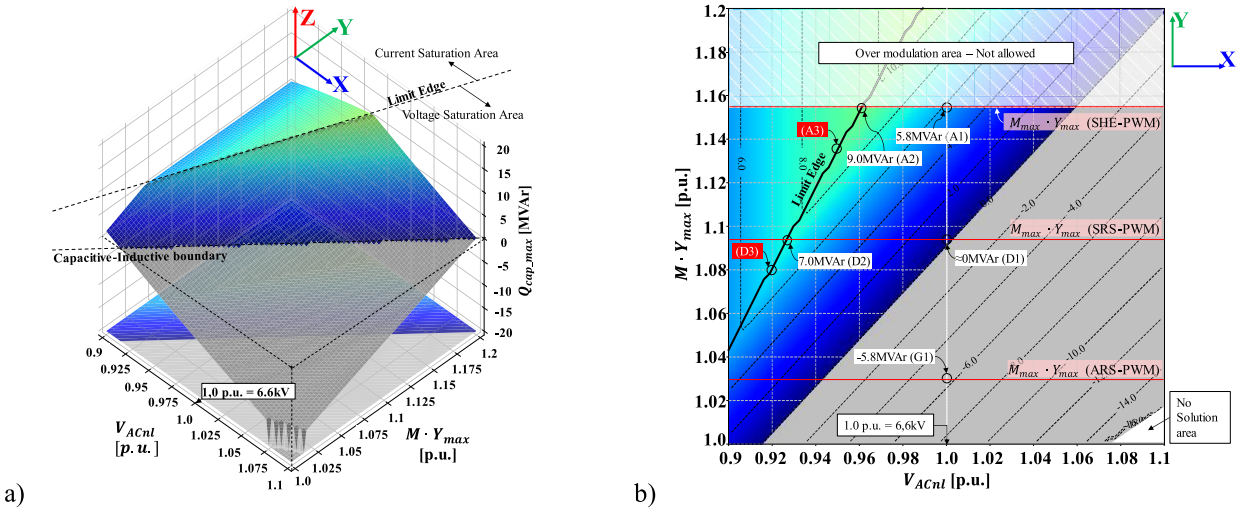


FIGURE 14. Max Q_{cap_max} edge at $V_{net(-)\%} = 0\%$ (Grid Scenario 1 – rated conditions).

can be processed as described in the second step. At this point, the procedure arrives to the final decision point where all calculated V_{ACnl} values must converge into a single value selected for manufacturing the real SOP transformer. In such cases, a trade-off value is calculated as an average of all the previous.

Results obtained from applying the proposed methodology to the 20 MW SOP converter introduced in Table 1 are shown in Fig. 14 to Fig. 16 highlighted with individual markers. Besides, most relevant details on these specific points are summarized in Table 6. Note that the SOP converter is dispatched at rated active power, i.e., 20 MW, to attain the maximum limits of the capacity curve.

Table 6 quantifies Q_{cap_max} values corresponding to each of the three scenarios considered in the exercise. It compares results attained on the one hand with base converter voltages and on the other hand, with optimized V_{ACnl} values resulting from the proposed method.

Base converter voltages correspond to standard values used for designing a converter brand. The latter typically correspond to industrial standards, e.g., 3.3 kV or 6.6 kV as most typical values. In the case of the 20MV MV 3L NPC converter considered in this paper it belongs to the MV900 converter family designed for 6.6 kV (6.6 kV is considered as 1.0 p.u.).

Optimized voltage values are represented using two different notations: Optimal Absolute V_{ACnl} and Optimal Average V_{ACnl}. Highest Q_{cap_max} values are attained at Optimal Absolute V_{ACnl} voltages that represent the intersection between the Limit Edge and the $M_{max}Y_{max}$ limit that corresponds to each modulation technique. From these values, the Optimal Average V_{ACnl} is calculated representing a trade-off of Optimal Absolute values among the three grid scenarios. The Optimal Average V_{ACnl} corresponds to the connection voltage value that would be used to build the physical transformers used to couple the SOP with the grid.

Evaluating results based on optimal Average V_{ACnl}, considering SHE-PWM modulation, the proposed method has allowed to determine connection voltages that increase Q_{cap_max} by 46% from values attained at base voltage. A similar trend has been identified in SRS-PWM with an absolute gain of 6.5MVAr from a null Q_{cap_max} capacity displayed at base voltage. When it comes to ARS-PWM, the same trend is also identified in the results, nevertheless values are much lower than in previously assessed modulation techniques and remain out of the plotting area. Therefore, compared to SHE-PWM and SRS-PWM, ARS-PWM can be considered an unsuitable modulation technique for applications that require to maximize capacitive reactive power limits.

In overall, the proposed voltage optimization method has implied a reduction of voltage values that, in the worst case, has determined an average V_{ACnl} value that is 0.08 p.u. lower than the base. Find next a detailed comparison that permits to address technical and cost-related differences observed from the implementation of the proposed method on the 20 MVA SOP converter.

The comparison considers, on the one hand, a base design in which the connection voltage is not optimized but imposed to the predetermined 6.6 kV. Then, it is compared with an equivalent design built on same core components but having optimized its connection voltage with the proposed method. The comparison will focus on key performance metrics from Table 6 as well as on costs, with a twofold assessment on the latter based on capital and operational expenditures (CAPEX and OPEX, respectively). The comparative study will consider rated conditions assumed in grid scenario 1 referred in Table 6 and will focus on SHE-PWM and SRS-PWM modulations as most suitable techniques.

Detailed results are shown in Fig. 18 considering four case-studies: A) Base design SRS-PWM, B) Optimized design SRS-PWM, C) Base design SHE-PWM and D) Optimized

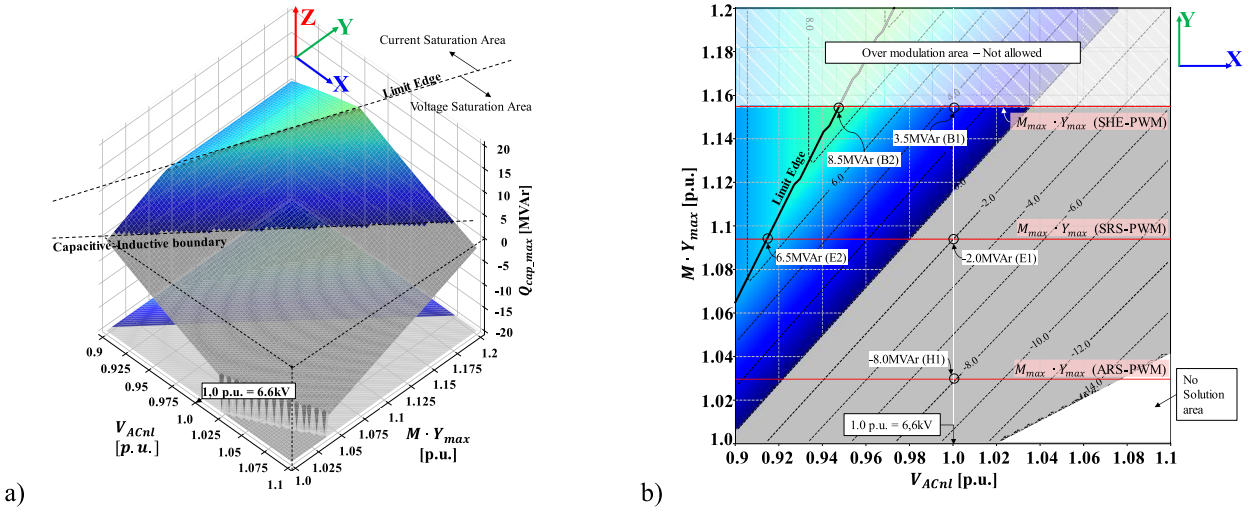


FIGURE 15. Max Q_{cap_max} edge at $V_{net(-)\%} = 2\%$ and $K_{droop(-)} = 0$ (Grid Scenario 2).

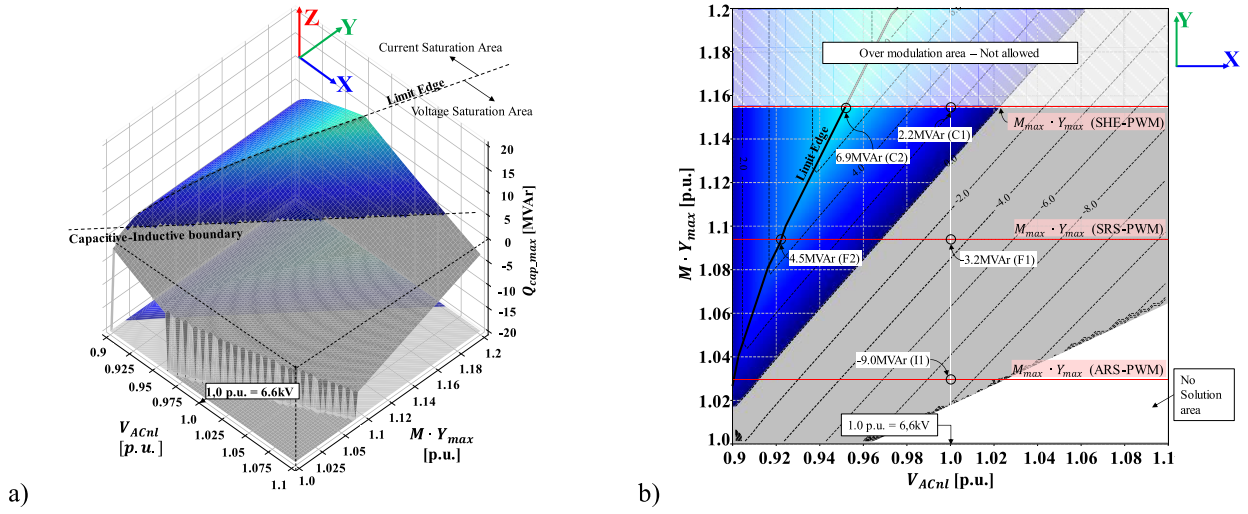


FIGURE 16. Max Q_{cap_max} edge at $V_{net(-)\%} = 2\%$ and $K_{droop(-)} = 2$ (Grid Scenario 3).

design SHE-PWM. Firstly, Fig. 18-a and Fig. 18-b show how Q_{cap_max} and overall efficiency vary between base and optimized solutions. To complete the information given on key performance metrics, Fig. 18-c quantifies how the converter maximum inductive reactive power Q_{ind_max} is affected by the optimized connection voltage.

Maximum values of Q_{cap_max} and Q_{ind_max} are jointly represented in Fig. 18-d using PQ capacity curves that compare base and optimized results for the SRS-PWM modulation technique (case study A and B, respectively). With the proposed method, capacitive and inductive limits are homogenized showing PQ curves that cover an area delimited by the same Q_{cap_max} and Q_{ind_max} measured over the evaluation axis that represents ± 20 MW. This area is referred as the symmetrical PQ area. The convergence of both capacitive and inductive limits is achieved because the optimized V_{ACnl} is determined by the intersection of the maximum modulation index limit ($M_{max} \cdot Y_{max}$) with the limit edge where current and voltage saturation limits converge. Compared to this, the PQ curve of the base design, prior to the optimization, showed an uneven distribution of Q_{ind_max} and Q_{cap_max}, the latter being close to zero. Similar result trends are observed for the SHE-PWM modulation technique. Finally, Fig. 18-e and Fig. 18-f quantify CAPEX and OPEX variations among compared options.

CAPEX values, representing the cost of acquiring the equipment, are only modified by the increased permanent current sizing of the SOP transformers in the optimized case-studies. The transformer current increase is proportional to the difference between the base voltage 6.6 kV and the

TABLE 6. Optimal SOP V_{ACnl} calculation results for different grid scenarios.

Mod. Technique	References	Grid Scenario 1 (Fig. 14b) (rated – no Neg. Sequence) $V_{net(-)\%}$=0%			Grid Scenario 2 (Fig. 15b) $V_{net(-)\%}$=2% / $K_{droop(-)}$=0		Grid Scenario 3 (Fig. 16b) $V_{net(-)\%}$=2% / $K_{droop(-)}$=2	
		Base V_{ACnl}	Optimal Absolute V_{ACnl}	Optimal Average V_{ACnl}	Base V_{ACnl}	Optimal Absolute V_{ACnl}	Base V_{ACnl}	Optimal Absolute V_{ACnl}
SHE-PWM	Marker point	A1	A2	A3	B1	B2	C1	C2
	V_{ACnl} [kV]/[p.u.]	6.6 / 1.0	6.34 / 0.96	6.28 / 0.951	6.6 / 1.0	6.25 / 0.948	6.6 / 1.0	6.27 / 0.95
	Q_{cap_max} [MVAr]	5.8	9.0 (reached at $M \cdot Y_{max}$=1.154)	8.5 (reached at $M \cdot Y_{max}$=1.136)	3.5	8.5 (reached at $M \cdot Y_{max}$=1.154)	2.2	6.9 (reached at $M \cdot Y_{max}$=1.154)
	Efficiency loss (**) [%]	N/A	0.061	0.077	Efficiency is only assessed in Scenario 1			
SRS-PWM	Marker point	D1	D2	D3	E1	E2	F1	F2
	V_{ACnl} [kV]/[p.u.]	6.6 / 1.0	6.12 / 0.927	6.07 / 0.92	6.6 / 1.0	6.02 / 0.912	6.6 / 1.0	6.08 / 0.921
	Q_{cap_max} [MVAr]	0.0	7.0 (reached at $M \cdot Y_{max}$=1.092)	6.5 (reached at $M \cdot Y_{max}$=1.08)	-2.0	6.5 (reached at $M \cdot Y_{max}$=1.092)	-3.2	4.5 (reached at $M \cdot Y_{max}$=1.092)
	Efficiency loss (**) [%]	N/A	0.12	0.134	Efficiency is only assessed in Scenario 1			
ARS-PWM	Marker point	G1	(*)	(*)	H1	(*)	I1	(*)
	V_{ACnl} [kV]/[p.u.]	6.6 / 1.0	(*)	(*)	6.6 / 1.0	(*)	6.6 / 1.0	(*)
	Q_{cap_max} [MVAr]	-5.8	(*)	(*)	-8.0	(*)	-9.0	(*)
	Efficiency loss (**) [%]	N/A	(*)	(*)	Efficiency is only assessed in Scenario 1			

(*): Not displayed. The referred market point remains out of the plotting area.
(**): Efficiency data is provided as the difference in p.u. (efficiency loss) compared to the losses calculated in scenario 1, considering base V_{ACnl} (i.e., 6.6kV) and a SOP converter dispatch of 20MW at unity power factor.

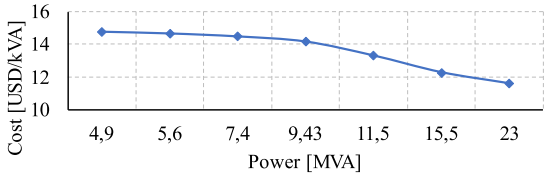


FIGURE 17. State-of-the-art industrial power transformers cost trend.

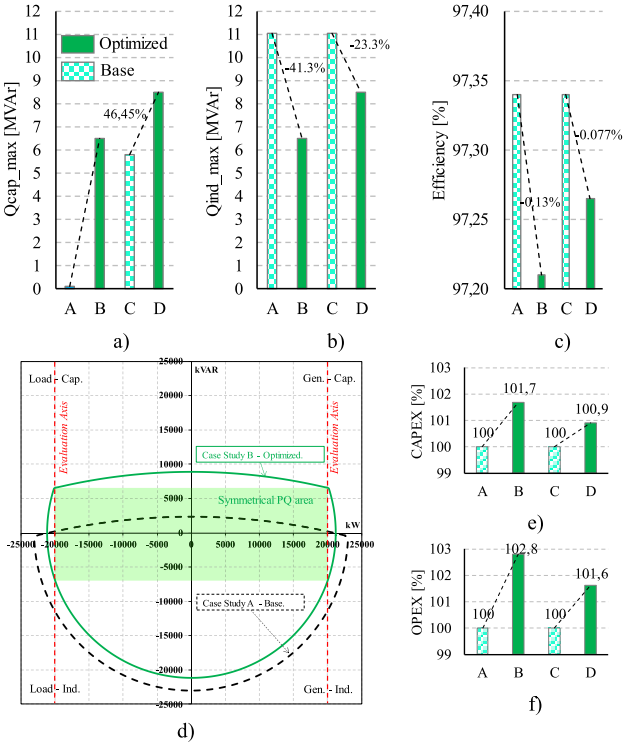


FIGURE 18. Base and Optimized SOP design key performance metrics and cost comparison a) Q_{cap_max}, b) Q_{ind_max}, c) Overall Efficiency, d) PQ curves, e) CAPEX, f) OPEX.

Optimal Average V_{ACnl} defined in Table 6 for each case. The SOP converter remains the same in all case-study scenarios. Based on the above, considering state-of-the-art industrial transformers prices shown in Fig. 17 and assuming that in MV SOP applications, transformers account for 25% of the total costs [7], a maximum CAPEX increase of 1.7% is estimated in the worst case (Fig. 18-e).

OPEX values representing the sum of costs related to the operation of the equipment over its predicted life are affected by the difference in losses (i.e., efficiency) among case studies. Refer to Appendix A to address the method and parameters that have been used for calculating OPEX values. Based on the latter and efficiency differences shown in Fig. 18-c, a maximum OPEX increase of 2.8%, compared to base case-studies, is estimated for the worst case (Fig. 18-f).

B. DEFINITION OF OPTIMAL VESSEL CONNECTION VOLTAGE IN S2SP CONVERTERS

In a similar way as in SOP applications, the V_{ACnl} connection voltage at vessel terminals must be accurately calculated to allow for an optimal integration of S2SP converters. Compared to this, connection voltage at the grid terminal is usually defined to industrial standards (e.g., 6.6 kV for AFE type

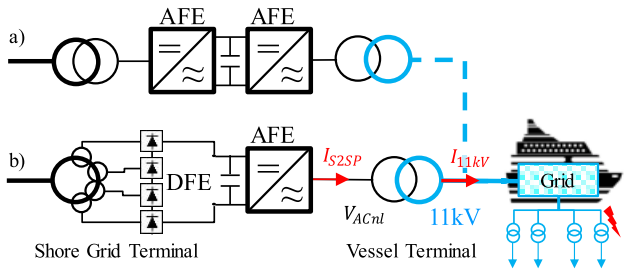


FIGURE 19. S2SP converter types a) AFE type b) DFE type - current notations.

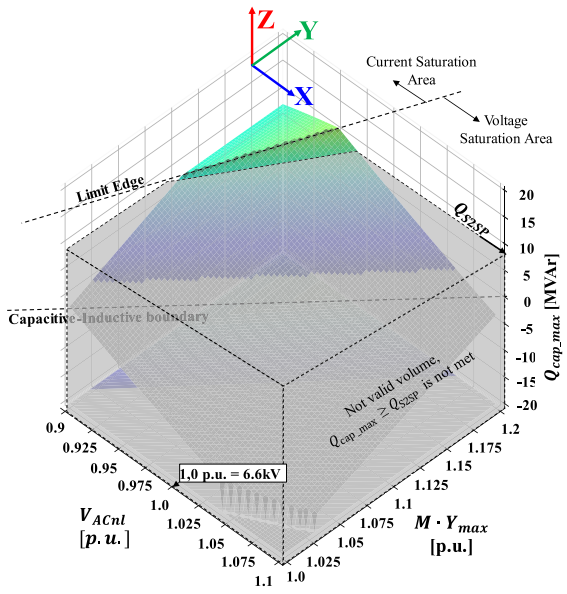


FIGURE 20. AFE type S2SP converter Q_{cap_max} limits.

converters or 1.95 kV for equivalent series-connected 24 pulse DFE converters, Fig. 19). In any case, this topic remains out of the scope of this paper.

To calculate the optimal V_{ACnl} at vessel terminals, the calculation method described in the flow chart of Fig. 13 must be followed. As it can be seen, the first step of the method is common for SOP and S2SP whereas the two remaining correspond to a variant adapted to S2SP applications. In the second step, the valid area that meets minimum reactive power requirements at vessel side (Q_{S2SP}) is identified. The minimum value of Q_{S2SP} is calculated considering active power and power factor requirements from vessel loads. The third and last step corresponds to the identification of the intersection point between the valid area edge and the $M_{max} \cdot Y_{max}$ limit of each modulation technique considered. This intersection point will correspond to the optimal V_{ACnl} at vessel connection point. Fig. 20 and Fig. 21 permit to identify graphically the meaning of the valid area that meets Q_{S2SP} requirements, as well as the intersection point that defines the optimal V_{ACnl}.

To accurately implement previous steps in a S2SP application, some application-specific details must be considered:

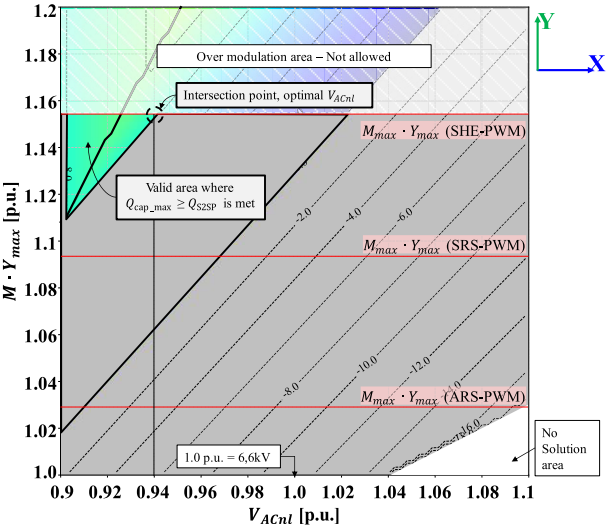


FIGURE 21. AFE type S2SP converter Q_{cap_max} limits – detail of valid area meeting Q_{S2SP} requirements and optimal V_{ACnl}.

- S2SP applications that use DFE grid interfaced converters will operate at DC bus voltages that are ≈0.95 p.u. of equivalent size AFE converters. This value is further reduced to ≈0.85 p.u. when the grid voltage falls to 0.9p.u. which typically corresponds to the lowest permissible limit in distribution networks. The latter represents the worst-case scenario to be considered for sizing purposes.
- The influence of grid negative sequence in multi-pulse DFE topologies can be considered as negligible; less than 0.5% of the average rectified voltage for $V_{net(-)} = 0.02$ p.u. according to [50]. Therefore, in DFE type converters, $V_{net(-)}$ can be considered as zero in the method for calculating the optimal vessel connection voltage, simplifying the overall process.
- Considering SCC requirements imposed at vessel side connection terminals (I_{11kV}), the higher V_{ACnl}, the lower current requirements at S2SP converter terminals (I_{S2SP}) as it can be easily deduced from (16) considering notations from Fig. 19. From an application perspective, SCC values ranging between 1.5p.u. and 2p.u. (16 MVA base) for time durations that last up to 2s can be considered in cruise-vessel projects. To meet such requirements at minimum cost, short-term current overload capability of S2SP converters must be explored. A typical value for water-cooled industrial MV converters is 1.5 p.u. as indicated in Table 1.

Based on the above, the optimal V_{ACnl} calculation method is applied to a typical cruise vessel S2SP practical example, described in Table 7.

Results are shown in Fig. 20 and Fig. 21, displayed only for an AFE type converter to permit a comparison with previously assessed SOP applications. As it can be observed, S2SP applications confront strict requirements that curtail the range of possible V_{ACnl} values to a very reduced area, as it is

TABLE 7. 16MVA cruise vessel S2SP practical example.

Requirement	Value	Requirement	Value
Active Power	13.5 MW	SCC at 11kV (I_{11kV}) (duration: 2s)	1500 A (1.78p.u.)
Power Factor (cap.) Reactive Power (Q_{S2SP})	0.85 p.u. 8.36 MVAr	Grid voltage at MV	0.9 p.u.
Vessel Frequency	60 Hz	Vessel voltage at 11kV	1.035 p.u.

TABLE 8. Optimal S2SP vessel side V_{ACnl} calculation results.

Modulation technique	Topology	Vessel side V_{ACnl} [p.u./kV]	Vessel side PE current sizing kA
SHE-PWM	DFE	0.81 / 5.346	2.06
	AFE	0.94 / 6.204	1.77
SRS-PWM	DFE	0.77 / 5.082	2.164
	AFE	0.9 / 5.94	1.851
ARS-PWM	DFE	0.72 / 4.752	2.314
	AFE	0.85 / 5.61	1.96

shown in Fig. 21. Considering the 20 MW type converter previously used in SOP studies (i.e., AFE type), only SHE-PWM modulation permits to meet S2SP requirements specified in Table 7. The use of ARS-PWM and SRS-PWM modulations requires further reduction of V_{ACnl} and subsequent increase of vessel side converter PE current sizing. This effect is even more pronounced in DFE type S2SP converters due to the impact entailed by a $V_{DC-S2SP}$ value that is 0.15 p.u. lower than in AFE type designs. A summary of results for AFE and DFE type converters as well as three evaluated modulation techniques is presented in Table 8.

$$I_{S2SP} = \frac{11kV}{V_{ACnl}} \cdot I_{11kV} \tag{16}$$

Vessel side PE current sizing values shown in Table 8 have been obtained considering: the optimal V_{ACnl} calculated for each case, the SCC value for I_{11kV} indicated in Table 7 and a current overloading capacity of 1.5p.u. (according to Table 1).

Higher current sizing needs are directly mirrored into higher costs of the overall solution. To quantify the latter and highlight differences between AFE and DFE type S2SP converters, electrical values shown in Table 8 have been capitalized and presented in Fig. 22 where DFE CAPEX (solid trace) and AFE CAPEX (dashed trace) are compared as a function of the required SCC value. This information is completed in Fig. 23 where a cost breakdown of main components is represented also as a function of the required SCC (only represented for SHE-PWM). Both graphs permit to address the cost impact derived from higher current sizing requirements of vessel side PE. More cost effective DFE PE options may cease to be so beyond a certain value of SCC, due to the overrating required at vessel side PE. This limit is highlighted for different modulation techniques by means of the so-called DFE/FE CAPEX boundary lines, represented in Fig. 22.

Finally, efficiency values of all options summarized in Table 8 are shown in Fig. 24-a, calculated for different active

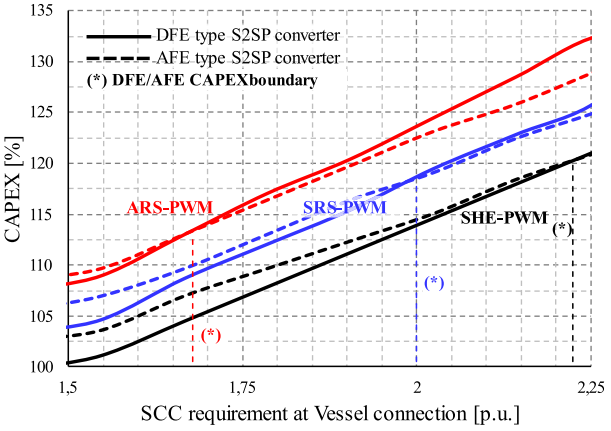


FIGURE 22. CAPEX comparison of S2SP – DFE and AFE topologies and different modulation techniques.

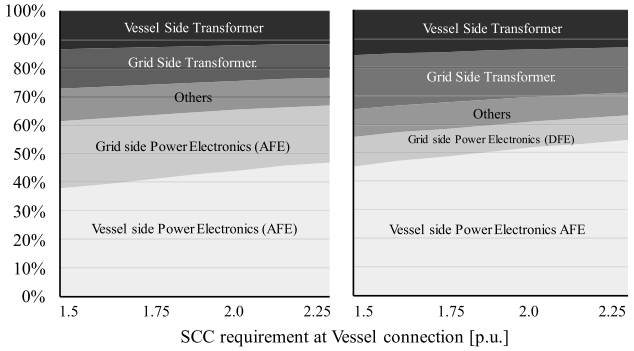


FIGURE 23. Cost breakdown between AFE (left) and DFE (right) type S2SP converter solutions – Obtained considering SHE-PWM modulation.

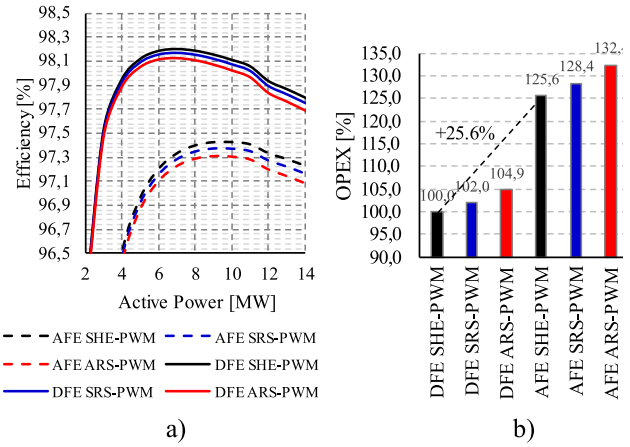


FIGURE 24. Efficiency a) and OPEX b) comparison of S2SP – DFE and AFE topologies and different modulation techniques.

power values. Note that efficiency calculations include losses of converters' PE and passive components as well as losses of both, grid and vessel side connection transformers. In the same manner as it has been done for SOP applications, intrinsic losses have been capitalized into OPEX figures. Considering this, Fig. 24-b shows that AFE designs account

for OPEX values that are >25% higher than in DFE. Note that the method used for calculating OPEX values is the same as the one used in SOP applications (refer to Appendix A).

V. CONCLUSION

This paper presents a methodology for calculating the optimal transformer-converter connection voltage of SOP and S2SP applications that permits to maximize Q_{cap} limits at minimal impact over costs and efficiency.

Firstly, the paper formulates in one single document all positive and negative sequence related expressions that have an influence over the Q_{cap_max} in converters. By doing so, it completes partial approaches identified in previous works. Secondly, the paper contributes with a novelty, particularized for SOP applications, analyzing the influence over Q_{cap_max} of the negative sequence affecting multiple converter terminals. Finally, it describes in detail how converter modulation limits are affected by semiconductor characteristics and quantifies its impact over Q_{cap_max} in industrially available converters. Related to this, three different modulation techniques are analyzed using data from a real 20 MW MV 3L NPC converter to support all calculations.

Based on the above, a method for calculating the optimal transformer-converter connection voltage is proposed. Results obtained from the application of this method to the specific SOP and S2SP applications defined in the paper show the following key findings:

- SOP converters Q_{cap_max} is maximized showing increments that range on >45% with efficiency reduction values that are lower than 0.15%. The impact on costs, combining CAPEX and OPEX values, show an increase of 4.5% in the worst case studied.
- SOP converters PQ capacity curves acquire a symmetrical shape showing similar values of Q_{cap_max} and Q_{ind_max} at rated P.
- Regarding S2SP applications, 3L MV-NPC topologies in either AFE or DFE variants, require the definition of an optimized connection voltage at vessel side. DFE topologies are most restrictive in this sense.
- SHE-PWM modulation technique has proved to be the most suitable for both SOP and S2SP applications.

To finalize, find next possible future research lines that could derive from the study that has been presented in the paper:

- The study on modulations has been focused on three state-of-the-art techniques. Nevertheless, it could be extended to other modulation types to widen the comparative study. The proposed method permits to compare results with any modulation technique, using the standard parameters that have been defined for that.
- The paper uses explicit data from real converters built upon silicon type (Si) semiconductors. The state-of-the-art offers other options (e.g., Silicon Carbide, SiC) for being used in equivalent converters.
- SOP applications could potentially be used in LV distribution grids to overcome grid congestion and voltage profile issues. The proposed method could be used in this particular use case and contribute to an optimal integration of SOP applications into LV grids.

TABLE 9. Cost Factors used in the calculation of OPEX.

Cost Factor	Description	Value (*)	Units
SC	Avoided cost of system capacity	71,4	$/kW-yr
EC	Avoided cost of energy	8,43	¢/kWh-yr
HPY	Hours per year energized	8760	h
FCR	Fixed charge rate	17	%
LM	Loss multiplier	1,1	pu
RF	Peak responsibility factor	0,9	pu
LSF	Transformer loss factor	0,15	pu
PL_I^2	Levelized equivalent annual peak load^2	1,1574	pu

(*): Data obtained from Tables 6-7 in [51] as trade-off values to carry out an OPEX comparative.

APPENDIX A
CALCULATION OF OPERATIONAL EXPENSES

The calculation of the operational expenses (OPEX) used in the paper is based on the formulation of the Total Owning Cost (TOC) defined in the IEEE guide for the evaluation of losses in distribution, power transformers and reactors [51].

$$TOC = CAPEX + OPEX \tag{17}$$

OPEX can be split into several terms, as described next:

$$OPEX = A \times NL + B \times LL + B_{aux} \times L_{aux} \tag{18}$$

where:

A: is the equivalent first cost of no-load losses, per watt.

NL: is the no-load loss of the equipment (watts).

B: is the equivalent first cost of load losses, per watt.

LL: is the load loss of the equipment (watts).

B_{aux} : is the equivalent first cost of auxiliary losses, per watt.

L_{aux} : is the auxiliary loss (watts).

It is worth mentioning that [51] does not address losses related to power electronics converters. To the authors best knowledge, literature does not offer an equivalent guideline for capitalizing power converters' losses. Nevertheless, converter losses can be split into the same terms that are used in [51]: no-load, load and auxiliaries losses. Moreover, they are intrinsically linked, meaning that converter and transformers, are both subject to the same load. Based on this, losses from converters and transformers could be grouped into the aforementioned terms and be jointly used in the capitalization formulas defined in [51].

It is not the aim of this paper to reproduce the formulas related to each one of the terms described above, considering that they are defined and described in detail in [51]. However, Table 9 defines the parameters (i.e., cost factors) used for calculating OPEX values declared in the paper. OPEX values are presented in this paper in percent units, considering the

most efficient solution (i.e., the one showing least losses) as the comparing reference, rated to 100%. Then, OPEX values of the rest of solutions are presented with the corresponding percent value over the reference, permitting a clear comparison of OPEX cost increment among solutions.

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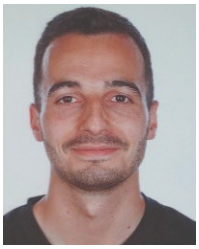

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