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Modulation and LCR Filter Optimum Design Procedure for Medium Voltage Adjustable Speed Drives

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«Drive», «Passive filter», «Modulation Strategy», «Multilevel converters», «Pulse Width Modulation (PWM)», « Pulsed power converter», «Voltage Source Converter (VSC)»,

Abstract

This paper proposes a systematic procedure in order to make an optimal comparison/selection of modulation techniques and output LCR filter components for adjustable speed drives. Useful indicators are identified, which may help the designer to a global solution, optimizing the modulation-filter selection. The procedure is applied into the design of a real 6.6 kV equipment.

Introduction

As power electronics are becoming a more mature technology, their usage is clearly increasing for several kind of applications. Medium Voltage (MV) drives are a highly demanded application for the power electronics market [1]. As the power required to the power electronics gets larger, a clear trend is to augment the output voltage of the converters in order to reduce the power losses derived by the high currents. This voltage limit to be risen is limited by the available semiconductor technology, both, in current and voltage [2]. Nowadays, applications up to 6.6 kV are quite extended [1], [3]. Focusing on this voltage range, quadratic loads like centrifugal fans or pumps are in high demand.

Furthermore, even multilevel converter topologies are normally used to reach this voltage range to enhance the output voltage total harmonic distortion (THD), output filters (LCR) connected after the inverter and before the machine need to be in many times included. Added to this, these filters are sometimes required with the aim of ensuring the insulation of the machine, depending on the voltage steps given in the inverter output voltage.

Additionally, if drive applications oriented to quadratic loads are analyzed, semiconductor current constraint may lead to the combination of different modulation techniques as the output frequency demanded by the load is increased [4], [5]. Two main modulations are normally used, by combination of which output THD can be enhanced without reaching the thermal limit [6]:

- Space Vector Modulation (SVM). This technique is based on the combination of different voltage vectors in one modulation period, so as to accomplish the mean value of the voltage reference asked by the control [7].
- Selective Harmonic Elimination (SHE). This alternative is based on the off-line calculation of switching angles of each phase, in order to eliminate undesired harmonics and control the fundamental voltage value. There are different alternatives depending on the number of calculated angles for the first 90 ° of the fundamental period [8].

The combination of these modulation techniques is essential to be taken into account when designing the converter output filter. In fact, [4] and [5] talk about the modulation combination in order to reach

output frequencies in drives without exceeding the thermal limit. However, none of them takes clearly into account the combination of modulations so as to design the filter at the same time. The proper filter design results on a very important task, in order to achieve the desired THD output values and to avoid possible resonances which may be originated.

This paper proposes a systematic procedure to compare and select different modulation technique alternatives, taking into account the filter design. With this aim, different indicators are proposed which help the designer to select the most optimal modulation for each output frequency range, depending on the demanded load profile. Once the modulation strategy is fixed, the procedure serves different indicators in order to select LCR filter components. With this indicators, the designer can select some restrictions and analyze the possible LCR combinations that meet with the objective. Finally, system behavior is re-evaluated with the whole solution. Taking modulation-filter into a systematic design is the main contribution of this paper.



Fig. 1: 6.6 kV-1.5 MVA drive scheme based on 3L-NPC converter.

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With the purpose of illustrating the applicability of this procedure, it is applied in the design of a converter of the data served in Table I, which can be an example of a Medium Voltage drive. Open loop V/f control is considered to drive a quadratic load. As it can be seen, a 6.6 kV and 5 line-to-line voltage drive is going to be designed by means of this procedure, Fig. 1. Hence, modulation and filter design will be selected.

Table I. Characteristics of the converter to be designed	
Maximum Output Power	1.35 MVA
Maximum Output Voltage	6.6 kV
Maximum Output Frequency	50 Hz
Number of Line-to-line Voltage Levels	5
DC-Bus Voltage (Vpc)	10 kV

Proposed comparison and filter design procedure

In order to choose the optimum modulation combination and to minimize the output filter performance, a comparison and design procedure is proposed. In a first step, the performance of several SVM and SHE modulations is compared in terms of semiconductors thermal constraints and output voltage quality. Afterwards, based on resultant modulations, filter components are selected. Main inputs and outputs of the procedure are summarized in Fig. 2.



Fig. 2: Modulation selection and filter design procedure layout, defining inputs and outputs.

Inputs

As it can be seen in Fig. 2, five main inputs can be distinguished:

- **Semiconductors**. Used semiconductors need to be characterized in order to thermally evaluate the layout.
- **Cooling**. Apart from the semiconductors, the cooling system behavior needs to be known for thermal calculation purposes.
- Load profile. The load needs to be defined in order to adapt the modulation selection and the filter design to it.
- **Topology**. Used inverter topology marks voltage and current available values. Added to this, in order to calculate the filter, the number of levels sets the voltage step, which creates current ripple.
- **Modulation**. The way the orders are given to semiconductors is determinant. This is the parameter it is going to be analyzed (and changed as input) in this paper.

Once all of them are defined, the modulation performance can be evaluated, by means of the proposed indicators. If one of the inputs is changed, all the calculations can be carried out again, obtaining another system behavior for other inputs. In this case, after evaluating all the modulation types, a clear modulation strategy can be defined. After this, filter design is accomplished using the modulation pattern as input.

Modulation scheme selection

Current Thermal Restrictions

Each modulation strategy implies the switching of the semiconductors of the converter, which frequency may vary depending on the output frequency. When Pulse Width Modulation (PWM) or SVM is applied, the switching frequency of the semiconductors remains constant regardless of the output frequency. On the contrary, if a SHE modulation is applied, as the number of switchings during an output fundamental period remains constant, the switching frequency of the semiconductors varies in accordance with the output frequency, as depicts Fig. 3.



Fig. 3: Switching frequency evolution for different modulation techniques, depending on the output frequency.



Fig. 4: Output current limit of the analyzed converter, depending on the switching frequency.

On the other hand, the semiconductors current conducting/switching capability is reduced as its switching frequency increases due to thermal restrictions, as describes the procedure shown in [9]. In the considered example, a maximum junction temperature of 110 °C is considered. If the current/switching frequency limit of the analyzed converter is obtained (Fig. 4) and the switching frequency of each modulation strategy as a function of the output frequency (Fig. 3) is substituted, the current/switching frequency limit of each modulation can be identified as a function of the output fundamental frequency, Fig. 5(a). The comparison of the reference current curve and the thermal current limits of the different modulations returns the output frequency limits of each modulation, Fig. 5(b). Hence, each modulation is only considered within its frequency limits.



Fig. 5: Output current limit for each output frequency, considering different modulation techniques. (a) Current limit. (b) Current limit, considering load current profile; maximum output frequency of the modulation methods is marked with vertical dashed lines.

The role of the current provided by the filter needs to be taken into account, since the current through the inverter may decrease, depending on the load type. In the given example, an asynchronous application is assumed, thus, the dimensioned filter will partially provide the required reactive power to the load. Therefore, it is assumed that the inverter current amplitude will be slightly lower (7.5 % in the given example) than the total current in the load. This recursive calculation needs to be done once the filter components are selected.

Voltage Quality Restrictions

The switching frequency of the semiconductors also determines the synthesized output voltage quality. Two indicators are considered to analyze the synthesized voltage quality: the first harmonic band ($f_{1st,h}$) and the Weighted Total Harmonic Distortion (WTHD) [5], [9].

The first harmonic band defines the harmonic frequency where the first non-negligible harmonic appears. Generally speaking, the higher the first harmonic band frequency of the synthesized voltage is, less attenuation requirements are required to obtain a good quality output current waveform. Depending on the modulation technique, the first harmonic band appears in different ways:

- PWM and SVM techniques theoretically have their first harmonic band in the line-to-line voltage at least around the twice (or higher multiples) of the semiconductors switching frequency. However, apart from the switching harmonics, other lower harmonics may appear, depending on the switching and the output frequencies, which may not be considered negligible.
- SHE techniques theoretically present a first undesired harmonic in the line-to-line voltage at a frequency proportional to the output frequency (f_o) and directly related to the number of calculated angles. However, due to combination of SHE and SHM (Selective Harmonic Mitigation, [10]), in some calculated angle solutions, this relationship is not compulsorily fulfilled and non-negligible harmonics may appear at low frequencies.

In order to identify the first harmonic band of each modulation, the first harmonic frequency in which a harmonic overcomes a given percentage limit of the fundamental harmonic is sought for each modulation/output frequency combination, as depicts Fig. 6(a), where a $V_{H,lim} = 3$ % limit of the fundamental harmonic is considered.

Some modulations contain non-negligible harmonics at very low harmonic frequencies, which cannot be properly attenuated by means of a filter with realistic components. Hence, a minimum allowed frequency limit ($f_{1st,h,LIM}$) is selected (Fig. 6(a)). This frequency limit needs to strictly be set up higher than the maximum allowed resonance frequency for the LCR filter design ($f_{res,LIM} = 400$ Hz in Fig. 6(a)), otherwise, the resonance frequency of the LCR filter might be excited. Therefore, if the first harmonic band of a modulation appears below this limit, the modulation is discarded. In the given example a minimum first band frequency higher than 15 % over the resonance frequency is considered ($f_{1st,h>3\%,LIM} = 460$ Hz in Fig. 6(a)).



Fig. 6: Performance of each modulation technique depending on output frequency. (a) First non-negligible harmonic frequency. (b) WTHD.

Simultaneously, the WTHD of each modulation/output frequency pair is also studied, Fig. 6(b). The WTHD can be considered as an equivalent of the current THD that would be produced by the inverter voltage supplying an inductive load [5]. However, using WTHD of line-to-tine voltage there is no need of knowing the load, while current THD would need a proper load definition. Added to this, as appearing harmonics are weighted, the WTHD may indicate the size of the designed filter.

Finally, the most suitable modulation is chosen for each output frequency. For each output frequency range the modulation that provides a lower WTHD is chosen, among the alternatives that fulfill the current thermal restrictions and minimum voltage first harmonic band restrictions. According to the given example in Fig. 3-Fig. 6, the modulation scheme served in Fig. 7 is chosen.



Fig. 8: Inverter line-to-line output voltage waveforms and spectra. (a) SVM ($f_{sw} = 900$ Hz) waveform. (b) SVM ($f_{sw} = 900$ Hz) spectrum. (c) SHE 5 waveform. (d) SHE 5 spectrum.

Filter design procedure

Once the modulation techniques are selected, next step is the design of the LCR filter. For that purpose, a tradeoff between the reduction of the filter components and the harmonic content attenuation is necessary. With this objective, an automatized LCR filter designing process which solves selection problem of many dimensions and degrees of freedom is presented.

The considered designing restrictions are listed below:

- **THD**_{VLOAD}. Total harmonic distortion of the load voltage.
- THD_{I,LOAD}. Total harmonic distortion of the load current. •
- ΔI_{INV} . Maximum percentage of the inverter current ripple over its fundamental component. •
- dV/dt. Maximum dV/dt derivative of the line-to-line voltage of the load. •
- \mathbf{f}_{res} . Maximum resonance frequency of the filter-load system.
- VINVILITING.1. Maximum synthesizable inverter voltage. The inverter has to be able to synthesize the fundamental voltage needed to compensate the voltage-drop in the filter and obtaining the desired load voltage.
- P_{Losses} . Maximum percentage of power losses in the filter over the nominal output active power. •
- X_{Cf}/X_{Lm} . Minimum ratio between filter capacitor impedance and load magnetizing inductance.

The proposed automatized procedure considers only the fulfillment of these restrictions with the modulation technique previously selected at rated output frequency. In the given example, according to the modulation scheme shown in Fig. 7, the filter will be designed for a SHE 5 modulation. Table II lists the values considered in the given example.

Table II. Considered designing restriction for the example case given in Table I	
Thdv,load,lim	5 %
Thdi,load,lim	5 %
$\Delta I_{INV,LIM}$	30 %
dV/dt _{LIM}	50 V/µs
f _{res,LIM}	400 Hz
PLosses,LIM	0.5 %
X _{Cf} /X _{Lm}	0.90
V _{INV,ll,rms,1,lim} (SHE 5)	7017 V

The procedure consists basically in evaluating pairs of filter inductance (L_f) and capacitor (C_f) altogether with its respective damping resistor (R_d), which is adjusted to achieve a given gain at the resonance frequency. For each set of $L_f-C_f-R_d$ values, the voltage-drop in the filter and the fundamental voltage that needs to be synthesized in the inverter is calculated. The inverter voltage waveform and spectrum are accordingly calculated. Thereafter, the performance of the whole inverter-filter-load system is evaluated, Fig. 9. Each horizontal plane in Fig. 9(a)-(h) represents the considered restriction while the curved surface represents the evolution of each measured variable of the system depending on the evaluated L_f-C_f pair. Among the evaluated L_f-C_f pairs, the ones that fulfill all the restrictions are identified, Fig. 9(i).

From the previous experience it is well known that in MV applications the major part of the filter weight and cost falls on the inductance rather than the capacitor. Among the available pairs, the one that guarantees less expensive L_{f} - C_{f} - R_{d} components is selected, as shown in Fig. 10. In the given example, a $L_f = 14$ mH, $C_f = 26\mu$ F and $R_d = 0.68\Omega$ set of components is automatically chosen in order to achieve the less expensive LCR filter. Other L_f-C_f-R_d sets would be chosen in order to optimize other factors such as the volume, weight or stored energy.



Fig. 9: Calculated indicators and their restrictions for L_f-C_f pairs with SHE 5 modulation. (a) THD_{V,LOAD} < 5.0%. (b) THD_{I,LOAD} < 5.0%. (c) ΔI_{INVI} < 30%. (d) dV/dt < 50 V/µs. (e) f_{res} < 400 Hz. (f) P_{Losses}/P_{nom} < 0.5%. (g) X_{Cf}/X_{Lm} > 0.90. (h) V_{INV,II,rms,1} < 7017 V. (i) Identification of restriction fulfilling L_f-C_f pairs (green shaded).



Fig. 10: Filter component possible solutions based on the indicators served in Table II; selected solution is marked with a cross. (a) L_f-C_f pair. (b) R_d-C_f pair. (c) Filter components total cost.

Filter design verification

The performance of the chosen inverter-filter-load system is analyzed for different operation conditions of the V/f curve of the quadratic load application. Results shown in Fig. 11 demonstrate that the designed filter guarantees the fulfillment of the fixed restrictions at nominal conditions. Moreover, results also show the performance at lower output frequencies, in which under certain conditions the drive operates under the fixed restrictions.



Fig. 11: Calculated indicators for the whole output frequency range. (a) Load voltage. (b) Load current. (c) Load voltage THD. (d) Load current THD. (e) Inverter output current ripple. (f) Filter resistor power loss with respect to the output power.

Added to this, the Bode diagrams of the load voltage and current depending on the inverter voltage are shown in Fig. 12. It is important to note that this frequency responses are only considered to understand the harmonic content attenuation, because they do not model the fundamental harmonic response of the load.

Moreover, the voltage and current waveforms are given in Fig. 13 at 25 Hz and 50 Hz output frequency operation conditions. It is demonstrated how the RC branch of the filter substantially improved the voltage and current seen by the load.



Fig. 12: Bode diagrams of the selected $L_f = 14$ mH, $C_f = 26\mu$ H, $R_d = 0.68\Omega$ filter considering a $L_\sigma = 10.95$ mH leakage inductance of the load. (a) Load voltage vs Inverter voltage. (b) Load current vs Inverter current.



Fig. 13: Output waveforms. From top to bottom: inverter output voltage and current, filter current, load voltage and current. (a) SVM for 25 Hz of output frequency. (b) SHE 5 for 50 Hz of output frequency.

Conclusion

In this paper a systematic procedure is presented in order to select the modulation strategy and the inverter output filter (LCR) components from variable speed drives. Compared to the existing literature, the design of the filter is taken into account when defining the modulation strategy, which leads to quantitative optimization of the problem. In order to make a proper selection, indicators such as thermal behavior, output voltage/current distortion and first appearing harmonic band are evaluated for different Space Vector Modulation and Selective Harmonic Elimination solutions. The applicability of the indicators proposed is demonstrated with the modulation selection and filter design of a 6.6 kV

converter. However, this procedure can be easily extended to different converter topologies, filter types and modulation techniques.

References

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- [1] S. Kouro, J. Rodriguez, B. Wu, S. Bernet and M. A. Perez, "Powering the Future of Industry: High-Power Adjustable Drive Topologies," *IEEE Industry Applications Magazine*, vol. 18, pp. 26-39, 2012.
- [2] F. Filsecker, R. Alvarez and S. Bernet, "Comparison of 4.5-kV Press-Pack IGBTs and IGCTs for Medium-Voltage Converters," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 440-449, 2013.
- [3] S. Kouro, M. Malinowski, K. Gopakumar, L. G. Franquelo, J. Pou, J. Rodriguez, B. Wu, M. A. Perez and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2553-2580, 2010.
- [4] J. Janning and J.-C. Mercier, "Medium Voltage Three-Level Inverter for High Speed Applications," in *European Conference on Power Electronics and Applications (EPE07)*, 2007.
- [5] A. Sanchez-Ruiz, G. Abad, S. Alvarez and L. M. Tolbert, "Modulation Selection Procedure Applied to a High-Power Adjustable High-Speed Drive," in *15th European Conference on Power Electronics and Applications (EPE2013)*, 2013.
- [6] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez y B. Wu, «The Essential Role and the Continuous Evolution of Modulation Techniques for Voltage-Source Inverters in the Past, Present, and Future Power Electronics,» *IEEE Transactions on Industrial Electronics*, vol. 63, n° 5, pp. 2688-2701, 2016.
- [7] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Transactions on Industrial Applications*, vol. 37, no. 2, pp. 637-641, 2001.
- [8] M. S. A. Dahidah, G. Konstantinou and V. G. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4091-4106, 2015.
- [9] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad and I. Baraia, "Medium Voltage–High Power Converter Topologies Comparison Procedure, for a 6.6 kV Drive Application Using 4.5 kV IGBT Modules," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 3, pp. 1462-1476, 2012.
- [10] J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo y M. A. Aguirre, «Selective Harmonic Mitigation Technique for High-Power Converters,» *IEEE Transactions on Industrial Electronics*, vol. 57, nº 7, pp. 2315-2323, 2010.