

Multiple current amplifier-based gate driving for parallel operation of discrete SiC MOSFETs

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Abstract

The shorter switching times of silicon carbide (SiC) MOSFETs enable power converters to operate at higher frequencies than with silicon IGBTs. However, because SiC MOSFET die sizes are still relatively small, several devices have to be connected in parallel to cope with the high current ratings demanded. For the total current to be evenly distributed among all the MOSFETs, the gate circuit and power layout must meet stringent symmetry requirements. However, space limitations on the circuit surface hinders the achievement of full symmetries on both the power and gate layouts because they constrain one another. This paper proposes a solution for safely paralleling discrete SiC MOSFETs while decoupling the gate and power layout designs. It requires placing one BJT-based fast current amplifier as close as possible to each MOSFET rather than using just one to feed all the MOS gates. This reduces the noise in the received gating signals and, more importantly, reduces the sensitivity of driver-gate path geometric / electric mismatches. This makes it possible to safely relax the symmetry requirements for the gating circuitry, thereby providing designers with more freedom to achieve better symmetry in the power layout.

1 | INTRODUCTION

The sequence in the evolution of materials used for semiconductor devices anticipated by William Shockley has already reached the level of silicon carbide (SiC) [1–4]. The well-known trade-off between blocking voltage V_B and specific on-resistance $R_{ON,SP}$ expressed as the figure-of-merit $V_B^2 R_{ON,SP}$ is orders of magnitude higher in SiC than in silicon [5, 6]. However, manufacturers still have to use relatively small die sizes to achieve reasonable product yields [7]. Thus, despite the superior properties of SiC as a base material, in practice SiC MOSFETs must be parallelised to achieve the current levels demanded [8–11].

Given that MOSFETs are unipolar devices, meaning that their $R_{ON,SP}$ has a positive temperature coefficient that favours an equitable current balance (in contrast to IGBTs'), it is tempting to believe that this implies that they have no specific extra difficulties.

However, this is only true of the drift-region contribution to $R_{ON,SP}$, which is dominant once the turn-on transient has died out. Indeed, the channel resistance—whose temperature coefficient is negative—prevails during transients [12]. Moreover, this happens not only in the more mature planar double-diffused structures, but also in younger trench-based gate designs [13].

In addition, it is much harder to grow silica on SiC than on silicon substrates [14]. This poses a substantial challenge for the fabrication of MOS structures and results in, for example, a wider than desirable dispersion of threshold voltages among different devices of the same model [11, 15, 16]. Therefore, effective switching synchronisation is crucial for reliable parallelisation of SiC MOSFETs. Moreover, the switching command must reach all the gates at the same time and rise / fall as simultaneously as possible [17–21].

Active gate driving techniques are a well-known alternative to passive component-based driving circuits [15, 22–24]. Thus, SiC

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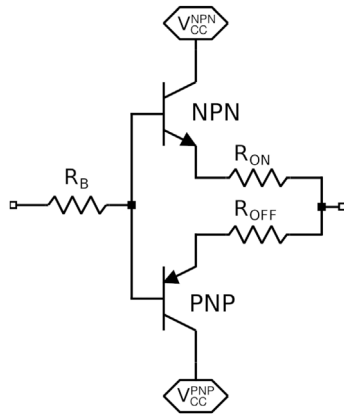


FIGURE 1 A generic push-pull current-amplifying buffer

MOSFET gates are no longer charged through a single resistor, as was usual for their silicon counterparts [7, 10, 25–27]. Most active drives of this type incorporate a push-pull buffer that acts as a current amplifier which speeds up the charging and discharging of MOS capacitance and guarantees faster switching times in spite of the non-negligible stray inductances involved [28, 29].

The aim of this paper is to show how to leverage BJT-based current amplification for the parallelisation of discrete (i.e. single-chip) SiC MOSFETs. Thus, this work proposes the use of one buffer per MOSFET instead of a single buffer for all the MOSFETs (compare Figure 2a,b). Each buffer should be placed as close as possible to its corresponding MOSFET. As a result, gate-attack paths carry one gate current each, thereby greatly reducing their effect on stray inductances and improving switching synchronisation.

While this proposal does not erase stray inductances (rather, it passes them back to the driver-buffer paths), it is shown that its overall performance is less sensitive to the mismatch of the driver-buffer path electrical behaviour than it is to that of the buffer-device paths. This can be expected to relax the symmetry requirements on the driving / gating side, thus achieving independence between power-side and driving / gating-side designs. In turn, this would make it easier to optimise the symmetric design of the power side, which is mandatory for good layout practice.

2 | EFFECTIVE DRIVER-GATE STRAY INDUCTANCES

Figure 1 depicts a generic BJT-based push-pull buffer. Essentially it comprises an NPN+PNP emitter follower pair so that output current can be sourced as well as sunk. This configuration is widely found in power amplifiers, where it is termed a ‘class-B’ output stage [30, 31].

When seen from the load side, looking towards the emitter, an emitter follower presents the Thévenin impedance of the source driving its base as though it were $\beta + 1$ times smaller than it actually is, in addition to a contribution resulting from

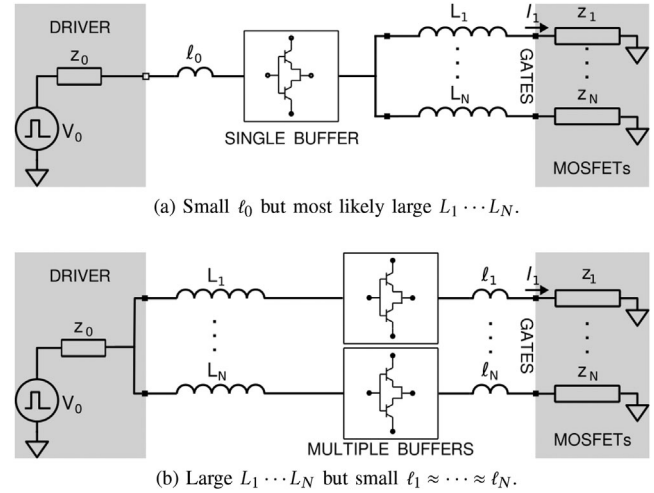


FIGURE 2 Typical parallel gating (a) versus new proposal (b)

the emitter dynamic resistance r_e , sometimes expressed through $r_\pi = (\beta + 1)r_e$. Therefore, these stages are typically appended to voltage sources that cannot cope with the current levels demanded by their loads.

Note, however, that the value for β (the current gain of the BJT) should be taken at the frequency of interest, where it is likely to have fallen significantly from its dc-value. This performance degradation, which is usually captured by the BJT’s unit-gain ‘transition frequency’ (f_T), drops for increasing collector current levels [32].

Figure 2 introduces a MOSFET parallelisation scenario. Because several gates must be fed, a decision has to be made: either use a single buffer to feed all the gates (which cannot possibly be placed near all the gates), or dedicate one buffer to each gate, thus minimising the buffer-gate stray inductance.

Let us compare the s -domain performance of these two setups in terms of I_1 , the current supplied to the first MOSFET. To simplify these expressions, in this section it is assumed that all the MOSFETs and their gate paths are electrically equivalent, and so $z_1 = \dots = z_N$, $L_1 = \dots = L_N$, and $l_1 = \dots = l_N \approx l_0$. In addition, both R_{ON} and R_{OFF} are set to zero both for simplicity and because no such resistors were used in this work.

- Single-buffer setup. Because the total current provided by the only stage equals $NI_1 = \frac{V_0}{\frac{z_0 + s l_0 + R_B + r_\pi}{\beta + 1} + \frac{s L_1 + z_1}{N}}$, then

$$I_1(\text{Single}) = \frac{V_0}{N \frac{z_0 + s l_0 + (R_B + r_\pi)}{\beta + 1} + s L_1 + z_1}. \quad (1)$$

- Multiple-buffer setup. Let us imagine that z_0 is split into N equal, parallel-connected impedances of $N z_0$ ohms each. Thanks to symmetry, $N z_0$ ohms can be assigned to each branch, which means that every branch ‘sees’ V_0 in series with

$N\tilde{\zeta}_0$, and therefore

$$I_1(\text{Multiple}) = \frac{V_0}{\frac{N\tilde{\zeta}_0 + sL_1 + (R_B + r_\pi)}{\beta + 1} + s\ell_1 + \tilde{\zeta}_1}. \quad (2)$$

Naturally, the smaller the denominators of (1)-(2), the faster the response and, therefore, the better the performance. These denominators have five addends. Two of them, $\frac{N\tilde{\zeta}_0}{\beta + 1}$ and $\tilde{\zeta}_1$, would be kept the same. In addition, the contribution of $(R_B + r_\pi)$ would be reduced by a factor of N from (1) to (2).

However, more interestingly, although the effect of the small stray inductance of the edges of the path changes from $\frac{N\ell_0}{\beta + 1}$ to ℓ_1 , the bulk of the stray inductance would be reduced by a factor of $\beta + 1$. This is a major advantage because it reduces the effective Thévenin inductance seen from the gates, and so a faster response can be expected. In addition, because the weight of such inductances in the overall denominator is reduced, the impairment on the synchronisation of the gating signals caused by individual variations of $L_1 \cdots L_N$ from the average value (resulting from path asymmetries) should also reduce.

Moreover, from the perspective of the dynamic response to a step input, that is, the switching control signal, the behaviour of both setups is equivalent to that of a basic RLC network. Thus, examining the damping factor, $\alpha = \frac{R}{2L}$, and the natural frequency, $\omega_n = \frac{1}{\sqrt{LC}}$, of both configurations, and bearing in mind that underdamping occurs whenever $\alpha < \omega_n$, the inequality $L > \frac{CR^2}{4}$ applies. As (1) and (2) show, the C (within $\tilde{\zeta}$) and R values are approximately the same for both configurations, and the main contribution of the inductance value L is due to L_1 and ℓ_1 , respectively. Therefore, assuming $L_1 > \ell_1$, the single push-pull configuration is more likely to be overdamped than its counterpart in the same conditions, thereby implying that the magnitude and oscillations of dv/dt in the single-buffer configuration will be higher during switching.

In the following sections these two topologies will be assessed in more detail, also considering possible mismatches in the values of $L_1 \cdots L_N$. This means that a total of four cases will be studied: ‘single-buffer, symmetric paths’ (SS), ‘single-buffer, asymmetric paths’ (SA), ‘multiple-buffer, symmetric paths’ (MS), and ‘multiple-buffer, asymmetric paths’ (MA). However, as it is shown below, the simulated performance of the SA case was so poor and so dangerous that there was little point in considering it for experimental validation.

3 | REARRANGING THE CURRENT-AMPLIFYING STAGE

Once the potential interest of the multiple-buffer topology has been justified, according to the methodology followed, it

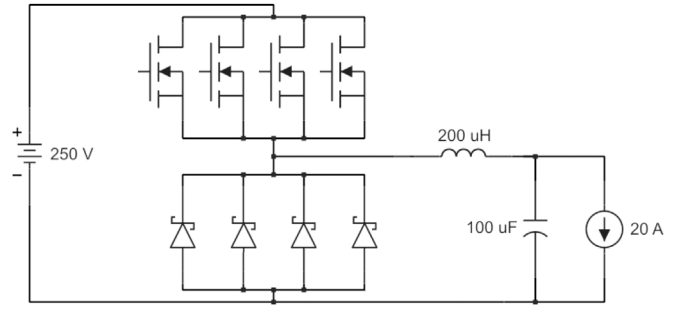


FIGURE 3 Schematic of the buck converter, emphasising the power part (and ignoring parasitics for clarity)

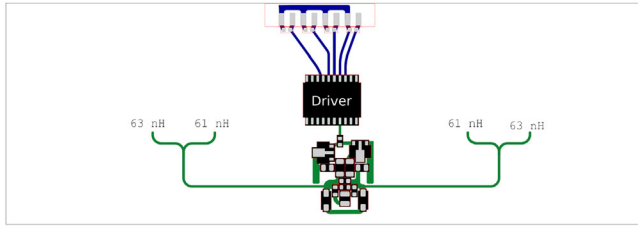
remains to: (i) select a simple, illustrative power conversion environment; (ii) pre-design the layouts and estimate their bulk stray inductances, (iii) simulate the resulting four circuits, incorporating the models of the active devices involved (including the power switching devices), and finally (iv) develop and implement the relevant cases, to experimentally validate their actual performance.

Thus, one of the simplest converter topologies was chosen (see Figure 3): a standard step-down dc-dc converter running from a 250-V supply, equipped with an output LC filter of 200 μH and 100 μF , and feeding a 20-A d.c. load (although 10 A and 5 A were also considered for some simulations, as it is shown in the following section). As to the power switching, $N = 4$ SiC MOSFETs (Wolfspeed C3M0075120J) worked in parallel along with four SiC Schottky diodes (STMicroelectronics STPSC20H12G), all switching at $f = 125$ kHz with a 50% duty cycle.

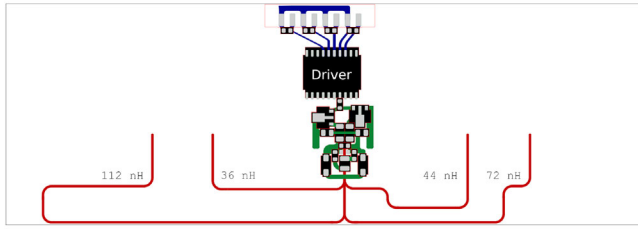
The current-amplifying buffers (recall Figure 1) were implemented using one PBSS4041NX NPN and one PBSS4041PX PNP, both made by Nexperia. They were selected because of their current handling capabilities and low saturation voltages, in spite of their modest f_T of 130-110 MHz at ± 0.1 A. The collector supply voltages were chosen so that $V_{CC}^{\text{NPN}} = 19$ V and $V_{CC}^{\text{PNP}} = -5$ V. In all the instances, R_B was set to 47 Ω in order to maintain the base currents within reasonable ranges. In addition, $R_{\text{ON}} = R_{\text{OFF}} = 0$, and no external gate resistors were added, meaning that R_B would indirectly limit the speed of the gate charging.

Figures 4 and 5 show the corresponding pre-designed layouts and indicate the estimated bulk stray inductances of the driver-to-buffer and buffer-to-gate pathways. Namely, these $L_1 \cdots L_4$ values were obtained using FastHenry software [33], based on the geometry of the tracks, and switching frequency considerations to account for the skin effect.

For both symmetric layouts, the result of these inductances was nearly identical: 62 ± 1 nH in the SS case, and 60 ± 1 nH for the MS case. Subsequently, both topologies were deliberately rerouted wrongly (hence the red-coloured tracks), but because the preliminary simulations gave such a poor (and dangerous) result for the SA case (Figure 6), it was immediately discarded. In contrast, the MA case was based on inductance values of 110, 34, 42, and 70 nH.

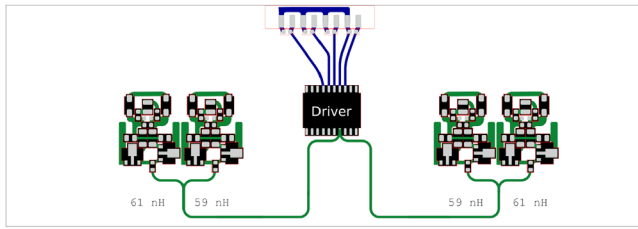


(a) SS setup: a single buffer feeds all the gates.

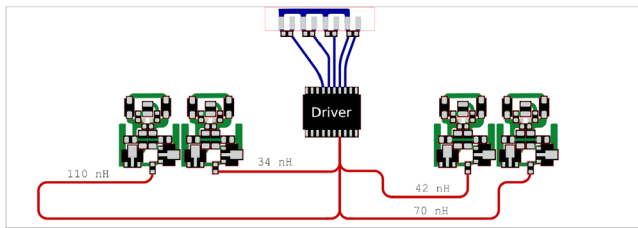


(b) SA setup: the same as above, but deliberately misrouted.

FIGURE 4 Pre-designs of the single-buffer layouts



(a) MS setup: one buffer for each gate.



(b) MA setup: the same as above, but deliberately misrouted.

FIGURE 5 Pre-designs of the multiple-buffer layouts

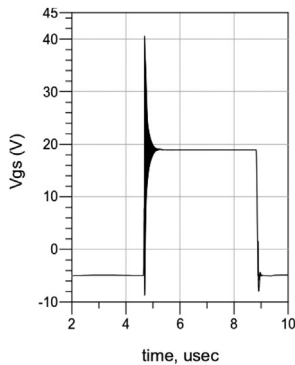


FIGURE 6 Extreme turn-on ringing of v_{GS} in the SA case

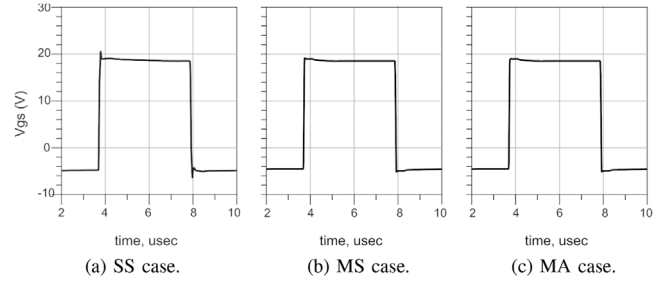


FIGURE 7 Simulated turn-on voltages

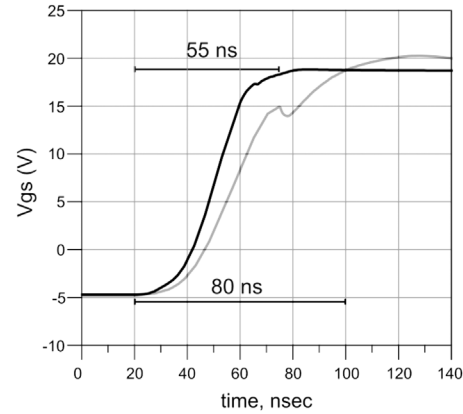


FIGURE 8 Simulated turn-on voltage rising edges: SS (grey) versus MS (black)

4 | SOFTWARE SIMULATIONS

Several simulations were carried out using Keysight’s ADS software. They were focused on gaining insight into the shapes of $v_{GS}(t)$, the gate-source voltages at the end of the MOSFET, in terms of their overshoots, rise times, and mutual synchronisations. Indeed, the simulations also looked into the waveforms of the drain voltage and drain currents, but no differences could be perceived among the cases studied, and so they provided no useful information in comparative terms.

To begin with, as shown in Figure 6, a significant inductance mismatch would cause the extreme ringing in an SA case and so it was discarded from the following studies.

Figure 7 shows the remaining three cases; in the SS case, v_{GS} exhibited a noteworthy 2-V overshoot in both the rising and the falling edges. This is in contrast with the well-behaved signal in the MS case. Finally, the signal displayed for the MA case, which corresponds to the branch with the largest driver-to-buffer inductance, was not hindered by this excess stray inductance.

Figure 8 provides a closer look at the rising v_{GS} edges of the SS and MS cases. In line with the previous observations, the signal of the former rose slower than the latter, that is, 80 versus 55 ns, and so it took a 30% less time for the MS signal to rise.

Figure 9 compares the rising edges of the four MA turn-on signals. By zooming in around the typical 2.54-V gate-voltage threshold of the Wolfspeed SiC C3M0075120J MOSFET (see

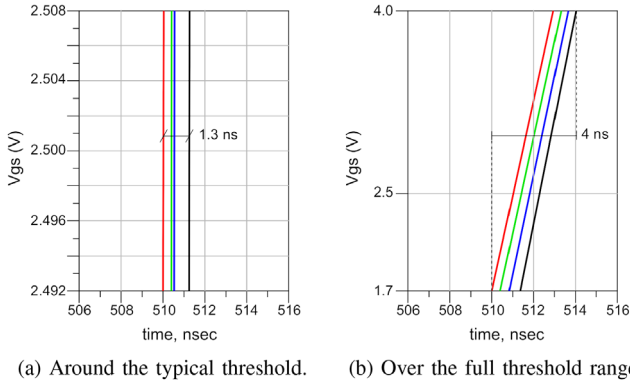


FIGURE 9 Simulated v_{GS} rising edges, MA case

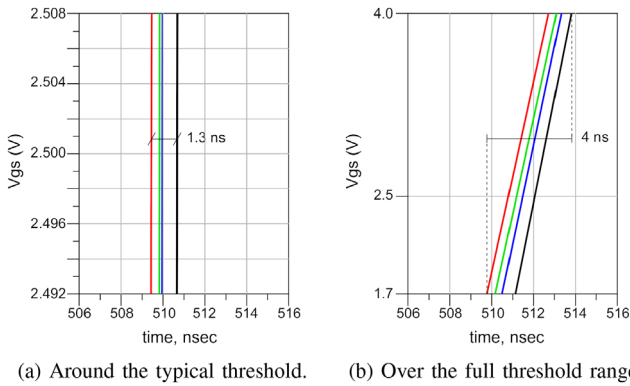


FIGURE 10 Rising edges with load current = 10 A

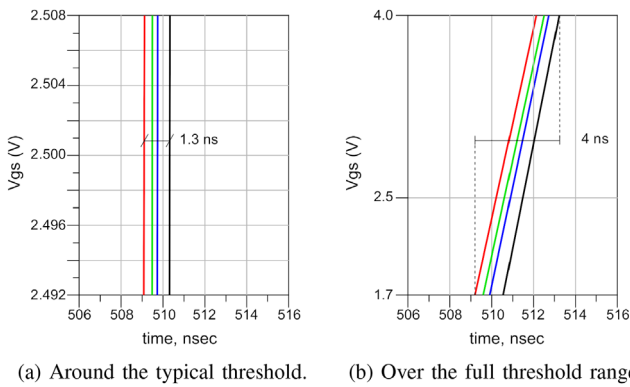


FIGURE 11 Rising edges with load current = 5 A

Figure 9a), it can be seen that the asymmetry of the inductive paths caused a short 1.3-ns gap between the rising edges of the branches (which had the smallest and largest inductances).

However, over the full range of possible threshold voltages (1.7–4.0 V) the gap increased to 4 ns (see Figure 9b). Nevertheless, because the activation delay of these MOSFETs was about 8 ns, the application of the proposal being presented here seemed to result in an admissible deviation which should not entail critical synchronisation problems. Also note that the same results were obtained with load currents of 10 A and 5 A, as shown in Figures 10 and 11.

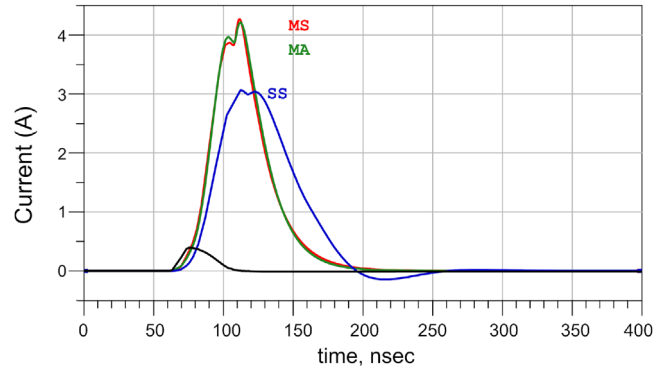
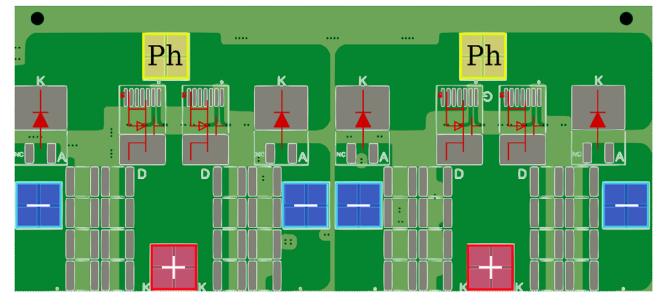
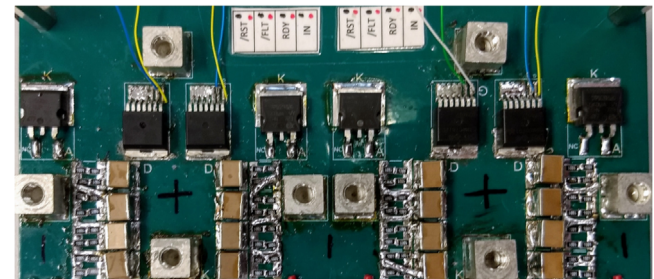


FIGURE 12 Aggregate gate turn-on currents of MS (red), MA (green) and SS (blue) cases; buffer input current also shown (black)



(a) Pre-design of the power layout.



(b) Board with mounted components.

FIGURE 13 Top views of the power area

Finally, it is instructive to briefly analyse the current amplification performance of the buffers. Thus, Figure 12 compares the sum of all four gate currents; the buffer input current (which is the same for both MS and SS) is also shown for reference. Faster rise times are achieved in the multiple buffer cases (MS and MA), and unlike the SS case, there is no negative current at all, leading to more efficient driving of the MOSFETs. This also suggests that the larger the number of parallelised MOSFETs, N , the more noticeable the improvement will be.

5 | EXPERIMENTAL VALIDATION AND DISCUSSION

Figure 13 displays the power stage of the buck converter, whose two “Ph” tags correspond to the MOSFET sources and

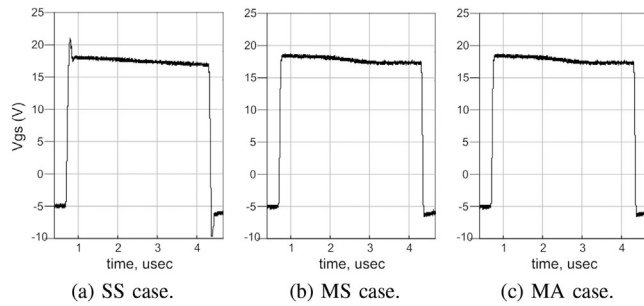


FIGURE 14 Measured turn-on voltages

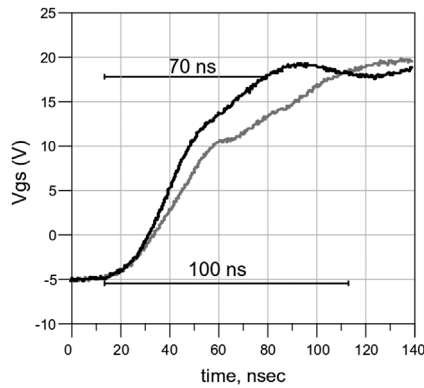


FIGURE 15 Measured turn-on voltage rising edges: SS (grey) versus MS (black)

diode cathodes, with two MOSFETs and two diodes joining at each “Ph”.

The experimental tests confirmed the benefits that had been anticipated in the simulations. Concerning the turn-on v_{GS} signals and their overshoots, the measured traces shown in Figure 14 resembled those of Figure 7. The real SS case also clearly overshoot (even more markedly at about 3 V) in both its rising and falling edges, whereas the MS and worst-case MA signals both turned out to be neat and well shaped.

In addition, Figure 15 shows the rise times measured for the SS and MS cases. Although they were both longer than those of Figure 8, their relationship is essentially the same: the MS signal rose 30% faster.

Finally, as far as the synchronisation is concerned, the four gate signals had to be measured to account for device parameter dispersion. Figures 16a–18a focus on the typical 2.5-V threshold; the synchronisation between the individual gate voltage signals is exceptionally good in all cases, with the best behaviour exhibited by the MS case with a maximum deviation of 3 ns.

However, when the threshold range is extended to encompass all the values between the minimum and maximum limits provided by the manufacturer, that is, from 1.7 to 4.0 V, the picture completely changes (Figures 16b–18b): 10 ns were measured in the SS case, whereas 7 and 8 ns were measured in the MS and MA cases, respectively.

Thus, given that the activation time of these MOSFETs (provided by their datasheets) lies at around 8 ns, the use of a single buffer could cause serious synchronisation problems, resulting

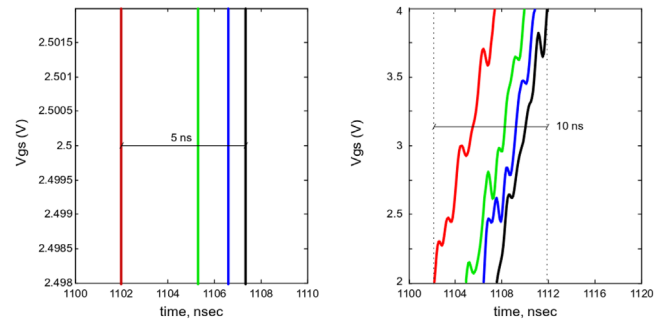


FIGURE 16 Measured rising edges, SS case

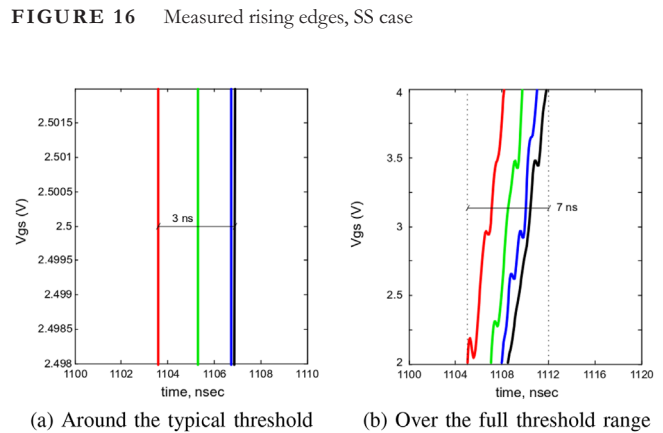


FIGURE 17 Measured rising edges, MS case

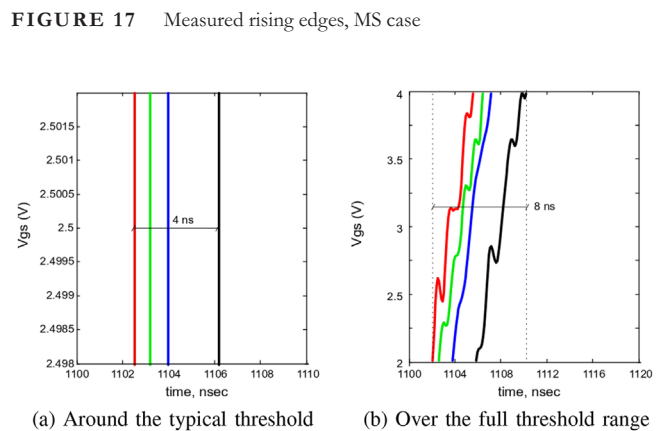


FIGURE 18 Measured rising edges, MA case

in one of the MOSFETs being fully on while another is still off. This risk would be greatly reduced if the designer instead opted for the multiple push–pull buffer arrangement, which can also be expected to yield much neater gating signals with 30% shorter turn-on rise times in the cases studied here.

6 | CONCLUSIONS

This work deals with the use of BJT-based push–pull buffers as current amplifiers for the gate-attack circuitry of discrete SiC MOSFETs operating in parallel. In particular, it studies the use of one buffer per MOSFET, instead of one single buffer for all MOSFETs, as is usual in commercially available multichip

modules. Because the buffers can then be placed very close to their companion MOSFETs, the stray inductance of the driver-to-gate path no longer concentrates on the buffer-to-gate portion of the path but rather, on the driver-to-buffer portion, through which much lower currents pass.

To assess the benefits of this new setup, one of the simplest possible converter topologies was chosen, namely a step-down dc-dc converter with four MOSFETs in parallel with four fast diodes on the low side. The simulations conducted, as well as their subsequent experimental validation, revealed two important advantages of this setup. On one hand, because the control signals reaching the gates were much neater, harmful overshoots and ringing oscillations were avoided, and therefore the risk of self-turn-on was reduced.

On the other hand, the electric performance was less sensitive to the degree of asymmetry between the diverse buffer-to-gate paths, which resulted in a reduced risk of non-simultaneous switching. This means that for a given risk, a greater level of asymmetry could be tolerated in the gate-attack circuitry which would, in turn, aid in design efforts to achieve higher symmetry levels on the power-side layout.

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

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